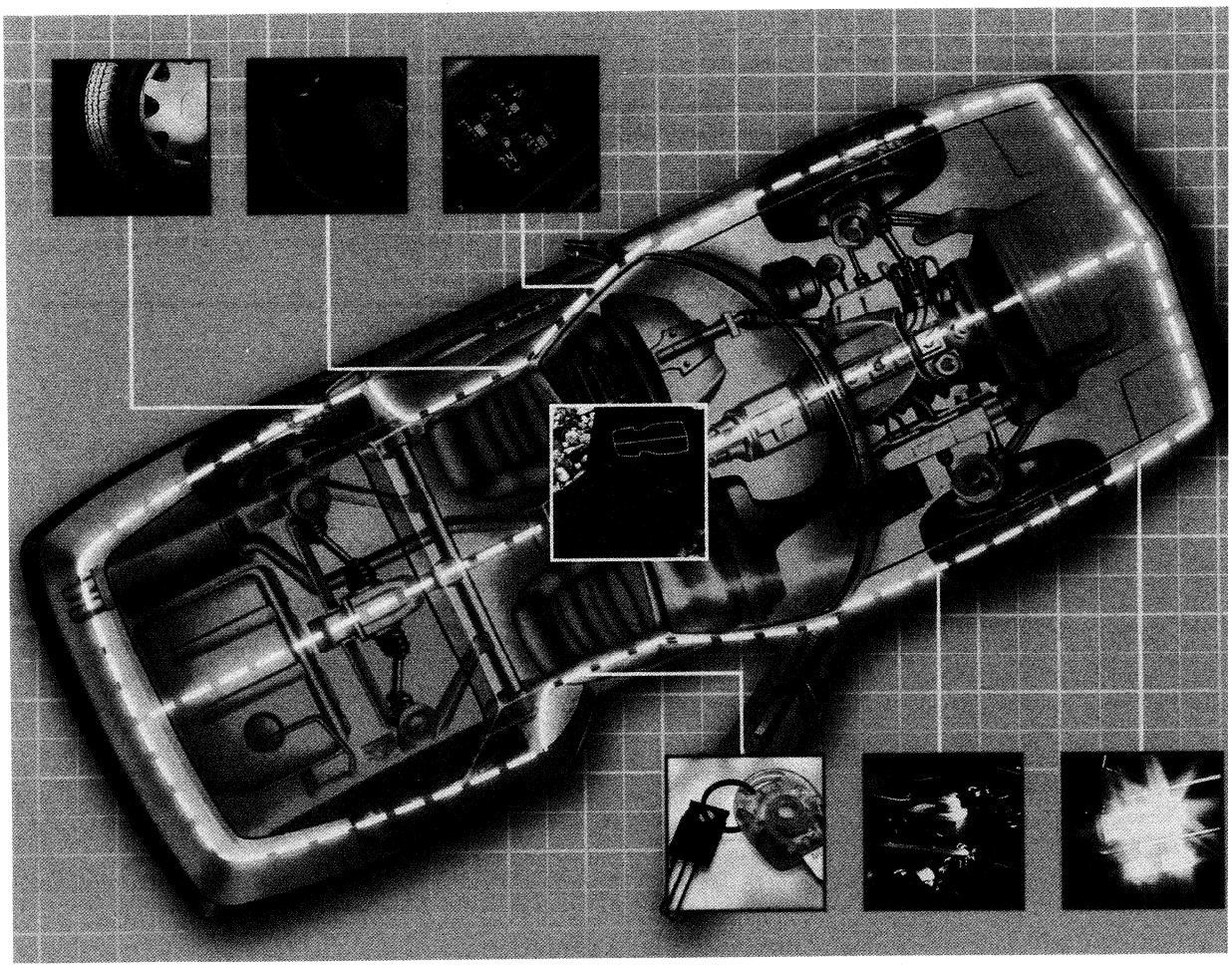
EGRATED CIRCUITS

Semiconductors for In-car Electronics



1996

DATA HANDBOOK IC18

Philips
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QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

Semiconductors for In-Car Electronics

CONTENTS

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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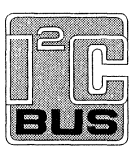


Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

Preface

Few industrial markets are developing faster than automotive electronics, and current predictions are that by 2005, one third of a car's components will be electrical or electronic. The increasing use of electronically-controlled systems in cars is not only to satisfy legislation with regard to safety, security and air pollution, but also to satisfy owner's demands to make vehicles safer, easier to drive, more comfortable, more efficient, and more reliable. Though the use of microcomputer-based systems is now well-established for controlling engines, there is undoubtedly still greater scope for the use of high-reliability electronic systems in other areas such as airbags, ABS, EPAS (electronic power-assisted steering) and driver information systems.

To cater for this vast, varied and highly-competitive market, only those semiconductor manufacturers with major resources, and a commitment to innovation will meet the standards of tomorrow. Philips Semiconductors is such a manufacturer; one with complete solutions for the industry's current needs, and with well-defined roadmaps for those of the future. Furthermore, recognizing the unique characteristics of the automotive market, Philips Semiconductors is increasingly focusing on this market as a technology, quality and logistics driver for its other operations. For example, major automotive research projects in which Philips has participated include CARESSE, PROMETHEUS and SOCRATES. Participation has provided the solid base on which today's extensive range of commodity and custom products were defined.

Some well-known automotive electronics applications
Information, communication and in-car entertainment Car phones/fax, RDC-TMC, CARIN, radio/cassette/CD/DCC players, TV, driver information systems, sensing and gauging
Power train Engine management, gearbox control, exhaust emission control, diagnostics
Body Lights, dashboard, diagnostics, electronic key, anti-theft, battery charging/alternator
Safety ABS, airbag, seat belt tightener, central locking
Comfort and convenience Climate control, power-operated seats, windows, mirrors, EPAS

Technology leader

Philips Semiconductors is a recognized leader in high-density mixed-signal automotive ASICs and microcontroller derivatives. Specifically, the company is a leading innovator of products for:

- multiplexed systems, notably those using the CAN* or J1850 multimaster real-time communications protocol for which the company has many standard/custom products
- airbag and anti-lock braking systems using mixed-signal technology
- driver information systems
- car entertainment systems
- car phones
- sensing and metering (gauging) systems.

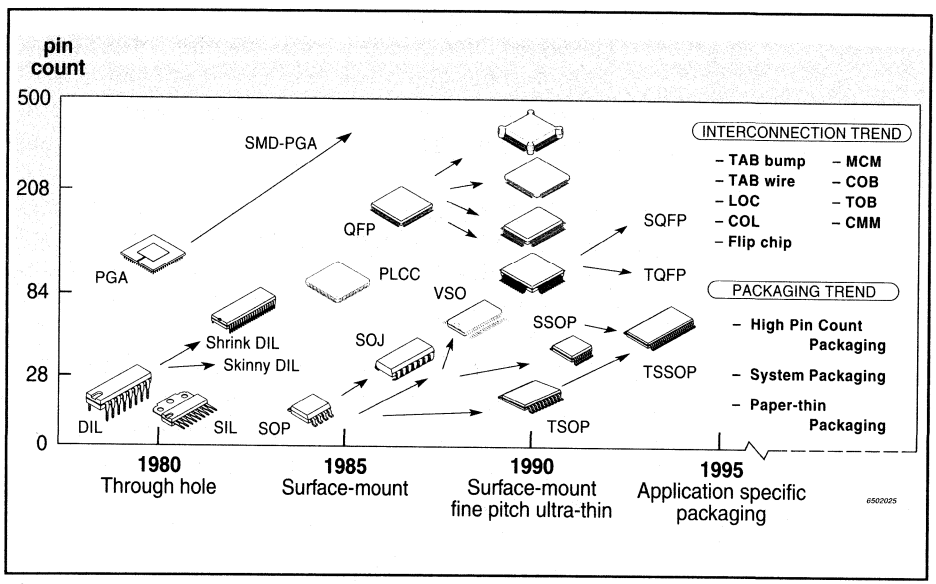
Implementation of electronic systems such as these demands a broad knowledge, not only at systems level, but also at the interconnection and component level.

* CAN is a Bosch proprietary system which Philips is licensed to use.

Philips' current semiconductor fabrication processes		
Mixed processes		Voltage
QA	1.0 µm BiCMOS	40 V to 80 V
QUBIC	1.0 µm BiCMOS	10 V
Advanced bipolar		
RC5	2.0 µm bipolar, HV oxide-isolated	32 V
HS3	2.0 µm bipolar, HV oxide-isolated	10 V
Q2	5.0 µm bipolar, junction-isolated	50 V
SACMOS		
SAC	1-3 µm Self Aligned CMOS, low voltage	6 V
CMOS		
QK	3.0 µm CMOS	20 V
C300	1.6 µm CMOS, single metal, single poly, 25 nm gate oxide	5 V
C3SC	1.6 µm CMOS, single metal, double poly (switched capacitor), 25 nm gate oxide	5 V
C2DM	1.2 µm CMOS, double metal, single poly, 25 nm gate oxide	5 V
C200SC	1.0 µm CMOS, single metal, double poly, 20 nm gate oxide	5 V
C200DM	1.0 µm CMOS, double metal, single poly, 20 nm gate oxide	5 V
C200LT	1.0 µm CMOS, double metal, single poly, 20 nm gate oxide	3.3 V
Sub-micron CMOS		
C150DM	0.8 µm CMOS, double metal, single poly, 15 nm gate oxide	5 V
C150LP	0.8 µm CMOS, double metal, single poly, 15 nm gate oxide	3.3 V
C150DC	0.8 µm CMOS, double metal, double poly, 15 nm gate oxide	5 V
C150PD	0.8 µm CMOS, double metal, double poly, 15 nm gate oxide	50 V
DMOS		
L51	Vertical DMOS	250 V
L11	High-voltage Vertical DMOS	700 V
L03	Low-voltage Vertical DMOS with CMOS capability	80 V

Unrivalled resources

Philips Semiconductors has one of the widest portfolios of technologies and semiconductors to meet the needs of the automotive market. World-class designs, advanced fabrication processes and up-to-date manufacturing plants and logistics has established Philips Semiconductors as a world-class supplier. Quality Assurance is based on internationally-accepted quality standards such as ISO 9000 as well as customer-specific standards such as Ford's TQE - awarded to Philips Semiconductors in 1995.



IC packaging and interconnection trends. Philips Semiconductors has a reputation for innovation in IC and discrete semiconductor packages.

Customer cooperation and world-wide support

Cooperation with customers is vital for securing market acceptance of both customers' products and our own. In addition, we believe that technology partnerships are extremely important for stimulating further development of automotive electronics technology, and have successful partnerships with major electronic systems suppliers and car manufacturers.

Design-in support

To facilitate co-development with these systems suppliers and manufacturers, Philips Semiconductors operates the following automotive facilities:

for ICs:

- North American Regional Automotive Centre (NARAC), Sunnyvale, Ca., USA
- European Automotive Centre (EURAC), Nijmegen, The Netherlands

and for automotive power discretes:

- Philips Semiconductors (Hazel Grove) Stockport, England.

Then there are the Automotive Application Support Groups based at our Application Laboratories in:

- Hamburg, Germany – our Centre of Excellence for CAN bus including the latest low bus-speed applications
- Sunnyvale, USA – our Centre of Excellence for ABS, and driver information systems.

We can also draw upon the expertise and knowledge of the world's largest privately-funded research facilities. And naturally, Philips' research laboratories in the USA (Briarcliff) and in Europe (Aachen and Eindhoven) all have extensive automotive programs.

With these resources, we can guarantee the timely introductions of technologies, processes and designs to provide advanced cost-effective solutions to your product needs. To access this wealth of design and development support, first contact your local Philips Semiconductors sales office (address on back cover).

A winning product portfolio

This book provides an overview of the comprehensive range of commodity ICs and discrete semiconductors for automotive applications. Many products are acknowledged as 'best in their class'. And while the listed products will satisfy most demands for rugged, high-quality automotive ICs and discrete semiconductors, custom products can always be supplied.

Philips automotive product milestones	
First automotive custom IC from Philips Semiconductors	1977
Announcement of CAN license from Bosch	November 1987
Release of the first CAN product (stand-alone CAN controller PCx82C200)	1989
First rotational angle sensor (KM110BH)	1991
First IGBT	June 1991
First 3-pin TOPFET	October 1991
First 5-pin TOPFET	September 1992
First integrated rotational speed sensor (KM110/B)	October 1992
First microcontroller with a CAN interface:	
- P87C592 (EPROM)	1991
- P83C592 (ROM version)	1993
Release of CAN transceiver P82C250	1993
First encapsulated angle sensor (KMA10/70)	1993
Release of CAN transceiver P82C251 (for bus and truck environments)	1995
Release of CAN transceiver P82C252 (for low-speed applications)	1996

A winning product portfolio

This book provides an overview of the comprehensive range of commodity ICs and discrete semiconductors for automotive applications. Many products are acknowledged as `best in their class'. And while the listed products will satisfy most demands for rugged, high-quality automotive ICs and discrete semiconductors, custom products can always be supplied.

SELECTION GUIDE

page

CAN bus specification 2.0

Parts A and B

Preface

The acceptance and introduction of serial communication to more and more applications has led to requirements that the assignment of message identifiers to communication functions be standardized for certain applications. These applications can be realized with CAN more comfortably, if the address range that originally has been defined by 11 identifier bits is enlarged.

Therefore a second message format ('extended format') is introduced that provides a larger address range defined by 29 bits. This will relieve the system designer from compromizes with respect to defining well-structured naming schemes. Users of CAN who do not need the identifier range offered by the extended format, can rely on the conventional 11 bit identifier range ('standard format') further on. In this case they can make use of the CAN implementations that are already available on the market, or of new controllers that implement both formats.

In order to dinstiguish standard and extended format the first reserved bit of the CAN message format, as it is defined in CAN Specification 1.2, is used. This is done in such a way that the message format in CAN Specification 1.2 is equivalent to the standard format and therefore is still valid. Furthermore, the extended format has been defined so that messages in standard format and extended format can coexist within the same network.

This CAN Specification 2.0 consists of two parts, with

- **Part A** describing the CAN message format as it is defined in CAN Specification 1.2;
- **Part B** describing both standard and extended message formats.

In order to be compatible with this CAN Specification 2.0 it is required that a CAN implementation be compatible with either Part A or Part B.

Note
CAN implementations that are designed according to part A of this or according to previous CAN Specifications, and CAN implementations that are designed according to part B of this specification can communicate with each other as long as it is not made use of the extended format.

Contents, PART A

1. Introduction

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed realtime control with a very high level of security. Its domain of application ranges from high speed networks to low cost multiplex wiring.

In automotive electronics, engine control units, sensors, anti-skid-systems, etc. are connected using CAN with bit rates up to 1 Mbit/s.

At the same time it is cost-effective to build into vehicle body electronics, e. g. lamp clusters, electric windows etc. to replace the wiring harness otherwise required.

The intention of this specification is to achieve compatibility between any two CAN implementations. Compatibility, however, has different aspects, regarding e. g. electrical features and the interpretation of data to be transferred. To achieve design transparency and implementation flexibility, CAN has been subdivided into different layers.

- the (CAN-) object layer,
- the (CAN-) transfer layer,
- the physical layer.

The object layer and the transfer layer comprise all services and functions of the data link layer defined by the ISO/OSI model. The scope of the object layer includes

- finding which messages are to be transmitted,
- deciding which messages received by the transfer layer are actually to be used,
- providing an interface to the application layer related hardware.

There is much freedom in defining object handling. The scope of the transfer layer mainly is the transfer protocol, i. e. controlling the framing, performing arbitration, error checking, error signalling and fault confinement. Within the transfer layer it is decided whether the bus is free for starting a new transmission or whether a reception is just starting. Also some general features of the bit timing are regarded as part of the transfer layer. It is in the nature of the transfer layer that there is no freedom for modifications.

The scope of the physical layer is the actual transfer of the bits between the different nodes with respect to all electrical properties. Within one network the physical layer, of course, has to be the same for all nodes. There may be, however, much freedom in selecting a physical layer.

The scope of this specification is to define the transfer layer and the consequences of the CAN protocol on the surrounding layers.

2. Basic Concepts

CAN has the following properties

- prioritization of messages
- guarantee of latency times
- configuration flexibility
- multicast reception with time synchronization
- system wide data consistency
- multimaster
- error detection and error signalling
- automatic retransmission of corrupted messages as soon as the bus is idle again
- distinction between temporary errors and permanent failures of nodes and autonomous switching off of defective nodes.

Table 1. Layered Structure of a CAN Node

Application Layer
Object Layer – Message Filtering – Message and Status Handling
Transfer Layer – Fault Confinement – Error Detection and Signalling – Message Validation – Acknowledgement – Arbitration – Message Framing – Transfer Rate and Timing
Physical Layer – Signal Level and Bit Representation – Transmission Medium

- The *Physical Layer* defines how signals are actually transmitted. Within this specification the physical layer is not defined so as to allow transmission medium and signal level implementations to be optimized for their application.
- The *Transfer Layer* represents the kernel of the CAN protocol. It presents messages received to the object layer and accepts messages to be transmitted from the object layer. The transfer layer is responsible for bit timing and synchronization, message framing, arbitration, acknowledgement, error detection and signalling, and fault confinement.
- The *Object Layer* is concerned with message filtering as well as status and message handling.

The scope of this specification is to define the transfer layer and the consequences of the CAN protocol on the surrounding layers.

Messages
Information on the bus is sent in fixed format messages of different but limited length (see section 3: Message Transfer). When the bus is free, any connected unit may start to transmit a new message.

Information Routing
In CAN systems, a CAN node does not make use of any information about the system configuration (e. g. station addresses). This has several important consequences.

System Flexibility: Nodes can be added to the CAN network without requiring any change in the software or hardware of any node and application layer.

Message Routing: The content of a message is named by an IDENTIFIER. The IDENTIFIER does not indicate the destination of the message, but describes the meaning of the data, so that all nodes in the network are able to decide by MESSAGE FILTERING whether the data is to be acted upon by them or not.

Multicast: As a consequence of the concept of MESSAGE FILTERING, any number of nodes can receive and simultaneously act upon the same message.

Data Consistency: Within a CAN network it is guaranteed that a message is simultaneously accepted either by all nodes or by no node. Thus, data consistency of a system is achieved by the concepts of multicast and by error handling.

Bit rate
The speed of CAN may be different in different systems. However, in a given system the bitrate is uniform and fixed.

Priorities
The IDENTIFIER defines a static message priority during bus access.

Remote Data Request
By sending a REMOTE FRAME, a node requiring data may request another node to send the corresponding DATA FRAME. The DATA FRAME and the corresponding REMOTE FRAME are named by the same IDENTIFIER.

Multimaster
When the bus is free, any unit may start to transmit a message. The unit with the message of highest priority to be transmitted gains bus access.

Arbitration
Whenever the bus is free, any unit may start to transmit a message. If 2 or more units start transmitting messages at the same time, the bus access conflict is resolved by bitwise arbitration using the IDENTIFIER. The mechanism of arbitration guarantees that neither information nor time is lost. If a DATA FRAME and a REMOTE FRAME with the same IDENTIFIER are initiated at the same time, the DATA FRAME prevails over the REMOTE FRAME. During arbitration, every transmitter compares the level of the bit transmitted with the level that is monitored on the bus. If these levels are equal the unit may continue to send. When a 'recessive' level is sent and a 'dominant' level is monitored (see Bus Values), the unit has lost arbitration and must withdraw without sending one more bit.

Safety
In order to achieve the utmost safety of data transfer, powerful measures for error detection, signalling and self-checking are implemented in every CAN node.

Error Detection
For detecting errors, the following measures have been taken:

- Monitoring (transmitters compare the bit levels to be transmitted with the bit levels detected on the bus),
- Cyclic Redundancy Check,
- Bit Stuffing,
- Message Frame Check.

Performance of Error Detection
The error detection mechanisms have the following properties:

- all global errors are detected.
- all local errors at transmitters are detected.
- up to 5 randomly distributed errors in a message are detected.
- burst errors of length less than 15 in a message are detected.
- errors of any odd number in a message are detected.

Total residual error probability for undetected corrupted messages:

less than

message error rate $\times$ 4.7×10^{-11}.

Error Signalling and Recovery Time
Corrupted messages are flagged by any node detecting an error. Such messages are aborted and will be retransmitted automatically. The recovery time from detecting an error until the start of the next message is at most 29 bit times, if there is no further error.

Fault Confinement
CAN nodes are able to distinguish short disturbances from permanent failures. Defective nodes are switched off.

Connections
The CAN serial communication link is a bus to which a number of units may be connected. This number has no theoretical limit. Practically the total number of units will be limited by delay times and / or electrical loads on the bus line.

Single Channel
The bus consists of a single bidirectional channel that carries bits. From this data, resynchronization information can be derived. The way in which this channel is implemented is not fixed in this specification. E.g. single wire (plus ground), two differential wires, optical fibres, etc. may be used.

Bus values
The bus can have one of two complementary logical values: 'dominant' or 'recessive'. During simultaneous transmission of 'dominant' and 'recessive' bits, the resulting bus value will be 'dominant'. For example, in case of a wired-AND implementation of the bus, the 'dominant' level would be represented by a logical '0' and the 'recessive' level by a logical '1'. Physical states (e. g. electrical voltage, light) that represent the logical levels are not given in this specification.

Acknowledgement
All receivers check the consistency of the message being received and will acknowledge a consistent message and flag an inconsistent message.

Sleep Mode / Wake-up
To reduce the system's power consumption, a CAN device may be set into sleep mode without any internal activity and with disconnected bus drivers. The sleep mode is finished with a wake-up by any bus activity or by internal conditions of the system. On wake-up, the internal activity is restarted, although the transfer layer will be waiting for the system's oscillator to stabilize and it will then wait until it has synchronized itself to the bus activity (by checking for eleven consecutive 'recessive' bits), before the bus drivers are set to "on-bus" again.

In order to wake up other nodes of the system which are in sleep-mode, a special wake-up message with the dedicated, lowest possible IDENTIFIER (rrr rrrd rrrr; r = 'receive', d = 'dominant') may be used.

3. Message Transfer

3.1. Frame Types

Message transfer is manifested and controlled by four different frame types:

A *DATA FRAME* carries data from a transmitter to the receivers.

A *REMOTE FRAME* is transmitted by a bus unit to request the transmission of the DATA FRAME with the same IDENTIFIER.

An *ERROR FRAME* is transmitted by any unit on detecting a bus error.

An *OVERLOAD FRAME* is used to provide for an extra delay between the preceding and the succeeding DATA or REMOTE FRAMEs.

DATA FRAMEs and REMOTE FRAMEs are separated from preceding frames by an INTERFRAME SPACE.

3.1.1. DATA FRAME

A DATA FRAME (Fig.1) is composed of seven different bit fields:

START OF FRAME, ARBITRATION FIELD, CONTROL FIELD, DATA FIELD, CRC FIELD, ACK FIELD, END OF FRAME.

The DATA FIELD can be of length zero.

START OF FRAME (Fig. 1 and 2) marks the beginning of DATA FRAMEs and REMOTE FRAMEs. It consists of a single 'dominant' bit.

A station is only allowed to start transmission when the bus is idle (see BUS IDLE). All stations have to synchronize to the leading edge caused by START OF FRAME (see 'HARD SYNCHRONIZATION') of the station starting transmission first.

ARBITRATION FIELD
The ARBITRATION FIELD (Fig.2) consists of the IDENTIFIER and the RTR BIT.

IDENTIFIER
The IDENTIFIER's length is 11 bits. These bits are transmitted in the order from ID-10 to ID-0. The least significant bit is ID-0. The 7 most significant bits (ID-10 to ID-4) must not be all 'recessive'.

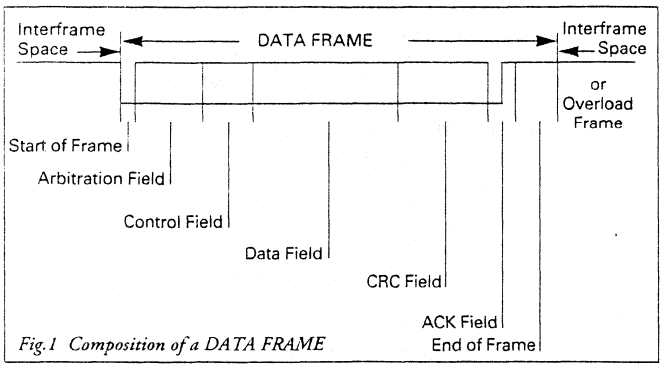


Fig.1 Composition of a DATA FRAME

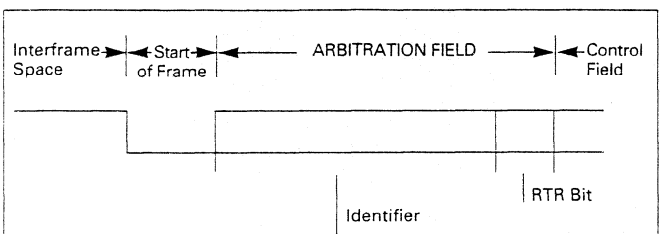


Fig.2 ARBITRATION FIELD

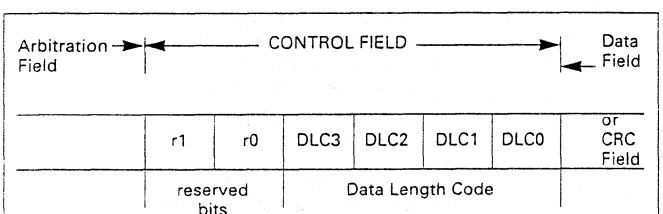


Fig.3 Composition of the CONTROL FIELD

Table 2. Coding of the number of data bytes by the DATA LENGTH CODE

abbreviations: d = 'dominant', r = 'recessive'

Number of Data Bytes	Data Length Code DLC3	DLC2	DLC1	DLC0
0	d	d	d	d
1	d	d	d	r
2	d	d	r	d
3	d	d	r	r
4	d	r	d	d
5	d	r	d	r
6	d	r	r	d
7	d	r	r	r
8	r	d	d	d

DATA FRAME: admissible numbers of data bytes: {0,1, ..., 7, 8}. Other values may not be used.

RTR BIT
(Remote Transmission Request BIT)
In DATA FRAMEs the RTR BIT has to be 'dominant'. Within a REMOTE FRAME the RTR BIT has to be 'recessive'.

CONTROL FIELD
The CONTROL FIELD (Fig.3) consists of six bits. It includes the DATA LENGTH CODE and two bits reserved for future expansion. The reserved bits have to be sent 'dominant'. Receivers accept 'dominant' and 'recessive' bits in all combinations.

DATA LENGTH CODE
The number of bytes in the DATA FIELD is indicated by the DATA LENGTH CODE (see Table 2). This DATA LENGTH CODE is 4 bits wide and is transmitted within the CONTROL FIELD (see Fig.3).

DATA FIELD
The DATA FIELD consists of the data to be transferred within a DATA FRAME. It can contain from 0 to 8 bytes, each containing 8 bits which are transferred MSB first.

CRC Field (Fig.4)
contains the CRC SEQUENCE followed by a CRC DELIMITER.

CRC SEQUENCE
The frame check sequence is derived from a cyclic redundancy code best suited for frames with bit counts less than 127 bits (BCH Code).

In order to carry out the CRC calculation, the polynomial to be divided is defined as the polynomial, the coefficients of which are given by the destuffed bit stream consisting of START OF FRAME, ARBITRATION FIELD, CONTROL FIELD, DATA FIELD (if present) and, for the 15 lowest coefficients, by 0. This polynomial is divided (the coefficients are calculated modulo-2) by the generator-polynomial:

$X^{15} + X^{14} + X^{10} + X^8 + X^7 + X^4 + + X^3 + 1$.

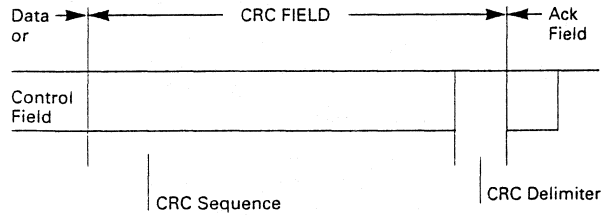


Fig.4 CRC FIELD

Table 3. Calculation of the CRC sequence

```
CRC_RG = 0;                                  // initialize shift register
REPEAT
  CRCNXT = NXTBIT EXOR CRC_RG (14);
  CRC_RG (14:1) = CRC_RG (13:0);             // shift left by
  CRC_RG (0) = 0;                            // 1 position
  IF CRCNXT THEN
    CRC_RG (14:0) = CRC_RG (14:0) EXOR (4599hex);
  ENDIF
UNTIL (CRC SEQUENCE starts or there is an ERROR condition)
```

After the transmission / reception of the last bit of the Data Field, CRC_RG contains the CRC sequence.

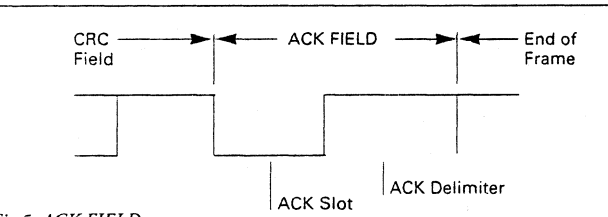


Fig.5 ACK FIELD

The remainder of this polynomial division is the CRC SEQUENCE transmitted over the bus. In order to implement this function, a 15 bit shift register CRC_RG (14:0) can be used. If NXTBIT denotes the next bit of the bit stream, given by the destuffed bit sequence from START OF FRAME until the end of the DATA FIELD, the CRC SEQUENCE is calculated as shown in Table 3.

CRC DELIMITER
The CRC SEQUENCE is followed by the CRC DELIMITER which consists of a single 'recessive' bit.

ACK FIELD
The ACK FIELD (Fig.5) is two bits long and contains the ACK SLOT and the ACK DELIMITER. In the ACK FIELD the transmitting station sends two 'recessive' bits.

A RECEIVER which has received a valid message correctly, reports this to the TRANSMITTER by sending a 'dominant' bit during the ACK SLOT (it sends 'ACK').

ACK SLOT
All stations having received the matching CRC SEQUENCE report this within the ACK SLOT by superscribing the 'recessive' bit of the TRANSMITTER by a 'dominant' bit.

ACK DELIMITER
The ACK DELIMITER is the second bit of the ACK FIELD and has to be a 'recessive' bit. As a consequence, the ACK SLOT is surrounded by two 'recessive' bits (CRC DELIMITER, ACK DELIMITER).

END OF FRAME
Each DATA FRAME and REMOTE FRAME is delimited by a flag sequence consisting of seven 'recessive' bits.

3.1.2. REMOTE FRAME

A station acting as a RECEIVER for certain data can initiate the transmission of the respective data by its source node by sending a REMOTE FRAME (see Fig.6, next page). A REMOTE FRAME is composed of six different bit fields:

START OF FRAME, ARBITRATION FIELD, CONTROL FIELD, CRC FIELD, ACK FIELD, END OF FRAME.

Contrary to DATA FRAMEs, the RTR bit of REMOTE FRAMEs is 'recessive'. There is no DATA FIELD, independent of the values of the DATA LENGTH CODE which may be signed any value within the admissible range 0...8. The value is the DATA LENGTH CODE of the corresponding DATA FRAME.

The polarity of the RTR bit indicates whether a transmitted frame is a DATA FRAME (RTR bit 'dominant') or a REMOTE FRAME (RTR bit 'recessive').

3.1.3. ERROR FRAME

The ERROR FRAME (Fig.7, next page) consists of two different fields. The first field is given by the superposition of ERROR FLAGS contributed from different stations. The following second field is the ERROR DELIMITER.

In order to terminate an ERROR FRAME correctly, an 'error passive' node may need the bus to be 'bus idle' for at least 3 bit times (if there is a local error at an 'error passive' receiver). Therefore, the bus should not be loaded to 100%.

Error Flag

There are 2 forms of an ERROR FLAG: an ACTIVE ERROR FLAG and a PASSIVE ERROR FLAG.

1. The ACTIVE ERROR FLAG consists of six consecutive 'dominant' bits.

2. The PASSIVE ERROR FLAG consists of six consecutive 'recessive' bits unless it is overwritten by 'dominant' bits from other nodes.

An 'error active' station detecting an error condition signals this by transmission of an ACTIVE ERROR FLAG. The ERROR FLAG's form violates the law of bit stuffing (see CODING) applied to all fields from START OF FRAME to CRC DELIMITER or destroys the fixed form ACK FIELD or END OF FRAME field. As a consequence, all other stations detect an error condition and on their part start transmission of an ERROR FLAG. So the sequence of 'dominant' bits which actually can be monitored on the bus results from a superposition of different ERROR FLAGs transmitted by individual stations. The total length of this sequence varies between a minimum of six and a maximum of twelve bits.

An 'error passive' station detecting an error condition tries to signal this by transmission of a PASSIVE ERROR FLAG. The 'error passive' station waits for six consecutive bits of equal polarity, beginning at the start of the PASSIVE ERROR FLAG. The PASSIVE ERROR FLAG is complete when these 6 equal bits have been detected.

Error Delimiter

The ERROR DELIMITER consists of eight 'recessive' bits.

After transmission of an ERROR FLAG, each station sends 'recessive' bits and monitors the bus until it detects a 'recessive' bit. Afterwards it starts transmitting seven more 'recessive' bits.

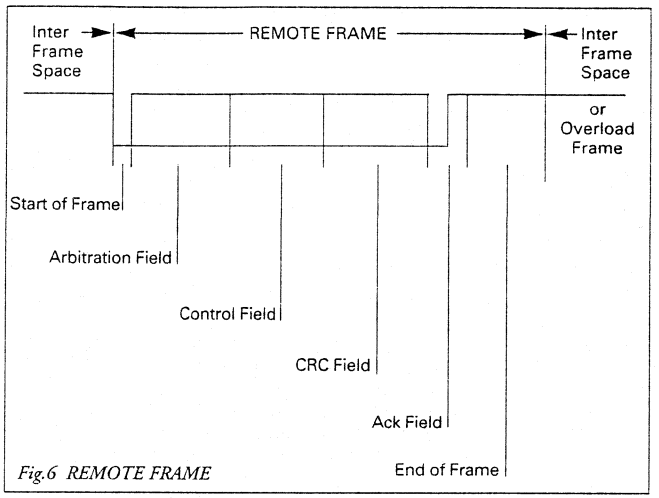


Fig.6 REMOTE FRAME

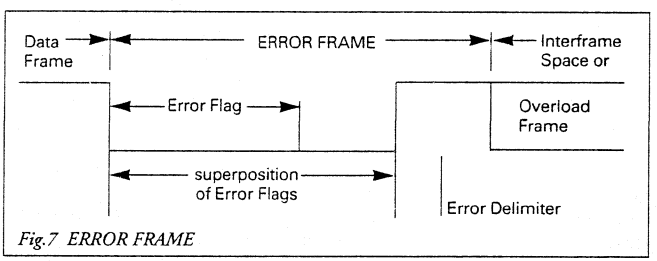


Fig.7 ERROR FRAME

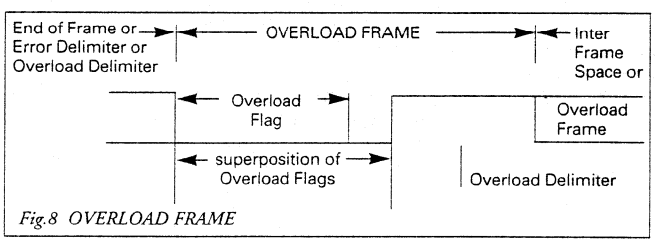


Fig.8 OVERLOAD FRAME

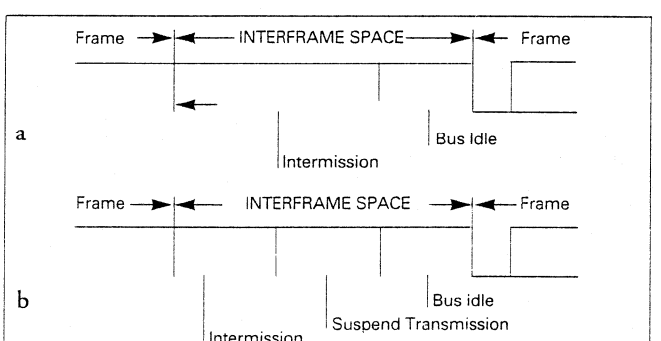


Fig.9 INTERFRAME SPACE

a) for not 'error passive' stations or those having been TRANSCEIVER of the previous message
b) for 'error passive' stations having been TRANSMITTER of the previous message

3.1.4. Overload Frame

The OVERLOAD FRAME (Fig.8) contains the two bit fields OVERLOAD FLAG and OVERLOAD DELIMITER.

There are two kinds of OVERLOAD conditions which both lead to the transmission of an OVERLOAD FLAG:

1. The internal conditions of a receiver which requires a delay of the next DATA FRAME or REMOTE FRAME.
2. Detection of a 'dominant' bit during INTERMISSION.

An OVERLOAD FRAME due to OVERLOAD condition 1 is only allowed to be started at the first bit time of an expected INTERMISSION, whereas OVERLOAD FRAMEs due to OVERLOAD condition 2 start one bit after detecting the 'dominant' bit.

At most, two OVERLOAD FRAMEs may be generated to delay the next DATA or REMOTE FRAME.

Overload Flag
consists of six 'dominant' bits. The overall form corresponds to that of the ACTIVE ERROR FLAG.

The OVERLOAD FLAG's form destroys the fixed form of the INTERMISSION field. As a consequence, all other stations also detect an OVERLOAD condition and on their part start transmission of an OVERLOAD FLAG. (In case that there is a 'dominant' bit detected during the 3rd bit of INTERMISSION locally at some node, the other nodes will not interpret the OVERLOAD FLAG correctly, but interpret the first of these six 'dominant' bits as START OF FRAME. The sixth 'dominant' bit violates the rule of bit stuffing causing an error condition).

OVERLOAD DELIMITER
consists of eight 'recessive' bits.

The OVERLOAD DELIMITER is of the same form as the ERROR DELIMITER. After transmission of an OVERLOAD FLAG the station monitors the bus until it detects a transition from a 'dominant' to a 'recessive' bit. At this point of time every bus station has finished sending its OVERLOAD FLAG and all stations start transmission of seven more 'recessive' bits in coincidence.

3.1.5. Interframe Spacing

DATA FRAMEs and REMOTE FRAMEs are separated from preceding frames whatever type they are (DATA FRAME, REMOTE FRAME, ERROR FRAME, OVERLOAD FRAME) by a bit field called INTERFRAME SPACE. In contrast, OVERLOAD FRAMEs and ERROR FRAMEs are not preceded by an INTERFRAME SPACE and multiple OVERLOAD FRAMEs are not separated by an INTERFRAME SPACE.

Interframe Space
contains the bit fields INTERMISSION and BUS IDLE and, for 'error passive' stations which have been TRANSMITTER of the previous message, SUSPEND TRANSMISSION.

Fig.9 shows the INTERFRAME SPACE structure for stations which are not 'error passive' or have been RECEIVER of the previous message (Fig.9a), as well as for 'error passive' stations which have been TRANSMITTER of the previous message (Fig.9b).

INTERMISSION
consists of three 'recessive' bits.

During INTERMISSION no station is allowed to start transmission of a DATA FRAME or REMOTE FRAME. The only action to be taken is signalling an OVERLOAD condition.

BUS IDLE
The period of BUS IDLE may be of arbitrary length. The bus is recognized to be free and any station having something to transmit can access the bus. A message which is pending for transmission during the transmission of another message is started in the first bit following INTERMISSION.

The detection of a 'dominant' bit on the bus is interpreted as START OF FRAME.

SUSPEND TRANSMISSION
After an 'error passive' station has transmitted a message, it sends eight 'recessive' bits following INTERMISSION, before starting to transmit a further message or recognizing the bus to be idle. If meanwhile a transmission (caused by another station) starts, the station will become receiver of this message.

3.2.Definition of TRANSMITTER /RECEIVER

Transmitter
A unit originating a message is called "TRANSMITTER" of that message. The unit stays TRANSMITTER until the bus is idle or the unit loses ARBITRATION.

Receiver
A unit is called "RECEIVER" of a message, if it is not Transmitter of that message and the bus is not idle.

4. Message Validation

The point of time at which a message is taken to be valid, is different for the transmitter and the receivers of the message.

Transmitter:
The message is valid for the transmitter, if there is no error until the end of END OF FRAME. If a message is corrupted, retransmission will follow automatically and according to prioritization. In order to be able to compete for bus access with other messages, retransmission has to start as soon as the bus is idle.

Receivers:
The message is valid for the receivers, if there is no error until

the last but one bit of END OF FRAME.

5. Coding

Bit Stream Coding

The frame segments START OF FRAME, ARBITRATION FIELD, CONTROL FIELD, DATA FIELD and CRC SEQUENCE are coded by the method of bit stuffing. Whenever a transmitter detects five consecutive bits of identical value in the bit stream to be transmitted, it automatically inserts a complementary bit in the actual transmitted bit stream.

The remaining bit fields of the DATA FRAME or REMOTE FRAME (CRC DELIMITER, ACK FIELD and END OF FRAME) are of fixed form and not stuffed. The ERROR FRAME and the OVERLOAD FRAME are of fixed form as well and not coded by the method of bit stuffing.

The bit stream in a message is coded according to the Non-Return-to-Zero (NRZ) method. This means that, during the total bit time, the generated bit level is either 'dominant' or 'recessive'.

6. Error Handling

6.1. Error Detection

There are 5 different error types (which are not mutually exclusive):

- ***Bit Error***
  A unit that is sending a bit on the bus also monitors the bus. A BIT ERROR has to be detected at the bit time, when the bit value that is monitored is different from the bit value that is sent. An exception is the sending of a 'recessive' bit during the stuffed bit stream of the ARBITRATION FIELD or during the ACK SLOT. Then no BIT ERROR occurs when a 'dominant' bit is monitored. A TRANSMITTER sending a PASSIVE ERROR FLAG and detecting a 'dominant' bit does not interprete this as a BIT ERROR.

- ***Stuff Error***
  A STUFF ERROR has to be detected at the bit time of the 6th consecutive equal bit level in a message field that should be coded by the method of bit stuffing.

- ***CRC Error***
  The CRC sequence consists of the result of the CRC calculation by the transmitter. The receivers calculate the CRC in the same way as the transmitter. A CRC ERROR has to be detected, if the calculated result is not the same as that received in the CRC sequence.

- ***Form Error***
  A FORM ERROR has to be detected when a fixed-form bit field contains one or more illegal bits.

- ***Acknowledgement Error***
  An ACKNOWLEDGEMENT ERROR has to be detected by a transmitter whenever it does not monitor a 'dominant' bit during ACK SLOT.

6.2. Error Signalling

A station detecting an error condition signals this by transmitting an ERROR FLAG. For an 'error active' node it is an ACTIVE ERROR FLAG, for an 'error passive' node it is a PASSIVE ERROR FLAG.

Whenever a BIT ERROR, a STUFF ERROR, a FORM ERROR or an ACKNOWLEDGEMENT ERROR is detected by any station, transmission of an ERROR FLAG is started at the respective station at the next bit.

Whenever a CRC ERROR is detected, transmission of an ERROR FLAG starts at the bit following the ACK DELIMITER, unless an ERROR FLAG for another error condition has already been started.

7. Fault Confinement

With respect to fault confinement, a unit may be in one of three states:

- 'error active',
- 'error passive',
- 'bus off'.

An 'error active' unit can normally take part in bus communication and sends an ACTIVE ERROR FLAG when an error has been detected.

An 'error passive' unit must not send an ACTIVE ERROR FLAG. It takes part in bus communication, but when an error has been detected only a PASSIVE ERROR FLAG is sent. Also after a transmission, an 'error passive' unit will wait before initiating a further transmission. (See SUSPEND TRANSMISSION)

A 'bus off' unit is not allowed to have any influence on the bus. (E.g. output drivers switched off.)

For fault confinement, two counts are implemented in every bus unit:

1) TRANSMITTER ERROR COUNT
2) RECEIVE ERROR COUNT

These counts are modified according to the following rules:

(note that more than one rule may apply during a given message transfer)

1. When a RECEIVER detects an error, the RECEIVE ERROR COUNT will be increased by 1, except when the detected error was a BIT ERROR during the sending of an ACTIVE ERROR FLAG or an OVERLOAD FLAG.

2. When a RECEIVER detects a 'dominant' bit as the first bit after sending an ERROR FLAG, the RECEIVE ERROR COUNT will be increased by 8.

3. When a TRANSMITTER sends

an ERROR FLAG, the TRANSMIT ERROR COUNT is increased by 8.

Exception 1:
If the TRANSMITTER is 'error passive' and detects an ACKNOWLEDGEMENT ERROR because of not detecting a 'dominant' ACK and does not detect a 'dominant' bit while sending its PASSIVE ERROR FLAG.

Exception 2:
If the TRANSMITTER sends an ERROR FLAG because a STUFF ERROR occured during ARBITRATION whereby the STUFF-BIT is located before the RTR bit, and should have been 'recessive', and has been sent as 'recessive' but monitored as 'dominant'.

In exceptions 1 and 2, the TRANSMIT ERROR COUNT is not changed.

4. If a TRANSMITTER detects a BIT ERROR while sending an ACTIVE ERROR FLAG or an OVERLOAD FLAG, the TRANSMIT ERROR COUNT is increased by 8.

5. If a RECEIVER detects a BIT ERROR while sending an ACTIVE ERROR FLAG or an OVERLOAD FLAG, the RECEIVE ERROR COUNT is increased by 8.

6. Any node tolerates up to 7 consecutive 'dominant' bits after sending an ACTIVE ERROR FLAG, PASSIVE ERROR FLAG or OVERLOAD FLAG. After detecting the 14th consecutive 'dominant' bit (in case of an ACTIVE ERROR FLAG or an OVERLOAD FLAG) or after detecting the 8th consecutive 'dominant' bit following a PASSIVE ERROR FLAG, and after each sequence of additional eight consecutive 'dominant' bits, every TRANSMITTER increases its TRANSMIT ERROR COUNT by 8 and every RECEIVER increases its RECEIVE ERROR COUNT by 8.

7. After the successful transmission of a message (getting ACK and no error until END OF FRAME is finished), the TRANSMIT ERROR COUNT is decreased by 1 unless it was already 0.

8. After the successful reception of a message (reception without error up to the ACK SLOT and the successful sending of the ACK bit), the RECEIVE ERROR COUNT is decreased by 1, if it was between 1 and 127. If the RECEIVE ERROR COUNT was 0, it stays 0, and if it was greater than 127, then it will be set to a value between 119 and 127.

9. A node is 'error passive' when the TRANSMIT ERROR COUNT equals or exceeds 128, or when the RECEIVE ERROR COUNT equals or exceeds 128. An error condition letting a node become 'error passive' causes the node to send an ACTIVE ERROR FLAG.

10. A node is 'bus off' when the TRANSMIT ERROR COUNT is greater than or equal to 256.

11. An 'error passive' node becomes 'error active' again when both the TRANSMIT ERROR COUNT and the RECEIVE ERROR COUNT are less or equal to 127.

12. A node which is 'bus off' is permitted to become 'error active' (no longer 'bus off') with its error counters both set to 0 after 128 occurrances of 11 consecutive 'recessive' bits have been monitored on the bus.

Note:
An error count value greater than about 96 indicates a heavily disturbed bus. It may be of advantage to provide means to test for this condition.

Note:
Start-up / Wake-up:
If during system start-up only one node is online, and if this node transmits some message, it will get no acknowledgement, detect an error and repeat the message. It can become 'error passive' but not 'bus off' due to this reason.

8. Bit Timing Requirements

Nominal Bit Rate:
The Nominal Bit Rate is the number of bits per second transmitted in the absence of resynchronization by an ideal transmitter.

Nominal Bit Time:

Nominal Bit Time
= 1 / Nominal Bit Rate

The Nominal Bit Time can be thought of as being divided into separate non-overlapping time segments forming the bit time as shown in Fig.10:

- SYNCHRONIZATION SEGMENT (SYNC_SEG),
- PROPAGATION TIME SEGMENT (PROP_SEG),
- PHASE BUFFER SEGMENT 1 (PHASE_SEG1),
- PHASE BUFFER SEGMENT 2 (PHASE_SEG2).

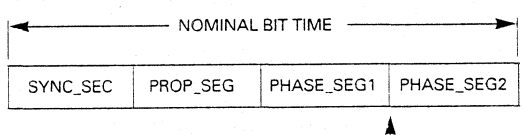


Fig.10 Partition of the Bit Time

SYNC SEG
This part of the bit time is used to synchronize the various nodes on the bus. An edge is expected to lie within this segment.

PROP SEG
This part of the bit time is used to compensate for the physical delay times within the network. It is twice the sum of the signal's propagation time on the bus line, the input comparator delay, and the output driver delay.

PHASE SEG1, PHASE SEG2
These Phase-Buffer-Segments are used to compensate for edge phase errors. These segments can be lengthened or shortened by resynchronization.

SAMPLE POINT
The SAMPLE POINT is the point of time at which the bus level is read and interpreted as the value of that respective bit. It's location is at the end of PHASE_SEG1.

INFORMATION PROCESSING TIME
The INFORMATION PROCESSING TIME is the time segment starting with the SAMPLE POINT reserved for calculation of the subsequent bit level.

TIME QUANTUM
The TIME QUANTUM is a fixed unit of time derived from the oscillator period. There exists a programmable prescaler with integral values, ranging at least from 1 to 32. Starting with the MINIMUM TIME QUANTUM, the TIME QUANTUM can have a length of

TIME QUANTUM
= m x MINIMUM TIME QUANTUM

with m the value of the prescaler.

Length of Time Segments

- SYNC_SEG is 1 TIME QUANTUM long.
- PROP_SEG is programmable to be 1, 2, ..., 8 TIME QUANTA long.
- PHASE_SEG1 is programmable to be 1, 2, ..., 8 TIME QUANTA long.
- PHASE_SEG2 is the maximum of PHASE_SEG1 and the INFORMATION PROCESSING TIME.
- The INFORMATION PROCESSING TIME is less than or equal to 2 TIME QUANTA long.

The total number of TIME QUANTA in a bit time has to be programmable at least from 8 to 25.

Synchronization

HARD SYNCHRONIZATION
After a HARD SYNCHRONIZATION the internal bit time is restarted with SYNC_SEG. Thus, HARD-SYNCHRONIZATION forces the edge which has caused the HARD-SYNCHRONIZATION to lie within the SYNCHRONIZATION SEGMENT of the restarted bit time.

RESYNCHRONIZATION JUMP WIDTH
As a result of RESYNCHRONIZATION, PHASE_SEG1 may be lengthened or PHASE_SEG2 may be shortened. The amount of lengthening or shortening of the PHASE BUFFER SEGMENTs has an upper bound given by the RESYNCHRONIZATION JUMP WIDTH. The RESYNCHRONIZATION JUMP WIDTH shall be programmable between 1 and min (4, PHASE_SEG1).

Clocking information may be derived from transitions from one bit value to the other. The property that only a fixed maximum number of successive bits have the same value provides the possibility of resynchronizing a bus unit to the bit stream during a frame. The maximum length between two transitions which can be used for resynchronization is 29 bit times.

PHASE ERROR of an edge
The PHASE ERROR of an edge is given by the position of the edge relative to SYNC_SEG, measured in TIME QUANTA. The sign of PHASE ERROR is defined as follows:

- e = 0, if the edge lies within SYNC_SEG.
- e > 0, if the edge lies before the SAMPLE POINT.
- e < 0, if the edge lies after the SAMPLE POINT of the previous bit.

RESYNCHRONIZATION
The effect of a RESYNCHRONIZATION is the same as that of a HARD SYNCHRONIZATION, when the magnitude of the PHASE ERROR of the edge which causes the RESYNCHRONIZATION is less than or equal to the programmed value of the RESYNCHRONIZATION JUMP WIDTH.

When the magnitude of the PHASE ERROR is larger than the RESYNCHRONIZATION JUMP WIDTH,

- and if the PHASE ERROR is *positive*, then PHASE_SEG1 is *lengthened* by an amount equal to the RESYNCHRONIZATION JUMP WIDTH.
- and if the PHASE ERROR is *negative*, then PHASE_SEG2 is *shortened* by an amount equal to the RESYNCHRONIZATION JUMP WIDTH.

Synchronization Rules
HARD SYNCHRONIZATION and RESYNCHRONIZATION are the two forms of SYNCHRONIZATION. They obey the following rules:

1. Only one SYNCHRONIZATION within one bit time is allowed.
2. An edge will be used for SYNCHRONIZATION only if the value detected at the previous SAMPLE POINT (previous read bus value) differs from the bus value immediately after the edge.
3. HARD SYNCHRONIZATION is performed whenever there is a 'recessive' to 'dominant' edge during BUS IDLE.

4. All other 'recessive' to 'dominant' edges (and optionally 'dominant' to 'recessive' edges in case of low bit rates) fulfilling the rules 1 and 2 will be used for RESYNCHRONIZATION with the exception that a node transmitting a dominant bit will not perform a RESYNCHRONIZATION as a result of a 'recessive' to 'dominant' edge with a positive PHASE ERROR, if only 'recessive' to 'dominant' edges are used for RESYNCHRONIZATION.

9. Increasing CAN Oscillator Tolerance

This section describes an upward compatible modification of the CAN protocol, as specified in sections 1 to 8.

9.1. Protocol Modifications

In order to increase the maximum oscillator tolerance from the 0.5% currently possible to 1.5%, the following modifications, being upward compatible to the existing CAN specification, are necessary:

[1] If a CAN node samples a dominant bit at the third bit of INTERMISSION, then it will interpret this bit as a START OF FRAME bit.

[2] If a CAN node has a message waiting for transmission and it samples a dominant bit at the third bit of INTERMISSION, it will interpret this as a START OF FRAME bit, and, with the next bit, start transmitting its message with the first bit of its IDENTIFIER without first transmitting a START OF FRAME bit and without becoming receiver.

[3] If a CAN node samples a dominant bit at the eighth bit (the last bit) of an ERROR DELIMITER or OVERLOAD DELIMITER, it will, at the next bit, start transmitting an OVERLOAD FRAME (not an ERROR FRAME). The Error Counters will not be incremented.

[4] Only recessive to dominant edges will be used for synchronization.

In agreement with the existing specification, the following rules are still valid:

[5] All CAN controllers synchronize on the START OF FRAME bit with a hard synchronization.

[6] No CAN controller will send a START OF FRAME bit until it has counted three recessive bits of INTERMISSION.

This modifications allow a maximum oscillator tolerance of 1.58% and the use of a ceramic resonator at a bus speed of up to 125 Kbits per second. For the full bus speed range of the CAN protocol, still a quartz oscillator is required. The compatibility of the enhanced and the existing protocol is maintained, as long as:

[7] CAN controllers with the enhanced and existing protocols, used in one and the same network, have all to be provided with a quartz oscillator.

The chip with the highest requirement for its oscillator accuracy determines the oscillator accuracy which is required from all the other nodes. Ceramic resonators can only be used when all the nodes in the network use the enhanced protocol.

– End of PART A –

Contents, PART B

1. Introduction

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed realtime control with a very high level of security. Its domain of application ranges from high speed networks to low cost multiplex wiring.

In automotive electronics, engine control units, sensors, anti-skid-systems, etc. are connected using CAN with bit rates up to 1 Mbit/s.

At the same time it is cost effective to build into vehicle body electronics, e. g. lamp clusters, electric windows etc. to replace the wiring harness otherwise required.

The intention of this specification is to achieve compatibility between any two CAN implementations. Compatibility, however, has different aspects regarding e. g. electrical features and the interpretation of data to be transferred. To achieve design transparency and implementation flexibility, CAN has been subdivided into different layers according to the ISO/OSI Reference Model:

- the Data Link Layer
  - the Logical Link Control (LLC) sublayer
  - the Medium Access Control (MAC) sublayer
- the Physical Layer

Note that in previous versions of the CAN Specification, the services and functions of the LLC and MAC sublayers of the Data Link Layer had been described in layers denoted as 'object layer' and 'transfer layer'. The scope of the LLC sublayer is

- to provide services for data transfer and for remote data request,
- to decide which messages received by the LLC sublayer are actually to be accepted,
- to provide means for recovery management and overload notifications.

There is much freedom in defining object handling. The scope of the MAC sublayer mainly is the transfer protocol, i. e. controlling the Framing, performing Arbitration, Error Checking, Error Signalling and Fault Confinement. Within the MAC sublayer it is decided whether the bus is free for starting a new transmission or whether a reception is just starting. Also some general features of the bit timing are regarded as part of the MAC sublayer. It is in the nature of the MAC sublayer that there is no freedom for modifications.

The scope of the physical layer is the actual transfer of the bits between the different nodes with respect to all electrical properties. Within one network the physical layer, of course, has to be the same for all nodes. There may be, however, much freedom in selecting a physical layer.

The scope of this specification is to define the MAC sublayer and a small part of the LLC sublayer of the Data Link Layer and to describe the consequences of the CAN protocol on the surrounding layers.

2. Basic Concepts

CAN has the following properties:

- prioritization of messages
- guarantee of latency times
- configuration flexibility
- multicast reception with time synchronization
- system wide data consistency
- multimaster
- error detection and error signalling
- automatic retransmission of corrupted messages as soon as the bus is idle again
- distinction between temporary errors and permanent failures of nodes and autonomous switching off of defect nodes.

Layered Architecture of CAN according to the OSI Reference Model (Fig.1)

- The Physical Layer defines how signals are actually transmitted and therefore deals with the description of Bit Timing, Bit Encoding, and Synchronization. Within this specification, the Driver/Receiver Characteristics of the Physical Layer are not defined so as to allow transmission medium and signal level implementations to be optimized for their application.
- The MAC sublayer represents the kernel of the CAN protocol. It presents messages received

from the LLC sublayer and accepts messages to be transmitted to the LLC sublayer. The MAC sublayer is responsible for Message Framing, Arbitration, Acknowledgement, Error Detection and Signalling. The MAC sublayers are supervised by a management entity called Fault Confinement which is a self-checking mechanism for distinguishing short disturbances from permanent failures.

- The LLC sublayer is concerned with Message Filtering, Overload Notification and Recovery Management.

The scope of this specification is to define the Data Link Layer and the consequences of the CAN protocol on the surrounding layers.

Messages
Information on the bus is sent in fixed format messages of different but limited length (see section 3: Message Transfer). When the bus is free, any connected unit may start to transmit a new message.

Information Routing
In CAN systems a CAN node does not make use of any information about the system configuration (e.g. station addresses). This has several important consequences:

System Flexibility: Nodes can be added to the CAN network without requiring any changes in the software or hardware of any node and application layer.

Message Routing: The content of a message is named by an IDENTIFIER. The IDENTIFIER does not indicate the destination of the message, but describes the meaning of the data, so that all nodes in the network are able to decide by Message Filtering whether the data is to be acted upon by them or not.

Multicast: As a consequence of the concept of Message Filtering, any number of nodes can receive and simultaneously act upon the same message.

Data Consistency: Within a CAN network it is guaranteed that a message is simultaneously accepted either by all nodes or by no node. Thus, data consistency of a system is achieved by the concepts of multicast and by error handling.

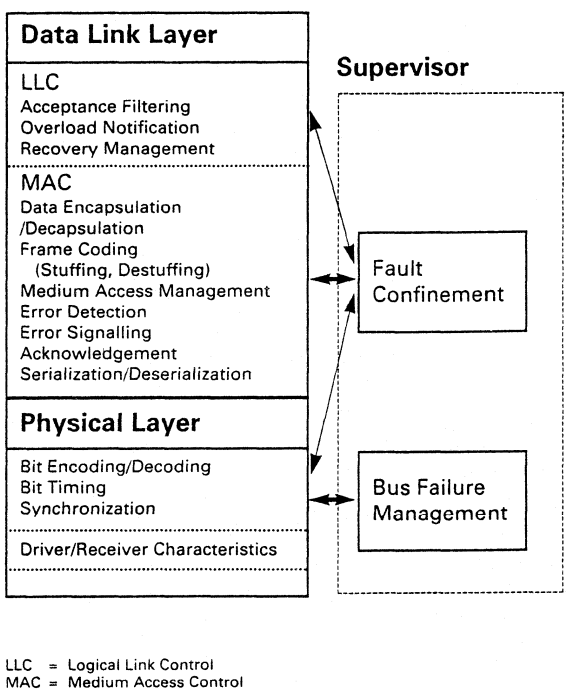


Fig. 1 Layered Architecture of CAN according to the OSI Reference Model

Bit rate
The speed of CAN may be different in different systems. However, in a given system the bit-rate is uniform and fixed.

Priorities
The IDENTIFIER defines a static message priority during bus access.

Remote Data Request
By sending a REMOTE FRAME, a node requiring data may request another node to send the corresponding DATA FRAME. The DATA FRAME and the corresponding REMOTE FRAME are named by the same IDENTIFIER.

Multimaster
When the bus is free, any unit may start to transmit a message. The unit with the message of highest priority to be transmitted gains bus access.

Arbitration
Whenever the bus is free, any unit may start to transmit a message. If 2 or more units start transmitting messages at the same time, the bus access conflict is resolved by bitwise arbitration using the IDENTIFIER. The mechanism of arbitration guarantees that neither

information nor time is lost. If a DATA FRAME and a REMOTE FRAME with the same IDENTIFIER are initiated at the same time, the DATA FRAME prevails over the REMOTE FRAME. During arbitration, every transmitter compares the level of the bit transmitted with the level that is monitored on the bus. If these levels are equal, the unit may continue to send. When a 'recessive' level is sent and a 'dominant' level is monitored (see Bus Values), the unit has lost arbitration and must withdraw without sending one more bit.

Safety
In order to achieve the utmost safety of data transfer, powerful measures for error detection, signalling and self-checking are implemented in every CAN node.

Error Detection
For detecting errors, the following measures have been taken:

- Monitoring (transmitters compare the bit levels to be transmitted with the bit levels detected on the bus),
- Cyclic Redundancy Check,
- Bit Stuffing,
- Message Frame Check.

Performance of Error Detection
The error detection mechanisms have the following properties:

- all global errors are detected.
- all local errors at transmitters are detected.
- up to 5 randomly distributed errors in a message are detected.
- burst errors of length less than 15 in a message are detected.
- errors of any odd number in a message are detected.

Total residual error probability for undetected corrupted messages:

less than

message error rate $\times 4.7 \cdot 10^{-11}$.

Error Signalling and Recovery Time
Corrupted messages are flagged by any node detecting an error. Such messages are aborted and will be retransmitted automatically. The recovery time from detecting an error until the start of the next message is at most 31 bit times, if there is no further error.

Fault Confinement
CAN nodes are able to distinguish short disturbances from permanent failures. Defective nodes are switched off.

Connections
The CAN serial communication link is a bus to which a number of units may be connected. This number has no theoretical limit. Practically the total number of units will be limited by delay times and / or electrical loads on the bus line.

Single Channel
The bus consists of a single bidirectional channel that carries bits. From this data, resynchronization information can be derived. The way in which this channel is implemented is not fixed in this specification. E. g. single wire (plus ground), two differential wires, optical fibres, etc. may be used.

Bus values
The bus can have one of two complementary logical values: 'dominant' or 'recessive'. During simultaneous transmission of 'dominant' and 'recessive' bits, the resulting bus value will be 'dominant'. For example, in case of a wired-AND implementation of the bus, the 'dominant' level would be represented by a logical '0' and the 'recessive' level by a logical '1'. Physical states (e.g. electrical voltage, light) that represent the logical levels are not given in this specification.

Acknowledgement
All receivers check the consistency of the message being received and will acknowledge a consistent message and flag an inconsistent message.

Sleep Mode / Wake-up
To reduce the system's power consumption, a CAN device may be set into sleep mode without any internal activity and with disconnected bus drivers. The sleep mode is finished with a wake-up by any bus activity or by internal conditions of the system. On wake-up, the internal activity is restarted, although the MAC sublayer will be waiting for the system's oscillator to stabilize and it will then wait until it has synchronized itself to the bus activity (by checking for eleven consecutive 'recessive' bits), before the bus drivers are set to "on-bus" again.

Oscillator Tolerance
The Bit Timing requirements allow ceramic resonators to be used in applications with transmission rates of up to 125 kbit/s as a rule of thumb; for a more precise evaluation refer to

Dais, S.; Chapman, M:
"Impact of Bit Representation on Transport Capacity and Clock Accuracy in Serial Data Streams"
SAE Technical Paper Series 890532,
Multiplexing in Automobil SP-773, March 1989.

For the full bus speed range of the CAN protocol, a quartz oscillator is required.

3. Message Transfer

3.1. Frame Formats

There are two different formats which differ in the length of the IDENTIFIER field: Frames with the number of 11 bit IDENTIFIER are denoted *Standard Frames*.
In contrast, frames containing 29 bit IDENTIFIER are denoted *Extended Frames*.

3.2. Frame Types

Message transfer is manifested and controlled by four different frame types:

A *DATA FRAME*
carries data from a transmitter to the receivers.

A *REMOTE FRAME*
is transmitted by a bus unit to request the transmission of the DATA FRAME with the same IDENTIFIER.

An *ERROR FRAME*
is transmitted by any unit on detecting a bus error.

An *OVERLOAD FRAME*
is used to provide for an extra delay between the preceding and the succeeding DATA or REMOTE FRAMEs.

DATA FRAMEs and REMOTE FRAMES can be used both in *Standard Frame* Format and *Extended Frame* Format; they are separated from preceding frames by an INTERFRAME SPACE.

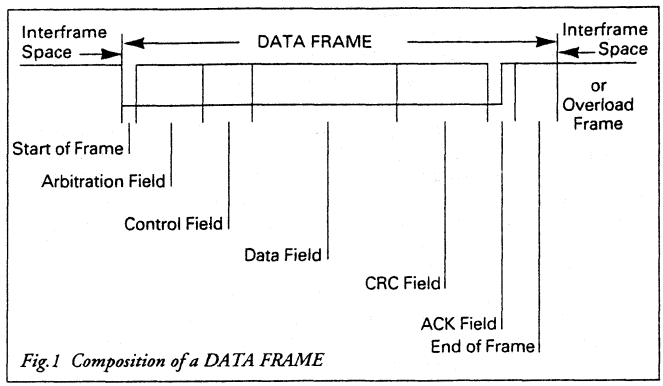


Fig.1 Composition of a DATA FRAME

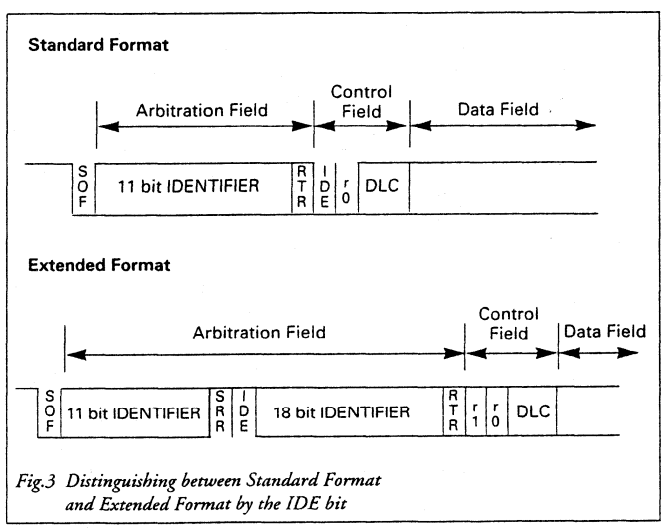


Fig.3 Distinguishing between Standard Format and Extended Format by the IDE bit

3.2.1 Data Frame

A DATA FRAME (Fig.2) is composed of seven different bit fields:

START OF FRAME, ARBITRATION FIELD, CONTROL FIELD, DATA FIELD, CRC FIELD, ACK FIELD, END OF FRAME. The DATA FIELD can be of length zero.

Start of Frame (*Standard Format* as well as *Extended Format*)

The START OF FRAME (SOF) marks the beginning of DATA FRAMEs and REMOTE FRAMEs. It consists of a single 'dominant' bit (see Fig. 2 and 3).

A station is only allowed to start transmission when the bus is idle (see 'INTERFRAME Spacing'). All stations have to synchronize to the leading edge caused by START OF FRAME (see 'HARD SYNCHRONIZATION') of the station starting transmission first.

Arbitration Field
The format of the ARBITRATION FIELD is different for *Standard Format* and *Extended Format* Frames:

- In *Standard Format* the ARBITRATION FIELD consists of the 11 bit IDENTIFIER and the RTR-BIT. The IDENTIFIER bits are denoted ID-28 ... ID-18.
- In *Extended Format* the ARBITRATION FIELD consists of the 29 bit IDENTIFIER, the SRR-Bit, the IDE-Bit, and the RTR-BIT. The IDENTIFIER bits are denoted ID-28 ... ID-0.

In order to distinguish between Standard Format and Extended Format, the reserved bit r1 in previous CAN Specifications, versions 1.0 to 1.2, now is denoted as IDE Bit (compare Fig.3).

IDENTIFIER

IDENTIFIER – *Standard Format:*

The IDENTIFIER's length is 11 bits and corresponds to the *Base ID* in *Extended Format.* These bits are transmitted in the order from ID-28 to ID-18. The least significant bit is ID-18. The 7 most significant bits (ID-28 to ID-22) must not be all 'recessive'.

IDENTIFIER – *Extended Format:*

In contrast to the Standard Format, the Extended Format consists of 29 bits. The format comprises two sections:

- the *Base ID* with 11 bits,
- the *Extended ID* with 18 bits.

Base ID
The Base ID consists of 11 bits. It is transmitted in the order from ID-28 to ID-18. It is equivalent to the format of the Standard Identifier. The Base ID defines the Extended Frame's *base priority.*

Extended ID
The Extended ID consists of 18 bits. It is transmitted in the order of ID-17 to ID-0.

In a standard Frame, the IDENTIFIER is followed by the RTR bit.

RTR BIT (*Standard Format* as well as *Extended Format*)
(Remote Transmission Request)

In DATA FRAMEs the RTR BIT has to be 'dominant'. Within a REMOTE FRAME the RTR BIT has to be 'recessive'.

In an Extended Frame the Base ID is transmitted first, followed by the IDE bit and the SRR bit. The Extended ID is transmitted after the SRR bit.

SRR BIT (*Extended Format*)
(Substitute Remote Request)

The SRR bit is a recessive bit. It is transmitted in Extended Frames at the position of the RTR bit in Standard Frames and so substitutes the RTR bit in the Standard Frame.

Therefore, collisions of a Standard Frame and an Extended Frame, the Base ID (see 'Extended IDENTIFIER' below) of which is the same as the Standard Frame's Identifier, are resolved in such a way that the Standard Frame prevails the Extended Frame.

IDE BIT *(Extended Format)*
(Identifier Extension Bit)

The IDE Bit belongs to

- the ARBITRATION FIELD for the *Extended Format,*
- the CONTROL FIELD for the *Standard Format.*

The IDE bit in the Standard Format is transmitted 'dominant', whereas in the Extended Format the IDE bit is recessive.

CONTROL FIELD (*Standard Format* as well as *Extended Format*)

The CONTROL FIELD (see Fig.4) consists of six bits. The format of the CONTROL FIELD is different for *Standard Format* and *Extended Format.* Frames in Standard Format include the DATA LENGTH CODE, the IDE bit which is transmitted 'dominant' (see above), and the reserved bit r0. Frames in Extended Format include the DATA LENGTH CODE and two reserved bits r1 and r0. The reserved bits have to be sent 'dominant', but Receivers accept 'dominant' and 'recessive' bits in all combinations.

DATA LENGTH CODE (*Standard Format* as well as *Extended Format*)

The number of bytes in the DATA FIELD is indicated by the DATA LENGTH CODE. This DATA LENGTH CODE is 4 bits wide and is transmitted within the CONTROL FIELD (see Fig.4 and Table 1).

DATA FIELD (*Standard Format* as well as *Extended Format*)

The DATA FIELD consists of the data to be transferred within a DATA FRAME. It can contain from 0 to 8 bytes, each containing 8 bits which are transferred MSB first.

CRC FIELD (Fig.5, *Standard Format* as well as *Extended Format*)

contains the CRC SEQUENCE followed by a CRC DELIMITER.

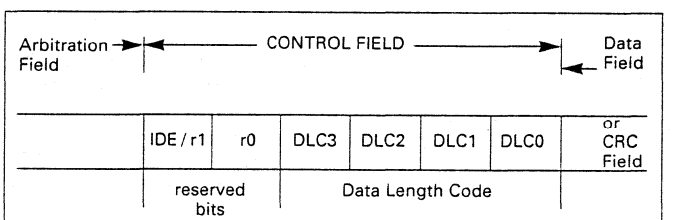


Fig.4 Composition of the CONTROL FIELD

Table 1. Coding of the number of data bytes by the DATA LENGTH CODE

abbreviations: d = 'dominant', r = 'recessive'

Number of Data Bytes	Data Length Code			
	DLC3	DLC2	DLC1	DLC0
0	d	d	d	d
1	d	d	d	r
2	d	d	r	d
3	d	d	r	r
4	d	r	d	d
5	d	r	d	r
6	d	r	r	d
7	d	r	r	r
8	r	d	d	d

DATA FRAME: admissible numbers of data bytes: {0, 1, ..., 7, 8}.
Other values may not be used.

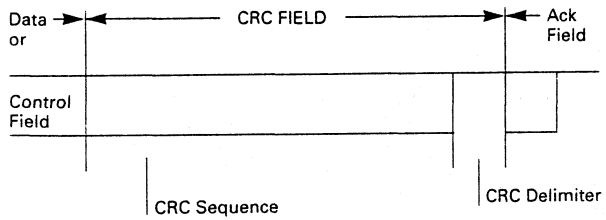


Fig.5 CRC FIELD

Table 2. Calculation of the CRC sequence

```
CRC_RG = 0;                                  // initialize shift register
REPEAT
  CRCNXT = NXTBIT EXOR CRC_RG (14);
  CRC_RG (14:1) = CRC_RG (13:0);             // shift left by
  CRC_RG (0) = 0;                            // 1 position
  IF CRCNXT THEN
    CRC_RG (14:0) = CRC_RG (14:0) EXOR (4599hex);
  ENDIF
UNTIL (CRC SEQUENCE starts or there is an ERROR condition)
```

After the transmission / reception of the last bit of the Data Field, CRC_RG contains the CRC sequence.

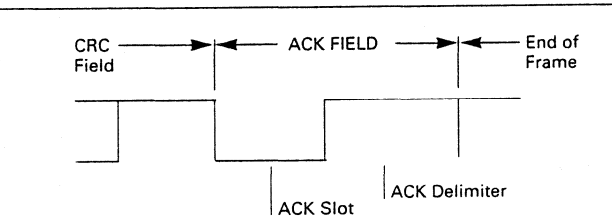


Fig.6 ACK FIELD

CRC SEQUENCE (*Standard Format* as well as *Extended Format*)

The frame check sequence is derived from a cyclic redundancy code best suited for frames with bit counts less than 127 bits (BCH Code).

In order to carry out the CRC calculation, the polynomial to be divided is defined as the polynomial, the coefficients of which are given by the destuffed bit stream consisting of START OF FRAME, ARBITRATION FIELD, CONTROL FIELD, DATA FIELD (if present) and, for the 15 lowest coefficients, by 0. This polynomial is divided (the coefficients are calculated modulo-2) by the generator-polynomial:

$$X^{15} + X^{14} + X^{10} + X^8 + X^7 + X^4 + X^3 + 1.$$

The remainder of this polynomial division is the CRC SEQUENCE transmitted over the bus. In order to implement this function, a 15 bit shift register CRC_RG (14:0) can be used. If NXTBIT denotes the next bit of the bit stream, given by the destuffed bit sequence from START OF FRAME until the end of the DATA FIELD, the CRC SEQUENCE is calculated as shown in Table 2.

CRC DELIMITER (*Standard Format* as well *as Extended Format*)

The CRC SEQUENCE is followed by the CRC DELIMITER which consists of a single 'recessive' bit.

ACK FIELD (Fig.6, *Standard Format* as well as *Extended Format*)

The ACK FIELD is two bits long and contains the ACK SLOT and the ACK DELIMITER. In the ACK FIELD the transmitting station sends two 'recessive' bits.

A RECEIVER which has received a valid message correctly, reports this to the TRANSMITTER by sending a 'dominant' bit during the ACK SLOT (it sends 'ACK').

ACK SLOT
All stations having received the matching CRC SEQUENCE report this within the ACK SLOT by superscribing the 'recessive' bit of the TRANSMITTER by a 'dominant' bit.

ACK DELIMITER
The ACK DELIMITER is the second bit of the ACK FIELD and has to be a 'recessive' bit. As a consequence, the ACK SLOT is surrounded by two 'recessive' bits (CRC DELIMITER, ACK DELIMITER).

END OF FRAME (*Standard Format* as well as *Extended Format*)

Each DATA FRAME and REMOTE FRAME is delimited by a flag sequence consisting of seven 'recessive' bits.

3.2.2. Remote Frame

A station acting as a RECEIVER for certain data can initiate the transmission of the respective data by its source node by sending a REMOTE FRAME (see Fig.7).

A REMOTE FRAME exists both in Standard Format and in Extended Format. In both cases it is composed of six different bit fields:

START OF FRAME, ARBITRATION FIELD, CONTROL FIELD, CRC FIELD, ACK FIELD, END OF FRAME.

Contrary to DATA FRAMEs, the RTR bit of REMOTE FRAMEs is 'recessive'. There is no DATA FIELD, independent of the values of the DATA LENGTH CODE which may be signed any value within the admissible range 0...8. The value is the DATA LENGTH CODE of the corresponding DATA FRAME.

The polarity of the RTR bit indicates whether a transmitted frame is a DATA FRAME (RTR bit 'dominant') or a REMOTE FRAME (RTR bit 'recessive').

3.2.3. ERROR FRAME

The ERROR FRAME (Fig.8) consists of two different fields. The first field is given by the superposition of ERROR FLAGS contributed from different stations. The following second field is the ERROR DELIMITER.

In order to terminate an ERROR FRAME correctly, an 'error passive' node may need the bus to be 'bus idle' for at least 3 bit times (if there is a local error at an 'error passive' receiver). Therefore, the bus should not be loaded to 100%.

Error Flag
There are 2 forms of an ERROR FLAG: an ACTIVE ERROR FLAG and a PASSIVE ERROR FLAG:

1. The ACTIVE ERROR FLAG consists of six consecutive 'dominant' bits.
2. The PASSIVE ERROR FLAG consists of six consecutive 'recessive' bits unless it is overwritten by 'dominant' bits from other nodes.

An 'error active' station detecting an error condition signals this by transmission of an ACTIVE ERROR FLAG. The ERROR FLAG's form violates the law of bit stuffing (see CODING) applied to all fields from START OF FRAME to CRC DELIMITER or destroys the fixed

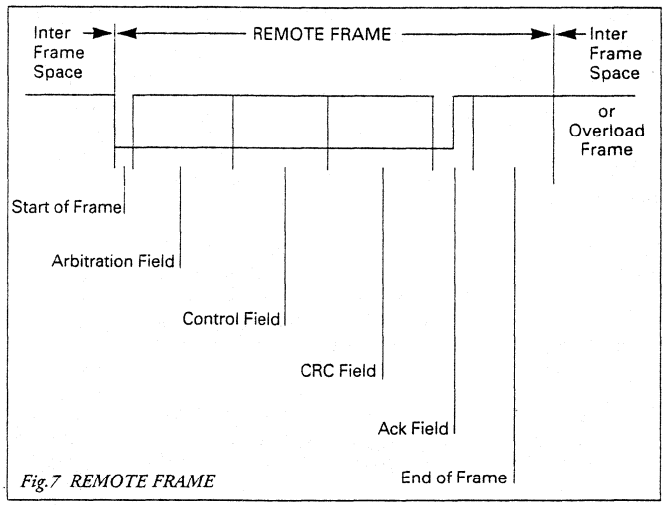


Fig.7 REMOTE FRAME

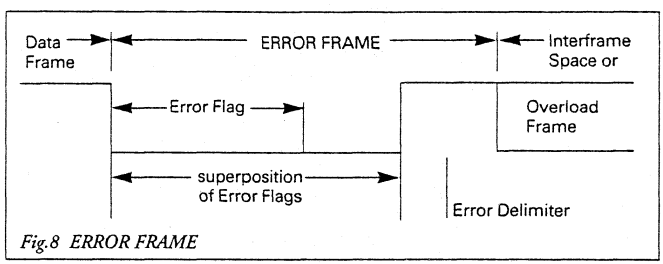


Fig.8 ERROR FRAME

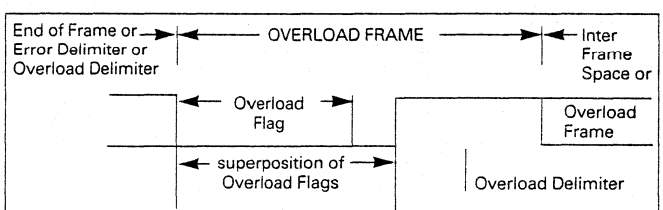


Fig.9 OVERLOAD FRAME

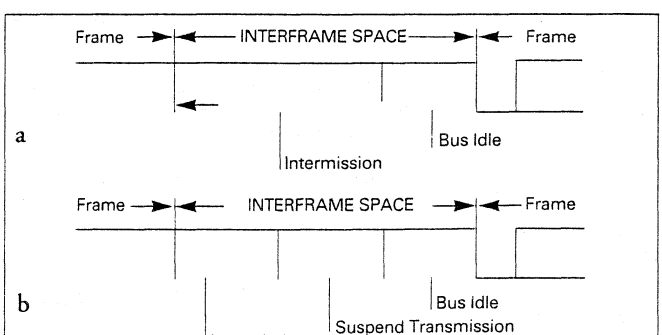


Fig.10 INTERFRAME SPACE

a) for not 'error passive' stations or those having been TRANSCEIVER of the previous message
b) for 'error passive' stations having been TRANSMITTER of the previous message

form ACK FIELD or END OF FRAME field. As a consequence, all other stations detect an error condition and on their part start transmission of an ERROR FLAG. So the sequence of 'dominant' bits which actually can be monitored on the bus results from a superposition of different ERROR FLAGs transmitted by individual stations. The total length of this sequence varies between a minimum of six and a maximum of twelve bits.

An 'error passive' station detecting an error condition tries to signal this by transmission of a PASSIVE ERROR FLAG. The 'error passive' station waits for six consecutive bits of equal polarity, beginning at the start of the PASSIVE ERROR FLAG. The PASSIVE ERROR FLAG is complete when these 6 equal bits have been detected.

Error Delimiter
The ERROR DELIMITER consists of eight 'recessive' bits.

After transmission of an ERROR FLAG, each station sends 'recessive' bits and monitors the bus until it detects a 'recessive' bit. Afterwards it starts transmitting seven more 'recessive' bits.

3.2.4. Overload Frame

The OVERLOAD FRAME (Fig.9) contains the two bit fields OVERLOAD FLAG and OVERLOAD DELIMITER.

There are two kinds of OVERLOAD conditions which both lead to the transmission of an OVERLOAD FLAG:

1. The internal conditions of a receiver which requires a delay of the next DATA FRAME or REMOTE FRAME.
2. Detection of a 'dominant' bit at the first and second bit of INTERMISSION.
3. If a CAN node samples a dominant bit at the eighth bit (the last bit) of an ERROR DELIMITER or OVERLOAD DELIMITER, it will start transmitting an OVERLOAD FRAME (not an ERROR FRAME). The Error Counters will not be incremented.

An OVERLOAD FRAME due to OVERLOAD condition 1 is only allowed to be started at the first bit time of an expected INTERMISSION, whereas OVERLOAD FRAMEs due to OVERLOAD condition 2 and condition 3 start one bit after detecting the 'dominant' bit.

At most, two OVERLOAD FRAMEs may be generated to delay the next DATA or REMOTE FRAME.

Overload Flag
consists of six 'dominant' bits. The overall form corresponds to that of the ACTIVE ERROR FLAG.

The OVERLOAD FLAG's form destroys the fixed form of the INTERMISSION field. As a consequence, all other stations also detect an OVERLOAD condition and on their part start transmission of an OVERLOAD FLAG. In case that there is a 'dominant' bit detected during the 3rd bit of INTERMISSION then it will interpret this as START OF FRAME.

Note:
Controllers based on the CAN Specification version 1.0 and 1.1 have another interpretation of the 3rd bit of INTERMISSION: If a dominant bit was detected locally at some node, the other nodes will not interpret the OVERLOAD FLAG correctly, but interpret the first of these six 'dominant' bits as START OF FRAME; the sixth 'dominant' bit violates the rule of bit stuffing causing an error condition.

OVERLOAD DELIMITER
consists of eight 'recessive' bits.

The OVERLOAD DELIMITER is of the same form as the ERROR DELIMITER. After transmission of an OVERLOAD FLAG the station monitors the bus until it detects a transition from a 'dominant' to a 'recessive' bit. At this point of time every bus station has finished sending its OVERLOAD FLAG and all stations start transmission of seven more 'recessive' bits in coincidence.

3.2.5. Interframe Spacing

DATA FRAMEs and REMOTE FRAMEs are separated from preceding frames whatever type they are (DATA FRAME, REMOTE FRAME, ERROR FRAME, OVERLOAD FRAME) by a bit field called INTERFRAME SPACE. In contrast, OVERLOAD FRAMEs and ERROR FRAMEs are not preceded by an INTERFRAME SPACE and multiple OVERLOAD FRAMEs are not separated by an INTERFRAME SPACE.

Interframe Space
contains the bit fields INTERMISSION and BUS IDLE and, for 'error passive' stations which have been TRANSMITTER of the previous message, SUSPEND TRANSMISSION.

Fig.10 shows the INTERFRAME SPACE structure for stations which are not 'error passive' or have been RECEIVER of the previous message (Fig.10a), as well as for 'error passive' stations which have been TRANSMITTER of the previous message (Fig.10b).

INTERMISSION
consists of three 'recessive' bits.

During INTERMISSION the only action to be taken is signalling an OVERLOAD condition and no station is allowed to actively start a transmission of a DATA FRAME or REMOTE FRAME.

Note:
If a CAN node has a message waiting for transmission and it samples a dominant bit at the third bit of INTERMISSION, it will interpret this as a START OF FRAME bit, and, with the next bit, start transmitting its

message with the first bit of its IDENTIFIER without first transmitting a START OF FRAME bit and without becoming receiver.

BUS IDLE
The period of BUS IDLE may be of arbitrary length. The bus is recognized to be free and any station having something to transmit can access the bus. A message which is pending for transmission during the transmission of another message is started in the first bit following INTERMISSION.

The detection of a 'dominant' bit on the bus is interpreted as START OF FRAME.

SUSPEND TRANSMISSION
After an 'error passive' station has transmitted a message, it sends eight 'recessive' bits following INTERMISSION, before starting to transmit a further message or recognizing the bus to be idle. If meanwhile a transmission (caused by another station) starts, the station will become receiver of this message.

3.3. Conformance with regard to Frame Formats

The Standard Format is equivalent to the Data / Remote Frame Format as it is described in the CAN Specification 1.2. In contrast, the Extended Format is a new feature of the CAN protocol. In order to allow the design of relatively simple controllers, the implementation of the Extended Format to its full extent is not required (e. g. send messages or accept data from messages in Extended Format), whereas the Standard Format must be supported without restriction.

New controllers are considered to be in conformance with this CAN Specification, if they have at least the following properties with respect to the Frame Formats defined in 3.1 and 3.2:

- Every new controller supports the Standard Format;
- Every new controller can receive messages of the Extended Format. This requires that Extended Frames are not destroyed just because of their format. It is, however, not required that the Extended Format must be supported by new controllers.

3.4.Definition of TRANSMITTER /RECEIVER

Transmitter
A unit originating a message is called "TRANSMITTER" of that message. The unit stays TRANSMITTER until the bus is idle or the unit loses ARBITRATION.

Receiver
A unit is called "RECEIVER" of a message, if it is not TRANSMITTER of that message and the bus is not idle.

4. Message Filtering

Message filtering is based upon the whole Identifier. Optional mask registers that allow any Identifier bit to to be set 'don't care' for message filtering, may be used to select groups of Identifiers to be mapped into the attached receive buffers.

If mask registers are implemented every bit of the mask registers must be programmable, i. e. they can be enabled or disabled for message filtering. The length of the mask register can comprise the whole IDENTIFIER or only part of it.

5. Message Validation

The point of time at which a message is taken to be valid, is different for the transmitter and the receivers of the message.

Transmitter:
The message is valid for the transmitter, if there is no error until the end of END OF FRAME. If a message is corrupted, retransmission will follow automatically and according to prioritization. In order to be able to compete for bus access with other messages, retransmission has to start as soon as the bus is idle.

Receivers:
The message is valid for the receivers, if there is no error until the last but one bit of END OF FRAME. The value of the last bit of END OF FRAME is treated as 'don't care', a dominant value does not lead to a FORM ERROR (cf. section 7.1).

6. Coding

Bit Stream Coding

The frame segments START OF FRAME, ARBITRATION FIELD, CONTROL FIELD, DATA FIELD and CRC SEQUENCE are coded by the method of bit stuffing. Whenever a transmitter detects five consecutive bits of identical value in the bit stream to be transmitted, it automatically inserts a complementary bit in the actual transmitted bit stream.

The remaining bit fields of the DATA FRAME or REMOTE FRAME (CRC DELIMITER, ACK FIELD and END OF FRAME) are of fixed form and not stuffed. The ERROR FRAME and the OVERLOAD FRAME are of fixed form as well and not coded by the method of bit stuffing.

The bit stream in a message is coded according to the Non-Return-to-Zero (NRZ) method. This means that, during the total bit time, the generated bit level is either 'dominant' or 'recessive'.

7. Error Handling

7.1. Error Detection

There are 5 different error types (which are not mutually exclusive):

- ***Bit Error***
  A unit that is sending a bit on the bus also monitors the bus. A BIT ERROR has to be detected at the bit time, when the bit value that is monitored is different from the bit value that is sent. An exception is the sending of a 'recessive' bit during the stuffed bit stream of the ARBITRATION FIELD or during the ACK SLOT. Then no BIT ERROR occurs when a 'dominant' bit is monitored. A TRANSMITTER sending a PASSIVE ERROR FLAG and detecting a 'dominant' bit does not interprete this as a BIT ERROR.

- ***Stuff Error***
  A STUFF ERROR has to be detected at the bit time of the 6th consecutive equal bit level in a message field that should be coded by the method of bit stuffing.

- ***CRC Error***
  The CRC sequence consists of the result of the CRC calculation by the transmitter. The receivers calculate the CRC in the same way as the transmitter. A CRC ERROR has to be detected, if the calculated result is not the same as that received in the CRC sequence.

- ***Form Error***
  A FORM ERROR has to be detected when a fixed-form bit field contains one or more illegal bits.(Note that, for a Receiver, a dominant bit during the last bit of END OF FRAME is not treated as FORM ERROR).

- ***Acknowledgement Error***
  An ACKNOWLEDGEMENT ERROR has to be detected by a transmitter whenever it does not monitor a 'dominant' bit during ACK SLOT.

7.2. Error Signalling

A station detecting an error condition signals this by transmitting an ERROR FLAG. For an 'error active' node it is an ACTIVE ERROR FLAG, for an 'error passive' node it is a PASSIVE ERROR FLAG.

Whenever a BIT ERROR, a STUFF ERROR, a FORM ERROR or an ACKNOWLEDGEMENT ERROR is detected by any station, transmission of an ERROR FLAG is started at the respective station at the next bit. Whenever a CRC ERROR is detected, transmission of an ERROR FLAG starts at the bit following the ACK DELIMITER, unless an ERROR FLAG for another error condition has already been started.

8. Fault Confinement

With respect to fault confinement, a unit may be in one of three states:

- 'error active',
- 'error passive',
- 'bus off'.

An 'error active' unit can normally take part in bus communication and sends an ACTIVE ERROR FLAG when an error has been detected.

An 'error passive' unit must not send an ACTIVE ERROR FLAG. It takes part in bus communication, but when an error has been detected only a PASSIVE ERROR FLAG is sent. Also after a transmission, an 'error passive' unit will wait before initiating a further transmission. (See SUSPEND TRANSMISSION)

A 'bus off' unit is not allowed to have any influence on the bus. (E.g. output drivers switched off.)

For fault confinement, two counts are implemented in every bus unit:

1) TRANSMITTER ERROR COUNT
2) RECEIVE ERROR COUNT

These counts are modified according to the following rules:

(note that more than one rule may apply during a given message transfer)

1. When a RECEIVER detects an error, the RECEIVE ERROR COUNT will be increased by 1, except when the detected error was a BIT ERROR during the sending of an ACTIVE ERROR FLAG or an OVERLOAD FLAG.

2. When a RECEIVER detects a 'dominant' bit as the first bit after sending an ERROR FLAG, the RECEIVE ERROR COUNT will be increased by 8.

3. When a TRANSMITTER sends an ERROR FLAG, the TRANSMIT ERROR COUNT is increased by 8.

   Exception 1:
   If the Transmitter is 'error passive' and detects an ACKNOWLEDGEMENT ERROR because of not detecting a 'dominant' ACK and does not detect a 'dominant' bit while sending its PASSIVE ERROR FLAG.

   Exception 2:
   If the TRANSMITTER sends an ERROR FLAG because a STUFF ERROR occured during ARBITRATION whereby the STUFF-BIT is located before the RTR bit, and should have been 'recessive', and has been sent as 'recessive' but monitored as 'dominant'.

   In exceptions 1 and 2, the TRANSMIT ERROR COUNT is not changed.

4. If a TRANSMITTER detects a BIT ERROR while sending an ACTIVE ERROR FLAG or an OVERLOAD FLAG, the TRANSMIT ERROR COUNT is increased by 8.

5. If a RECEIVER detects a BIT ERROR while sending an ACTIVE ERROR FLAG or an OVERLOAD FLAG, the RECEIVE ERROR COUNT is increased by 8.

6. Any node tolerates up to 7 consecutive 'dominant' bits after sending an ACTIVE ERROR FLAG, PASSIVE ERROR FLAG or OVERLOAD FLAG. After de-

tecting the 14th consecutive 'dominant' bit (in case of an ACTIVE ERROR FLAG or an OVERLOAD FLAG) or after detecting the 8th consecutive 'dominant' bit following a PASSIVE ERROR FLAG, and after each sequence of additional eight consecutive 'dominant' bits, every TRANSMITTER increases its TRANSMIT ERROR COUNT by 8 and every RECEIVER increases its RECEIVE ERROR COUNT by 8.

7. After the successful transmission of a message (getting ACK and no error until END OF FRAME is finished), the TRANSMIT ERROR COUNT is decreased by 1 unless it was already 0.

8. After the successful reception of a message (reception without error up to the ACK SLOT and the successful sending of the ACK bit), the RECEIVE ERROR COUNT is decreased by 1, if it was between 1 and 127. If the RECEIVE ERROR COUNT was 0, it stays 0, and if it was greater than 127, then it will be set to a value between 119 and 127.

9. A node is 'error passive' when the TRANSMIT ERROR COUNT equals or exceeds 128, or when the RECEIVE ERROR COUNT equals or exceeds 128. An error condition letting a node become 'error passive' causes the node to send an ACTIVE ERROR FLAG.

10. A node is 'bus off' when the TRANSMIT ERROR COUNT is greater than or equal to 256.

11. An 'error passive' node becomes 'error active' again when both the TRANSMIT ERROR COUNT and the RECEIVE ERROR COUNT are less or equal to 127.

12. A node which is 'bus off' is permitted to become 'error active' (no longer 'bus off') with its error counters both set to 0 after 128 occurrances of 11 consecutive 'recessive' bits have been monitored on the bus.

Note:
An error count value greater than about 96 indicates a heavily disturbed bus. It may be of advantage to provide means to test for this condition.

Note:
Start-up / Wake-up:
If during system start-up only one node is online, and if this node transmits some message, it will get no acknowledgement, detect an error and repeat the message. It can become 'error passive' but not 'bus off' due to this reason.

9. Oscillator Tolerance

A maximum oscillator tolerance of 1.58% is given and therefore the use of a ceramic resonator at a bus speed of up to 125 Kbits/s as a rule of thumb; for a more precise evaluation refer to

Dais, S; Chapman, M:
"Impact of Bit Representation on Transport Capacity and Clock Accuracy in Serial Data Streams",

SAE Technical Paper Series 890532,
Multiplexing in Automobil SP-773, March 1989.

For the full bus speed range of the CAN protocol, a quartz oscillator is required.

The chip of the CAN network with the highest requirement for its oscillator accuracy determines the oscillator accuracy which is required from all the other nodes.

Note:
CAN controllers following this CAN Specification and controllers following the previous versions 1.0 and 1.1, used in one and the same network, must all be equipped with a quartz oscillator. That means, ceramic resonators can only be used in a network with all the nodes of the network following CAN Protocol Specification versions 1.2 or later.

10. Bit Timing Requirements

Nominal Bit Rate:
The Nominal Bit Rate is the number of bits per second transmitted in the absence of resynchronization by an ideal transmitter.

Nominal Bit Time:

Nominal Bit Time
= 1 / Nominal Bit Rate

The Nominal Bit Time can be thought of as being divided into separate non-overlapping time segments forming the bit time as shown in Fig.11:

- SYNCHRONIZATION SEGMENT (SYNC_SEG),
- PROPAGATION TIME SEGMENT (PROP_SEG),
- PHASE BUFFER SEGMENT 1 (PHASE_SEG1),
- PHASE BUFFER SEGMENT 2 (PHASE_SEG2).

SYNC SEG
This part of the bit time is used to synchronize the various nodes on the bus. An edge is expected to lie within this segment.

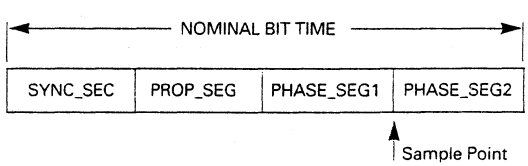


Fig.11 Partition of the Bit Time

PROP SEG
This part of the bit time is used to compensate for the physical delay times within the network. It is twice the sum of the signal's propagation time on the bus line, the input comparator delay, and the output driver delay.

PHASE SEG1, PHASE SEG2
These Phase-Buffer-Segments are used to compensate for edge phase errors. These segments can be lengthened or shortened by resynchronization.

SAMPLE POINT
The SAMPLE POINT is the point of time at which the bus level is read and interpreted as the value of that respective bit. It's location is at the end of PHASE_SEG1.

INFORMATION PROCESSING TIME
The INFORMATION PROCESSING TIME is the time segment starting with the SAMPLE POINT reserved for calculation of the subsequent bit level.

TIME QUANTUM
The TIME QUANTUM is a fixed unit of time derived from the oscillator period. There exists a programmable prescaler with integral values, ranging at least from 1 to 32. Starting with the MINIMUM TIME QUANTUM, the TIME QUANTUM can have a length of

TIME QUANTUM
= m x MINIMUM TIME QUANTUM

with m the value of the prescaler.

Length of Time Segments

- SYNC_SEG is 1 TIME QUANTUM long.
- PROP_SEG is programmable to be 1, 2, ..., 8 TIME QUANTA long.
- PHASE_SEG1 is programmable to be 1, 2, ..., 8 TIME QUANTA long.
- PHASE_SEG2 is the maximum of PHASE_SEG1 and the INFORMATION PROCESSING TIME.
- The INFORMATION PROCESSING TIME is less than or equal to 2 TIME QUANTA long.

The total number of TIME QUANTA in a bit time has to be programmable at least from 8 to 25.

Note:
It is often intended that control units do not make use of different oscillators for the local CPU and its communication device. Therefore the oscillator frequency of a CAN device tends to be that of the local CPU and is determined by the requirements of the control unit. In order to derive the desired bit rate, programmability of the bit timing is necessary.

In case of CAN implementations that are designed for use without a local CPU, the bit timing cannot be programmable. On the other hand, these devices allow to choose an external oscillator in such a way that the device is adjusted to the appropriate bit rate so that the programmability is dispensable for such components.

The position of the sample point, however, should be selected in common for all nodes. Therefore the bit timing of CAN devices without local CPU should be compatible to the bit time as defined in Fig.12.

HARD SYNCHRONIZATION
After a HARD SYNCHRONIZATION, the internal bit time is restarted with SYNC_SEG. Thus, HARD-SYNCHRONIZATION forces the edge which has caused the HARD-SYNCHRONIZATION to lie within the SYNCHRONIZATION SEGMENT of the restarted bit time.

RESYNCHRONIZATION JUMP WIDTH
As a result of RESYNCHRONIZATION, PHASE_SEG1 may be lengthened or PHASE_SEG2 may be shortened. The amount of lengthening or shortening of the PHASE BUFFER SEGMENTs has an upper bound given by the RESYNCHRONIZATION JUMP WIDTH. The RESYNCHRONIZATION JUMP WIDTH shall be programmable between 1 and min (4, PHASE_SEG1).

Clocking information may be derived from transitions from one bit value to the other. The property that only a fixed maximum number of successive bits have the same value provides the possibility of resynchronizing a bus unit to the bit stream during a frame. The maximum length between two transitions which can be used for resynchronization is 29 bit times.

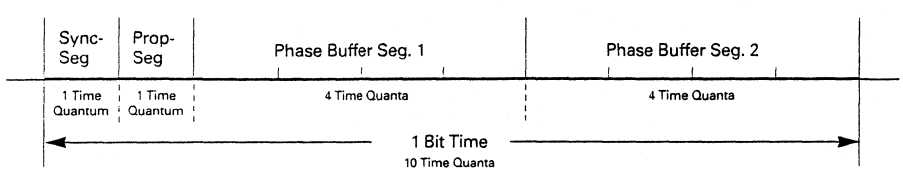


Fig.12 Definition of the Bit Time for CAN devices without local CPU

PHASE ERROR of an edge
The PHASE ERROR of an edge is given by the position of the edge relative to SYNC_SEG, measured in TIME QUANTA. The sign of PHASE ERROR is defined as follows:

- e = 0, if the edge lies within SYNC_SEG.
- e > 0, if the edge lies before the SAMPLE POINT.
- e < 0, if the edge lies after the SAMPLE POINT of the previous bit.

RESYNCHRONIZATION
The effect of a RESYNCHRONIZATION is the same as that of a HARD SYNCHRONIZATION, when the magnitude of the PHASE ERROR of the edge which causes the RESYNCHRONIZATION is less than or equal to the programmed value of the RESYNCHRONIZATION JUMP WIDTH.

When the magnitude of the PHASE ERROR is larger than the RESYNCHRONIZATION JUMP WIDTH,

- and if the PHASE ERROR is *positive*, then PHASE_SEG1 is *lengthened* by an amount equal to the RESYNCHRONIZATION JUMP WIDTH.
- and if the PHASE ERROR is *negative*, then PHASE_SEG2 is *shortened* by an amount equal to the RESYNCHRONIZATION JUMP WIDTH.

Synchronization Rules
HARD SYNCHRONIZATION and RESYNCHRONIZATION are the two forms of SYNCHRONIZATION. They obey the following rules:

1. Only one SYNCHRONIZATION within one bit time is allowed.
2. An edge will be used for SYNCHRONIZATION only if the value detected at the previous SAMPLE POINT (previous read bus value) differs from the bus value immediately after the edge.
3. HARD SYNCHRONIZATION is performed whenever there is a 'recessive' to 'dominant' edge during BUS IDLE.
4. All other 'recessive' to 'dominant' edges (and optionally 'dominant' to 'recessive' edges in case of low bit rates) fulfilling the rules 1 and 2 will be used for RESYNCHRONIZATION with the exception that a node transmitting a dominant bit will not perform a RESYNCHRONIZATION as a result of a 'recessive' to 'dominant' edge with a positive PHASE ERROR, if only 'recessive' to 'dominant' edges are used for RESYNCHRONIZATION.

– End of PART B –

GENERAL

TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ, and the CECC system of conformity. Our factories are certified to ISO 9000 and CECC by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

BASIC TYPE NUMBER

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

First and second letters

DIGITAL FAMILY CIRCUITS

The first two letters identify the family.(1)

SOLITARY CIRCUITS

The first letter divides solitary circuits into:

SSolitary digital circuits

T Analog circuits

U Mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(2)

MICROPROCESSORS

The first two letters identify microprocessors and related circuits:

MA Microcomputer or central processing unit

MB Slice processor (functional slice of microprocessor)

MD Related memories

ME Other related circuits such as interfaces, clocks, peripheral controllers, etc.

CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

The first two letters identify:

NHHybrid circuits

NL Logic circuits

NM Memories

NS Analog signal processing using switched capacitors

NT Analog signal processing using charge-transfer devices

NX Imaging devices

NY Other related circuits.

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

(2) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

Third letter

The third letter indicates the operating ambient temperature range:

A temperature range not specified below

B 0 to + 70 °C

C −55 to +125 °C

D −25 to + 70 °C

E −25 to + 85 °C

F −40 to + 85 °C

G −55 to + 85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

SERIAL NUMBER

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

VERSION LETTER

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C Cylindrical

D Ceramic dual in-line (CERDIL, CERDIP)

F Flat pack (two leads)

G Flat pack (four leads)

H Quad flat pack (QFP)

L Chip on tape (foil)

P Plastic dual in-line (DIL)

Q Quad in-line (QUIL)

T Mini pack (SOL, SO, VSO)

U Uncased chip.

TWO-LETTER SUFFIX

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

First letter (general shape)

C Cylindrical

D Dual in-line (DIL)

E Power DIL (with external heatsink)

F Flat pack (leads on two sides)

G Flat pack (leads on four sides)

H Quad flat pack (QFP)

K Diamond (TO-3 family)

M Multiple in-line (except dual, triple and quad)

Q Quad in-line (QUIL)

R Power QUIL (with external heatsink)

S Single in-line (SIL)

T Triple in-line

W Leaded chip carrier (LCC)

X Leadless chip carrier (LLCC)

Y Pin grid array (PGA).

Second letter (material)

C Metal-ceramic

G Glass-ceramic

M Metal

P Plastic.

EXAMPLES

PCF1105WP: digital IC; PC family; operating temperature range –40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range –55 to +125 °C; serial number 2000.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental

conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor.
- All mains-powered electrical equipment should be connected via an earth leakage switch.
- Equipment cases should be earthed.
- Relative humidity should be maintained between 50 and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

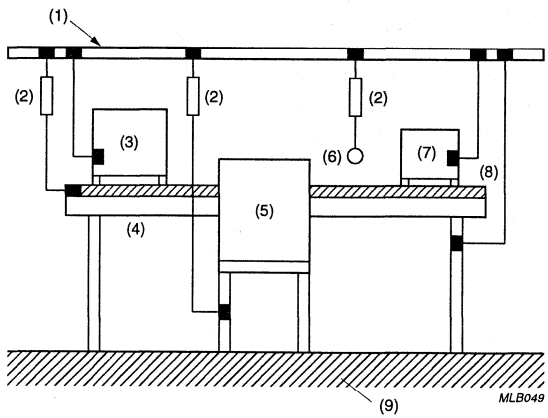
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.
(9) Antistatic floor.

Fig.1 Protected work station.

DEVICE DATA
AND APPLICATION INFORMATION

CONTROL DEVICES FOR AUTOMOTIVE

Bit timing parameters for CAN networks

Summary

For a CAN application the nominal data rate can be programmed in the range from about 5 kbit/s up to 1 Mbit/s. Some additional parameters can be programmed (within a fixed data rate) and hence the network's performance can be influenced regarding

- compensation of propagation delays (extension limit of the network),
- compensation of oscillator tolerances.

After an introduction to CAN networks (chapter 1), the definitions of all symbols for the CAN bit timing parameters can be found in chapter 2.

The method, how a desired data rate can be programmed generally, is presented in chapter 3. The way how the bit timing can be varied in order to optimize it regarding propagation delays is shown in chapter 4.

In most cases there is no need to optimize the bit timing regarding maximum oscillator tolerance. Chapter 5 shows how the compensation of oscillator tolerances can be increased, if necessary.

For a couple of commonly used bit rates the results of above calculations can be found in the tables of Appendix A.

Bit timing parameters for CAN networks

Application report
KIE 07/91 ME

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Appendices

Bit timing parameters for CAN networks

Application report
KIE 07/91 ME

1. Introduction

CAN (Controller Area Network) is an advanced serial communication protocol, which efficiently supports distributed real-time control with a very high safety level. CAN allows the flexible configuration of networks with different types of microprocessors and microcontrollers. Typical applications of CAN-based networks can be found in automotive and industrial environment:

- o Automotive Systems:
  - multiplex wiring (< 100 kbit/s)
  - engine control, ABS (up to 1 Mbit/s)
- o Industrial Systems:
  - field bus applications
  - robotics, numeric machine control

The PCA 82C200 is a highly integrated stand-alone controller for CAN, which has on the one hand the serial bus link and on the other hand a parallel microprocessor interface. The serial link of the PCA 82C200 supports different physical bus layers, while the parallel interface allows the connection to a wide range of microprocessors/-controllers.

The P8xC592 is a stand-alone high-performance microcontroller designed for use in automotive and general industrial applications. In addition to the 80C51 standard features this device provides a number of dedicated hardware functions for these applications. It basically combines the functions of the existing P8xC552 (without I^2C hardware) and the PCA 82C200 (see above), with the following enhanced features:

- o 16 KByte program memory
- o 2 * 256 Byte data memory
- o DMA between CAN Transmit/Receive Buffer and internal RAM

Fig. 1 shows a schematic network using a microcontroller plus the PCA 82C200 or just the P8xC592 for distributed control applications.

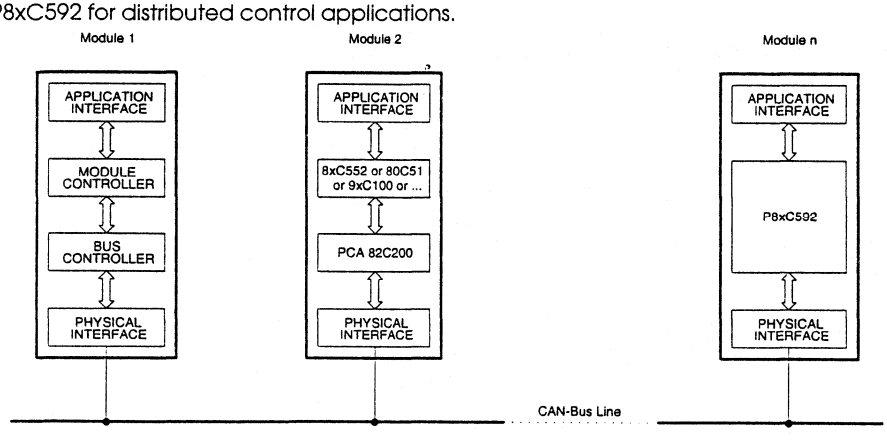

Fig. 1 Example of a "Controller Area Network"

Bit timing parameters for CAN networks

Application report
KIE 07/91 ME

For a CAN application the nominal data rate can be programmed in the range from about 5 kbit/s up to 1 Mbit/s. Not only the nominal data rate can be programmed, but also parameters like the location of the sample point within one bit period or the synchronization behaviour can be programmed in order to optimize the network's performance regarding

- possible extension of the network,
- tolerance to oscillator drifts.

This paper intends to help to find the appropriate values for the Bus Timing Registers of Philips' CAN controllers (e.g. PCA 82C200 or P8xC592) for programming of the CAN bit timing. It also presents the formulas for calculation of the network's performance.

It is assumed that

- the nominal bit time (bit rate) has already been chosen,
- the oscillators' tolerances are known,
- there is knowledge about the propagation delay times of
  - the cable
  - the transceiver circuits
  - the internal delays on-chip (see data sheets 'PCA 82C200' or 'P8xC592').

The reader should be familiar with at least one of the documents

- Product Specification PCA 82C200 (October 1990)
- Preliminary Target Device Specification 8xC592 Version 2.0 (1990)

2. Symbol Definitions

In this chapter the symbols used for the formulas are introduced. The symbols are relating to implementations of the 'CAN protocol' like the PCA 82C200 or the CAN interface on the P8xC592. The symbols are used in the same way like it is done in the product specifications of these devices.

Other CAN devices, which might be used in the same network, may be characterized by other symbols or even by the same symbols but with different meanings (see Appendix B).

2.1 Bit Timing Definitions

Fig.2 shows the general structure of a bit period. A bit period consists of a number of system clocks (SCL). The system clock's cycle time is derived from the oscillator's cycle time by multiplying it with an integer value (defined by the "Baud Rate Prescaler").

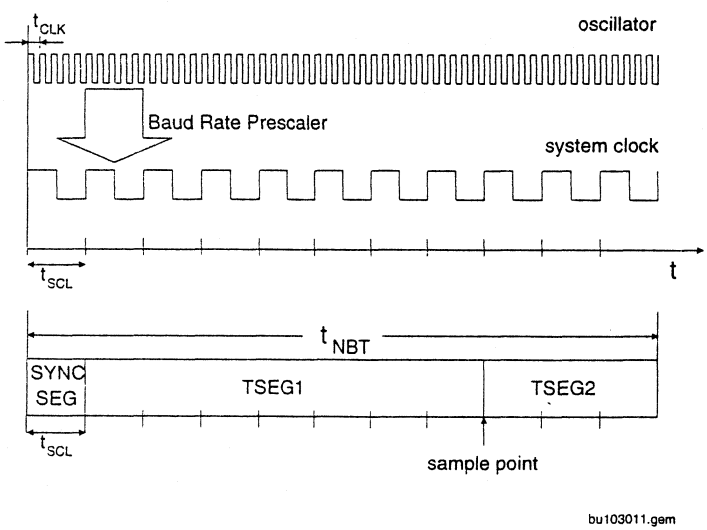

Fig. 2 General structure of a bit period

A bit period starts with one system clock being reserved for synchronization purposes, the segment SYNCSEG.

Then the bit period has two segments which follow, the programmable segments TSEG1 and TSEG2. The sample point within a bit period is located at the end of TSEG1.

t_{CLK}: time for 1 oscillator period
N_{BRP}: Baud Rate Prescaler value
t_{SCL}: time for 1 system clock: $t_{SCL} = N_{BRP} \cdot 2 \cdot t_{CLK}$

SYNCSEG: name of the first segment of a bit
N_{SYNC}: number of t_{SCL}s for SYNCSEG: always = 1
t_{SYNC}: time for SYNCSEG: $t_{SYNC} = 1 \cdot t_{SCL}$

TSEG1: name of the segment between SYNCSEG and TSEG2
N_{TSEG1}: number of t_{SCL}s for TSEG1 (programmable)
t_{TSEG1}: time for TSEG1: $t_{TSEG1} = N_{TSEG1} \cdot t_{SCL}$

TSEG2: name of the last segment
N_{TSEG2}: number of t_{SCL}s for TSEG2 (programmable)
t_{TSEG2}: time for TSEG2: $t_{TSEG2} = N_{TSEG2} \cdot t_{SCL}$

NBT: name of a bit period during states without resynchronization
N_{NBT}: number of t_{SCL}s for NBT
t_{NBT}: time for NBT, 'nominal bit time'

With these definitions the nominal bit time t_{NBT} can be calculated as:

$t_{NBT} = t_{SYNC} + t_{TSEG1} + t_{TSEG2} = (N_{SYNC} + N_{TSEG1} + N_{TSEG2}) \cdot t_{SCL}$
(with t_{SCL}, see above), $\underbrace{\qquad\qquad\qquad\qquad}_{= N_{NBT}}$

Beyond the definition of the nominal bit timing, it can be programmed, how much a bit can be lengthened or shortened for compensation of phase drifts of the oscillators in the network:

SJW: name of the segment by which a bit time may be lengthened or shortened
N_{SJW}: number of t_{SCL}s for SJW (programmable)
t_{SJW}: time for SJW: $t_{SJW} = N_{SJW} \cdot t_{SCL}$

2.2 Bus Timing Registers

Fig.3 shows the layout of the Bus Timing Registers (BTR 0 and BTR 1).

With BTR 0 the Baud Rate Prescaler (BRP) and the Synchronization Jump Width (SJW) can be defined. The part of BTR 0 that defines SJW (or BRP) is a 2-bit (or 6-bit) binary number, named P_{SJW} (or P_{BRP}, respectively):

$P_{SJW} = 2 \cdot SJW.1 + SJW.0$
$P_{BRP} = 32 \cdot BRP.5 + 16 \cdot BRP.4 + 8 \cdot BRP.3 + 4 \cdot BRP.2 + 2 \cdot BRP.1 + BRP.0$

P_{SJW} is the programmed numerical value of SJW: $N_{SJW} = P_{SJW} + 1$
P_{BRP} is the programmed numerical value of BRP: $N_{BRP} = P_{BRP} + 1$

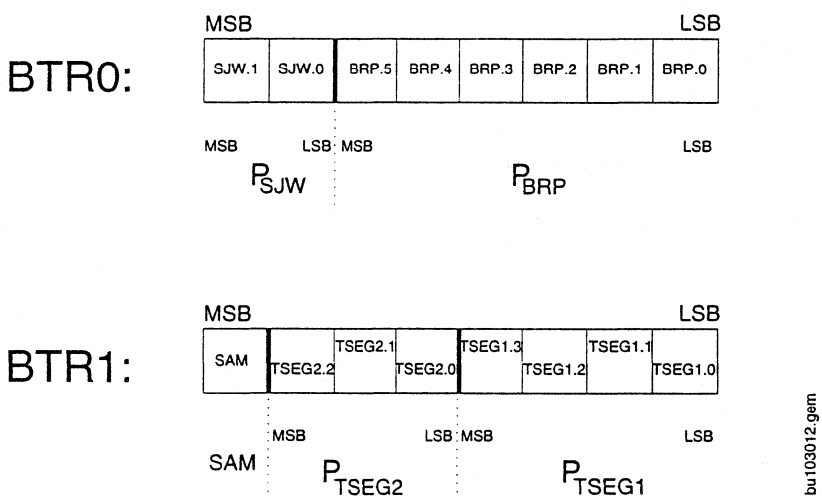

Fig. 3 Layout of the Bus Timing Registers

With BTR 1 the Time Segment 1 (TSEG1) and the Time Segment 2 (TSEG2) can be defined. Additionally there is one bit SAM that defines the sampling mode:

SAM = 0 --> each bit is sampled once.
SAM = 1 --> each bit is sampled three times (= simple digital filter).

The part of BTR 1 that defines TSEG1 (or TSEG2) is a 4-bit (or 3-bit) binary number, named P_{TSEG1} (or P_{TSEG2}, respectively):

$P_{TSEG1} = 8 \cdot TSEG1.3 + 4 \cdot TSEG1.2 + 2 \cdot TSEG1.1 + TSEG1.0$
$P_{TSEG2} = 4 \cdot TSEG2.2 + 2 \cdot TSEG2.1 + TSEG2.0$

P_{TSEG1} is the programmed numerical value of TSEG1: $N_{TSEG1} = P_{TSEG1} + 1$
P_{TSEG2} is the programmed numerical value of TSEG2: $N_{TSEG2} = P_{TSEG2} + 1$

2.3 Criteria for Optimization

Fig.4 illustrates which system parameters are important for the CAN bit timing.

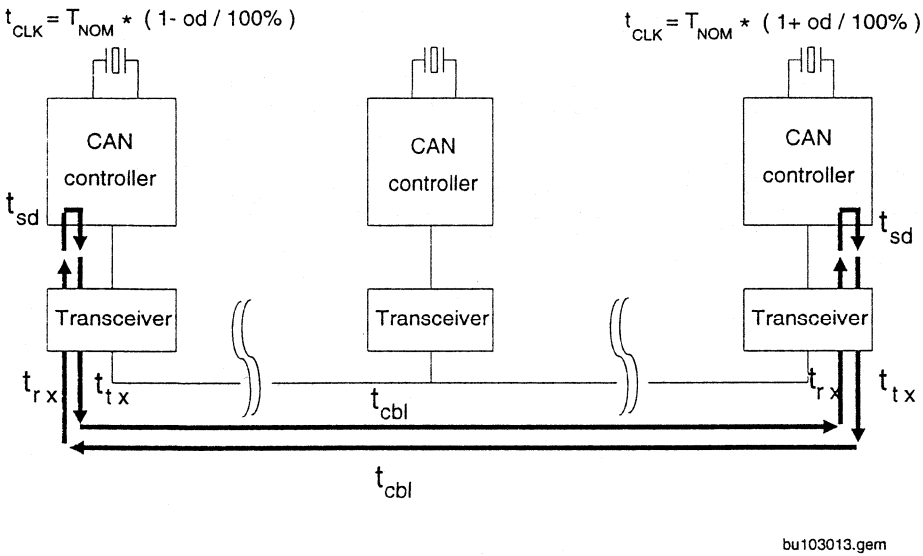

Fig. 4 Worst case of oscillator drift and path of propagation delay

2.3.1 Propagation Delay

The longest distance between two CAN controllers in the same network determines the maximum Propagation Delay (t_{prop}) that has to be compensated by the CAN controller. The Propagation Delay is the time needed by the signal to go from one CAN controller to the other one plus the time needed to go back again. The Propagation Delay has to be compensated especially during the Arbitration Field and the Acknowledge Field of a message.

The times contributing to t_{prop} are:

t_{sd} = the sum of the input and output delay times of the CAN controller
t_{tx} = the transmission delay time of the transceiver circuit
t_{rx} = the reception delay time of the transceiver circuit
t_{cbl} = the signal delay time of the cable for the longest distance between two CAN controllers in the network

t_{prop} = $2 \cdot (t_{sd} + t_{tx} + t_{rx} + t_{cbl})$

2.3.2 Oscillator Tolerance

The CAN protocol tolerates phase drifts of the CAN controllers' oscillators. In chapter 5 it is assumed that all oscillators in the network have the same nominal cycle time ($T_{NOM} = 1/f_{NOM}$) with a tolerance of $\pm$ *od* (%). The actual cycle time t_{CLK} then is in the range of

T_{NOM} (1 - od/100%) < t_{CLK} < T_{NOM} (1 + od/100%).

The formulas cover the worst case, that means for two communicating CAN controllers the one is clocked with the longest clock cycle time and the other one is clocked with the shortest one.

Note: instead of 'od' (accuracy related to the nominal cycle time) also the accuracy of the nominal frequency (in %) can be used: The error made by this approximation is negligible.

3. Calculation of the values for the Bus Timing Registers

This chapter presents the method how to calculate all possible solutions for programming the Bus Timing Registers for a desired bit rate. It is assumed, that the oscillator's frequency is known.

With the definition of the nominal bit time

$t_{NBT} = N_{NBT} \cdot t_{SCL} = N_{NBT} \cdot N_{BRP} \cdot 2 \cdot t_{CLK}$

we get the requirement, that the nominal bit time can be derived from the oscillator's duty cycle by a multiplication with an even integer number (N_{MUL}):

$N_{MUL} = N_{NBT} \cdot N_{BRP} \cdot 2$

If this requirement is met, then we can split N_{MUL} into its prime factors, and assign them (except one factor '2') to the operands N_{NBT} and N_{BRP} such a way that

- $4 < N_{NBT} < 26$,
- $0 < N_{BRP} < 65$.

Note: Often it is advantageous to take N_{NBT} the highest value that is still less than (19+SAM+1), if possible (cf. the note below).

With N_{BRP} we get $t_{SCL} = N_{BRP} \cdot 2 \cdot t_{CLK}$.

Then N_{NBT} has to be parted into the segments SYNCSEG, TSEG1 and TSEG2 with

- $N_{NBT} = N_{SYNC} + N_{TSEG1} + N_{TSEG2}$
- $N_{SYNC} = 1$
- $1 < N_{TSEG1} < 17$
- $1 + SAM < N_{TSEG2} < 9$ (SAM = 0 or SAM = 1, see 2.2)
- $N_{TSEG2} < N_{TSEG1} + 1$

Note: Often it is advantageous to take N_{TSEG2} as small as possible, implying that N_{TSEG1} is as high as possible (cf. chapter 4).

Now N_{SJW} can be chosen with

- $0 < N_{SJW} < 5$
- $N_{SJW} + SAM < N_{TSEG1}$
- $N_{SJW} < N_{TSEG2} + 1$

Finally, the values to be programmed into BTR0 and BTR1 are

- $P_{BRP} = N_{BRP} - 1$
- $P_{SJW} = N_{SJW} - 1$
- $P_{TSEG1} = N_{TSEG1} - 1$
- $P_{TSEG2} = N_{TSEG2} - 1$

Usually there are several solutions for N_{BRP}, N_{TSEG1}, N_{TSEG2} and N_{SJW}. Which is the best solution, depends on the used criteria like propagation delay or oscillator tolerance. Chapters 4 and 5 describe how the optimized solution regarding those criteria can be found.

3.1 Example

Given t_{CLK} = 1/16 MHz = 0.0625 µs, t_{NBT} = 10 µs (for 100 kbit/s), SAM = 0

$N_{MUL} = t_{NBT} / t_{CLK} = 160 = 2 \cdot 2 \cdot 2 \cdot 2 \cdot 2 \cdot 5$

one solution: $N_{MUL} = 2 \cdot N_{NBT} \cdot N_{BRP}$

resulting in $t_{SCL} = 2 \cdot N_{BRP} \cdot t_{CLK}$ = 0.625 µs,

N_{NBT} (= 16) can be parted into e.g.:

N_{SYNC} = 1 (obligatory)
N_{TSEG1} = 13
N_{TSEG2} = 2

leaving N_{SJW} = 1 or 2 as possibilities for SJW. If we take N_{SJW} = 1, we get:

BTR0 to be programmed with 04H (P_{SJW} = 0, P_{BRP} = 4)
BTR1 to be programmed with 1CH (SAM = 0, P_{TSEG2} = 1, P_{TSEG1} = 12)

4. Calculation of the Max. Propagation Delay

This chapter presents the formulas that are needed to calculate the max. Propagation Delay (relating to the max. length of the bus cable) for a given setup of the CAN bit timing.

for SAM = 0 (one sample per bit):

$1/2 \cdot t_{prop} < 1/2 \cdot (P_{TSEG1} - P_{SJW} + 1) \cdot t_{SCL}$

for SAM = 1 (three samples per bit):

$1/2 \cdot t_{prop} < 1/2 \cdot (P_{TSEG1} - P_{SJW} - 1) \cdot t_{SCL}$

These requirements must be met in order to make communication possible even in the worst case of resynchronization. For the three-sample mode it is also foreseen that all three samples are taken correctly. It has been considered that the first of the three samples is taken 2 system clocks before the end of TSEG1.

Apparently, large numbers of P_{TSEG1} combined with small numbers of P_{SJW} lead to long propagation delays that are compensated. Or, we can say that:

> In order to allow long bus cables it is favorable to put the sample point as close as possible to the end of a bit period.

4.1 Example

Continuing our example of chapter 3.1 we now can calculate the tolerated propagation delay for

$P_{TSEG1} = 12$, $P_{SJW} = 0$, SAM = 0, $t_{SCL} = 0.625\ \mu s$:

$1/2\ t_{prop} < 1/2 \cdot (12 - 0 + 1) \cdot 0.625\ \mu s = 4.0625\ \mu s$

Assuming a propagation delay on the cable of pcbl = 5.5 ns/m, internal delay times on-chip being $t_{sd} = 62.5$ ns and transceiver parameters being $t_{rx} = 100$ ns and $t_{tx} = 100$ ns, we get for the maximum length L of the bus cable for this example:

$L \cdot pcbl < 1/2\ t_{prop} - t_{sd} - t_{rx} - t_{tx}$

$$L < \frac{1/2\ t_{prop} - t_{sd} - t_{rx} - t_{tx}}{pcbl} = \frac{3.8\ \mu s}{5.5 ns/m} = 690\ m$$

5. Calculation of the Oscillator Tolerance

This chapter presents the formulas that are needed to calculate the max. oscillator's tolerance 'od' for a given setup of the CAN bit timing. The formulas are given with respect to the selected synchronization mode (1-edge or 2-edge mode, see CAN controllers' data sheets for description of the SYNCH bit in the CONTROL Register).

for 1-edge mode (SYNCH = 0):

$$od < N_{SJW} \cdot 100\% / 2 \cdot (30 \cdot N_{NBT} - N_{TSEG2})$$

for 2-edge mode (SYNCH = 1):

$$od < N_{SJW} \cdot 100\% / 2 \cdot (26 \cdot N_{NBT} - N_{TSEG2})$$

Apparently, the best results for the tolerance of the CAN bit timing against oscillator drifts is achieved when N_{SJW} is as high as possible (means $P_{SJW} = 3$) and the bit consists only of few system clocks (optimum: $N_{NBT} = 10$). The latter shows that an optimized phase drift tolerance implies restrictions for the compensation of propagation delays and vice versa.

> In order to allow best compensation of oscillator tolerances, it is favorable to take $N_{SJW} = 4$ ($P_{SJW} = 3$) and the smallest N_{NBT}.

> Optimization regarding oscillator tolerance is contrary to optimization regarding compensation of propagation delays.

Note: For most cases it is sufficient to optimize the bit timing regarding compensation of propagation delays. The resulting required oscillator tolerance is satisfied by most types of crystal oscillators, or, P_{SJW} has to be increased until 'od' is big enough. The latter often requires to increase N_{TSEG2} and decrease N_{TSEG1} simultaneousiy (cf. chapter 3).

5.1 Example

We now can complete the calculations for the example of chapters 3.1 and 4.1: We have had $N_{NBT} = 16$ and $N_{SJW} = 1$, and, assuming SYNCH = 1, we obtain

$$od < 1 \cdot 100\% / 2 \cdot (26 \cdot 16 - 2) = 0.12\%$$

As crystals usually perform better than 0.1 % tolerance, in this example there would not be the need for an increase of P_{SJW}.

6. Summary

For a CAN application the nominal data rate can be programmed in the range from about 5 kbit/s up to 1 Mbit/s. Some additional parameters can be programmed (within a fixed data rate) and hence the network's performance can be influenced regarding

- compensation of propagation delays (extension limit of the network),
- compensation of oscillator tolerances.

After an introduction to CAN networks (chapter 1), the definitions of all symbols for the CAN bit timing parameters can be found in chapter 2.

The method, how a desired data rate can be programmed generally, is presented in chapter 3. The way how the bit timing can be varied in order to optimize it regarding propagation delays is shown in chapter 4.

In most cases there is no need to optimize the bit timing regarding maximum oscillator tolerance. Chapter 5 shows how the compensation of oscillator tolerances can be increased, if necessary.

For a couple of commonly used bit rates the results of above calculations can be found in the tables of Appendix A.

Appendices

A. Examples for Commonly Used Bit Rates at t_{clk} = 1 / (16 MHz)

In this Appendix tables provide the appropriate values of the Bus Timing Registers for commonly used bit rates. For these bit rates the adjustments have been optimized with respect to max. propagation delay, or they perform suboptimal max. propagation delays, but improved compensation of oscillator tolerances, respectively.

The oscillator tolerances in the tables have been calculated with the formulas of chapter 5, but in order to simplify the table (only one value for oscillator tolerance for SAM = 0 and SAM = 1) the approximations

$(30 \cdot N_{NBT} - N_{TSEG2}) \approx (30 \cdot N_{NBT} - N_{SJW})$, and
$(26 \cdot N_{NBT} - N_{TSEG2}) \approx (26 \cdot N_{NBT} - N_{SJW})$

have been made. The error made by these approximations is negligible.

There are 4 tables for the same bit rates, each with a different setting of P_{SJW}. There may occur two entries for the same bit rate in one table, as it was not evident which of both is 'better'.

As P_{SJW}=0 allows the best compensation of propagation delays, the corresponding table can be found in section A.1.

The tables with P_{SJW} = 1, 2 or 3 show the settings for better compensation of oscillator tolerances and thus reduced propagation delay compensation. They can be found in section A.2.

A.1 Recommended Values for Max. Propagation Delay

(16.00 MHz) P_{SJW} = 0

bitrate [kbit/s]	BTR0 hex		SAM = 0 BTR1 hex	SAM = 0 $t_{prop}/2$ [us]	SAM = 1 BTR1 hex	SAM = 1 $t_{prop}/2$ [us]	osc.tolerance 1 edge	osc.tolerance 2 edge
1600.00	0	**	11	0.125			0.336 %	0.388 %
1333.33	0	**	12	0.188			0.279 %	0.323 %
1000.00	0		14*	0.313	A3*	0.125	0.209 %	0.242 %
800.00	0		16*	0.438	A5*	0.250	0.167 %	0.193 %
500.00	0		1C*	0.813	AB*	0.625	0.104 %	0.120 %
400.00	0		2F	1.000	AF*	0.875	0.083 %	0.096 %
250.00	1		1C	1.625	AB	1.250	0.104 %	0.120 %
200.00	1		2F	2.000	AF	1.750	0.083 %	0.096 %
125.00	3		1C	3.250	AB	2.500	0.104 %	0.120 %
100.00	3		2F	4.000	AF	3.500	0.083 %	0.096 %
100.00	4		1C	4.063	AB	3.125	0.104 %	0.120 %
80.00	4		2F	5.000	AF	4.375	0.083 %	0.096 %
62.50	7		1C	6.500	AB	5.000	0.104 %	0.120 %
50.00	7		2F	8.000	AF	7.000	0.083 %	0.096 %
50.00	9		1C	9.125	AB	6.250	0.104 %	0.120 %
40.00	9		2F	10.000	AF	8.750	0.083 %	0.096 %
31.25	F		1C	13.000	AB	10.000	0.104 %	0.120 %
25.00	F		2F	16.000	AF	14.000	0.083 %	0.096 %
25.00	13		1C	16.250	AB	12.500	0.104 %	0.120 %
20.00	13		2F	20.000	AF	17.500	0.083 %	0.096 %
20.00	18		1C	20.313	AB	15.625	0.104 %	0.120 %
16.00	18		2F	25.000	AF	21.875	0.083 %	0.096 %
15.63	1F		1C	26.000	AB	20.000	0.104 %	0.120 %
12.50	1F		2F	32.000	AF	28.000	0.083 %	0.096 %
12.50	27		1C	32.500	AB	25.000	0.104 %	0.120 %
10.00	27		2F	40.000	AF	35.000	0.083 %	0.096 %
10.00	31		1C	40.625	AB	31.250	0.104 %	0.120 %
8.00	31		2F	50.000	AF	43.750	0.083 %	0.096 %
7.81	3F		1C	52.000	AB	40.000	0.104 %	0.120 %
6.25	3F		2F	64.000	AF	56.000	0.083 %	0.096 %
5.00	3F		7F	64.000	FF	56.000	0.067 %	0.077 %

bit.dat, produced by: bit3.C , time: Mon Mar 18 15:10:23 1991

A.2 Compromise Values for Higher Oscillator Tolerance

(16.00 MHz) P_{SJW} = 1

bitrate [kbit/s]	BTR0 hex		SAM = 0 BTR1 hex	SAM = 0 $t_{prop}/2$ [us]	SAM = 1 BTR1 hex	SAM = 1 $t_{prop}/2$ [us]	osc.tolerance 1 edge	osc.tolerance 2 edge
1333.33	40	**	12	0.125			0.562 %	0.649 %
1000.00	40		14*	0.250			0.420 %	0.485 %
800.00	40		16*	0.375	A5*	0.188	0.336 %	0.388 %
500.00	40		1C*	0.750	AB*	0.563	0.209 %	0.242 %
400.00	40		2F	0.938	AF*	0.813	0.167 %	0.193 %
250.00	41		1C*	1.500	AB	1.125	0.209 %	0.242 %
200.00	41		2F	1.875	AF	1.625	0.167 %	0.193 %
125.00	43		1C*	3.000	AB	2.250	0.209 %	0.242 %
100.00	43		2F	3.750	AF	3.250	0.167 %	0.193 %
100.00	44		1C*	3.750	AB	2.813	0.209 %	0.242 %
80.00	44		2F	4.688	AF	4.063	0.167 %	0.193 %
62.50	47		1C*	6.000	AB	4.500	0.209 %	0.242 %
50.00	47		2F	7.500	AF	6.500	0.167 %	0.193 %
50.00	49		1C*	7.500	AB	5.625	0.209 %	0.242 %
40.00	49		2F	9.375	AF	8.125	0.167 %	0.193 %
31.25	4F		1C*	12.000	AB	9.000	0.209 %	0.242 %
25.00	4F		2F	15.000	AF	13.000	0.167 %	0.193 %
25.00	53		1C*	15.000	AB	11.250	0.209 %	0.242 %
20.00	53		2F	18.750	AF	16.250	0.167 %	0.193 %
20.00	58		1C*	18.750	AB	14.063	0.209 %	0.242 %
16.00	58		2F	23.438	AF	20.313	0.167 %	0.193 %
15.63	5F		1C*	24.000	AB	18.000	0.209 %	0.242 %
12.50	5F		2F	30.000	AF	26.000	0.167 %	0.193 %
12.50	67		1C*	30.000	AB	22.500	0.209 %	0.242 %
10.00	67		2F	37.500	AF	32.500	0.167 %	0.193 %
10.00	71		1C*	37.500	AB	28.125	0.209 %	0.242 %
8.00	71		2F	46.875	AF	40.625	0.167 %	0.193 %
7.81	7F		1C*	48.000	AB	36.000	0.209 %	0.242 %
6.25	7F		2F	60.000	AF	52.000	0.167 %	0.193 %
5.00	7F		7F	60.000	FF	52.000	0.134 %	0.154 %

(16.00 MHz) P_{SJW} = 2

bitrate [kbit/s]	BTR0 hex	SAM = 0 BTR1 hex	SAM = 0 $t_{prop}/2$ [us]	SAM = 1 BTR1 hex	SAM = 1 $t_{prop}/2$ [us]	osc.tolerance 1 edge	osc.tolerance 2 edge
1000.00	80	23*	0.125			0.633 %	0.732 %
800.00	80	25*	0.250	A5*	0.125	0.505 %	0.584 %
500.00	80	2B*	0.625	AB*	0.500	0.314 %	0.363 %
400.00	80	2F*	0.875	AF*	0.750	0.251 %	0.290 %
250.00	81	2B*	1.250	AB*	1.000	0.314 %	0.363 %
200.00	81	2F*	1.750	AF*	1.500	0.251 %	0.290 %
125.00	83	2B*	2.500	AB*	2.000	0.314 %	0.363 %
100.00	83	2F*	3.500	AF*	3.000	0.251 %	0.290 %
100.00	84	2B*	3.125	AB*	2.500	0.314 %	0.363 %
80.00	84	2F*	4.375	AF*	3.750	0.251 %	0.290 %
62.50	87	2B*	5.000	AB*	4.000	0.314 %	0.363 %
50.00	87	2F*	7.000	AF*	6.000	0.251 %	0.290 %
50.00	89	2B*	6.250	AB*	5.000	0.314 %	0.363 %
40.00	89	2F*	8.750	AF*	7.500	0.251 %	0.290 %
31.25	8F	2B*	10.000	AB*	8.000	0.314 %	0.363 %
25.00	8F	2F*	14.000	AF*	12.000	0.251 %	0.290 %
25.00	93	2B*	12.500	AB*	10.000	0.314 %	0.363 %
20.00	93	2F*	17.500	AF*	15.000	0.251 %	0.290 %
20.00	98	2B*	15.625	AB*	12.500	0.314 %	0.363 %
16.00	98	2F*	21.875	AF*	18.750	0.251 %	0.290 %
15.63	9F	2B*	20.000	AB*	16.000	0.314 %	0.363 %
12.50	9F	2F*	28.000	AF*	24.000	0.251 %	0.290 %
12.50	A7	2B*	25.000	AB*	20.000	0.314 %	0.363 %
10.00	A7	2F*	35.000	AF*	30.000	0.251 %	0.290 %
10.00	B1	2B*	31.250	AB*	25.000	0.314 %	0.363 %
8.00	B1	2F*	43.750	AF*	37.500	0.251 %	0.290 %
7.81	BF	2B*	40.000	AB*	32.000	0.314 %	0.363 %
6.25	BF	2F*	56.000	AF*	48.000	0.251 %	0.290 %
5.00	BF	7F	56.000	FF	48.000	0.201 %	0.232 %

(16.00 MHz) P_{SJW} = 3

bitrate [kbit/s]	BTR0 hex	SAM = 0 BTR1 hex	SAM = 0 $t_{prop}/2$ [us]	SAM = 1 BTR1 hex	SAM = 1 $t_{prop}/2$ [us]	osc.tolerance 1 edge	osc.tolerance 2 edge
800.00	C0	34*	0.125			0.676 %	0.781 %
500.00	C0	3A*	0.500	BA*	0.375	0.420 %	0.485 %
400.00	C0	3E*	0.750	BE*	0.625	0.336 %	0.388 %
250.00	C1	3A*	1.000	BA*	0.750	0.420 %	0.485 %
200.00	C1	3E*	1.500	BE*	1.250	0.336 %	0.388 %
125.00	C3	3A*	2.000	BA*	1.500	0.420 %	0.485 %
100.00	C3	3E*	3.000	BE*	2.500	0.336 %	0.388 %
100.00	C4	3A*	2.500	BA*	1.875	0.420 %	0.485 %
80.00	C4	3E*	3.750	BE*	3.125	0.336 %	0.388 %
62.50	C7	3A*	4.000	BA*	3.000	0.420 %	0.485 %
50.00	C7	3E*	6.000	BE*	5.000	0.336 %	0.388 %
50.00	C9	3A*	5.000	BA*	3.750	0.420 %	0.485 %
40.00	C9	3E*	7.500	BE*	6.250	0.336 %	0.388 %
31.25	CF	3A*	8.000	BA*	6.000	0.420 %	0.485 %
25.00	CF	3E*	12.000	BE*	10.000	0.336 %	0.388 %
25.00	D3	3A*	10.000	BA*	7.500	0.420 %	0.485 %
20.00	D3	3E*	15.000	BE*	12.500	0.336 %	0.388 %
20.00	D8	3A*	12.500	BA*	9.375	0.420 %	0.485 %
16.00	D8	3E*	18.750	BE*	15.625	0.336 %	0.388 %
15.63	DF	3A*	16.000	BA*	12.000	0.420 %	0.485 %
12.50	DF	3E*	24.000	BE*	20.000	0.336 %	0.388 %
12.50	E7	3A*	20.000	BA*	15.000	0.420 %	0.485 %
10.00	E7	3E*	30.000	BE*	25.000	0.336 %	0.388 %
10.00	F1	3A*	25.000	BA*	18.750	0.420 %	0.485 %
8.00	F1	3E*	37.500	BE*	31.250	0.336 %	0.388 %
7.81	FF	3A*	32.000	BA*	24.000	0.420 %	0.485 %
6.25	FF	3E*	48.000	BE*	40.000	0.336 %	0.388 %
5.00	FF	7F	52.000	FF	44.000	0.268 %	0.310 %

* This setting is compatible to the CAN Specification Version 1.1 or 1.2 and is supported by the Philips CAN devices. But, as not all CAN chips from other manufacturers show that performance, it might be necessary to find another setting in case of such devices being used in the same network (see Appendix B).

** Bit rates higher than 1Mbit/s are not subject of the CAN Specification.

B. Bit Timing Conversion Formulas for Intel's AN 82526 CAN Controller

In principal CAN controllers from different manufacturers can be used in the very same CAN network. For example the devices PCA 82C200 or P8xC592 can be used together with Intel's AN 82526 for data rates up to 1Mbit/s.

Regarding bit timing caution is necessary, because in contrast to the Philips devices the Intel AN 82526 does not completely comply with the recent CAN specification Versions 1.1 or 1.2. The same nominal data rate can be run with all these devices, but in some cases the use of the AN 82526 reduces the performance of the network (i.e. resulting in considerable limitations for the usable bus length).

In the following the bit timing conversion formulas are given to use the Philips devices and the AN 82526 in the very same network.

It is assumed that the reader has calculated the bit timing for his CAN devices like it has been described in chapters 3 to 5. The values of

- SAM,
- P_{BRP},
- P_{SJW},
- P_{TSEG1},
- P_{TSEG2}

can be programmed into the Bus Timing Registers (Fig.3) of the devices PCA 82C200 or P8xC592, for example.

The values of

- SAM,
- P_{BRP},
- P_{SJW},
- i_{TSEG1} instead of P_{TSEG1},
- i_{TSEG2} instead of P_{TSEG2}

can be programmed into the Bus Timing Registers (Fig.5) of the device AN 82526, in order to get the identical bit timing into that device with

$$i_{TSEG1} = P_{TSEG1} - P_{SJW} - 1$$
$$i_{TSEG2} = P_{TSEG2} - P_{SJW} - 1$$

That is because for the device AN 82526 the nominal bit time is defined as

$$t_{NBT} = \underbrace{(1 + P_{SJW} + 1 + i_{TSEG1} + 1 + i_{TSEG2} + 1 + P_{SJW} + 1)}_{= N_{NBT}} \cdot t_{SCL}$$

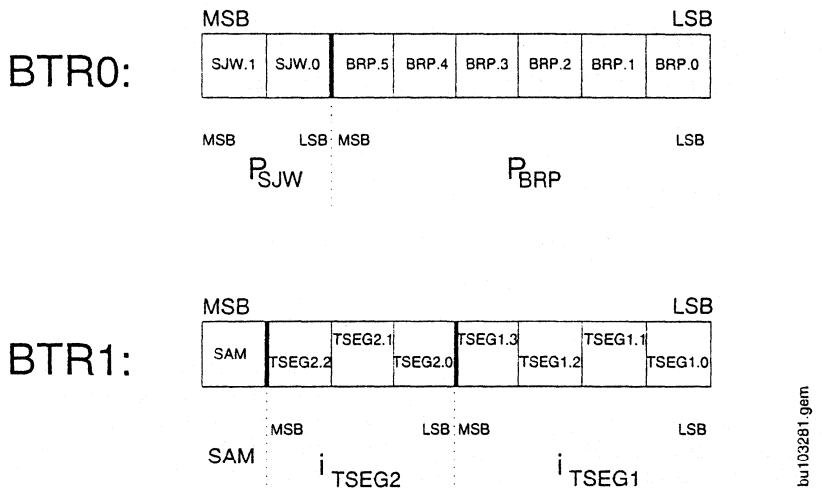

Fig. 5 Layout of the Bus Timing Registers of the AN 82526.

Some of the settings for the bit rates of the tables in appendix A may not be programmable into the AN 82526, as there are additional restrictions for the bit timing for that device like:

1. $P_{TSEG2} > P_{SJW}$

   This restriction affects all bit rates with $N_{TSEG2} = N_{SJW}$. In these cases the propagation delay for the AN 82526 is shorter than those documented in the tables for the Philips devices, as the sample point would have to be moved one t_{SCL} back (i.e. N_{TSEG2} incremented and N_{TSEG1} decremented).

2. if $P_{BRP} = 0$:
   P_{TSEG2} - SAM > 1,
   P_{TSEG1} - P_{SJW} - SAM > 2

   These restrictions affect high bit rates with $N_{BRP} = 1$. For example, the AN 82526 does not support bit rates higher than 1Mbit/s.

For the example in chapter 3.1 we get the corresponding values for the AN 82526 with the conversion formulas:

$i_{TSEG1} = 11$, $i_{TSEG2} = 0$, -> BTR1(AN82526) = 0BH

Thus, if both devices are used in the same network, they can be programmed to drive the identical CAN bit timing in this example.

Using the CAN Transceiver 82C250 with Unshielded Bus Cables

Harald Eisele and Hans-Werner Lütjens

Philips Semiconductors

1. ABSTRACT

This paper discusses requirements on the CAN physical layer in order to meet current automotive EMC standards. It also presents EMC measurement results on an advanced CAN transceiver product along with implementation hints. New EMC investigations show that unshielded bus cable is suitable even for higher bit rates, provided that the physical layer components are EMC-optimized.

2. INTRODUCTION

The CAN bus system is now being employed in a number of vehicles and is also widely accepted in the automation industry. Integrated CAN transceiver products according to ISO 11898 are commonly used to implement the CAN physical layer. These products are available from a number of semiconductor manufacturers and provide bus drive capability for a balanced differential pair. As in this paper depicted, the design of such transceivers is the key for using an unshielded pair of wires as data link between the CAN nodes. Some means for further enhancement of the EMC are given. Finally some measurement results are shown. These results give confidence for using unshielded bus cable for CAN systems in vehicles.

3. IMPACT OF EMC ON BUS SYSTEMS

A data bus system, like the CAN bus (Controller Area Network, [1]), consists of a certain number of bus nodes, being interconnected via a bus line. A bus system can also be described in terms of different layers, e.g. application

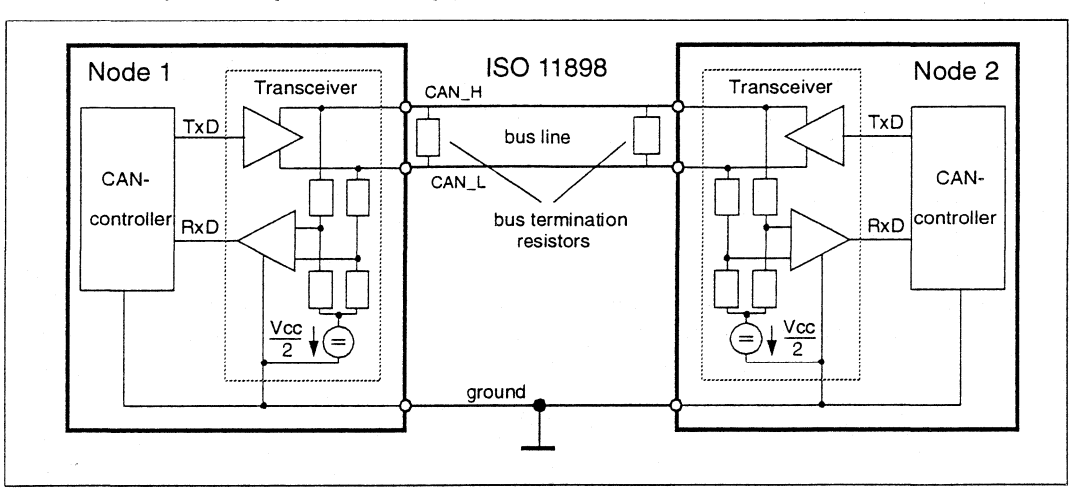

Fig. 3.1: Schematic of a minimum CAN system

layer, data link layer and physical layer [2]. In the following the relation between the physical layer and EMC shall be discussed. Principally there are a number of implementation concepts for physical layers including single wire, two-wire differential and optical link. However in practice a two-wire differential voltage link is common. ISO 11898 [3] includes a specification of a differential voltage link for the CAN bus.

One can assume that a bus node usually is small in physical size compared to the length of the bus cable. Therefore only a minor part of radiation will be emitted or received by the node itself. Consequently the bus cable is to be regarded as the major "antenna" for emission and susceptibility. The following discussion will be based on a minimum bus system set, consisting of two bus nodes being interconnected via an unshielded bus cable (figure 3.1).

Each CAN node essentially consists of a line driver buffer and a line receiver comparator, which are electrically connected to the bus wires CAN_H and CAN_L. The receiver comparator usually is attached to the bus line via a passive resistor divider network providing bus bias when all transmitters are passive (recessive state). These parts of a bus node can be implemented by discrete components, or by employing an IC, the so-called CAN transceiver being the interface between the bus cable and the protocol controller. Today, CAN controllers are available as stand-alone devices, microcontrollers with on-chip CAN controllers and dedicated CAN I/O controllers (so-called SLIOs). For safety reasons CAN employs bus monitoring while transmitting, so the transmitted bit value is permanently compared with the received one. The data link layer contributes to the system-safety mainly by means of detecting corrupted messages and possibly initiating e.g. automatic re-transmission. However measures in the data link layer only are not sufficient to ensure the reliability of a system. There is one safety-aspect of still increasing importance which has to be covered mainly by the physical layer. This is the aspect of electromagnetic compatibility (EMC) between the data link and its environment.

Having a closer look at electromagnetic compatibility we find the partitioning between electromagnetic emission/radiation and electromagnetic immunity/susceptibility. The physical layer has to take care of both aspects. There must be no disturbance of the function of other systems (e.g. car radio) and it has to be ensured that other systems (e.g. mobile telephone) do not disturb data transmission of the bus system. The magnitude of voltages of the emission sources is measured in the order of some microvolts to some millivolts on a receiving antenna. Nevertheless these magnitudes may already disturb the reception of a car radio. On the other hand a bus system in a vehicle has to operate without degradation when subjected to high-power electromagnetic fields, e.g. 100 V/m.

Principally, a symmetrically driven bus cable offers better EMC characteristics compared to an asymmetrically driven one. The information is transferred as a voltage difference between CAN_H and CAN_L. Thus electromagnetic noise and transients on e.g. adjacent power wiring, affecting both bus wires will not degrade the data signal, provided they equally affect both bus wires. This can be supported by implementing the bus wires as a twisted pair. Consequently the immunity of the data link essentially is determined by the common mode behavior of the physical layer. This is a major advantage of a differential link, as e.g. receiver comparators can be built in a way, that they can safely detect the differential voltage between the bus lines

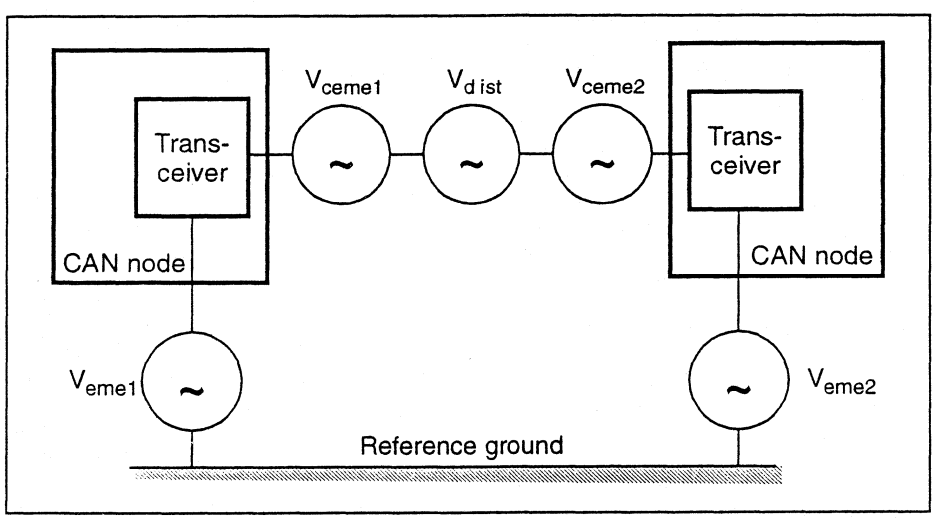

Fig. 3.2: Basic EMC-model of a CAN system

within a common mode input voltage range being much larger than the differential voltage of the data signal. Thus the immunity to radiated interference principally is superior to single-wire links.

If, in addition, the line driver controls the CAN_H and the CAN_L signal with respect to ground such, that in principle the CAN_H signal compensates the CAN_L signal, then almost all emission effects will be of common mode nature.

In real bus systems the compensation may be imperfect, because e.g. at a change of the bit value, the CAN_H and CAN_L signal may not change at the same instant or the slew rate of CAN_H and CAN_L may be different. Only these imperfect compensated parts of the data signal contribute to the overall emission level of a bus node.

As can be seen from figure 3.1, each bus wire together with the CAN nodes and the ground forms a loop. If both bus wires are implemented as a twisted pair, then the loop of each single wire has the same size. Because of this, both loops have to be regarded as one common source of emission and all disturbances coupled into the loops will affect both wires in the same manner. Thus, with respect to common mode effects the bus wires may be regarded as a single wire. Based on this, a basic EMC-model has been worked out for further discussion (see figure 3.2).

Each node contributes to the radiation with two emission sources. V_{emel} represents the disturbances which may be coupled into the ground lead of node 1 by the additional components of this node (e.g. CAN controller and/or microcontroller). V_{cemel} is the representation of the emission that occurs, due to an improper compensation between CAN_H and CAN_L voltage with respect to ground potential at data transmission. The joint reception of the interfering electromagnetic energy by CAN_H and CAN_L wires is represented by the source V_{dist}.

It should be noted, that the bit encoding scheme, also has some impact on EMC. This is due to the fact, that electromagnetic emission is related to the slew rate of edges on the bus line. Therefore bit encoding schemes, which allow less fast slew rates per data bit, e.g. NRZ-coding, are beneficial with respect to minimizing electromagnetic emission.

4. MEASURES TO OPTIMIZE EMC

CHARACTERISTICS OF ADVANCED TRANSCEIVER PRODUCTS - From the findings depicted so far, some essential requirements on differential transceivers can be derived.
Having a look at electromagnetic immunity we find the partitioning between common mode and differential mode noise. As discussed above common mode noise usually by far is dominating over differential mode noise. Consequently the immunity of the data link essentially depends upon the common mode characteristics of the transceiver device. Electromagnetic interference usually includes a wide frequency spectrum. Therefore the transceiver should provide a wide common mode range within a wide frequency range. Advanced differential transceiver products, like the PCA82C250, provide common mode ranges in the order of -7V to +12V corresponding to an interference level of about 7 V_{RMS} on the bus inputs [4]. Additionally a receiver hysteresis function is recommended e.g. to take care of small-signal differential noise. The PCA82C250 has been developed by Philips Semiconductors in cooperation with a leading automotive electronics system house.

With regard to minimizing emission, the transceiver's source (CAN_H) and sink (CAN_L) driver stage should operate as symmetrically and simultaneously as possible. This is needed in order to minimize common-mode voltage pulses at switching. In practice simultaneous switching can be approximated only because of different physical characteristics of the sink and source driver. This is due to for example the principally differing magnitudes of n- and p-type conductivity/mobility in a semiconductor device. Assuming a principally differing AC-behavior of the source and sink driver, there is a direct relation between the driver's slew rate and the electromagnetic emission level. The higher the slew rate of the output driver the more the spectrum of the resulting common mode pulse is shifted to high-frequency radiation. Assuming very fast switching, the timing diagram of the common-mode pulse is a rectangular pulse with a lot of spectral components in the VHF/UHF-range. To avoid this, advanced transceiver products feature a slope-control function, where the driver's slew rate can be adjusted to an optimum value. Employing this function, the slew rate can be decreased with respect to relevant parameters, e.g. bit rate, location of sample point, length and type of bus cable. Thus the slew rates of common mode pulses at switching are minimized too. This is a proven technique to minimize electromagnetic emission of a differential physical layer.

ADDITIONAL MEASURES AND IMPLEMENTATION HINTS - In some cases additional measures may be needed, depending e.g. upon application specific EMC requirements. This paragraph discusses what kind of measures should be considered. Chapter 5 provides some indication what degree of improvement can be expected.

First of all it is obvious that a bus node includes additional noise sources, especially clocked digital devices, like e.g. microcontrollers. To minimize emission generated by such components, e.g. clock frequencies including harmonics, additional measures are eventually needed.

Concerning electromagnetic emission, measures have to be evaluated with respect to two different noise sources. First source is RF-emission caused by the non-ideal com-

pensation of the signal slopes on CAN_H and CAN_L during switching of the bus driver output stages (fig. 3.2, V_{ceme1}). The second source is the voltage drop along the parasitic inductance/resistance of the ground wiring caused by clocked digital circuits in a node, like e.g. microcontrollers (fig. 3.2, V_{eme1}).

In case the emission level isn't sufficiently low for the intended application, several measures are to be considered. Good compensation of the two CAN line's electromagnetic fields requires a close coupling of the CAN wires. This can be implemented using twin wires. Additional reduction of the effect of unwanted common mode signals can be achieved by twisting the bus wires. In order to achieve a determined characteristic to ground potential, a ground line can be routed along with the bus wires e.g. two bus wires twisted with one ground wire parallel or three wires twisted or parallel.

For further improvement of the common mode behavior a good symmetry of the CAN signals to reference ground is recommended. This can be supported by AC-grounding of the bus termination resistor's center tap, as shown in figure 4.1. Another means is to insert a so-called common mode choke into the CAN_H and CAN_L wires (figure 4.1). A common-mode choke is a component including two coupled inductors dedicated to suppress current flow in the same orientation on both bus outputs. The choke increases the common mode impedance of the CAN lines thus reducing emission due to ground lead noise of a bus node. Furthermore, if there is a common mode signal gained by non-ideal compensation, this signal will be minimized by the magnetic coupling between the choke windings. Note, that capacitive coupling between the inputs and the outputs of the common-mode choke (capacitive bypass) should be minimized, e.g. no ground plane is recommended below the CM-choke.

The above mentioned measures are valid also for the enhancement of the immunity. In addition to this, the immunity of the CAN node can be improved further in the higher frequency range e.g. by grounding the transceiver's bus pins via suitable capacitors. Thus a low pass filter is built, reducing the common mode voltage at the transceiver's bus input pins at higher frequencies. Note, that immunity is best when the grounding capacitors are matched.

Generally, a number of parameters, e.g. bit rate, location of sample point, length and type of bus cable, determine which of the above mentioned EMC measures are suitable or needed. Recent investigations of car manufacturers indicate, that with the help of such measures, it is possible to operate CAN buses using unshielded bus cable at bit rates in the order of 250 kbit/s.

Finally it should be mentioned, that a layout of the printed circuit board taking care of EMC aspects is beneficial to achieve best EMC performance. In any case, the effort to improve EMC can be minimized through employment of advanced transceiver products.

5. EMC MEASUREMENT RESULTS

The transceiver product PCA82C250 has been tested at the "Product Concept and Application Laboratory Hamburg" of Philips Semiconductors using a set-up being derived from the IEC 801 EMC test standard [5]. This standard is being issued by the IEC technical committee TC65

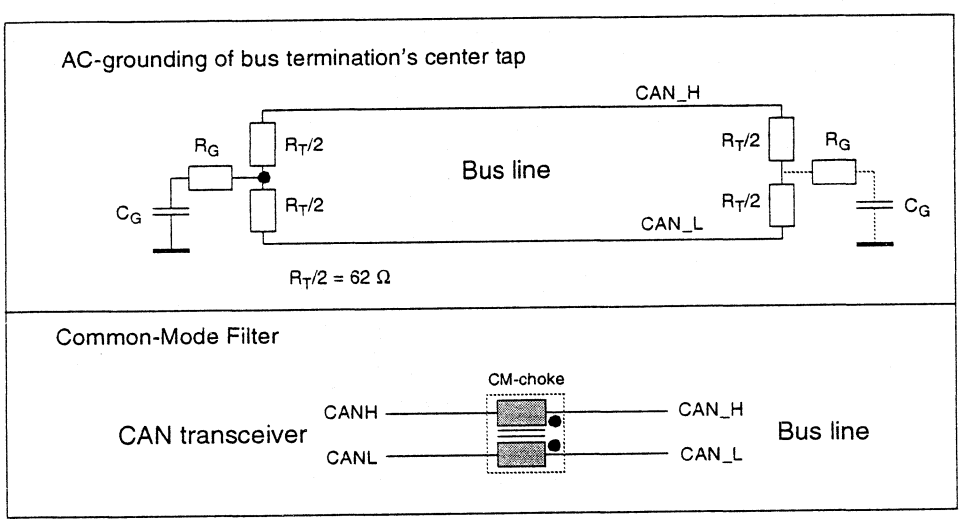

Fig. 4.1: Two optional EMC-measures for the CAN physical layer

Using the CAN transceiver 82C250 with unshielded bus cables

Application report

"Industrial Process Measurement and Control". Part 6 of this document includes a method covering the aspect of immunity to conducted disturbances induced by radio frequency fields in the range of 9 kHz to 80 MHz. An extension of the frequency range up to 230 MHz is possible. The advantage of this method is the limited test equipment effort. Especially immunity measurements do not require expensive high-power amplifiers thanks to galvanic coupling of the noise into the wires. Also tests can be carried out in an unshielded test site or in a small Faraday's cage. Galvanic coupling of noise and compact size of set-ups is also regarded as beneficial for minimizing parasitic resonance effects thus optimizing the aspect of reproducibility of test results. Furthermore it should be noted, that this test-method can be used for electromagnetic emission measurements as well [6].

The IEC 801-6 standard exhibits the basic structure of a test set-up only. For the evaluation of a system, a bus node or an IC in an application, a dedicated test set-up has to be developed. For evaluation of the EMC performance of the CAN physical layer, a test network consisting of two nodes and one bus cable substitute is used here. This basic system under test is placed in a metal box (Faraday's cage). Power supply and RF-noise energy is input into the box using coupling/decoupling networks as specified in IEC 801-6. The data signal is in- and output via optical links.

For differential voltage physical layer concepts there are different basic bus cable implementations to be considered, primarily unshielded twisted pair (UTP) and two-wire parallel, like e.g. ribbon-type cable. In vehicles, the length of a bus cable can be in the order of 40 m. However an EMC test using this cable length cannot be carried out in an open test site. Also in a small Faraday's cage such a cable cannot be placed. Therefore the cables are to be substituted by appropriate equivalent circuits. These circuits must take into account the relevant parameters of the cables. In figure 5.1 the used equivalent circuit for an unshielded twisted pair bus cable is depicted. For common mode investigations the cable can be substituted by the capacitor C1, which is the equivalent of the distributed capacitance between the two wires. The wire inductance has been dropped to simulate worst case conditions, e.g. maximum noise level at the node's bus inputs.

The cable characteristics are approximated by the differential capacitance C1 between the wires CAN_H and CAN_L. The interference field directly excites the bus wires, as those are unshielded. Thus, to form a coupling/decoupling network, the bus cable termination of two times 120 Ω is grouped together to a resistance of 60 Ω. This load resistance is split into two equal resistors R1 + R2 of 30 Ω each. This offers the opportunity to input the interference voltage into the node between R1 and R2. The RF-generator is coupled via a series connection of C2 and R3 where R3 is used to increase the source impedance to the standardized value of 150 Ω for each wire, and C2 provides AC-coupling according to IEC 801-6. Note, that the effective impedance of the RF-interference source is 150 Ω with respect to reference ground according to IEC 801-6.

Obviously this equivalent circuit can be used for emission measurements as well, provided the RF-generator equipment is replaced by a spectrum analyzer or a test receiver.

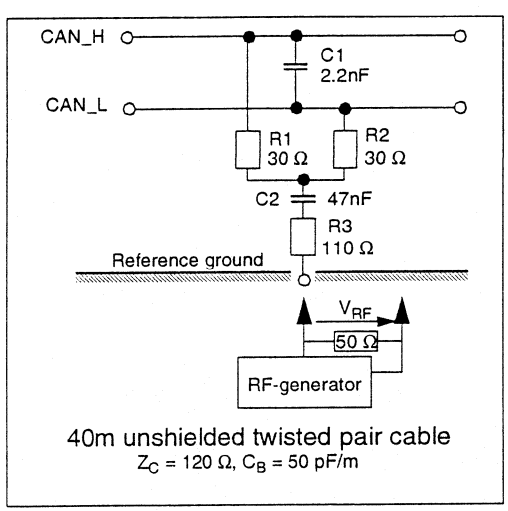

Fig. 5.1: Equivalent circuit for 40m unshielded bus cable with 120Ω termination

The following table contains general test conditions.

Parameter	Value	Remarks
Ambient temperature	25 °C	
Supply voltage	5 V	100nF bypass located at transceiver supply pins
Data signal frequency	125 kHz	equals 250 kbit/s with NRZ bit encoding
Data signal duty cycle	50%	data input signal
Tolerance range for duty cycle	10%	allowed deviation between duty cycle of data input and output signal
Frequency Range of Immunity Measurement	100 kHz - 240 MHz continuous wave, no modulat.	Maximum applied RF-amplifier output power level: 25 W
Frequency step	(fmax - fmin) / m	Number of RF- frequency steps per plot: m = 100
R_{ext} in slope-control mode	100 kΩ	slope adjust resistor at pin 8 of PCA82C250
R_{ext} in high-speed mode	0 Ω	
Common-mode choke	L = 51 µH, L_S = 2-3µH, sector winding, CM-insertion loss 30 dB @ 100MHz, Differential mode insertion loss 25 dB @ 100MHz	CM-choke type B82790-S0513-N201, manufactured by Siemens Matsushita Components

TABLE 1: EMC Measurement Parameters

The primary target here was to evaluate the EMC performance of transceiver products. Additionally the effect of a specific common-mode choke for CAN bus systems being recommended in [7] was of interest. For this purpose a data signal of rectangular pulse shape with a duty cycle of 50% and a frequency of 125 kHz was used. This is regarded as the representation of the worst case condition of a continuous NRZ-data signal at a bit rate of 250 kbit/s with alternating recessive and dominant bits.

To compare the EMC characteristics of different components, the layout of the transceiver board includes space and interconnections for appending a common-mode choke and also optional capacitors grounding the CANH and CANL outputs of the transceiver device.

ELECTROMAGNETIC IMMUNITY - The maximum interference level being input into the Faraday cage was around 27 V_{RMS} with an accuracy of about +/- 2 V, as the interference level was controlled in an open-loop manner. This corresponds to a power dissipation of as high as 15 W in the 50 Ω termination resistor of the RF-amplifier (fig. 5.1). In the following some results using the unshielded bus cable model shown in figure 5.1 are being presented. In figure 5.2 the level of immunity of the transceiver product PCA82C250, running in high-speed mode without any external filtering, is shown.
No degradation of the data signal was detected below an interference level of as high as 22 V_{RMS}. The dashed line in figure 5.2 indicates the immunity level of today's typical CAN transceiver products.

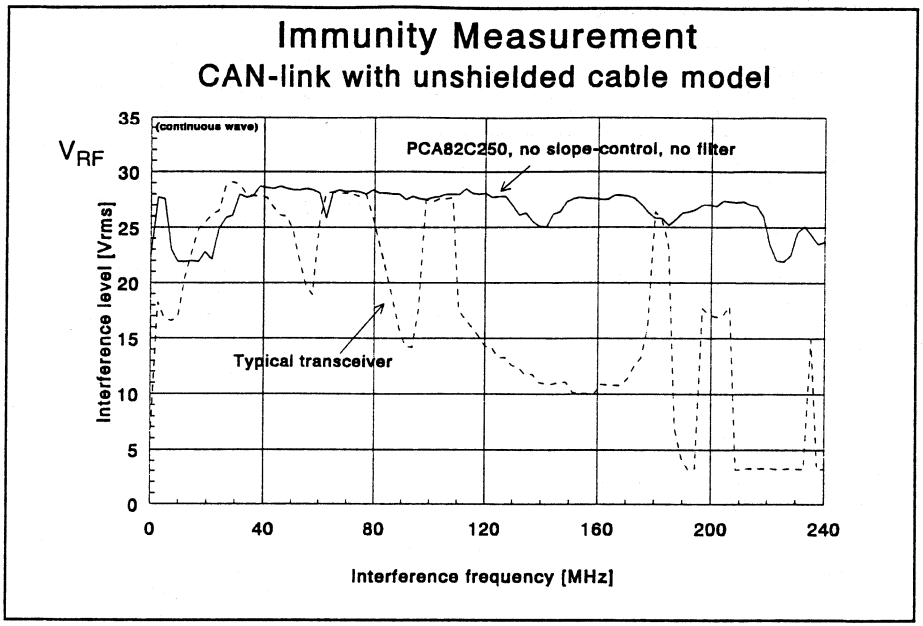

Fig. 5.2: Immunity level of PCA82C250 without filter

ELECTROMAGNETIC EMISSION - When replacing the RF-interference equipment by a spectrum analyzer, the electromagnetic emission of the CAN physical layer can be evaluated. Of course all test results being obtained in that way, are specific to the presented test method. A direct comparison with absolute noise levels of other test methods generally is not suitable.

The target here is to compare the effect of different EMC-measures, like slope-control function and common-mode choke, being proposed for reduction of the emission level. The results are depicted in figures 5.3 to 5.5. Note that emission levels below about 20 dBµV do not refer to the device under test, as they represent the so-called noise floor of the test equipment.

Figure 5.3 shows the amplitude spectrum of a CAN physical layer in high speed mode. The measured emission level decreases from about 60 dbµV @ 125 kHz to about 30 dbµV @ 90 MHz. This figure is typical for today's CAN

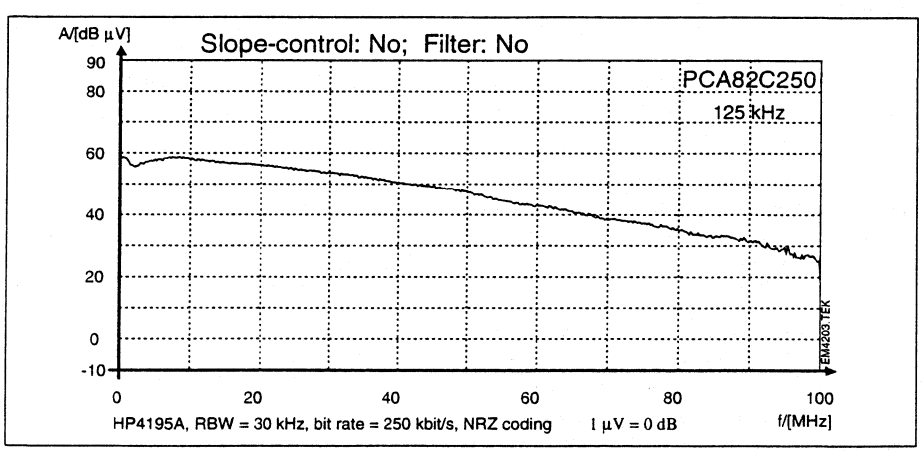

Fig. 5.3: Emission of CAN link in high speed mode

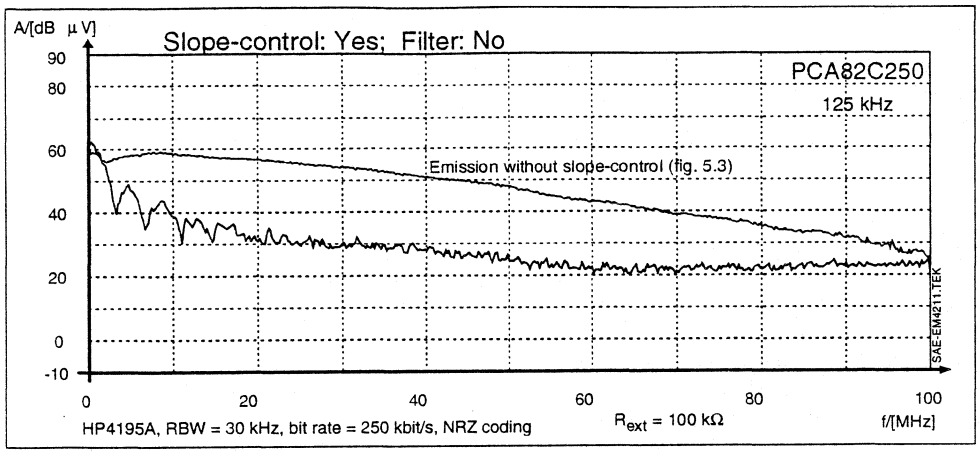

Fig. 5.4: Emission of CAN link in slope control mode

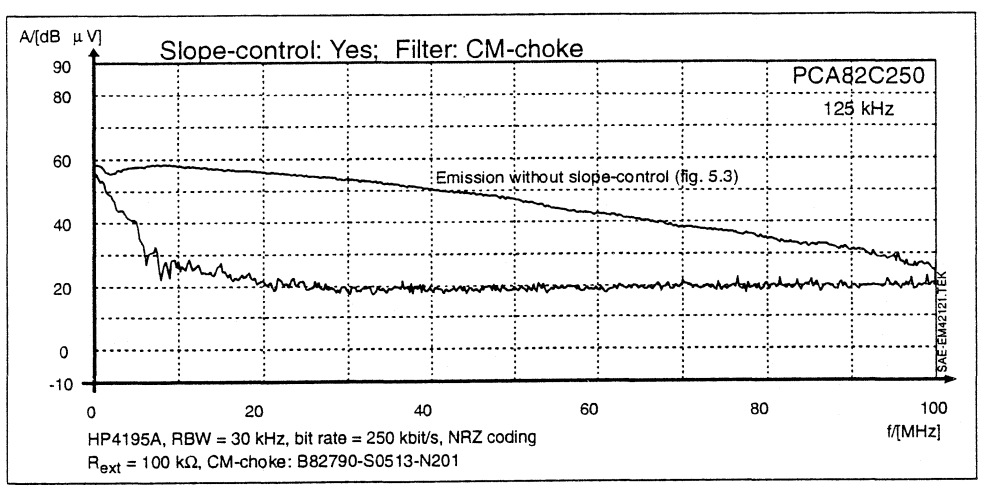

Fig. 5.5: Emission of CAN link in slope control mode with CM-choke

transceiver products without a slope-control function. A comparison to figure 5.4 shows that the emission level drops significantly faster to 30 dBµV @ 30 MHz by application of slope-control mode.

An even lower emission level is achieved when applying two measures, slope-control and common mode choke, as shown in figure 5.5. Here the emission level sharply drops down to the noise floor of the test equipment of about 20 dbµV at frequencies of 20 MHz and above.

6. CONCLUSION

The EMC performance of a bus system is mainly determined by the characteristics of its physical layer. Today's advanced CAN transceiver products feature special EMC related functions such as slope control function and extended common mode range. Using the presented IEC 801-6 based EMC test concept, the analysis is concluded with higher noise immunity and limited electromagnetic emission for the PCA82C250, when compared with typical CAN transceiver products. Due to this EMC performance, it is possible to operate CAN buses in vehicles with unshielded bus cables at bit rates in the range of 250 kbit/s. As this fact has direct impact on system cost, it will support the acceptance of serial data bus systems significantly.

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[7] EMI Suppression Chokes for Data and Signal Lines B82790, Data Book Supplement, Siemens Matsushita Components, 1994

CONTENTS

1 FEATURES

- 80C51 central processing unit (CPU)
- 16 kbytes on-chip ROM (EPROM), externally expandible to 64 kbytes
- 2 × 256 bytes on-chip RAM, externally expandible to 64 kbytes
- Two standard 16-bit timers/counters
- One additional 16-bit timer/counter coupled to four capture and three compare registers
- 10-bit ADC with 8 multiplexed analog inputs
- Two 8-bit resolution Pulse Width Modulated outputs
- 15 interrupt sources with 2 priority levels (2 to 6 external interrupt sources possible)
- Five 8-bit I/O ports, plus one 8-bit input port shared with analog inputs
- CAN-controller (CAN = Controller Area Network) with DMA data transfer facility to internal RAM
- 1 Mbit/s CAN-controller with bus failure management facility
- $\frac{1}{2}AV_{DD}$ reference voltage
- Full-duplex UART compatible with the standard 80C51
- On-chip Watchdog Timer (WDT)
- 1.2 to 16 MHz clock frequency (3.5 to 16 MHz for EPROM/OTP version).

2 GENERAL DESCRIPTION

The P8XC592 is a single-chip 8-bit high-performance microcontroller with on-chip CAN-controller, derived from the 80C51 microcontroller family.

It uses the powerful 80C51 instruction set.
Figure 1 shows a block diagram of the P8XC592.

The P8XC592 is manufactured in an advanced CMOS process, and is designed for use in automotive and general industrial applications. In addition to the 80C51 standard features, the device provides a number of dedicated hardware functions for these applications.

Three versions of the P8XC592 will be offered:

- P80C592 (without ROM)
- P83C592 (with ROM)
- P87C592 (EPROM/OTP; OTP = One Time Programmable).

Hereafter these versions will be referred to as P8XC592.

The temperature range includes (max. f_{CLK} = 16 MHz):

- –40 to +85 °C version, for general applications
- –40 to +125 °C version for automotive applications.

The P8XC592 combines the functions of the P8XC552 (microcontroller) and the PCA82C200 (Philips CAN-controller) with the following enhanced features:

- 16 kbytes Program Memory
- 2 × 256 bytes Data Memory
- DMA between CAN Transmit/Receive Buffer and internal RAM.

The main differences between P8XC592 and P8XC552 are:

- 16 kbytes programmable ROM resp. EPROM (P8XC552 has 8 kbytes)
- Additional 256 bytes RAM
- A CAN-controller instead of the I^2C-serial interface.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE (°C)	FREQ. (MHz)
	NAME	DESCRIPTION	VERSION		
Without ROM					
P80C592FFA	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2	–40 to +85	1.2 to 16
P80C592FHA				–40 to +125	
With ROM					
P83C592FFA	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2	–40 to +85	1.2 to 16
P83C592FHA				–40 to +125	
With EPROM/OTP					
P87C592EFL	CLCC68	ceramic leaded chip carrier (window); 68 leads	NO330	–40 to +85	3.5 to 16
P87C592EFA	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2		

4 BLOCK DIAGRAM

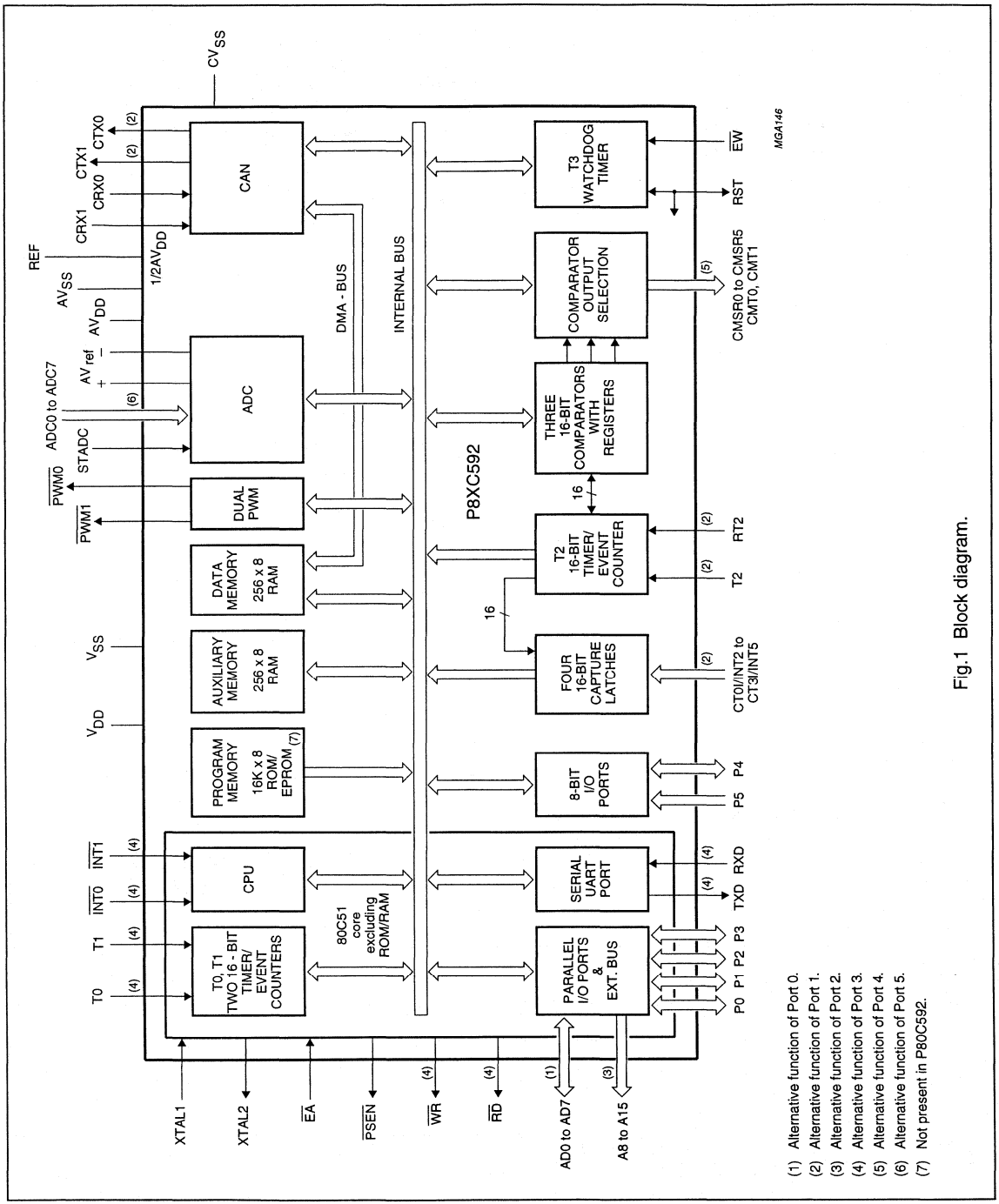
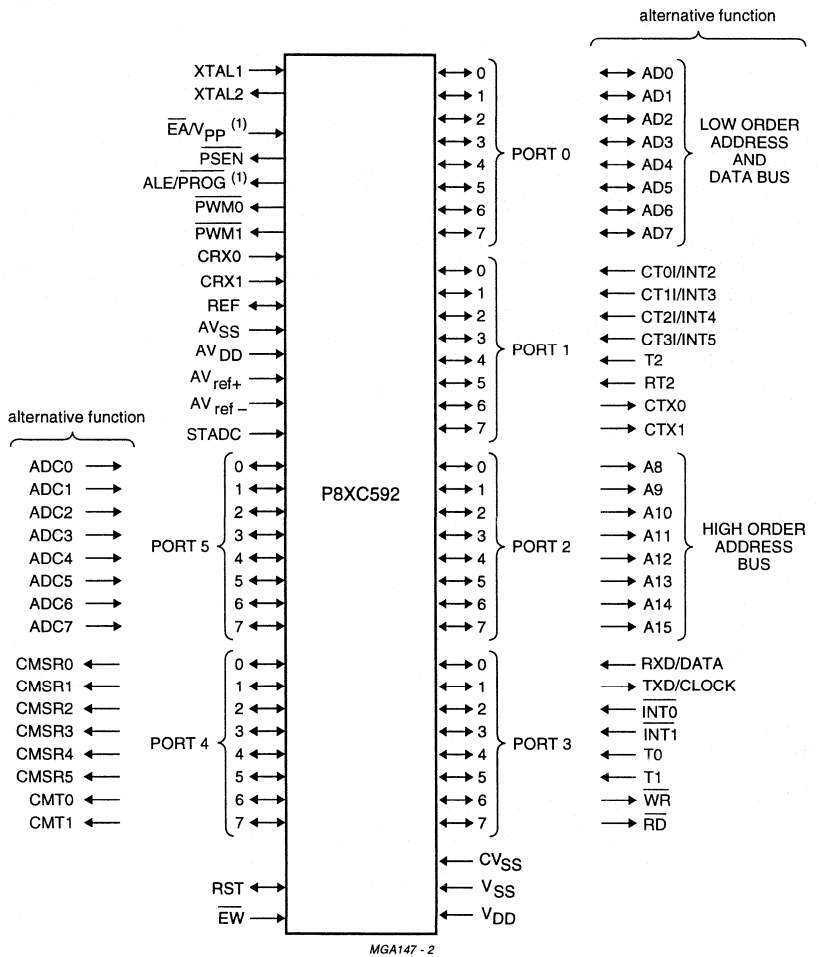


Fig.1 Block diagram.

(1) Alternative function of Port 0.
(2) Alternative function of Port 1.
(3) Alternative function of Port 2.
(4) Alternative function of Port 3.
(5) Alternative function of Port 4.
(6) Alternative function of Port 5.
(7) Not present in P80C592.

5 PINNING



(1) Only the **P87C592** with an alternative function.

Fig.2 Pin functions.

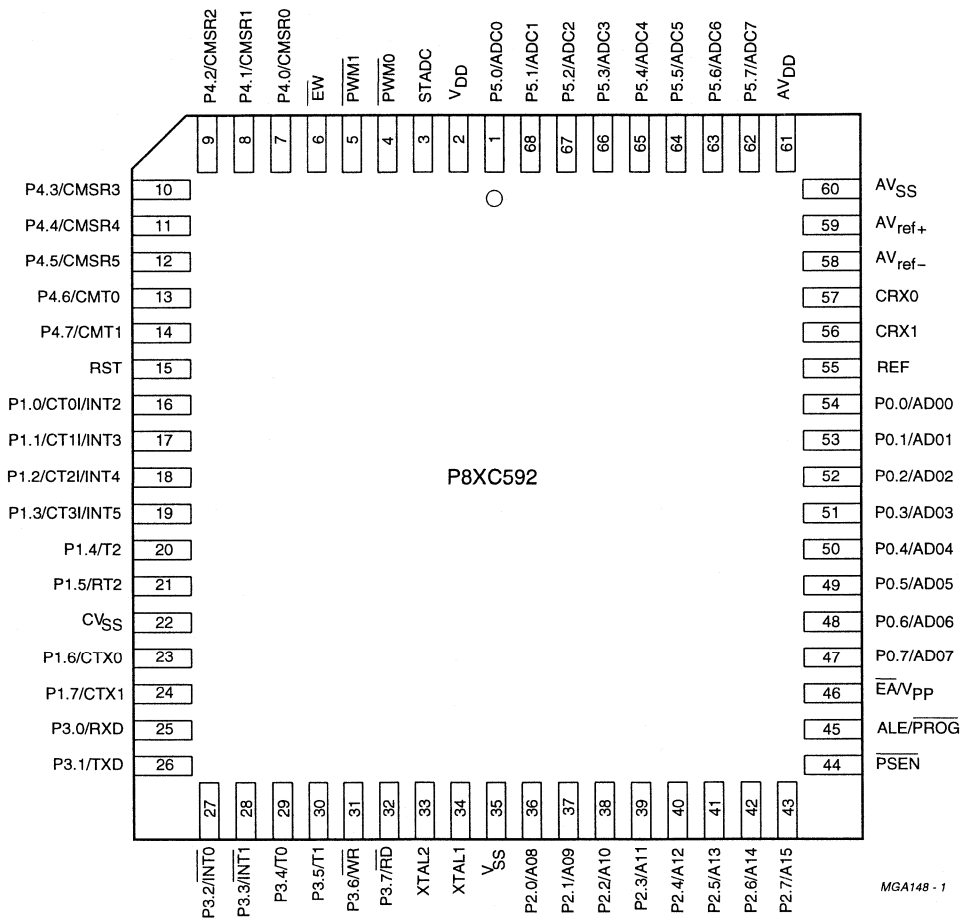


Fig.3 Pin configuration PLCC68/SOT188-2 version (P8XC592FFA; FHA; EFA).

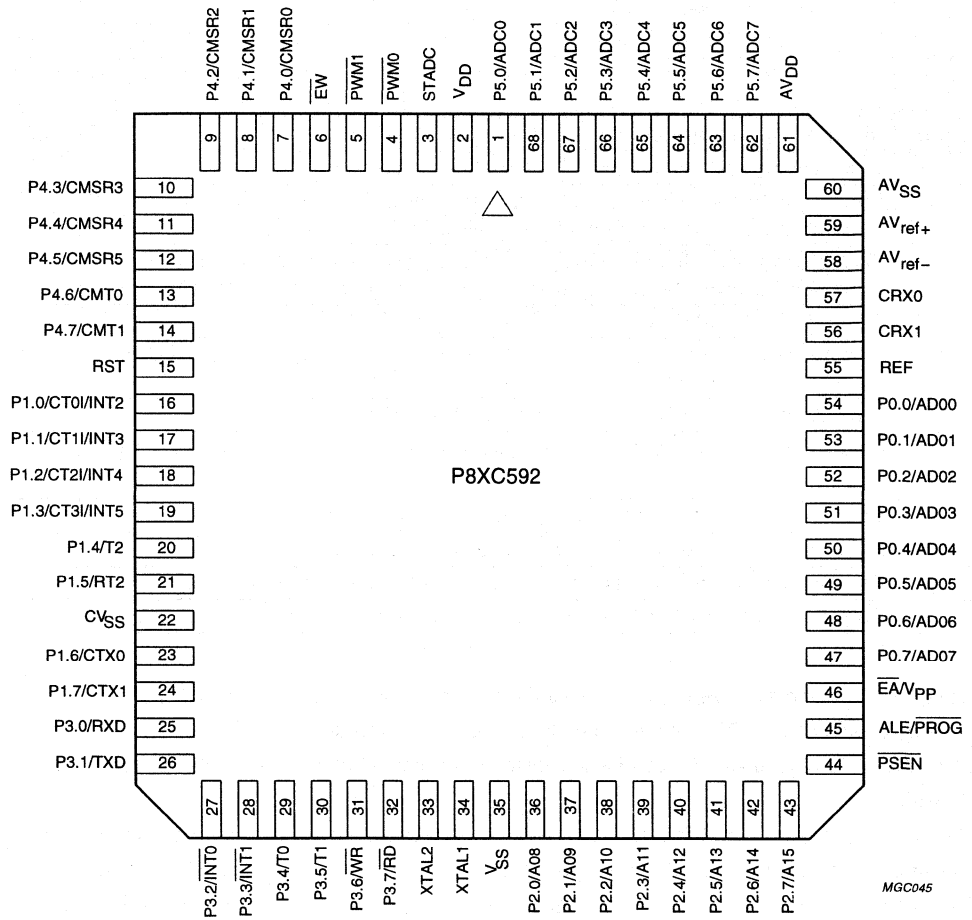


Fig.4 Pin configuration CLCC68/NO330 version (P87C592EFL).

Table 1 Pin description for **single function** pins (SOT188-2 and NO330; see note 1)

SYMBOL	PIN	DESCRIPTION
V_{DD}	2	**Power supply,** digital part (+5 V). For normal operation and power reduced modes.
STADC	3	**Start ADC operation.** Input starting analog-to-digital conversion (note 2). This pin must not float.
$\overline{PWM0}$	4	**Pulse width modulation output 0.**
$\overline{PMW1}$	5	**Pulse width modulation output 1.**
$\overline{EW}$	6	**Enable Watchdog Timer (WDT):** enable for T3 Watchdog Timer and disable Power-down mode. This pin must not float.
RST	15	**Reset:** input to reset the P8XC592 (note 3).
CV_{SS}	22	**CAN ground potential** for the CAN transmitter outputs.
XTAL2	33	**Crystal pin 2:** output of the inverting amplifier that forms the oscillator. When an external clock oscillator is used this pin is left open-circuit.
XTAL1	34	**Crystal pin 1:** input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external clock oscillator signal, when an external oscillator is used.
V_{SS}	35	**Ground**, digital part.
$\overline{PSEN}$	44	**Program Store Enable:** Read strobe to external Program Memory (active LOW). Drive: 8 × LSTTL inputs.
REF	55	**$\frac{1}{2}AV_{DD}$ reference voltage** output respectively input (note 4).
CRX1	56	**Inputs from the CAN-bus line** to the differential input comparator of the on-chip CAN-controller (note 5).
CRX0	57	
AV_{REF-}	58	**Low-end of ADC** (analog-to-digital) conversion reference resistor.
AV_{REF+}	59	**High-end of ADC** (analog-to-digital) conversion reference resistor (note 6).
AV_{SS}	60	**Ground**, analog part. For ADC, CAN receiver and reference voltage.
AV_{DD}	61	**Power supply**, analog part (+5 V). For ADC, CAN receiver and reference voltage.

Notes

1. To avoid a 'latch up' effect at power-on: $V_{SS} - 0.5\ V <$ 'voltage on any pin at any time' $< V_{DD} + 0.5\ V$.
2. Triggered by a rising edge. ADC operation can also be started by software.
3. RST also provides a reset pulse as output when timer T3 overflows or after a CAN wake-up from Power-down.
4. Pin 55, REF:
   a) Selection of input resp. output dependent of CAN Control Register bit 5 (CR.5; see Section 13.5.3 Table 32).
   b) If the internal reference is used, then REF should be connected to AV_{SS} via a capacitor with a value of ≥10 nF.
   c) After an external reset (RST = HIGH) the internal $\frac{1}{2}AV_{DD}$ source is activated and, REF is a reference output.
   d) If the CAN-controller is in the reset state, e.g. after an external reset, then the $\frac{1}{2}AV_{DD}$ source is switched off during Power-down mode.
5. CAN-bus line:
   a) CRX0 level > CRX1 level is interpreted as a logic 1 (recessive).
   b) CRX0 level < CRX1 level is interpreted as a logic 0 (dominant).
6. The level of AV_{REF+} must be higher than that of AV_{REF-}.

Table 2 Pin description for pins with **alternative functions** (SOT188-2 and NO330; see note 1)

SYMBOL		PIN	DESCRIPTION
DEFAULT	**ALTERNATIVE**		
Port 4			
P4.0 to P4.7		7 to 14	**8-bit quasi-bidirectional I/O port.**
	CMSR0	7	**Compare and Set/Reset outputs** for Timer T2.
	CMSR1	8	
	CMSR2	9	
	CMSR3	10	
	CMSR4	11	
	CMSR5	12	
	CMT0	13	**Compare and toggle outputs** for Timer T2.
	CMT1	14	
Port 1			
P1.0 to P1.7		16 to 21, 23, 24	**8-bit quasi-bidirectional I/O port.**
	CT0I/INT2	16	**Capture timer inputs** for Timer T2, or **External interrupt inputs.**
	CT1I/INT3	17	
	CT2I/INT4	18	
	CT3I/INT5	19	
	T2	20	**T2 event input** (rising edge triggered).
	RT2	21	**T2 timer reset input** (rising edge triggered).
	CTX0	23	**CAN transmitter output 0** (note 2).
	CTX1	24	**CAN transmitter output 1** (note 2).
Port 3			
P3.0 to P3.7		25 to 32	**8-bit quasi-bidirectional I/O port.**
	RXD	25	**Serial Input Port.**
	TXD	26	**Serial Output Port.**
	$\overline{\text{INT0}}$	27	**External interrupt inputs.**
	$\overline{\text{INT1}}$	28	
	T0	29	**Timer 0 external input.**
	T1	30	**Timer 1 external input.**
	$\overline{\text{WR}}$	31	**External Data Memory Write strobe.**
	$\overline{\text{RD}}$	32	**External Data Memory Read strobe.**
Port 2 (Sink/source: 1 × TTL = 4 × LSTTL inputs)			
P2.0 to P2.7		36 to 43	**8-bit quasi-bidirectional I/O port.**
	A08 to A15		**High-order address byte for external memory.**

SYMBOL		PIN	DESCRIPTION
DEFAULT	**ALTERNATIVE**		
ALE/$\overline{\text{PROG}}$ (Drive: 8 × LSTTL inputs; handles CMOS inputs without an external pull-up)			
ALE		45	**Address Latch Enable:** latches the Low-byte of the address during accesses to external memory (note 3).
	$\overline{\text{PROG}}$		**Programming-pulse input for P87C592.**
$\overline{\text{EA}}$/V_{PP}			
$\overline{\text{EA}}$		46	**External Access input.** See note 4.
	V_{PP}		**Programming supply voltage for P87C592.**
Port 0 (Sink/source: 8 × LSTTL inputs)			
P0.7 to P0.0		47 to 54	**8-bit open drain bidirectional I/O port.**
	AD7 to AD0		**Multiplexed Low-order address and Data bus for external memory.**
Port 5			
P5.7 to P5.0		62 to 68, 1	**8-bit input port.**
	ADC7 to ADC0		**8 input channels to ADC.**

Notes

1. To avoid a 'latch up' effect at power-on: $V_{SS} - 0.5\ V <$ 'voltage on any pin at any time' $< V_{DD} + 0.5\ V$.
2. If the CAN-controller is in the reset state (e.g. after a power-up reset; CAN Control Register bit CR.0; see Section 13.5.3 Table 32), the CAN transmitter outputs are floating and the pins P1.6 and P1.7 can be used as open-drain port pins. After a power-up reset the port data is HIGH, leaving the pins P1.6 and P1.7 floating.
3. ALE is activated every six oscillator periods. During an external data memory access one ALE pulse is skipped.
4. See Section 7.1, Table 3 for $\overline{\text{EA}}$ operation. For P83CXXX microcontrollers specified with the option 'ROM-code protection', the $\overline{\text{EA}}$ pin is latched during reset and is 'don't care' after reset, regardless of whether the ROM-code protection is selected or not.

6 FUNCTIONAL DESCRIPTION

The P8XC592 functions will be described as shown in the following overview:

- Memory organization
- I/O Port structure
- Pulse Width Modulated outputs
- Analog-to-digital Converter
- Timers/Counters
- Serial I/O Ports
- Interrupt system
- Power reduction modes
- Oscillator circuitry
- Reset circuitry
- Instruction Set.

7 MEMORY ORGANIZATION

The Central Processing Unit (CPU) manipulates operands in three memory spaces (see Fig.5) as follows:

- 16 kbytes internal resp. 64 kbytes external Program Memory
- 512 bytes internal Data Memory MAIN- and AUXILIARY RAM
- up to 64 kbytes external Data Memory (with 256 bytes residing in the internal AUXILIARY RAM).

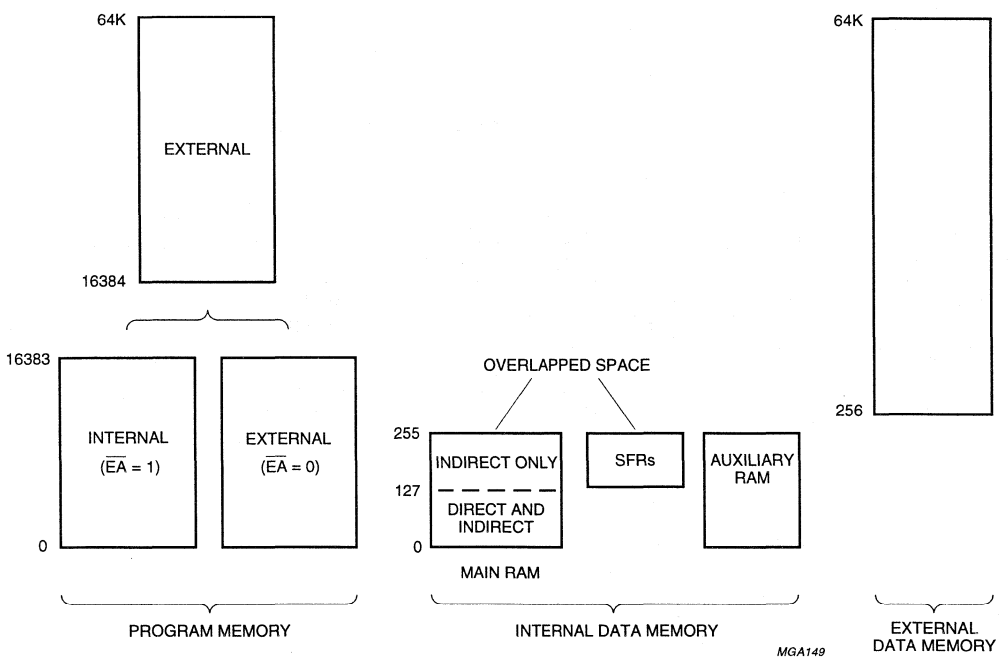


Fig.5 Memory map.

7.1 Program Memory

The Program Memory of the P8XC592 consists of 16 kbytes ROM respectively EPROM on-chip, externally expandible up to 64 kbytes.

Table 3 Instruction fetch controlled by $\overline{EA}$

PIN $\overline{EA}$ (note 1)		INSTRUCTIONS FETCHED FROM:	ADDRESS LOCATION
DURING RESET LATCHED TO:	AFTER RESET		
H	–	internal Program Memory (note 2)	0000H → 3FFFH
H	–	external Program Memory	4000H → FFFFH
L	–		0000H → FFFFH
–	'don't care'	–	–

Notes

1. This implementation prevents reading of the internal program code by switching from external Program Memory during a MOVC instruction.
2. By setting a security bit the internal Program Memory content is protected, which means it cannot be read out. If the security bit has been set to LOW there are no restrictions for the MOVC instruction. For code protection of the P87C592 see Section 22.2 "Security".

7.2 Internal Data Memory

The internal Data Memory is physically built-up and accessible as shown in Table 4 (see Fig.6).

Table 4 Internal Data Memory size and address mode

INTERNAL DATA MEMORY	SIZE	LOCATION	ADDRESS MODE		POINTERS
			DIRECT	INDIRECT	
MAIN RAM (note 1)	256 bytes	0 to 127	X	X	address pointers are R0 and R1 of the selected register bank
		128 to 255	–	X	
AUXILIARY RAM (note 2)	256 bytes	0 to 255	–	X	address pointers are R0 and R1 of the selected register bank and the DPTR
SFRs (note 3)	128 bytes	128 to 255	X	–	–

Notes

1. MAIN RAM can be addressed directly and indirectly as in the 80C51.
2. AUXILIARY RAM (0 to 255):
   a) Is indirectly addressable in the same way as the external Data Memory with MOVX instructions.
   b) Access will not affect the ports P0, P2, P3.6 and P3.7 during internal program execution.
3. SFRs = Special Function Registers.

7.2.1 MAIN RAM

Four 8-bit register banks occupy the lower RAM area,

- BANK 0: location 0 to 7
- BANK 1: location 8 to 15
- BANK 2: location 16 to 23
- BANK 4: location 24 to 31.

Only one of these banks may be enabled at the same time.

The next 16 bytes, locations 32 through 45, contains 128 directly addressable bit locations.

The stack can be located anywhere in the internal MAIN RAM address space. The stack depth is only limited by the internal RAM space available. All registers except the program counter and the four 8-bit register banks reside in the SFR address space.

7.3 External Data Memory

An access to external Data Memory locations higher than 255 will be performed with the MOVX @DPTR instructions in the same way as in the 80C51 structure, i.e. with P0 and P2 as data/address bus and P3.6 and P3.7 as Write and Read strobe signals.

Note that these external Data Memory locations cannot be accessed with R0 or R1 as address pointer.

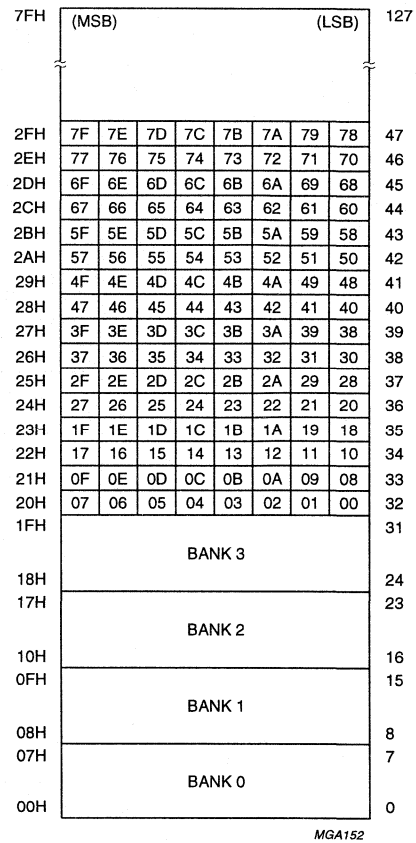


Fig.6 Internal MAIN RAM bit addresses.

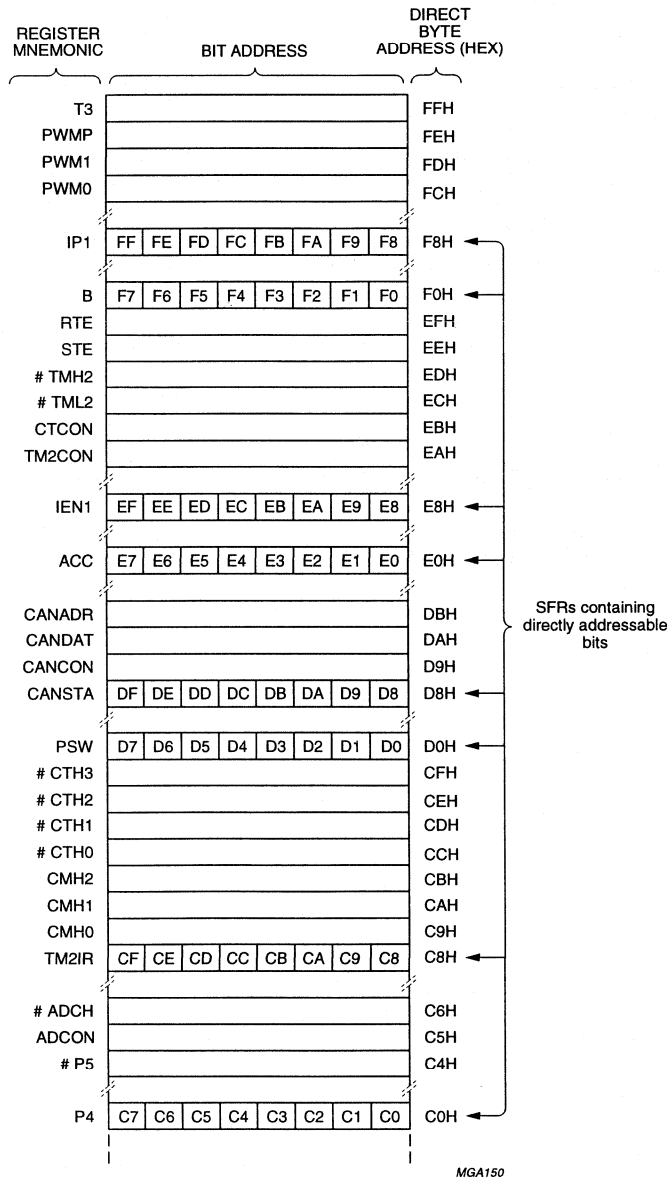


Fig.7 Special Function Register memory map (a).

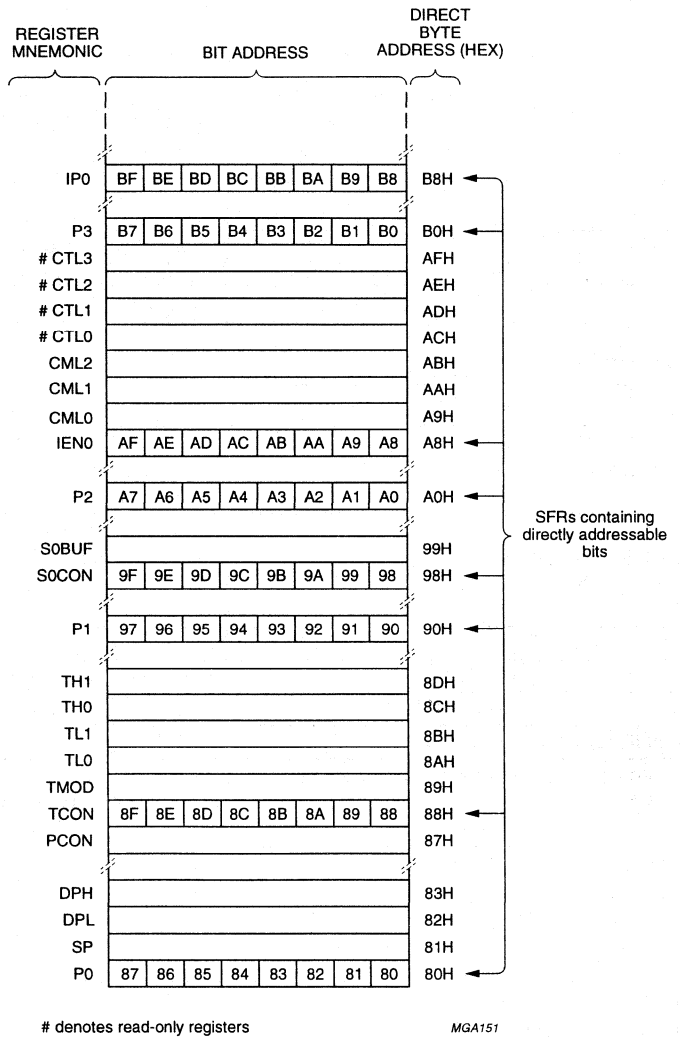


Fig.8 Special Function Register memory map (b).

8 I/O PORT STRUCTURE

The P8XC592 has six 8-bit parallel ports: Port 0 to Port 5. In addition to the standard 8-bit parallel ports, the I/O facilities also include a number of special I/O lines. The use of a Port 1, Port 3 or Port 4 pins as an alternative function is carried out automatically provided the associated SFR bit is set HIGH.

Table 5 Default Port functions

PORT	TYPE	FUNCTION	REMARKS
Port 0	I/O	The same as in the 80C51	Except for the additional functions of P1.6 and P1.7.
Port 1	I/O		
Port 2	I/O		
Port 3	I/O		
Port 4	I/O	Parallel I/O port	Parallel I/O function is identical to Port1, 2 and 3.
Port 5	I	Parallel input port with an input function only	May be used as normal inputs if the ADC function is inoperative.

Table 6 Alternative Port functions

PORT	TYPE	FUNCTION	REMARKS
Port 0	I/O	Multiplexed Low-order address and Data bus for external memory (AD7 to AD0)	Provides the multiplexed Low-order address and data bus used for expanding the P8XC592 with standard memories and peripherals.
Port 1	I/O	Capture timer inputs for Timer T2 (CT0I to CT3I), or External interrupt request inputs (INT2 to INT5)	External interrupt request inputs, if capture information is not utilized.
		T2 event input (T2)	External counter input.
		T2 timer reset input (RT2)	External counter reset input.
		CAN transmitter output 0 (CTX0)	CTX0 and CTX1 outputs of the CAN interface (note 1).
		CAN transmitter output 1 (CTX1)	
Port 2	I/O	High-order address byte for external memory (A08 to A15)	Port 2 provides the High-order address bus when the P8XC592 is expanded with external Program Memory and/or external Data Memory.
Port 3	I/O	Serial Input Port (RXD)	Receiver input of serial port SIO0 (UART).
		Serial Output Port (TXD)	Transmitter output of serial port SIO0 (UART).
		External interrupt ($\overline{INT0}$)	External interrupt request inputs.
		External interrupt ($\overline{INT1}$)	
		Timer 0 external input (T0)	Counter inputs.
		Timer 1 external input (T1)	
		External data memory Write strobe ($\overline{WR}$)	Control signal to write to external Data Memory.
		External data memory Read strobe ($\overline{RD}$)	Control signal to read from external Data Memory.
Port 4	I/O	Compare and Set/Reset outputs (CMSR0 to CMSR5)	Can be configured to provide signals indicating a match between Timer counter T2 and its compare registers.
		Compare and toggle outputs (CMT0, CMT1)	
Port 5	I	Input channels to ADC (ADC7 to ADC0)	Port 5 may be used in conjunction with the ADC interface (note 2).

Notes to the alternative Port functions

1. Port lines P1.6 and P1.7 may be selected as CTX0 and CTX1 outputs of the serial port SIO1 (CAN). After reset P1.6 and P1.7 may be used as normal I/O ports, if the CAN interface is not used.
2. Unused analog inputs can be used as digital inputs. As Port 5 lines may be used as inputs to the ADC, these digital inputs have an inherent hysteresis to prevent the input logic from drawing too much current from the power lines when driven by analog signals.
   Channel-to-channel crosstalk should be taken into consideration when both digital and analog signals are simultaneously input to Port 5 (see Chapter 20).

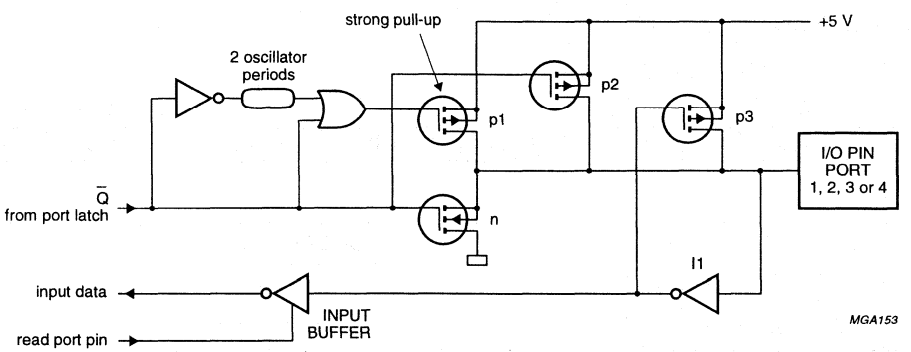


Fig.9 I/O buffers in the P8XC592 (P1.0 to P1.5, Ports 2, 3, and 4).

9 PULSE WIDTH MODULATED OUTPUTS (PWM)

Two Pulse Width Modulated (PWM) output channels are available with the P8XC592. These channels provide output pulses of programmable length and interval. The repetition frequency is defined by an 8-bit prescaler PWMP which generates the clock for the counter. Both the prescaler and counter are common to both PWM channels. The 8-bit counter counts modulo 255 i.e. from 0 to 254 inclusive. The value of the 8-bit counter is compared to the contents of two registers: PWM0 and PWM1.

Provided the contents of either of these registers is greater than the counter value, the output of $\overline{\text{PWM0}}$ or $\overline{\text{PWM1}}$ is set LOW. If the contents of these register are equal to, or less than the counter value, the output will be HIGH. The pulse-width-ratio is therefore defined by the contents of the register PWM0 and PWM1. The pulse-width-ratio is in the range of 0 to $^{255}/_{255}$ and may be programmed in increments of $^{1}/_{255}$.

The repetition frequency f_{PWM}, at the $\overline{\text{PWMn}}$ outputs is given by: $f_{PWM} = \frac{f_{CLK}}{2 \times (PWMP + 1) \times 255}$

When using an oscillator frequency of 16 MHz, for example, the above formula would give a repetition frequency range of 123 Hz to 31.4 kHz.

By loading the PWM registers with either 00H or FFH, the PWM outputs can be retained at a constant HIGH or LOW level respectively. When loading FFH to the PWM registers, the 8-bit counter will never actually reach this (FFH) value.
Both output pins $\overline{\text{PWMn}}$ are driven by push-pull drivers, and are not shared with any other function.

9.1 Prescaler frequency control register (PWMP)

Table 7 Prescaler frequency control register (address FEH)

7	6	5	4	3	2	1	0
PWMP.7	PWMP.6	PWMP.5	PWMP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.0

Table 8 Description of PWMP bits

BIT	SYMBOL	FUNCTION
7 to 0	PWMP.7 to PWMP.0	**Prescaler division factor.** The Prescaler division factor = (PWMP) + 1.

9.2 Pulse Width Register 0 (PWM0)

Table 9 Pulse Width Register (address FCH)

7	6	5	4	3	2	1	0
PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0

Table 10 Description of PWM0 bits

BIT	SYMBOL	FUNCTION
7 to 0	PWM0.7 to PWM0.0	**Pulse width ratio.** LOW/HIGH ratio of $\overline{PWMn}$ signals $= \frac{(PWMn)}{255 - (PWMn)}$

9.3 Pulse Width Register 1 (PWM1)

Table 11 Pulse width register (address FDH)

7	6	5	4	3	2	1	0
PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0

Table 12 Description of PWM1 bits

BIT	SYMBOL	FUNCTION
7 to 0	PWM1.7 to PWM1.0	**Pulse width ratio.** LOW/HIGH ratio of $\overline{PWMn}$ signals $= \frac{(PWMn)}{255 - (PWMn)}$

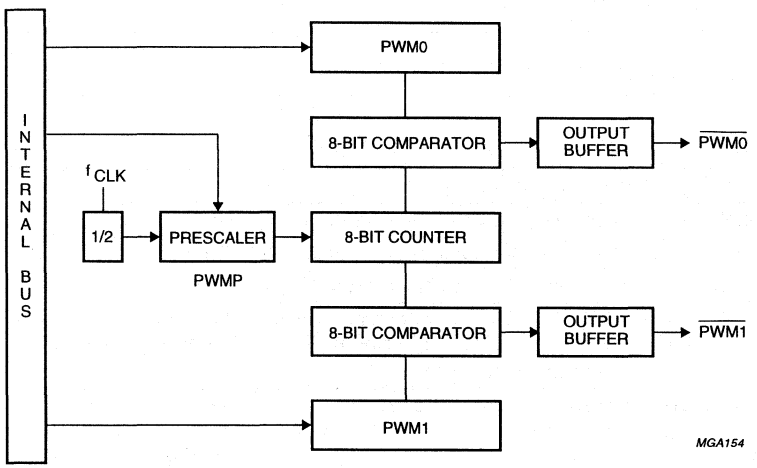


Fig.10 Functional diagram of Pulse Width Modulated outputs.

10 ANALOG-TO-DIGITAL CONVERTER (ADC)

The analog input circuitry consists of an 8-input analog multiplexer and an ADC with 10-bit resolution. The analog reference voltage and analog power supplies are connected via separate input pins. The conversion takes 50 machine cycles i.e. 37.5 µs at 16 MHz oscillator frequency. The input voltage swing is from 0 V to AV_{DD}. The ADC is controlled using the ADCON control register. Register bits ADCON.0 to ADCON.2 select the input channels of the analog multiplexer (see Fig.11).
The completion of the 10-bit analog-to-digital conversion is flagged by ADCI in the ADCON register and the result is stored in the SFR ADCH (upper 8-bits) and the 2 lower bits (ADC.1 and ADC.0) in register ADCON.

An analog-to-digital conversion in progress is unaffected by an external or software ADC start. The result of a completed conversion remains unchanged provided ADCI = HIGH. While ADCI or ADCS are HIGH, a new ADC START will be blocked and consequently lost. An analog-to-digital conversion already in progress is aborted when the Idle or Power-down mode is entered.

The result of a completed conversion (ADCI = HIGH) remains unaffected during the Idle mode.
The LOW-to-HIGH transition of STADC is recognized at the end of a machine cycle and the conversion commences at the beginning of the next cycle. When a conversion is initiated by software, the conversion starts at the beginning of the machine cycle following the instruction that sets ADCS.

The next two machine cycles are used to initiate the converter. At the end of this first cycle, the ADCS status flag is set to HIGH while the conversion is in progress. Sampling of the analog input commences at the end of the second cycle.

During the next eight machine cycles, the voltage at the previously selected pin of Port 5 is sampled and this input voltage should be stable in order to obtain a useful sample. In any case, the input voltage slew rate must be less than 10 V/ms (5 V conversion range) in order to prevent an undefined result. The conversion takes four machine cycles per bit.

10.1 ADC Control register (ADCON)

Table 13 ADC Control register (address C5H)

7	6	5	4	3	2	1	0
ADC.1	ADC.0	ADEX	ADCI	ADCS	AADR2	AADR1	AADR0

Table 14 Description of the ADCON bits

BIT	SYMBOL	FUNCTION
7	ADC.1	Bit 1 of ADC converted value.
6	ADC.0	Bit 0 of ADC converted value.
5	ADEX	Enable external start of conversion by STADC. If ADEX is: LOW, then conversion cannot be started externally by STADC (only by software by setting ADCS) HIGH, then conversion can be started externally by a rising edge on STADC or externally.
4	ADCI	**ADC interrupt flag.** This flag is set when an analog-to-digital conversion result is ready to be read. If enabled, an interrupt is invoked. The flag must be cleared by software. It cannot be set by software (see Table 15).
3	ADCS	**ADC start and status.** Setting this bit starts an analog-to-digital conversion. It may be set by software or by the external signal STADC. The ADC logic ensures that this signal is HIGH while the ADC is busy. On completion of the conversion, ADCS is reset at the same time the interrupt flag ADCI is set. ADCS can not be reset by software (see Table 15).
2	AADR2	**Analog input select**. This binary coded address selects one of the eight analog port pins of P5 to be input to the converter. It can only be changed when ADCI and ADCS are both LOW. AADR2 is the MSB. (e.g. 100B selects the analog input channel ADC4)
1	AADR1	
0	AADR0	

Table 15 ADCI and ADCS operating modes

If ADCI is cleared by software while ADCS is set at the same time a new analog-to-digital conversion with the same channel-number may be started. It is recommended to reset ADCI before ADCS is set.

ADCI	ADCS	OPERATION
0	0	ADC not busy, a conversion can be started.
0	1	ADC busy, start of a new conversion is blocked.
1	X (don't care)	Conversion completed; see note 1.

Note

1. Start of a new conversion requires ADCI = 0.

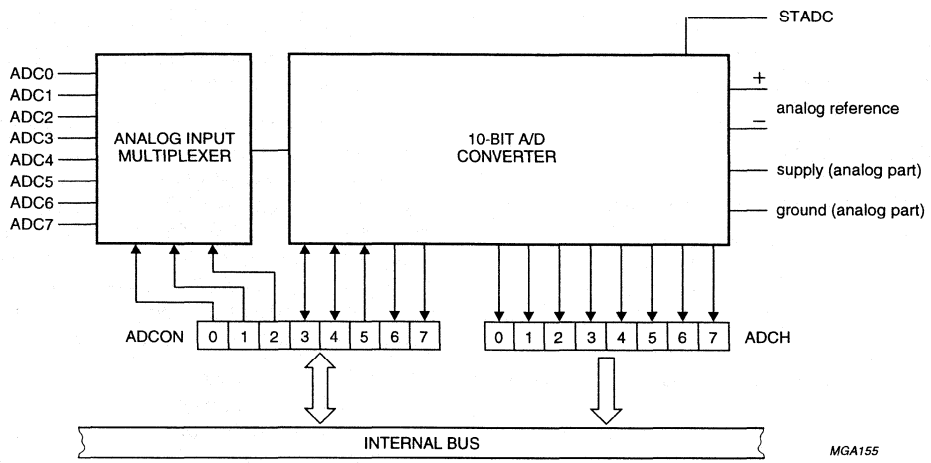


Fig.11 Functional diagram of analog input.

11 TIMERS/COUNTERS

The P8XC592 contains:

- Three 16-bit timer/event counters: Timer 0, Timer 1 and Timer T2
- One 8-bit timer, T3 (Watchdog WDT).

11.1 Timer 0 and Timer 1

Timer 0 and Timer 1 may be programmed to carry out the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests.

Timer 0 and Timer 1 can be programmed independently to operate in 3 modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.

Mode 1 16-bit timer-interval or event counter.

Mode 2 8-bit timer-interval or event counter with automatic reload upon overflow.

Timer 0 can be programmed to operate in an additional mode as follows:

Mode 3 one 8-bit time-interval or event counter and one 8-bit timer-interval counter.

When Timer 0 is in Mode 3, Timer 1 can be programmed to operate in Modes 0, 1 or 2 but cannot set an interrupt flag or generate an interrupt. However, the overflow from Timer 1 can be used to pulse the Serial Port baud-rate generator.

The frequency handling range of these counters with a 16 MHz crystal is as follows:

- In the timer function, the timer is incremented at a frequency of 1.33 MHz ($1/12$ of the oscillator frequency)
- 0 Hz to an upper limit of 0.66 MHz ($1/24$ of the oscillator frequency) when programmed for external inputs.

Both internal and external inputs can be gated to the counter by a second external source for directly measuring pulse durations. When configured as a counter, the register is incremented on every falling edge on the corresponding input pin, T0 or T1.

The earliest moment, when the incremented register value can be read is during the second machine cycle following the machine cycle within which the incrementing pulse occurred.The counters are started and stopped under software control. Each one sets its interrupt request flag when it overflows from all HIGHs to all LOWs (or automatic reload value), with the exception of Mode 3 as previously described.

11.2 Timer T2 Capture and Compare Logic

Timer T2 is a 16-bit timer/counter which has capture and compare facilities (see Fig.12).

The 16-bit timer/counter is clocked via a prescaler with a programmable division factor of 1, 2, 4 or 8. The input of the prescaler is clocked with $1/12$ of the oscillator frequency, or by an external source connected to the T2 input, or it is switched off. The maximum repetition rate of the external clock source is $1/12 f_{CLK}$, twice that of Timer 0 and Timer 1. The prescaler is incremented on a rising edge. It is cleared if its division factor or its input source is changed, or if the timer/counter is reset.

T2 is readable 'on the fly', without any extra read latches; this means that software precautions have to be taken against misinterpretation at overflow from least to most significant byte while T2 is being read. T2 is not loadable and is reset by the RST signal or at the positive edge of the input signal RT2, if enabled. In the Idle mode the timer/counter and prescaler are reset and halted.

T2 is connected to four 16-bit Capture Registers: CT0, CT1, CT2 and CT3. A rising or falling edge on the inputs CT0I, CT1I, CT2I or CT3I (alternative function of Port 1) results in loading the contents of T2 into the respective Capture Registers and an interrupt request.

Using the Capture Register CTCON, these inputs may invoke capture and interrupt request on a positive edge, a negative edge or on both edges. If neither a positive nor a negative edge is selected for capture input, no capture or interrupt request can be generated by this input.

The contents of the Compare Registers CM0, CM1 and CM2 are continually compared with the counter value of Timer T2. When a match occurs, an interrupt may be invoked. A match of CM0 sets the bits 0 to 5 of Port 4, a CM1 match resets these bits and a CM2 match toggles bits 6 and 7 of Port 4, provided these functions are enabled by the STE/RTE registers. A match of CM0 and CM1 at the same time results in resetting bits 0 to 5 of Port 4. CM0, CM1 and CM2 are reset by the RST signal.

Port 4 can be read and written by software without affecting the toggle, set and reset signals. At a byte overflow of the least significant byte, or at a 16-bit overflow of the timer/counter, an interrupt sharing the same interrupt vector is requested. Either one or both of these overflows can be programmed to request an interrupt. All interrupt flags must be reset by software.

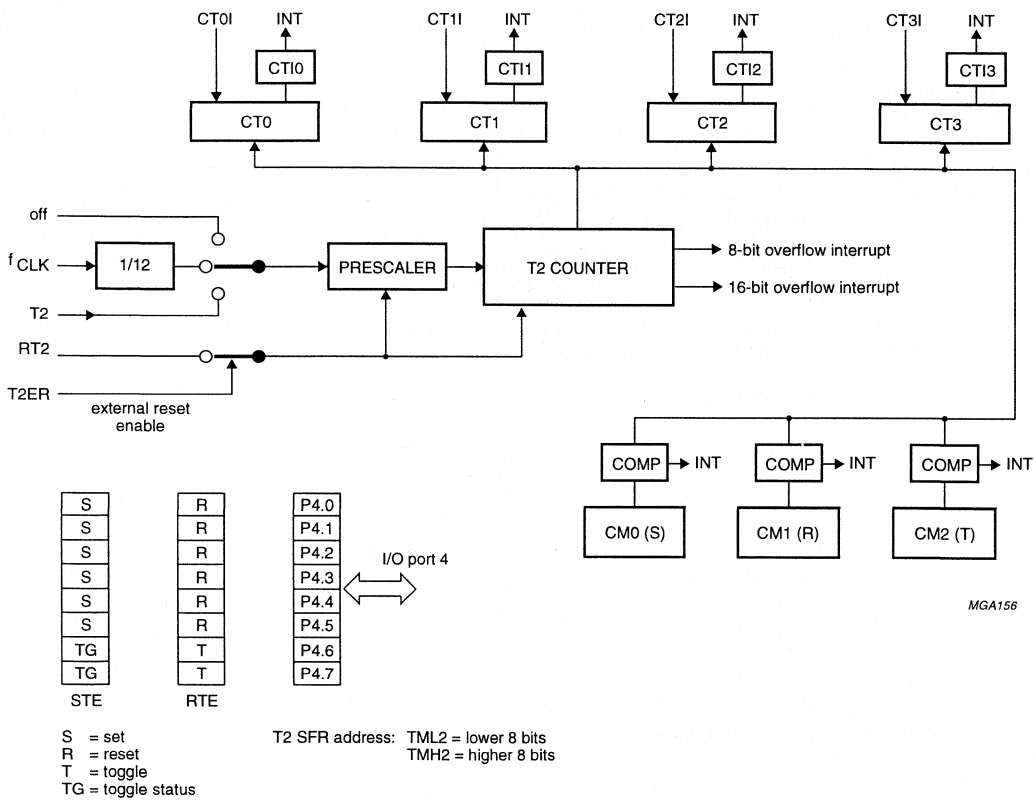


Fig.12 Block diagram of Timer T2 configuration.

11.2.1 Counter Control register (TM2CON)

Table 16 Counter Control register (address EAH)

7	6	5	4	3	2	1	0
T2IS1	T2IS0	T2ER	T2B0	T2P1	T2P0	T2MS1	T2MS0

Table 17 Description of the TM2CON bits

BIT	SYMBOL	FUNCTION
7	T2IS1	Timer 2 16-bit overflow interrupt select.
6	T2IS0	Timer 2 byte overflow interrupt select.
5	T2ER	Timer 2 external reset enable.
4	T2B0	Timer 2 byte overflow interrupt flag.
3	T2P1	Timer 2 prescaler select (see Table 18).
2	T2P0	
1	T2MS1	Timer 2 mode select (see Table 19).
0	T2MS0	

Table 18 Timer 2 prescaler select

T2P1	T2P0	T2 CLOCK
0	0	Clock source
0	1	$\frac{1}{2}$ Clock source
1	0	$\frac{1}{4}$ Clock source
1	1	$\frac{1}{8}$ Clock source

Table 19 Timer 2 mode select

T2MS1	T2MS0	MODE
0	0	Timer T2 is halted
0	1	T2 clock source = $\frac{1}{12}f_{CLK}$.
1	0	Test mode; do not use
1	1	T2 clock source = pin T2

11.2.2 Capture Control register (CTCON)

Table 20 Capture Control register (address EBH)

7	6	5	4	3	2	1	0
CTN3	CTP3	CTN2	CTP2	CTN1	CTP1	CTN0	CTP0

Table 21 Description of the CTCON bits

BIT	SYMBOL	FUNCTION	
		CAPTURE	INTERRUPT ON
7	CTN3	CT3I	negative edge
6	CTP3	CT3I	positive edge
5	CTN2	CT2I	negative edge
4	CTP2	CT2I	positive edge
3	CTN1	CT1I	negative edge
2	CTP1	CT1I	positive edge
1	CTN0	CT0I	negative edge
0	CTP0	CT0I	positive edge

11.2.3 TIMER INTERRUPT FLAG REGISTER (TM2IR)

Table 22 Timer Interrupt Flag register (address C8H)

7	6	5	4	3	2	1	0
T2OV	CMI2	CMI1	CMI0	CTI3	CTI2	CTI1	CTI0

Table 23 Description of the TM2IR bits (see notes 1 and 2)

BIT	SYMBOL	FUNCTION
7	T2OV	T2: 16-bit overflow interrupt flag
6	CMI2	CM2: interrupt flag
5	CMI1	CM1: interrupt flag
4	CMI0	CM0: interrupt flag
3	CTI3	CT3: interrupt flag
2	CTI2	CT2: interrupt flag
1	CTI1	CT1: interrupt flag
0	CTI0	CT0: interrupt flag

Notes

1. Interrupt Enable IEN1 is used to enable/disable Timer 2 interrupts (see Section 14.1.2).
2. Interrupt Priority Register IP1 is used to determine the Timer 2 interrupt priority (see Section 14.1.4).

11.2.4 SET ENABLE REGISTER (STE)

Table 24 Set Enable register (address EEH)

7	6	5	4	3	2	1	0
TG47	TG46	SP45	SP44	SP43	SP42	SP41	SP40

Table 25 Description of the STE bits (see notes 1 and 2)

BIT	SYMBOL	FUNCTION
7	TG47	if HIGH then P4.7 is reset on the next toggle, if LOW P4.7 is set on the next toggle
6	TG46	if HIGH then P4.6 is reset on the next toggle, if LOW P4.6 is set on the next toggle
5	SP45	if HIGH then P4.5 is set on a match of CM0 and T2
4	SP44	if HIGH then P4.4 is set on a match of CM0 and T2
3	SP43	if HIGH then P4.3 is set on a match of CM0 and T2
2	SP42	if HIGH then P4.2 is set on a match of CM0 and T2
1	SP41	if HIGH then P4.1 is set on a match of CM0 and T2
0	SP40	if HIGH then P4.0 is set on a match of CM0 and T2

Notes

1. If STE.n is LOW then P4.n is not affected by a match of CM0 and T2 (n = 0, 1, 2, 3, 4, 5).
2. STE.6 and STE.7 are read only.

11.2.5 RESET/TOGGLE ENABLE REGISTER (RTE)

Table 26 Reset/Toggle Enable register (address EFH)

7	6	5	4	3	2	1	0
TP47	TP46	RP45	RP44	RP43	RP42	RP41	RP40

Table 27 Description of the RTE bits (note 1)

BIT	SYMBOL	FUNCTION
7	TP47	if HIGH then P4.7 toggles on a match of CM2 and T2
6	TP46	if HIGH then P4.6 toggles on a match of CM2 and T2
5	RP45	if HIGH then P4.5 is reset on a match of CM1 and T2
4	RP44	if HIGH then P4.4 is reset on a match of CM1 and T2
3	RP43	if HIGH then P4.3 is reset on a match of CM1 and T2
2	RP42	if HIGH then P4.2 is reset on a match of CM1 and T2
1	RP41	if HIGH then P4.1 is reset on a match of CM1 and T2
0	RP40	if HIGH then P4.0 is reset on a match of CM1 and T2

Note

1. If RTE.n is LOW then P4.n is not affected by a match of CM1 and T2 or CM2 and T2.
   For more information, refer to the 8051-based *"8-bit Microcontrollers Data Handbook IC20"*.

11.3 Watchdog Timer (T3)

In addition to Timer T2 and the standard timers (Timer 0 and Timer 1), a Watchdog Timer (WDT) comprising an 11-bit prescaler and an 8-bit timer (T3) is also provided (see Fig.13).

The timer T3 is incremented every 1.5 ms, derived from the oscillator frequency of 16 MHz by the following

formula: $f_{timer} = \frac{f_{CLK}}{12 \times 2048}$

When a timer T3 overflow occurs, the microcontroller is reset and a reset-output-pulse is generated at pin RST. This short output pulse (3 machine cycles) may be suppressed if the RST pin is connected to a capacitor.

To prevent a system reset (by an overflow of the WDT), the user program has to reload T3 within periods that are shorter than the programmed Watchdog time interval.

If the processor suffers a hardware/software malfunction, the software will fail to reload the timer. This failure will produce a reset upon overflow thus preventing the processor running out of control.

The Watchdog Timer can only be reloaded if the condition flag WLE = PCON.4 has been previously set by software. At the moment the counter is loaded the condition flag is automatically cleared.

The timer interval between the timer's reloading and the occurrence of a reset depends on the reloaded value. For example, this may range from 1.5 ms to 0.375 s when using an oscillator frequency of 16 MHz.

In the Idle state the Watchdog Timer and reset circuitry remain active.

The Watchdog Timer (WDT) is controlled by the Enable Watchdog pin ($\overline{EW}$) (see Table 28).

Table 28 $\overline{EW}$ controlling WDT and Power-down mode

PIN $\overline{EW}$	WDT	POWER-DOWN MODE
LOW	enabled	disabled
HIGH	disabled	enabled

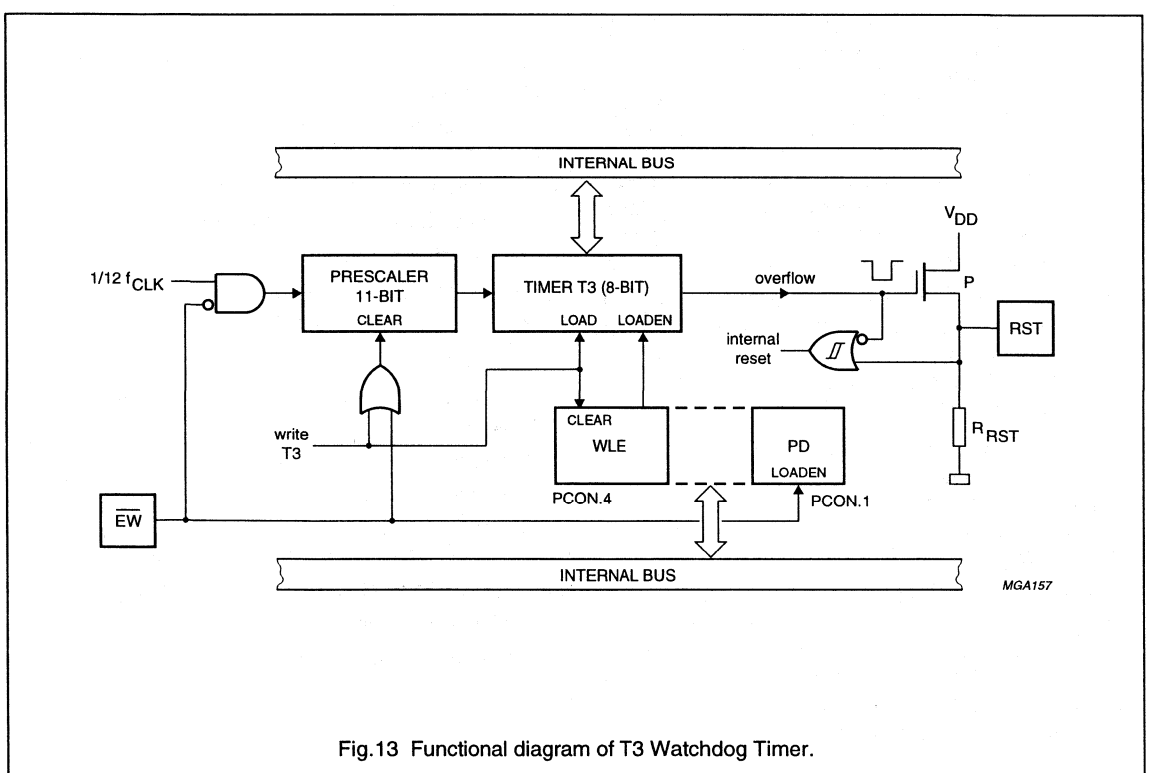


Fig.13 Functional diagram of T3 Watchdog Timer.

12 SERIAL I/O PORT: SIO0 (UART)

The Serial Port SIO0 is a full duplex (UART) serial I/O port i.e. it can transmit and receive simultaneously. This Serial Port is also receive-buffered. It can commence reception of a second byte before the previously received byte has been read from the receive register. However, if the first byte has still not been read by the time reception of the second byte is complete, one of these (first or second) bytes will be lost. The SIO0 receive and transmit registers are both accessed via the S0BUF SFR. Writing to S0BUF loads the transmit register, and reading S0BUF accesses to a physically separate receive register. SIO0 can operate in 4 modes:

Mode 0 Serial data is transmitted and received through RXD. TXD outputs the shift clock. 8 data bits are transmitted/received (LSB first). The baud rate is fixed at $1/12$ of the oscillator frequency.

Mode 1 10 bits are transmitted via TXD or received through RXD: a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit is put into RB8 of the S0CON SFR. The baud rate is variable.

Mode 2 11 bits are transmitted through TXD or received through RXD: a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8 in S0CON) can be assigned the value of 0 or 1. With nominal software, TB8 can be the parity bit (P in PSW). During a receive, the 9th data bit is stored in RB8 (S0CON), and the stop bit is ignored. The baud rate is programmable to either $1/32$ or $1/64$ of the oscillator frequency.

Mode 3 11 bits are transmitted through TXD or received through RXD: a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is the same as Mode 2 except for the baud rate which is variable in Mode 3.

In all four modes, transmission is initiated by any instruction that writes to the S0BUF SFR.
Reception is initiated in Mode 0 when RI = 0 and REN = 1. In the other three modes, reception is initiated by the incoming start bit provided that REN = 1.

Modes 2 and 3 are provided for multiprocessor communications. In these modes, 9 data bits are received with the 9th bit written to RB8 (S0CON). The 9th bit is followed by the stop bit. The port can be programmed so that with receiving the stop bit, the Serial Port interrupt will be activated if, and only if RB8 = 1.

This feature is enabled by setting bit SM2 in S0CON. This feature may be used in multiprocessor systems.

For more information about how to use the UART in combination with the registers S0CON, PCON, IE, SBUF and the Timer register, refer to the 8051-based *"8-bit Microcontrollers Data Handbook IC20"*.

13 SERIAL I/O PORT: SIO1 (CAN)

SIO1 (CAN) provides the CAN (Controller Area Network) serial-bus data communication interface. SIO1 (CAN) replaces the SIO1 (I^2C) serial interface as provided in the microcontroller derivative P8XC552.

13.1 On-chip CAN-controller

CAN is the definition of a high performance communication protocol for serial data communication. The P8XC592 on-chip CAN-controller is a full implementation of the CAN 2.0A protocol. With the P8XC592 powerful local networks can be built, both for automotive and general industrial environments. This results in a much reduced wiring harness and enhanced diagnostic and supervisory capabilities.

13.2 CAN Features

- Multi-master architecture
- Bus access priority determined by the message identifier
- 2032 message identifier (2^{11} standard frame CAN 2.0A)
- Guaranteed latency time for high priority messages
- Powerful error handling capability
- Data length from 0 up to 8 bytes
- Multicast and broadcast message facility
- Non destructive bit-wise arbitration
- Non-return-to-zero (NRZ) coding/decoding with bit-stuffing
- Programmable transfer rate (up to 1 Mbit/s)
- Programmable output driver configuration
- Suitable for use in a wide range of networks including the SAE's network classes A, B and C
- DMA providing high-speed on-chip data exchange
- Bus failure management facility
- $\frac{1}{2}AV_{DD}$ reference voltage.

13.3 Interface between CPU and CAN

The internal interface between the P8XC592's CPU and on-chip CAN-controller is achieved via the following four SFRs (see Fig.14):

- CANADR, to point to a register of the CAN-controller
- CANDAT, to read or write data
- CANCON, to read interrupt flags and to write commands
- CANSTA, to read status information and to write DMA pointer.

Additionally, the DMA-logic allows a high-speed data exchange between the CAN-controller and the CPU's on-chip MAIN RAM. For more information, see Section 13.5.15 "Handling of the CPU-CAN interface".

13.4 Hardware blocks of the CAN-controller

The P8XC592 CAN-controller contains all necessary hardware for high performance serial network communications (see Fig.15 and Table 29).

It controls the communication flow through the area network using the CAN-protocol. The CAN-controller meets the following automotive requirements:

- Short message length
- Bus access priority, determined by the message identifier
- Powerful error handling capability
- Configuration flexibility to allow area network expansion
- Guaranteed latency time for urgent messages;
  - The **latency time** defines the period between the initiation (Transmission Request) and the start of the transmission on the bus. The latency time strongly depends on a large variety of bus-related conditions. In the case of a message being transmitted on the bus and one distortion, the latency time can be up to 149 bit times (worst case). For more information see Chapter 23 "CAN application information".

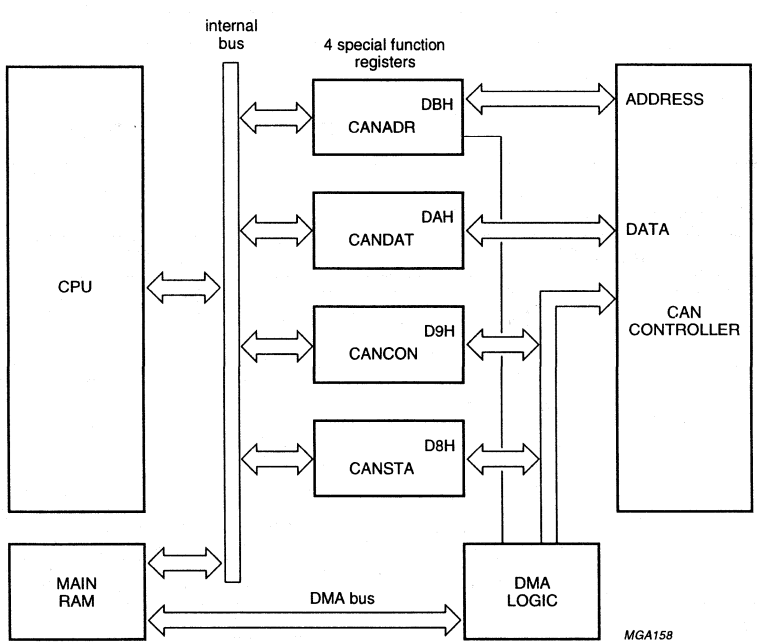


Fig.14 Interface between CPU and CAN-controller.

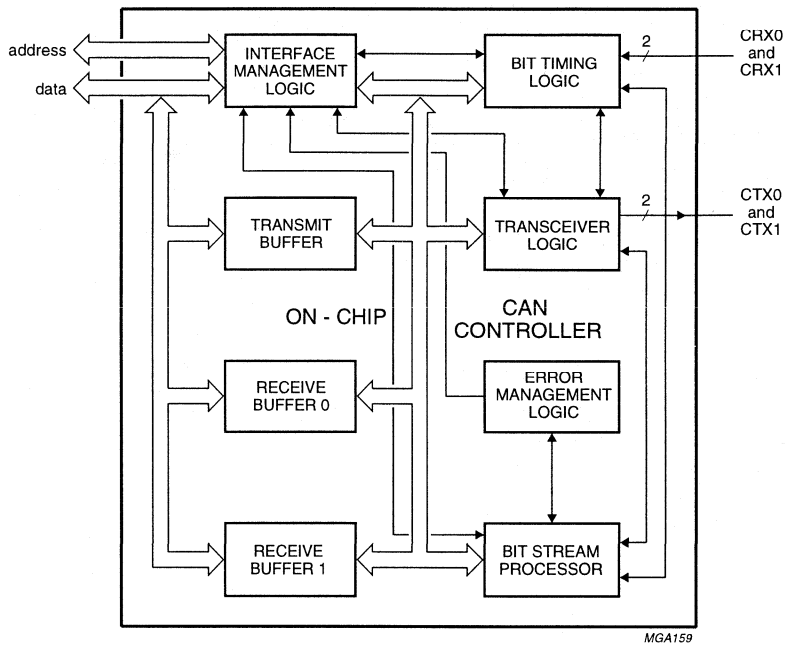


Fig.15 Block diagram of the P8XC592 on-chip CAN-controller.

Table 29 Hardware blocks of the CAN-controller (see Fig.15)

NAME	BLOCK	DESCRIPTION
Interface Management Logic	IML	Interprets commands from the CPU, allocates the message buffers (TBF, RBF0 and RBF1) and provides interrupts and status information to the microcontroller.
Transmit Buffer	TBF	10 bytes memory into which the CPU writes messages which are to be transmitted over the CAN network.
Receive Buffers (0 and 1)	RBF0	RBF0 and RBF1 are each 10 bytes memories which are alternatively used to store messages received from the CAN network. The CPU can process one message while another is being received.
	RBF1	
Bit Stream Processor	BSP	Is a sequencer, controlling the data stream between the Transmit Buffer, Receive Buffers (parallel data) and the CAN-bus (serial data).
Bit Timing Logic	BTL	Synchronizes the CAN-controller to the bitstream on the CAN-bus.
Transceiver Control Logic	TCL	Controls the output driver.
Error Management Logic	EML	Performs the error confinement according to the CAN-protocol.

13.5 Control Segment and Message Buffer description

The CAN-controller appears to the CPU as a memory-mapped peripheral, guaranteeing the independent operation of both parts.

13.5.1 Address allocation

The address area of the CAN-controller consists of the Control Segment and the message buffers. The Control Segment is programmed during an initialization down-load in order to configure communication parameters (e.g. bit timing). The communication over the CAN-bus is also controlled via this segment by the CPU. A message which is to be transmitted, must be written to the Transmit Buffer. After a successful reception the CPU may read the message from the Receive Buffer and then release it for further use.

13.5.2 Control Segment layout

The exchange of status, control and command signals between the CPU and the CAN-controller is performed in the control segment. The layout of this segment is shown in Fig.16. After an initial down-load, the contents of the registers Acceptance Code, Acceptance Mask, Bus Timing 0, Bus Timing 1 and Output Control should not be changed. These registers may only be accessed when the Reset Request bit in the Control Register is set HIGH (see Tables 30, 31 and 32).

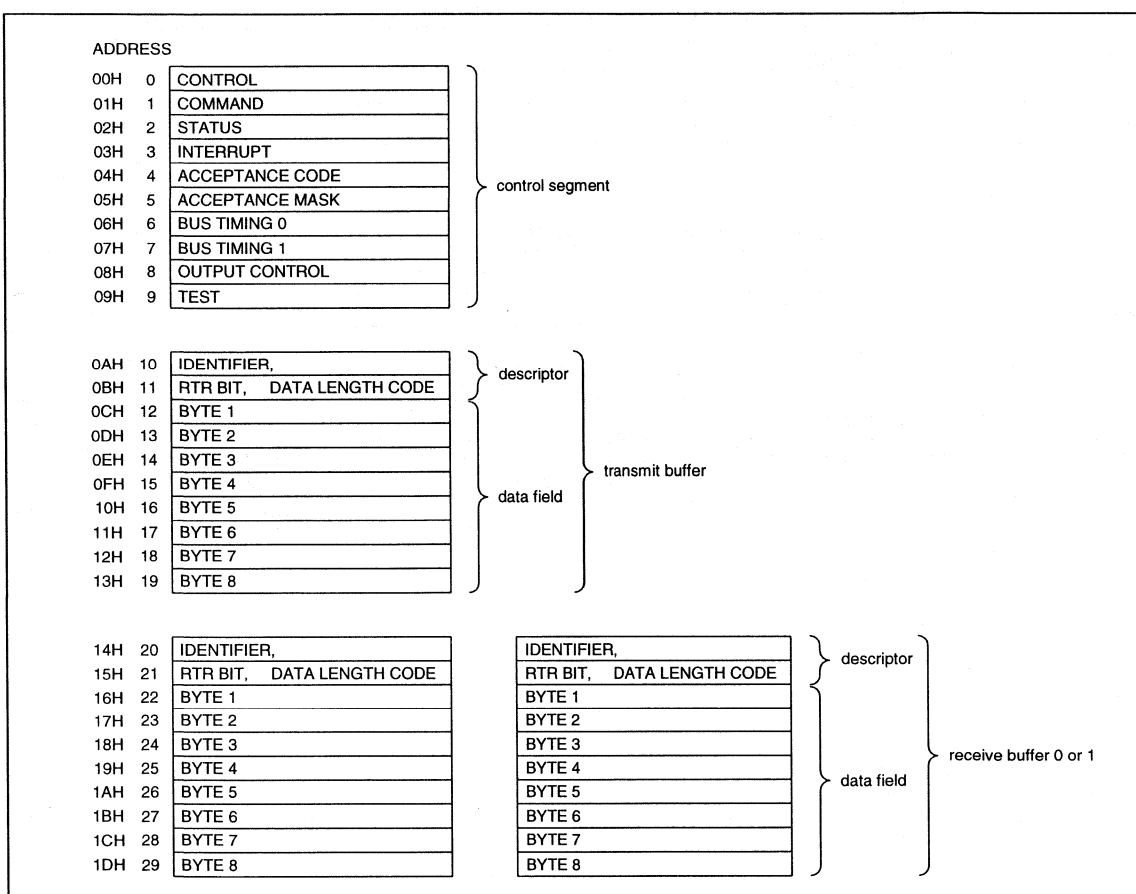


Fig.16 CAN-controller internal address allocation.

Table 30 CPU/CAN Register map

BIT							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Control Segment							
ADDRESS 0: CONTROL REGISTER							
TM	S	RA	OIE	EIE	TIE	RIE	RR
ADDRESS 1: COMMAND REGISTER							
RX0A	RX1A	WUM	SLP	COS	RRB	AT	TR
ADDRESS 2: STATUS REGISTER							
BS	ES	TS	RS	TCS	TBS	DO	RBS
ADDRESS 3: INTERRUPT REGISTER							
Reserved	Reserved	Reserved	WUI	OI	EI	TI	RI
ADDRESS 4: ACCEPTANCE CODE REGISTER							
AC.7	AC.6	AC.5	AC.4	AC.3	AC.2	AC.1	AC.0
ADDRESS 5: ACCEPTANCE MASK REGISTER							
AM.7	AM.6	AM.5	AM.4	AM.3	AM.2	AM.1	AM.0
ADDRESS 6: BUS TIMING REGISTER 0							
SJW.1	SJW.0	BRP.5	BRP.4	BRP.3	BRP.2	BRP.1	BRP.0
ADDRESS 7: BUS TIMING REGISTER 1							
SAM	TSEG2.2	TSEG2.1	TESG2.0	TSEG1.3	TSEG1.2	TSEG1.1	TSEG1.0
ADDRESS 8: OUTPUT CONTROL REGISTER							
OCTP1	OCTN1	OCPOL1	OCTP0	OCTN0	OCPOL0	OCMODE1	OCMODE0
ADDRESS 9: TEST REGISTER (note 1)							
Reserved	Reserved	Map Internal Register	Connect RX Buffer 0 CPU	Connect TX Buffer CPU	Access Internal Bus	Normal RAM Connect	Float Output Driver

BIT							
7	6	5	4	3	2	1	0
Transmit Buffer							
ADDRESS 10: IDENTIFIER							
ID.10	ID.9	ID.8	ID.7	ID.6	ID.5	ID.4	ID.3
ADDRESS 11: RTR, DATA LENGTH CODE							
ID.2	ID.1	ID.0	RTR	DLC.3	DLC.2	DLC.1	DLC.0
ADDRESS 12 TO 19: BYTES 1 TO 8							
Data	Data	Data	Data	Data	Data	Data	Data
Receive Buffer 0 and 1							
ADDRESS 20: IDENTIFIER							
ID.10	ID.9	ID.8	ID.7	ID.6	ID.5	ID.4	ID.3
ADDRESS 21: RTR, DATA LENGTH CODE							
ID.2	ID.1	ID.0	RTR	DLC.3	DLC.2	DLC.1	DLC.0
ADDRESS 22 TO 29: BYTES 1 TO 8							
Data	Data	Data	Data	Data	Data	Data	Data

Notes

1. The Test Register is used for production testing only.

13.5.3 CONTROL REGISTER (CR)

The contents of the Control Register are used to change the behaviour of the CAN-controller. Control bits may be set or reset by the CPU which uses the Control Register as a read/write memory.

Table 31 Control Register (address 0)

7	6	5	4	3	2	1	0
TM	S	RA	OIE	EIE	TIE	RIE	RR

Table 32 Description of the CR bits

BIT	SYMBOL	FUNCTION
7	TM	**Test Mode** (note 1).If the value of TM is: HIGH (enabled), then the CAN-controller enters Test Mode (normal operations impossible). LOW (disabled), then the CAN-controller is in normal operating mode.
6	S	**Sync** (note 2). If the value of S is: HIGH (2 edges), then bus-line transitions from recessive-to-dominant and vice-versa are used for resynchronization (see Sections 13.5.20 and 13.6). LOW (1 edge), then the only transitions from recessive-to-dominant are used for resynchronization.
5	RA	**Reference Active** (notes 2 and 3). If the value of RA is: HIGH (output), then the pin REF is an $\frac{1}{2}AV_{DD}$ reference output. LOW (input), then a reference voltage may be input.
4	OIE	**Overrun Interrupt Enable**. If the value of OIE is: HIGH (enabled) and the Data Overrun bit is set (see Section 13.5.5) then the CPU receives an Overrun Interrupt signal. LOW (disabled), then the CPU receives no Overrun Interrupt signal from the CAN-controller.
3	EIE	**Error Interrupt Enable**. If the value of EIE is: HIGH (enabled) and the Error or Bus Status change (see Section 13.5.5) then the CPU receives an Error Interrupt signal. LOW (disabled), then the CPU receives no Error Interrupt signal.
2	TIE	**Transmit Interrupt Enable**. If the value of TIE is: HIGH (enabled) and when a message has been successfully transmitted or the Transmit Buffer is accessible again, (e.g. after an Abort Transmission command), then the CAN-controller transmits a Transmit Interrupt signal to the CPU. LOW (disabled), then there is no transmission of the Transmit Interrupt signal by the CAN-controller to the CPU.
1	RIE	**Receive Interrupt Enable**. If the value of RIE is: HIGH (enabled) and when a message has been received without errors, then the CAN-controller transmits a Receive Interrupt signal to the CPU. LOW (disabled), then there is no transmission of the Receive Interrupt signal by the CAN-controller to the CPU.
0	RR	**Reset Request** (note 4). If the value of RR is: HIGH (present), then detection of a Reset Request results in the CAN-controller aborting the current transmission/reception of a message entering the reset state. LOW (absent), on the HIGH-to-LOW transition of the Reset Request bit, the CAN-controller returns to its normal operating state.

Notes to the description of the CR bits

1. The test mode is intended for factory testing and not for customer use.
2. A modification of the bits Reference Active and Sync is only possible with Reset Request = HIGH (present). It is allowed to set these bits while Reset Request is changed from a HIGH level to a LOW level. After an external reset (pin RST = HIGH) the Reference Active bit is set HIGH (output), the Sync bit is undefined.
3. For the P87C592 'CR' anomaly description, see Chapter 25 "P87C592 specification differences".
4. During an external reset (RST = HIGH) or when the Bus Status bit is set HIGH (Bus-OFF), the IML forces the Reset Request HIGH (present). After the Reset Request bit is set LOW (absent) the CAN-controller will wait for:
   a) One occurrence of the Bus-Free signal (11 recessive bits, see Section 13.6.9.6), if the preceding reset (Reset Request = HIGH) has been caused by an external reset or a CPU initiated reset.
   b) 128 occurrences of Bus-Free, if the preceding reset (Reset Request = HIGH) has been caused by a CAN-controller initiated Bus-OFF, before re-entering the Bus-On mode, see Section 13.6.9.
   c) When Reset Request is set HIGH (present), for whatever reason, the Control, Command, Status and Interrupt bits are affected, see Table 40. The registers at addresses 4 to 8 are only accessible when the Reset Request is set HIGH (present).

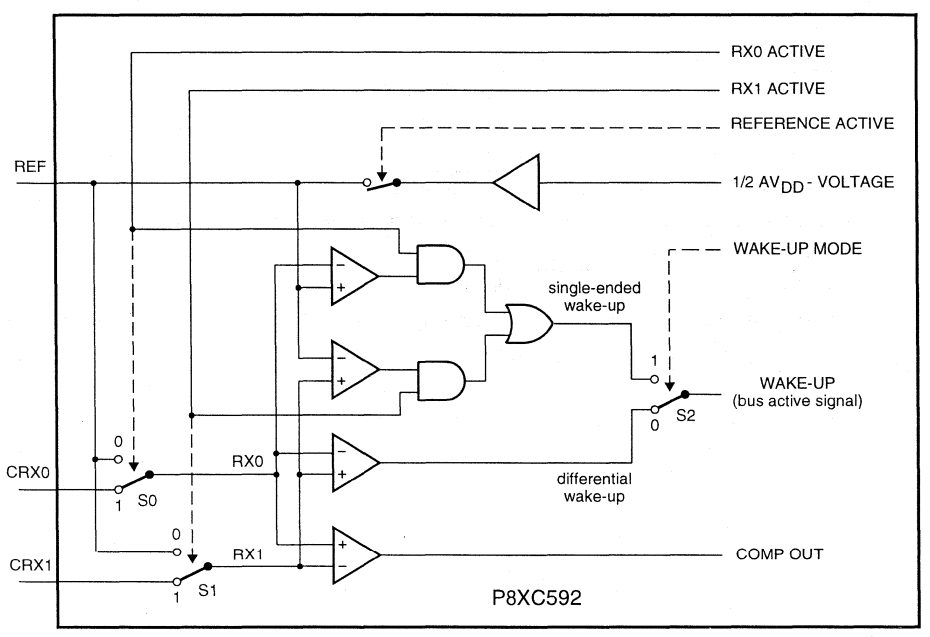


Fig.17 Configurable CAN receiver.

13.5.4 COMMAND REGISTER (CMR)

A command bit initiates an action within the transfer layer of the CAN-controller. The Command Register appears to the CPU as a read/write memory, except for the bits CMR.0 (TR) to CMR.3 (COS), which return a HIGH if being read.

Table 33 Command Register (address 1)

7	6	5	4	3	2	1	0
RX0A	RX1A	WUM	SLP	COS	RRB	AT	TR

Table 34 Description of the CMR bits

BIT	SYMBOL	FUNCTION
7	RX0A	**RX0 Active**. See Table 35; note 1.
6	RX1A	**RX1 Active**. See Table 35; note 1.
5	WUM	**Wake-up Mode** (note 2). If the value of WUM is: HIGH (single ended), then the difference of the RX signals to the internal reference voltage $\frac{1}{2}AV_{DD}$ is used for wake up. LOW (differential), then the differential signal between RX0 and RX1 is used for wake up.
4	SLP	**Sleep** (note 3). If the value of SLP is: HIGH (sleep), then the CAN-controller enters sleep mode if no CAN interrupt is pending and there is no bus activity. LOW (wake up), then the CAN-controller functions normally.
3	COS	**Clear Overrun Status** (note 4). If the value of COS is: HIGH (clear), then the Data Overrun status bit is set to LOW (see Table 37). LOW (no action), then there is no action.
2	RRB	**Release Receive Buffer** (note 5). If the value of RRB is: HIGH (released), then the Receive Buffer attached to the CPU is released. LOW (no action), then there is no action.
1	AT	**Abort Transmission** (note 6). If the value of AT is: HIGH (present) and if not already in progress, a pending Transmission Request is cancelled. LOW (absent), then there is no action.
0	TR	**Transmission Request** (note 7). If the value of TR is: HIGH (present), then a message shall be transmitted. LOW (absent), then there is no action.

Notes to the description of the CMR bits

1. The RX0/RX1 Active bits, if being read, reflect the status of the respective switches (see Fig.17). It is recommended to change the switches only during the reset state (Reset Request = HIGH).
2. The Wake-Up Mode bit should be set at the same time as the Sleep bit. The differential wake up mode is useful if both bus wires are fully functioning; it minimizes the amount of wake ups due to noise. The single ended wake up mode is recommended if a wake up must be possible even if one bus wire is already or may become disturbed (see Fig.17).
3. The CAN-controller will enter sleep mode, if the Sleep bit is set HIGH (sleep) there is no bus activity and no interrupt is pending. The CAN-controller will wake up after the Sleep bit is set LOW (wake up) or when there is bus activity. On wake up, a Wake-Up Interrupt (see Section 13.5.6) is generated (see also Chapter 15). A CAN-controller which is sleeping and then awaken by bus activity will not be able to receive this message until it detects a Bus-Free signal (see Section 13.6.9.6). The Sleep bit, if read, reflects the status of the CAN-controller.
4. This command bit is used to acknowledge the Data Overrun condition signalled by the Data Overrun status bit. It may be given or set at the same time as a Release Receive Buffer command bit.
5. After reading the contents of the Receive Buffer (RBF0 or RBF1) the CPU must release this buffer by setting Release Receive Buffer bit HIGH (released). This may result in another message becoming immediately available.
6. The Abort Transmission bit is used when the CPU requires the suspension of the previously requested transmission, e.g. to transmit an urgent message. A transmission already in progress is not stopped. In order to see if the original message had been either transmitted successfully or aborted, the Transmission Complete Status bit should be checked. This should be done after the Transmit Buffer Access bit has been set HIGH (released) or a Transmit Interrupt has been generated (see Section 13.5.6).
7. If the Transmission Request bit was set HIGH in a previous command, it cannot be cancelled by setting the Transmission Request bit LOW (absent). Cancellation of the requested transmission may be performed by setting the Abort Transmission bit HIGH (present).

Table 35 Combination of bits RX0A and RX1A (see Fig.17)

CONTROL		RX0	RX1
RX0A	RX1A		
1	1	CRX0	CRX1
1	0	CRX0	$\frac{1}{2}AV_{DD}$
0	1	$\frac{1}{2}AV_{DD}$	CRX1
0	0	No action	

13.5.5 STATUS REGISTER (SR)

The contents of the Status Register reflects the status of the CAN-controller. The Status Register appears to the CPU as a read only memory.

Table 36 Status Register (address 2)

7	6	5	4	3	2	1	0
BS	ES	TS	RS	TCS	TBS	DO	RBS

Table 37 Description of the SR bits

BIT	SYMBOL	FUNCTION
7	BS	**Bus Status** (note 1). If the value of BS is: HIGH (Bus-OFF), then the CAN-controller is not involved in bus activities. LOW (Bus-ON), then the CAN-controller is involved in bus activities.
6	ES	**Error Status**. If the value of ES is: HIGH (error), then at least one of the Error Counters (see Section 13.6.10) has reached the CPU Warning limit. LOW (ok), then both Error Counters have not reached the warning limit.
5	TS	**Transmit Status** (note 2). If the value of TS is: HIGH (transmit), then the CAN-controller is transmitting a message. LOW (idle), then no message is transmitted.
4	RS	**Receive Status** (note 2). If the value of RS is: HIGH (receive), then the CAN-controller is receiving a message. LOW (idle), then no message is received.
3	TCS	**Transmission Complete Status** (note 3). If the value of TCS is: HIGH (complete), then last requested transmission has been successfully completed. LOW (incomplete), then previously requested transmission is not yet completed.
2	TBS	**Transmit Buffer Access** (note 3). If the value of TBS is: HIGH (released), then the CPU may write a message into the TBF. LOW (locked), then the CPU cannot access the Transmit Buffer. A message is either waiting for transmission or is in the process of being transmitted.
1	DO	**Data Overrun** (note 4). If the value of DO is: HIGH (overrun), then this bit is set HIGH (Overrun), when both Receive Buffers are full and the first byte of another message should be stored. LOW (absent), then no data overrun has occurred since the Clear Overrun command was given.
0	RBS	**Receive Buffer Status** (note 5). If the value of RBS is HIGH (full), then this bit is set when a new message is available. LOW (empty), then no message has become available since the last Release Receive Buffer command bit was set.

Notes to the description of the SR bits

1. When the Bus Status bit is set HIGH (Bus-OFF), the CAN-controller will set the Reset Request bit HIGH (present). It will stay in this state until the CPU sets the Reset Request bit LOW (absent). Once this is completed the CAN-controller will wait the minimum protocol-defined time (128 occurrences of the Bus-Free signal) before setting the Bus Status bit LOW (Bus-ON), the Error Status bit LOW (ok) and resetting the Error Counters. During Bus-OFF the output drivers are switched off (floating); external transceiver circuits should output a recessive level in this case.
2. If both the Receive Status and Transmit Status bits are LOW (idle) the CAN-bus is idle.
3. If the CPU tries to write to the Transmit Buffer when the Transmit Buffer Access bit is LOW (locked), the written bytes will not be accepted and will be lost without this being signalled. The Transmission Complete Status bit is set LOW (incomplete) whenever the Transmission Request bit is set HIGH (present). If an Abort Transmission command is issued, the Transmit Buffer will be released. If the message, which was requested and then aborted, was not transmitted, the Transmission Complete Status bit will remain LOW.
4. If Data Overrun = HIGH (overrun) is detected, the currently received message is dropped. A transmitted message, granted acceptance, is also stored in a Receive Buffer. This occurs because it is not known if the CAN-controller will lose arbitration and so become a receiver of the message. If no Receive Buffer is available, Data Overrun is signalled. However, this transmitted and accepted message does neither cause a Receive Interrupt nor set the Receive Buffer Status bit to HIGH (full). Also, a Data Overrun does not cause the transmission of an Overload Frame (see Sections 13.6.1 and 13.6.5).
5. If the command bit Release Receive Buffer is set HIGH (released) by the CPU, the Receive Buffer Status bit is set LOW (empty) by IML. When a new message is stored in any of the receive buffers, the Receive Buffer Status bit is set HIGH (full) again.

13.5.6 INTERRUPT REGISTER (IR)

The Interrupt Register allows the identification of an interrupt source. When one or more bits of this register are set, a CAN interrupt (SI01) will be indicated to the CPU. All bits are reset by the CAN-controller after this register is read by the CPU. This register appears to the CPU as a read only memory.

Table 38 Interrupt Register (address 3)

7	6	5	4	3	2	1	0
–	–	–	WUI	OI	EI	TI	RI

Table 39 Description of the IR bits

BIT	SYMBOL	FUNCTION
7	–	Reserved.
6	–	Reserved.
5	–	Reserved.
4	WUI	**Wake-Up Interrupt**. The value of WUI is set to: HIGH (set), when the sleep mode is left. See Section 13.5.4. LOW (reset), by a read access of the Interrupt Register by the CPU.
3	OI	**Overrun Interrupt** (note 1). The value of OI is set to: HIGH (set), if both Receive Buffers contain a message and the first byte of another message should be stored (passed acceptance), and the Overrun Interrupt Enable is HIGH (enabled). LOW (reset), by a read access of the Interrupt Register by the CPU.
2	EI	**Error Interrupt**. The value of EI is set to: HIGH (set), on a change of either the Error Status or Bus Status bits, if the Error Interrupt Enable is HIGH (enabled). See Section 13.5.5. LOW (reset), by a read access of the Interrupt Register by the CPU.
1	TI	**Transmit Interrupt**. The value of TI is set to: HIGH (set), on a change of the Transmit Buffer Access from LOW to HIGH (released) and Transmit Interrupt Enable is HIGH (enabled). LOW (reset), after a read access of the Interrupt Register by the CPU.
0	RI	**Receive Interrupt** (note 2). The value of RBS is set to: HIGH (set), when a new message is available in the Receive Buffer and the Receive Interrupt Enable bit is HIGH (enabled). LOW (reset) automatically by a read access of Interrupt Register by the CPU.

Notes

1. Overrun Interrupt bit (if enabled) and Data Overrun bit (see Section 13.5.5) are set at the same time.
2. Receive Interrupt bit (if enabled) and Receive Buffer Status bit (see Section 13.5.5) are set at the same time.

Table 40 Effects of setting the Reset Request bit HIGH (present)

TYPE	BIT	SYMBOL	FUNCTION	EFFECT
Control	CR.7	TM	Test Mode	LOW (disabled)
	CR.5	RA	Reference Active	HIGH (output); note 1
Command	CMR.7	RX0A	RX0 Active	HIGH (RX0 = CRX0); note 1
	CMR.6	RX1A	RX1 Active	HIGH (RX1 = CRX1); note 1
	CMR.4	SLP	Sleep	LOW (wake-up)
	CMR.3	COS	Clear Overrun Status	HIGH (clear)
	CMR.2	RRB	Release Receive Buffer	HIGH (released)
	CMR.1	AT	Abort Transmission	LOW (absent)
	CMR.0	TR	Transmission Request	LOW (absent)
Status	SR.7	BS	Bus Status	LOW (Bus-On); note 1
	SR.6	ES	Error Status	LOW (no error); note 1
	SR.5	TS	Transmit Status	LOW (idle)
	SR.4	RS	Receive Status	LOW (idle)
	SR.3	TCS	Transmission Complete Status	HIGH (complete)
	SR.2	TBS	Transmit Buffer Access	HIGH (released)
	SR.1	DO	Data Overrun	LOW (absent)
	SR.0	RBS	Receive Buffer Status	LOW (empty)
Interrupt	IR.3	OI	Overrun Interrupt	LOW (reset)
	IR.1	TI	Transmit Interrupt	LOW (reset)
	IR.0	RI	Receive Interrupt	LOW (reset)

Note

1. Only after an external reset; see note 5 to Table 37 "Description of the SR bits".

13.5.7 Acceptance Code Register (ACR)

The Acceptance Code Register is part of the acceptance filter of the CAN-controller. This register can be accessed (read/write), if the Reset Request bit is set HIGH (present).

When a message is received which passes the acceptance test and if there is an empty Receive Buffer, then the respective Descriptor and Data Field (see Fig.16) are sequentially stored in this empty buffer.

In the event that there is no empty Receive Buffer, the Data Overrun bit is set HIGH (overrun); see Sections 13.5.5 and 13.5.6.

When the complete message has been correctly received the following occurs:

- The Receive Buffer Status bit is set HIGH (full)
- If the Receive Interrupt Enable bit is set HIGH (enabled), the Receive Interrupt is set HIGH (set).

During transmission of a message which passes the acceptance test, the message is also written to its own Receive Buffer. If no Receiver Buffer is available, Data Overrun is signalled because it is not known at the start of a message whether the CAN-controller will lose arbitration and so become a receiver of the message.

Table 41 Acceptance Code Register (address 4)

7	6	5	4	3	2	1	0
AC.7	AC.6	AC.5	AC.4	AC.3	AC.2	AC.1	AC.0

Table 42 Description of the ACR bits

BIT	SYMBOL	FUNCTION
7 to 0	AC.7 to AC.0	**Acceptance Code.** The Acceptance Code bits (AC.7 to AC.0) and the eight most significant bits of the message's Identifier (ID.10 to ID.3) must be equal to those bit positions which are marked relevant by the Acceptance Mask bits (AM.7 to AM.0). The acceptance is given, if the following equation is satisfied: (ID10 ... ID.3) = [(AC.7 ... AC.0) or (AM.7 ... AM.0)] = 1111 1111 B.

13.5.8 Acceptance Mask Register (AMR)

The Acceptance Mask Register is part of the acceptance filter of the CAN-controller.
This register can be accessed (read/write) if the Reset Request bit is set HIGH (present).

The Acceptance Mask Register qualifies which of the corresponding bits of the acceptance code are 'relevant' or 'don't care' for acceptance filtering.

Table 43 Acceptance Mask Register (address 5)

7	6	5	4	3	2	1	0
AM.7	AM.6	AM.5	AM.4	AM.3	AM.2	AM.1	AM.0

Table 44 Description of the AMR bits

BIT	SYMBOL	FUNCTION
7 to 0	AM.7 to AM.0	**Acceptance Mask.** If the Acceptance Mask bit is: HIGH (don't care), then this bit position is 'don't care' for the acceptance of a message. LOW (relevant), then this bit position is 'relevant' for acceptance filtering.

13.5.9 Bus Timing Register 0 (BTR0)

The contents of Bus Timing Register 0 defines the values of the Baud Rate Prescaler (BRP) and the Synchronization Jump Width (SJW).

This register can be accessed (read/write) if the Reset Request bit is set HIGH (present).
For further information on bus timing, see Sections 13.5.10 and 13.5.18.

Table 45 Bus Timing Register 0 (address 6)

7	6	5	4	3	2	1	0
SJW.1	SJW.0	BRP.5	BRP.4	BRP.3	BRP.2	BRP.1	BRP.0

Table 46 Description of the BTR0 bits

BIT	SYMBOL	FUNCTION
7	SJW.1	**Synchronization Jump Width.** To compensate for phase shifts between clock oscillators of different bus controllers, any bus controller must resynchronize on any relevant signal edge of the current transmission. The synchronization jump width defines the maximum number of clock cycles a bit period may be shortened or lengthened by one resynchronization: $t_{SJW} = t_{SCL}(2SJW.1 + SJW.0 + 1)$.
6	SJW.0	
5	BRP.5	**Baud Rate Prescaler.** The period of the system clock t_{SCL} is programmable and determines the individual bit timing.The system clock is calculated using the following equation: $t_{SCL} = 2t_{CLK}(32BRP.5 + 16BRP.4 + 8BRP.3 + 4BRP.2 + 2BRP.1 + BRP.0 + 1)$. Where t_{CLK} = time period of the P8XC592 oscillator.
4	BRP.4	
3	BRP.3	
2	BRP.2	
1	BRP.1	
0	BRP.0	

13.5.10 Bus Timing Register 1(BTR1)

The contents of Bus Timing Register 1 defines the length of the bit period, the location of the sample point and the number of samples to be taken at each sample point.

This register can be accessed (read/write) if the Reset Request bit is set HIGH (present).For further information on bus timing, see Sections 13.5.9 and 13.5.18.

Table 47 Bus Timing Register 1 (address 7)

7	6	5	4	3	2	1	0
SAM	TSEG2.2	TSEG2.1	TSEG2.0	TSEG1.3	TSEG1.2	TSEG1.1	TSEG1.0

Table 48 Description of the BTR1 bits

BIT	SYMBOL	FUNCTION
7	SAM	**Sampling**. If the bit SAM is: HIGH (3 samples), then three samples are taken. This is recommended for slow/medium speed buses (SAE class A and B) where filtering of spikes on the bus-line is beneficial (see Section 13.5.19.6) LOW (1 sample), the bus is sampled once. This is recommended for high speed buses (SAE class C).
6	TSEG2.2	**Time Segment 1 (TSEG1) and Time Segment 2 (TSEG2).** TSEG1 determines the number of clock cycles per bit period and the location of the sample point $t_{TSEG1} = t_{SCL}(8TSEG1.3 + 4TSEG1.2 + 2TSEG1.1 + TSEG1.0 + 1)$. TSEG2 determines the number of clock cycles per bit period and the location of the sample point: $t_{TSEG2} = t_{SCL}(4TSEG2.2 + 2TSEG2.1 + TSEG2.0 + 1)$.
5	TSEG2.1	
4	TSEG2.0	
3	TSEG1.3	
2	TSEG1.2	
1	TSEG1.1	
0	TSEG1.0	

13.5.11 Output Control Register (OCR)

The Output Control Register allows, under software control, the set-up of different output driver configurations. This register can be accessed (read/write) if the Reset Request bit is set HIGH (present). If the CAN-controller is in the sleep mode (Sleep = HIGH) a recessive level is output on the CTX0 and CTX1 pins. If the CAN-controller is in the reset state (Reset Request = HIGH) the output drivers are floating.

Tables 50 and 51, show the relationship between the bits of the Output Control Register and the two serial output pins CTX0 and CTX1 of the P8XC592 CAN-controller, connected to the serial bus (see Fig.15).

Table 49 Output Control Register (address 8)

7	6	5	4	3	2	1	0
OCTP1	OCTN1	OCPOL1	OCTP0	OCTN0	OCPOL0	OCMODE1	OCMODE0

Table 50 Description of the OCR bits

BIT	SYMBOL	FUNCTION
7	OCTP1	See Tables 51 and 52.
6	OCTN1	
5	OCPOL1	
4	OCTP0	
3	OCTN0	
2	OCPOL0	
1	OCMODE1	**Output Mode.**
0	OCMODE0	These bits select the output mode; see Table 51.

Table 51 Description of the Output Mode bits

OCMODE1	OCMODE0	DESCRIPTION
1	0	**Normal Output Mode**. The bit sequence (TXD) is sent via CTX0, CTX1. TXD is the data bit to be transmitted. The voltage levels on the output driver pins CTX0 and CTX1 depend on both the driver characteristic programmed by OCTPx, OCTNx (float, pull-up, pull-down, push-pull) and the output polarity programmed by OCPOLx (see Fig.18).
1	1	**Clock Output Mode**. For the CTX0 pin this is the same as in Normal Output Mode (CTX0: bit sequence). However, the data stream to CTX1 is replaced by the transmit clock (TXCLK). The rising edge of the transmit clock (non-inverted) marks the beginning of a bit period. The clock pulse width is t_{SCL}.
0	0	**Bi-phase Output Mode**. In contrast to Normal Output Mode the bit representation is time variant and toggled. If the bus controllers are galvanically decoupled from the bus-line by a transformer, the bit stream is not allowed to contain a DC component. This is achieved by the following scheme. During recessive bits all outputs are deactivated (floating). Dominant bits are sent alternately on CTX0 and CTX1, i.e. the first dominant bit is sent on CTX0, the second is sent on CTX1, and the third one is sent on CTX0 again, etc.
0	1	**Test Output Mode.** For the CTX0 pin this is the same as in Normal Output Mode (CTX0: bit sequence). To measure the delay time of the transmitter and receiver this mode connects the output of the input comparator (COMP OUT) with the input of the output driver CTX1. This mode is used for production testing only.

Table 52 Output pin set-up

DRIVE	OCTPx	OCTNx	OCPOLx	TXD	TPx[1]	TNx[2]	CTXx[3]
Float	0	0	0	0	OFF	OFF	float
	0	0	0	1	OFF	OFF	float
	0	0	1	0	OFF	OFF	float
	0	0	1	1	OFF	OFF	float
Pull-down	0	1	0	0	OFF	ON	LOW
	0	1	0	1	OFF	OFF	float
	0	1	1	0	OFF	OFF	float
	0	1	1	1	OFF	ON	LOW
Pull-up	1	0	0	0	OFF	OFF	float
	1	0	0	1	ON	OFF	HIGH
	1	0	1	0	ON	OFF	HIGH
	1	0	1	1	OFF	OFF	float
Push/Pull	1	1	0	0	OFF	ON	LOW
	1	1	0	1	ON	OFF	HIGH
	1	1	1	0	ON	OFF	HIGH
	1	1	1	1	OFF	ON	LOW

Notes

1. TPx is the on-chip output transistor x, connected to V_{DD}; x = 0 or 1.
2. TNx is the on-chip output transistor x, connected to CV_{SS}; x = 0 or 1.
3. CTXx is the serial output level on CTX0 or CTX1. It is required that the output level on the CAN-bus is dominant with TXD = 0 and recessive with TXD = 1, see Section 13.6.1.1 "Bit representation".

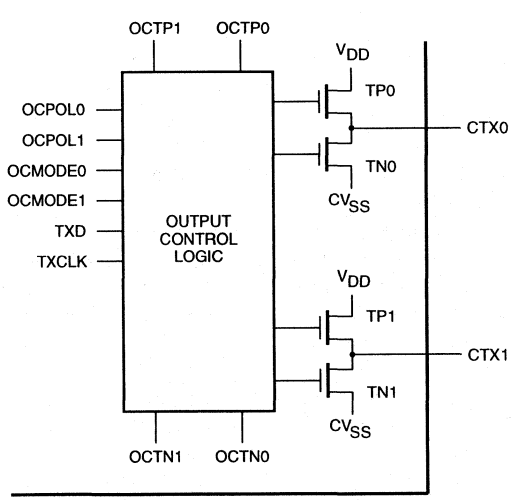


Fig.18 Configurable CAN Transmitter.

13.5.12 TEST REGISTER (TR)

The Test Register is used for production testing only.

Table 53 Test Register (address 9)

7	6	5	4	3	2	1	0
Reserved	Reserved	Map Internal Register	Connect RX Buffer 0 CPU	Connect TX Buffer CPU	Access Internal Bus	Normal RAM Connect	Float Output Driver

13.5.13 TRANSMIT BUFFER LAYOUT

The global layout of the Transmit Buffer is shown in Fig.16. This buffer serves to store a message from the CPU to be transmitted by the CAN-controller. It is subdivided into Descriptor and Data Field. The Transmit Buffer can be written to and read from by the CPU.

13.5.13.1 Descriptor

Table 54 Descriptor Byte 1 Register (DSCR1, address 10)

7	6	5	4	3	2	1	0
ID.10	ID.9	ID.8	ID.7	ID.6	ID.5	ID.4	ID.3

Table 55 Descriptor Byte 2 Register (DSCR2, address 11)

7	6	5	4	3	2	1	0
ID.2	ID.1	ID.0	RTR	DLC.3	DLC.2	DLC.1	DLC.0

Table 56 Description of the ID.n bits in DSCR1 and DSCR2

BIT	SYMBOL	FUNCTION
DSCR1		
7	ID.10	**Identifier.** The Identifier consists of 11 bits (ID.10 to ID.0). ID.10 is the most significant bit, which is transmitted first on the bus during the arbitration process. The Identifier acts as the messages' name, used in a receiver for acceptance filtering, and also determines the bus access priority during the arbitration process. The lower the binary value of the Identifier the higher the priority. This is due to the larger number of leading dominant bits during arbitration (see Section 13.6.7).
6	ID.9	
5	ID.8	
4	ID.7	
3	ID.6	
2	ID.5	
1	ID.4	
0	ID.3	
DSCR2		
7	ID.2	**Identifier**. See DSCR1.
6	ID.1	
5	ID.0	

Table 57 Description of the other DSCR2 bits

BIT	SYMBOL	FUNCTION
4	RTR	**Remote Transmission Request.** If the RTR bit is: HIGH (remote), then the Remote Frame will be transmitted by the CAN-controller. LOW (data), then the Data Frame will be transmitted by the CAN-controller.
3	DLC.3	**Data Length Code (DLC).** The number of bytes (Data Byte Count) in the Data Field of a message is coded by the Data Length Code. At the start of a Remote Frame transmission the Data Length Code is not considered due to the RTR bit being HIGH (remote). This forces the number of transmitted/received data bytes to be a logic 0. Nevertheless, the Data Length Code must be specified correctly to avoid bus errors, if two CAN-controllers start a Remote Frame transmission simultaneously. The range of the Data Byte Count is 0 to 8 bytes and coded as follows: Data Byte Count = 8DLC.3 + 4DLC.2 + 2DLC.1 + DLC.0. For reasons of compatibility no Data Byte Counts other than 0,1,2,....8 should be used.
2	DLC.2	
1	DLC.1	
0	DLC.0	

13.5.13.2 Data Field

The number of transferred data bytes is determined by the Data Length Code. The first bit transmitted is the most significant bit of data byte 1 at address 12.

13.5.14 RECEIVE BUFFER LAYOUT

The layout of the Receive Buffer and the individual bytes correspond to the definitions given for the Transmit Buffer layout, except that the addresses start at 20 instead of 10 (see Fig.16).

13.5.15 HANDLING OF THE CPU-CAN INTERFACE

Via the four special registers CANADR, CANDAT, CANCON and CANSTA the CPU has access to the CAN-controller and also to the DMA-logic. Note that CANCON and CANSTA have different meanings for a Read and Write access.

Table 58 The SFRs between CPU and CAN

Reserved bits are read as HIGH. R = Read; W = Write; R/W = Read/Write.

ADDRESS	ACCESS	BIT							
		7	6	5	4	3	2	1	0
CANADR									
DBH	R/W	DMA	Reserved	AutoInc	CANA4	CANA3	CANA2	CANA1	CANA0
CANDAT									
DAH	R/W	CAND7	CAND6	CAND5	CAND4	CAND3	CAND2	CAND1	CAND0
CANCON; Do not use a RMW instruction									
D9H	R	Reserved	Reserved	Reserved	WUI	OI	EI	TI	RI
	W	RX0A	RX1A	WUM	SLP	COS	RRB	AT	TR
CANSTA; The bit addresses of CANSTA (7 to 0) are DFH to D8H; do not use a RMW instruction									
DFH to D8H	R	BS	ES	TS	RS	TCS	TBS	DO	RBS
	W	RAMA7	RAMA6	RAMA5	RAMA4	RAMA3	RAMA2	RAMA1	RAMA0

13.5.15.1 Special Function Register CANADR

CANADR is implemented as a read/write register.

Table 59 SFR CANADR (address DBH)

7	6	5	4	3	2	1	0
DMA	–	AutoInc	CANA4	CANA3	CANA2	CANA1	CANA0

Table 60 Description of the CANADR bits

BIT	SYMBOL	FUNCTION
7	DMA	DMA-logic controlled via bit CANADR.7 (see Section 13.5.17).
6	–	Reserved.
5	AutoInc	Auto Address Increment mode controlled via bit CANADR.5 (see Section 13.5.16).
4	CANA4	The five least significant bits CANADR.4 to CANADR.0 define the address of one of the CAN-controller internal registers to be accessed via CANDAT. For instance, after an external hardware (e.g. power-on) reset CANADR contains the value 64H, and hence the CPU accesses (read/write) the Acceptance Code register of the CAN-controller, via the SFR CANDAT.
3	CANA3	
2	CANA2	
1	CANA1	
0	CANA0	

13.5.15.2 Special Function Register CANDAT

CANDAT is implemented as a read/write register.

Table 61 SFR CANDAT (address DAH)

7	6	5	4	3	2	1	0
CAND7	CAND6	CAND5	CAND4	CAND3	CAND2	CAND1	CAND0

Table 62 Description of the CANADR bits

BIT	SYMBOL	FUNCTION
7 to 0	CAND7 to CAND0	The SFR CANDAT appears as a port to the CAN-controller internal register (memory location) being selected by CANADR. Reading or writing CANDAT is effectively an access to that CAN-controller internal register, which is selected by CANADR.

13.5.15.3 Special Function Register CANCON

Table 63 SFR CANCON in **Read** access (address D9H)

7	6	5	4	3	2	1	0
–	–	–	WUI	OI	EI	TI	RI

Table 64 Description of the CANCON bits in **Read** access

When reading CANCON the Interrupt Register of the CAN-controller is accessed.

BIT	SYMBOL	FUNCTION
7	–	Reserved; bits are read as HIGH.
6	–	
5	–	
4	WUI	Wake-Up Interrupt (see Table 39).
3	OI	Overrun Interrupt (see Table 39).
2	EI	Error Interrupt (see Table 39).
1	TI	Transmit Interrupt (see Table 39).
0	RI	Receive Interrupt (see Table 39).

Table 65 SFR CANCON in **Write** access (address D9H)

7	6	5	4	3	2	1	0
RX0A	RX1A	WUM	SLP	COS	RRB	AT	TR

Table 66 Description of the CANCON bits in **Write** access

When writing to CANCON then the Command Register of the CAN-controller is accessed.

BIT	SYMBOL	FUNCTION
7	RX0A	RX0 Active (see Table 34).
6	RX1A	RX1 Active (see Table 34).
5	WUM	Wake-Up Mode (see Table 34).
4	SLP	Sleep (see Table 34).
3	COS	Clear Overrun Status (see Table 34).
2	RRB	Release Receive Buffer (see Table 34).
1	AT	Abort Transmission (see Table 34).
0	TR	Transmission Request (see Table 34).

13.5.15.4 Special Function Register CANSTA

CANSTA is implemented as a bit-addressable read/write register.
The bit addresses of CANSTA (7 to 0) are DFH to D8H.

Table 67 SFR CANCON in **Read** access (address DFH to D8H)

7	6	5	4	3	2	1	0
BS	ES	TS	RS	TCS	TBS	DO	RBS

Table 68 Description of the CANCON bits in **Read** access
When reading CANSTA the Status Register of the CAN-controller is accessed.

BIT	SYMBOL	FUNCTION
7	BS	Bus Status (see Table 37).
6	ES	Error Status (see Table 37).
5	TS	Transmit Status (see Table 37).
4	RS	Receive Status (see Table 37).
3	TCS	Transmission Complete Status (see Table 37).
2	TBS	Transmit Buffer Access (see Table 37).
1	DO	Data Overrun (see Table 37).
0	RBS	Receive Buffer Status (see Table 37).

Table 69 SFR CANCON in **Write** access (address DFH to D8H)

7	6	5	4	3	2	1	0
RAMA7	RAMA6	RAMA5	RAMA4	RAMA3	RAMA2	RAMA1	RAMA0

Table 70 Description of the CANSTA bits in **Write** access
Writing to CANSTA sets the address of the on-chip MAIN RAM (internal Data Memory) for a subsequent DMA transfer.

BIT	SYMBOL	FUNCTION
7 to 0	RAMA7 to RAMA0	–

13.5.16 AUTO ADDRESS INCREMENT

With the Auto Address Increment mode a fast stack-like reading and writing of CAN-controller internal registers is provided. If the bit CANADR.5 (AutoInc) is HIGH, the content of CANADR is incremented automatically after any read or write access to CANDAT. For instance, loading a message into the Transmit Buffer can be done by writing 2AH into CANADR and then moving byte by byte of the message to CANDAT. Incrementing CANADR beyond XX111111B resets the bit CANADR.5 (AutoInc) automatically (CANADR = XX000000B).

13.5.17 HIGH SPEED DMA

The DMA-logic allows you to transfer a complete message (up to 10 bytes) between CAN-controller and MAIN RAM in 2 instruction cycles at maximum; up to 4 bytes are transferred in 1 instruction cycle. The performance of the CPU is strongly enhanced because this very fast transfer is carried out in the background.

A DMA transfer is achieved by first writing the RAM address (00H to FFH) into CANSTA and then setting the TX- or RX-Buffer address in CANDR and the bit CANADR.7 (DMA) simultaneously; the RAM address points to the location of the first byte to be transferred. Setting the DMA bit causes an automatic evaluation of the Data Length Code and then the transfer; for a TX-DMA transfer the Data Length Code is expected at the location 'RAM address +1'.

In order to program a TX-DMA transfer the value 8AH (address 10) has to be written into CANADR. Then a complete message, consisting of the 2-byte Descriptor and the Data Field (0 to 8 bytes), starting at location 'RAM address' is transferred to the TX-Buffer.

The RX-DMA transfer is very versatile. By writing a value in the range of 94H (address 20) up to 9DH (address 29) into CANADR the whole or a part of the received message, starting at the specified address, is transferred to the internal Data Memory. This allows e.g. to transfer the bytes of the Data Field only.

After a successful DMA transfer the DMA-bit is reset.

During a DMA transfer the CPU can process the next instruction. However, an access to the Data Memory, CANADR, CANDAT, CANCON or CANSTA is not allowed. After having set the DMA-bit, every interrupt is disabled until the end of the transfer. Note, that disadvantageous programming may lead to an interrupt response time of at most 10 instruction cycles. The shortest interrupt response time is achieved by using 2 consecutive 1-cycle instructions directly after setting the DMA-bit.

During the reset state (bit Reset Request is HIGH) a DMA transfer is not possible.

13.5.18 BUS TIMING/SYNCHRONIZATION

The Bus Timing Logic (BTL) monitors the serial bus-line via the on-chip input comparator and performs the following functions (see Section 13.4):

- Monitors the serial bus-line level
- Adjusts the sample point, within a bit period (programmable)
- Samples the bus-line level using majority logic (programmable, 1 or 3 samples)
- Synchronization to the bit stream:
  - hard synchronization at the start of a message
  - resynchronization during transfer of a message.

The configuration of the BTL is performed during the initialization of the CAN-controller. The BTL uses the following three registers:

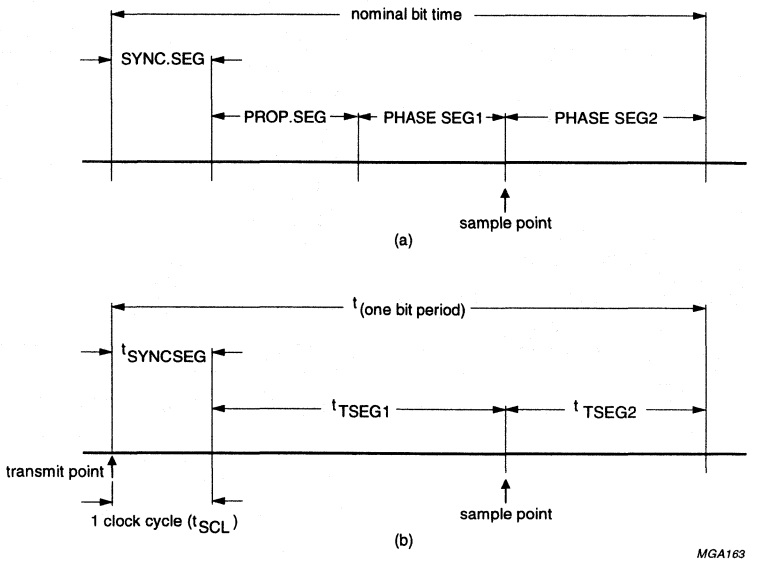
- Control Register (Sync)
- Bus Timing Register 0
- Bus Timing Register 1.

13.5.19 BIT TIMING

A bit period is built up from a number of system clock cycles (t_{SCL}), see Section 13.5.9.
One bit period is the result of the addition of the programmable segments TSEG1 and TSEG2 and the general segment SYNCSEG.

13.5.19.1 Synchronization Segment (SYNCSEG)

The incoming edge of a bit is expected during this state; this state corresponds to one system clock cycle ($1 \times t_{SCL}$).



(a) As defined by the CAN-protocol.
(b) As implemented in the P8XC592's on-chip CAN-controller.

Fig.19 Bit period.

13.5.19.2 Time Segment 1 (TSEG1)

This segment determines the location of the sampling point within a bit period, which is at the end of TSEG1. TSEG1 is programmable from 1 to 16 system clock cycles (see Section 13.5.10).

The correct location of the sample point is essential for the correct functioning of a transmission. The following points must be taken into consideration:

- A Start-Of-Frame (see Section 13.6.2) causes all CAN-controllers to perform a 'hard synchronization' (see Section 13.5.20) on the first recessive-to-dominant edge.
  During arbitration, however, several CAN-controllers may simultaneously transmit. Therefore it may require twice the sum of bus-line, input comparator and the output driver delay times until the bus is stable.
  This is the propagation delay time.
- To avoid sampling at an incorrect position, it is necessary to include an additional synchronization buffer on both sides of the sample point.
  The main reasons for incorrect sampling are:
  - Incorrect synchronization due to spikes on the bus-line
  - Slight variations in the oscillator frequency of each CAN-controller in the network, which results in a phase error.
- Time Segment 1 consists of the segment for compensation of propagation delays and the synchronization buffer segment directly before the sample point (see Fig.19).

13.5.19.3 Time Segment 2 (TSEG2)

This time segment provides:

- Additional time at the sample point for calculation of the subsequent bit levels (e.g. arbitration)
- Synchronization buffer segment directly after the sample point.

TSEG2 is programmable from 1 to 8 system clock cycles (see Section 13.5.10).

13.5.19.4 Synchronisation Jump Width (SJW)

SJW defines the maximum number of clock cycles (t_{SCL}) a period may be reduced or increased by one resynchronization. SJW is programmable from 1 to 4 system clock cycles, see Section 13.5.2.

13.5.19.5 Propagation Delay Time (t_{prop})

The Propagation Delay Time is:

$t_{prop} = 2 \times$ (physical bus delay + input comparator delay + output driver delay).

t_{prop} is rounded up to the nearest multiple of t_{SCL}.

13.5.19.6 Bit Timing Restrictions

Restrictions on the configuration of the bit timing are based on internal processing. The restrictions are:

- $t_{TSEG2} \geq 2t_{SCL}$
- $t_{TSEG2} \geq t_{SJW}$
- $t_{TSEG1} \geq t_{SEG2}$
- $t_{TSEG1} \geq t_{SJW} + t_{prop}$.

The three sample mode (SAM = HIGH) has the effect of introducing a delay of one system clock cycle on the bus-line. This must be taken into account for the correct calculation of TSEG1 and TSEG2:

- $t_{TSEG1} \geq t_{SJW} + t_{prop} + 2t_{SCL}$
- $t_{TSEG2} \geq 3t_{SCL}$.

13.5.20 SYNCHRONIZATION

Synchronization is performed by a state machine which compares the incoming edge with its actual bit timing and adapts the bit timing by hard synchronization or resynchronization.

This type of synchronization occurs only at the beginning of a message.

The CAN-controller synchronizes on the first incoming recessive-to-dominant edge of a message (being the leading edge of a message's Start-Of-Frame bit; see Section 13.6.2.

Resynchronization occurs during the transmission of a message's bit stream to compensate for:

- Variations in individual CAN-controller oscillator frequencies
- Changes introduced by switching from one transmitter to another (e.g. during arbitration).

As a result of resynchronization either t_{TSEG1} may be increased by up to a maximum of t_{SJW} or t_{TSEG2} may be decreased by up to a maximum of t_{SJW}:

- $t_{TSEG1} \leq t_{SCL}$ [(TSEG1 + 1) + (SJW + 1)]
- $t_{TSEG2} \geq t_{SCL}$ [(TSEG2 + 1) – (SJW + 1)].

TSEG1, TSEG2 and SJW are the programmed numerical values.

The phase error (e) of an edge is given by the position of the edge relative to SYNCSEG, measured in system clock cycles (t_{SCL}).

The value of the phase error is defined as:

- e = 0, if the edge occurs within SYNCSEG
- e > 0, if the edge occurs within TSEG1
- e < 0, if the edge occurs within TSEG2.

The effect of resynchronization is:

- The same as that of a hard synchronization, if the magnitude of the phase error (e) is less or equal to the programmed value of t_{SJW}
- To increase a bit period by the amount of t_{SJW}, if the phase error is positive and the magnitude of the phase error is larger than t_{SJW}
- To decrease a bit period by the amount of t_{SJW}, if the phase error is negative and the magnitude of the phase error is larger than t_{SJW}.

13.5.20.1 Synchronization Rules

The synchronization rules are as follows:

- Only one synchronization within one bit time is used.
- An edge is used for synchronization only if the value detected at the previous sample point differs from the bus value immediately after the edge.
- Hard synchronization is performed whenever there is a recessive-to-dominant edge during Bus-Idle (see Section 13.6.6).
- All other edges (recessive-to-dominant and optionally dominant-to recessive edges if the Sync bit is set HIGH (see Section 13.5.3) which are candidates for resynchronization will be used with the following exception:
  - A transmitting CAN-controller will not perform a resynchronization as a result of a recessive-to-dominant edge with positive phase error, if only these edges are used for resynchronization. This ensures that the delay times of the output driver and input comparator do not cause a permanent increase in the bit time.

13.6 CAN 2.0A Protocol description

13.6.1 FRAME TYPES

The P8XC592's CAN-controller supports the four different CAN-protocol frame types for communication:

- Data Frame, to transfer data
- Remote Frame, request for data
- Error Frame, globally signal a (locally) detected error condition
- Overload Frame, to extend delay time of subsequent frames (an Overload Frame is not initiated by the P8XC592 CAN-controller).

13.6.1.1 Bit representation

There are two logical bit representations used in the CAN-protocol:

- A recessive bit on the bus-line appears only if all connected CAN-controllers send a recessive bit at that moment.
- Dominant bits always overwrite recessive bits i.e. the resulting bit level on the bus-line is dominant.

13.6.2 DATA FRAME

A Data Frame carries data from a transmitting CAN-controller to one or more receiving ones.
A Data Frame is composed of seven different bit-fields:

- Start-Of-Frame
- Arbitration Field
- Control Field
- Data Field (may have a length of zero)
- CRC Field (CRC = Cyclic Redundancy Code)
- Acknowledge Field
- End-Of-Frame.

13.6.2.1 Start-Of-Frame bit

Signals the start of a Data Frame or Remote Frame. It consists of a single dominant bit use for hard synchronization of a CAN-controller in receive mode.

13.6.2.2 Arbitration Field

Consists of the message Identifier and the RTR bit. In the case of simultaneous message transmissions by two or more CAN-controllers the bus access conflict is solved by bit-wise arbitration, which is active during the transmission of the Arbitration Field.

13.6.2.3 Identifier

This 11-bit field is used to provide information about the message, as well as the bus access priority. It is transmitted in the order ID.10 to ID.0 (LSB). The situation that the seven most significant bits (ID.10 to ID.4) are all recessive must not occur.

An Identifier does not define which particular CAN-controller will receive the frame because a CAN based communication network does not differentiate between a point-to-point, multicast or broadcast communication.

13.6.2.4 RTR bit

A CAN-controller, acting as a receiver for certain information may initiate the transmission of the respective data by transmitting a Remote Frame to the network, addressing the data source via the Identifier and setting the RTR bit HIGH (remote; recessive bus level). If the data source simultaneously transmits a Data Frame containing the requested data, it uses the same Identifier. No bus access conflict occurs due to the RTR bit being set LOW (data; dominant bus level) in the Data Frame.

13.6.2.5 Control Field

This field consists of six bits. It includes two reserved bits (for future expansions of the CAN-protocol), transmitted with a dominant bus level, and is followed by the Data Length Code (4 bits).
The number of bytes (destuffed; number of data bytes to be transmitted/received) in the Data Field is indicated by the Data Length Code. Admissible values of the Data Length Code, and hence the number of bytes in the (destuffed) Data Field, are {0, 1, ..., 8}. A logic 0 (logic 1) in the Data Length Code is transmitted as dominant (recessive) bus level, respectively.

13.6.2.6 Data Field

The data, stored within the Data Field of the Transmit Buffer, are transmitted according to the Data Length Code. Conversely, data of a received Data Frame will be stored in the Data Field of a Receive Buffer. The Data Field can contain from 0 up to 8 bytes. The most significant bit of the first data byte (lowest address) is transmitted/received first.

13.6.2.7 Cyclic Redundancy Code Field (CRC)

The CRC Field consists of the CRC Sequence (15 bits) and the CRC Delimiter (1 recessive bit). The Cyclic Redundancy Code (CRC) encloses the destuffed bit stream of the Start-Of-Frame, Arbitration Field, Data Field and CRC Sequence. The most significant bit of the CRC Sequence is transmitted/received first. This frame check sequence, implemented in the CAN-controller is derived from a cyclic redundancy code best suited for frames with a total bit count of less than 127 bits, see Section 13.6.8.3. With Start-Of-Frame (dominant bit) included in the code word, any rotation of the code word can be detected by the absence of the CRC Delimiter (recessive bit).

13.6.2.8 Acknowledge Field (ACK)

The Acknowledge Field consists of two bits, the Acknowledge Slot and the Acknowledge Delimiter, which are transmitted with a recessive level by the transmitter of the Data Frame. All CAN-controllers having received the matching CRC Sequence, report this by overwriting the transmitter's recessive bit in the Acknowledge Slot with a dominant bit. Thereby a transmitter, still monitoring the bus level recognizes that at least one receiver within the network has received a complete and correct message (i.e. no error was found). The Acknowledge Delimiter (recessive bit) is the second bit of the Acknowledge Field. As a result, the Acknowledge Slot is surrounded by two recessive bits: the CRC Delimiter and the Acknowledge Delimiter.

All nodes within a CAN network may use all the information coming to the network by all CAN-controllers (shared memory concept). Therefore, acknowledgement and error handling are defined to provide all information in a consistent way throughout this shared memory. Hence, there is no reason to discriminate different receivers of a message in the acknowledge field. If a node is disconnected from the network due to bus failure, this particular node is no longer part of the shared memory. To identify a 'lost node' additional and application specific precautions are required.

13.6.2.9 End-Of-Frame

Each Data Frame or Remote Frame is delimited by the End-Of-Frame bit sequence which consists of seven recessive bits (exceeds the bit stuff width by two bits). Using this method a receiver detects the end of a frame independent of a previous transmission error because the receiver expects all bits up to the end of the CRC Sequence to be coded by the method of bit-stuffing, see Section 13.6.7.3. The bit-stuffing logic is deactivated during the End-Of-Frame sequence.

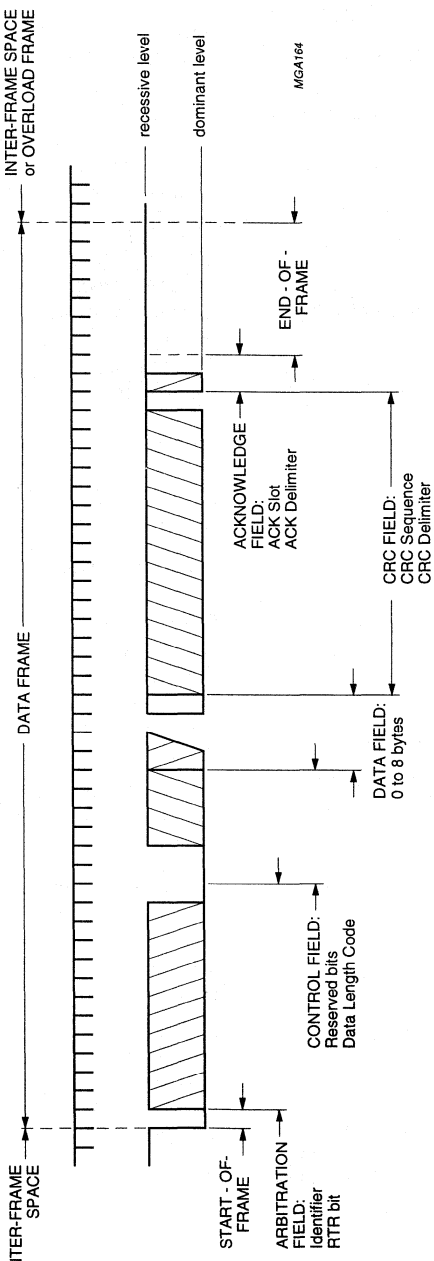


Fig.20 Data Frame.

13.6.3 REMOTE FRAME

A CAN-controller acting as a receiver for certain information may initiate the transmission of the respective data by transmitting a Remote Frame to the network, addressing the data source via the Identifier and setting the RTR bit HIGH (remote; recessive bus level). The Remote Frame is similar to the Data Frame with the following exceptions:

- RTR bit is set HIGH
- Data Length Code is ignored
- No Data Field contained.

Note that the value of the Data Length Code should be the one of the corresponding Data Frame, although it is ignored for a Remote Frame.

A Remote Frame is composed of six different bit fields:

- Start-of-Frame
- Arbitration Field
- Control Field
- CRC Field
- Acknowledge Field
- End-Of-Frame.

See Section 13.6.2 for more detailed explanation of the Remote Frame bit fields.

13.6.4 ERROR FRAME

The Error Frame consists of two different fields:

- The first field, accomplished by the superimposing of Error Flags contributed from different CAN-controllers
- The second field is the Error Delimiter.

13.6.4.1 Error Flag

There are two forms of an Error Flag:

- Active Error Flag, consists of six consecutive dominant bits.
- Passive Error Flag, consists of six consecutive recessive bits unless it is overwritten by dominant bits from other CAN-controllers.

An error-active CAN-controller (see Section 13.6.9) detecting an error condition signals this by transmission of an Active Error Flag. This Error Flag's form violates the bit-stuffing rule (see Section 13.6.7) applied to all fields, from Start-Of-Frame to CRC Delimiter, or destroys the fixed form of the fields Acknowledge Field or End-Of-Frame (see Fig.21).

Consequently, all other CAN-controllers detect an error condition and start transmission of an Error Flag. Therefore the sequence of dominant bits, which can be monitored on the bus, results from a superposition of different Error Flags transmitted by individual CAN-controllers. The total length of this sequence varies between six (minimum) and twelve (maximum) bits.

An error-passive CAN-controller (see Section 13.6.9) detecting an error condition tries to signal this by transmission of a Passive Error Flag. The error-passive CAN-controller waits for six consecutive bits with identical polarity, beginning at the start of the Passive Error Flag. The Passive Error Flag is complete when these six identical bits have been detected.

13.6.4.2 Error Delimiter

The Error Delimiter consists of eight recessive bits and has the same format as the Overload Delimiter. After transmission of an Error Flag, each CAN-controller monitors the bus-line until it detects a transition from a dominant-to-recessive bit level. At this point in time, every CAN-controller has finished sending its Error Flag and has additionally sent the first out of the 8 recessive bits of the Error Delimiter. Afterwards all CAN-controllers transmit the remaining recessive bits. After this event and an Intermission Field all error-active CAN-controllers within the network can start a transmission simultaneously.

If a detected error is signalled during transmission of a Data Frame or Remote Frame, the current message is spoiled and a retransmission of the message is initiated.

If a CAN-controller monitors any deviation of the Error Frame, a new Error Frame will be transmitted. Several consecutive Error Frames may result in the CAN-controller becoming error-passive and leaving the network unblocked.

In order to terminate an Error Flag correctly, an error-passive CAN-controller requires the bus to be Bus-Idle (see Section 13.6.6) for at least three bit periods (if there is a local error at an error-passive-receiver). Therefore a CAN-bus should not be 100% permanently loaded.

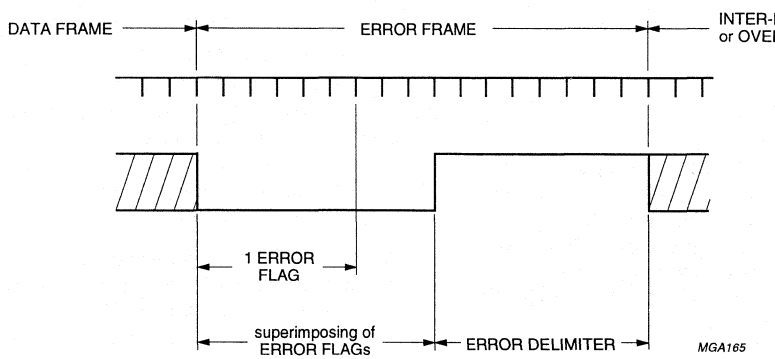


Fig.21 Error Frame.

13.6.5 OVERLOAD FRAME

The Overload Frame consists of two fields:

- The Overload Flag
- The Overload Delimiter.

The transmission of an Overload Frame may only start:

- Condition 1; during the first bit period of an expected Intermission Field.
- Condition 2; one bit period after detecting the dominant bit during Intermission Field.

The P8XC592's on-chip CAN-controller will never initiate transmission of a condition 1 Overload Frame and will only react on a transmitted condition 2 Overload Frame, according to the CAN-protocol. No more than two Overload Frames are generated to delay a Data Frame or a Remote Frame. Although the overall form of the Overload Frame corresponds to that of the Error Frame, an Overload Frame does not initiate or require the retransmission of the preceding frame.

13.6.5.1 Overload Flag

The Overload Flag consists of six dominant bits and has a similar format to the Error Flag.

There are two conditions in the CAN-protocol which lead to the transmission of an Overload Flag:

- Condition 1; receiver circuitry requires more time to process the current data before receiving the next frame (receiver not ready).
- Condition 2; detection of a dominant bit during Intermission Field (see Section 13.6.6).

The Overload Flag's form corrupts the fixed form of the Intermission Field. All other CAN-controllers detecting the overload condition also transmit an Overload Flag (condition 2).

13.6.5.2 Overload Delimiter

The Overload Delimiter consists of eight recessive bits and takes the same form as the Error Delimiter. After transmission of an Overload Flag, each CAN-controller monitors the bus-line until it detects a transition from a dominant-to-recessive bit level. At this point in time, every CAN-controller has finished sending its Overload Flag and all CAN-controllers start simultaneously transmitting seven more recessive bits.

13.6.6 INTER-FRAME SPACE

Data Frames and Remote Frames are separated from preceding frames (all types) by an Inter-Frame Space, consisting of an Intermission Field and a Bus-Idle. Error-passive CAN-controllers also send a Suspend Transmission (see Section 13.6.9) after transmission of a message. Overload Frames and Error Frames are not preceded by an Inter-Frame Space.

13.6.6.1 Intermission Field

The Intermission Field consists of three recessive bits. During an Intermission period, no frame transmissions will be started by the P8XC592's on-chip CAN-controller. An Intermission is required to have a fixed time period to allow a CAN-controller to execute internal processes prior to the next receive or transmit task.

13.6.6.2 Bus-Idle

The Bus-Idle time may be of arbitrary length (min. 0 bit). The bus is recognized to be free and a CAN-controller having information to transmit may access the bus. The detection of a dominant bit level during Bus-Idle on the bus is interpreted as the Start-Of-Frame.

13.6.7 BUS ORGANIZATION

Bus organization is based on five basic rules described in the following subsections.

13.6.7.1 Bus Access

CAN-controllers only start transmission during the Bus-Idle state. All CAN-controllers synchronize on the leading edge of the Start-Of-Frame (hard synchronization).

13.6.7.2 Bus Arbitration

If two or more CAN-controllers simultaneously start transmitting, the bus access conflict is solved by a bit-wise arbitration process during transmission of the Arbitration Field.

During arbitration every transmitting CAN-controller compares its transmitted bit level with the monitored bus level. Any CAN-controller which transmits a recessive bit and monitors a dominant bus level immediately becomes the receiver of the higher-priority message on the bus without corrupting any information on the bus. Each message contains an unique Identifier and a RTR bit describing the type of data within the message. The Identifier together with the RTR bit implicitly define the message's bus access priority. During arbitration the most significant bit of the Identifier is transmitted first and the RTR bit last. The message with the lowest binary value of the Identifier and RTR bit has the highest priority. A Data Frame has higher priority than a Remote Frame due to its RTR bit having a dominant level.

For every Data Frame there is an unique transmitter. For reasons of compatibility with other CAN-bus controllers, use of the Identifier bit pattern ID = 1111111XXXXB (X being bits of arbitrary level) is forbidden.

The number of available different Identifiers:

$(2^{11} - 2^4) = 2032.$

13.6.7.3 Coding/Decoding

The following bit fields are coded using the bit-stuffing technique:

- Start-Of-Frame
- Arbitration Field
- Control Field
- Data Field
- CRC Sequence.

When a transmitting CAN-controller detects five consecutive bits of identical polarity to be transmitted, a complementary (stuff) bit is inserted into the transmitted bit-stream.

When a receiving CAN-controller has monitored five consecutive bits with identical polarity in the received bit streams of the above described bit fields, it automatically deletes the next received (stuff) bit. The level of the deleted stuff bit has to be the complement of the previous bits; otherwise a Stuff Error will be detected and signalled (see Section 13.6.8).

The remaining bit fields or frames are of fixed form and are not coded or decoded by the method of bit-stuffing.

The bit-stream in a message is coded according to the Non-Return-to-Zero (NRZ) method, i.e. during a bit period, the bit level is held constant, either recessive or dominant.

13.6.7.4 Error Signalling

A CAN-controller which detects an error condition, transmits an Error Flag. Whenever a Bit Error, Stuff Error, Form Error or an Acknowledgement Error is detected, transmission of an Error Flag is started at the next bit. Whenever a CRC Error is detected, transmission of an Error Flag starts at the bit following the Acknowledge Delimiter, unless an Error Flag for another error condition has already started. An Error Flag violates the bit-stuffing law or corrupts the fixed form bit fields. A violation of the bit-stuffing law affects any CAN-controller which detects the error condition. These devices will also transmit an Error Flag.

An error-passive CAN-controller (see Section 13.6.9) which detects an error condition, transmits a Passive Error Flag. A Passive Error Flag is not able to interrupt a current message at different CAN-controllers but this type of Error Flag may be ignored (overwritten) by other CAN-controllers. After having detected an error condition, an error-passive CAN-controller will wait for six consecutive bits with identical polarity and when monitoring them, interpret them as an Error Flag.

After transmission of an Error Flag, each CAN-controller monitors the bus-line until it detects a transition from a dominant-to-recessive bit level. At this point in time, every CAN-controller has finished transmitting its Error Flag and all CAN-controllers start transmitting seven additional recessive bits (Error Delimiter, see Section 13.6.4).

The message format of a Data Frame or Remote Frame is defined in such a way that all detectable errors can be signalled within the message transmission time and therefore it is very simple for the CAN-controllers to associate an Error Frame to the corresponding message and to initiate retransmission of the corrupted message. If a CAN-controller monitors any deviation of the fixed form of an Error Frame, it transmits a new Error Frame.

13.6.7.5 Overload Signalling

Some CAN-controllers (but not the one on-chip of the P8XC592) require to delay the transmission of the next Data Frame or Remote Frame by transmitting one or more Overload Frames. The transmission of an Overload Frame must start during the first bit of an expected Intermission Field. Transmission of Overload Frames which are reactions on a dominant bit during an expected Intermission Field, start one bit after this event.

Though the format of Overload Frame and Error Frame are identical, they are treated differently. Transmission of an Overload Frame during Intermission Field does not initiate the retransmission of any previous Data Frame or Remote Frame. If a CAN-controller which transmitted an Overload Frame monitors any deviation of its fixed form, it transmits an Error Frame.

13.6.8 Error Detection

The processes described in the following sub-sections are implemented in the P8XC592's on-chip CAN-controller for error detection.

13.6.8.1 Bit Error

A transmitting CAN-controller monitors the bus on a bit-by-bit basis. If the bit level monitored is different from the transmitted one, a Bit Error is signalled.
The exceptions being:

- During the Arbitration Field, a recessive bit can be overwritten by a dominant bit. In this case, the CAN-controller interprets this as a loss of arbitration.
- During the Acknowledge Slot, only the receiving CAN-controllers are able to recognize a Bit Error.

13.6.8.2 Stuff Error

The following bit fields are coded using the bit-stuffing technique:

- Start-Of-Frame
- Arbitration Field
- Control Field
- Data Field
- CRC Sequence.

There are two possible ways of generating a Stuff Error:

- A disturbance generates more than the allowed five consecutive bits with identical polarity. These errors are detected by all CAN-controllers.
- A disturbance falsifies one or more of the five bits preceding the stuff bit. This error situation is not recognized as a Stuff Error by the receivers. Therefore, other error detection processes may detect this error condition such as:
  - CRC check, format violation at the receiving CAN-controllers, or
  - Bit Error detection by the transmitting CAN-controller.

13.6.8.3 CRC Error

To ensure the validity of a transmitted message all receivers perform a CRC check. Therefore, in addition to the (destuffed) information digits (Start-Of-Frame up to Data Field), every message includes some control digits (CRC Sequence; generated by the transmitting CAN-controller of the respective message) used for error detection.

The code used by all CAN-controllers is a (shortened) BCH code, extended by a parity check and has the following attributes:

- 127 bits as maximum length of the code.
- 112 bits as maximum number of information digits (max. 83 bits are used by the CAN-controller).
- Length of the CRC Sequence amounts to 15 bits.
- Hamming distance d = 6.

As a result, '(d–1)' random errors are detectable (some exceptions exist).

The CRC Sequence is determined (calculated) by the following procedure:

1. The destuffed bit stream consisting of Start-Of-Frame up to the Data Field (if present) is interpreted as polynomial with coefficients 0 or 1.
2. This polynomial is divided (modulo-2) by the following generator polynomial, which includes a parity check:

   $f(x) = (x^{14} + x^9 + x^8 + x^6 + x^5 + x^4 + x^2 + x + 1)$

   $(x + 1) = 1100010110011001$ B.
3. The remainder of this polynomial division is the CRC Sequence.

Burst errors are detected up to a length of 15 [degree of f(x)]. Multiple errors (number of disturbed bits at least d = 6) are not detected with a residual error probability of 2^{-15} (3×10^{-5}) by CRC check only.

13.6.8.4 Form Error

Form Errors result from violations of the fixed form of the following bit fields:

- CRC Delimiter
- Acknowledge Delimiter
- End-Of-Frame
- Error Delimiter
- Overload Delimiter.

During the transmission of these bit fields an error condition is recognized if a dominant bit level instead of a recessive one is detected.

13.6.8.5 Acknowledgement Error

This is detected by a transmitter whenever it does not monitor a dominant bit during the Acknowledge Slot.

13.6.8.6 Error detection by an Error Flag from another CAN-controller

The detection of an error is signalled by transmitting an Error Flag. An Active Error Flag causes a Stuff Error, a Bit Error or a Form Error at all other CAN-controllers.

13.6.8.7 Error Detection Capabilities

Errors which occur at all CAN-controllers (global errors) are 100% detected. For local errors, i.e. for errors occurring at some CAN-controllers only, the shortened BCH code, extended by a parity check, has the following error detection capabilities:

- Up to five single Bit Errors are 100% detected, even if they are distributed randomly within the code.
- All single Bit Errors are detected if their total number (within the code) is odd.
- The residual error probability of the CRC check amounts to (3×10^{-5}). As an error may be detected not only by CRC check but also by other detection processes described above the residual error probability is several magnitudes less than (3×10^{-5}).

13.6.9 Error confinement definitions

13.6.9.1 Bus-OFF

A CAN-controller which has too many unsuccessful transmissions, relative to the number of successful transmissions, will enter the Bus-OFF state. It remains in this state, neither receiving nor transmitting messages until the Reset Request bit is set LOW (absent) and both Error Counters set to 0 (see Section 13.6.10).

13.6.9.2 Acknowledge

A CAN-controller which has received a valid message correctly, indicates this to the transmitter by transmitting a dominant bit level on the bus during the Acknowledge Slot, independent of accepting or rejecting the message.

13.6.9.3 Error-Active

An error-active CAN-controller in its normal operating state is able to receive and to transmit normally and also to transmit an Active Error Flag (see Section 13.6.10).

13.6.9.4 Error-Passive

An error-passive CAN-controller may transmit or receive messages normally. In the case of a detected error condition it transmits a Passive Error Flag instead of an Active Error Flag. Hence the influence on bus activities by an error-active CAN-controller (e.g. due to a malfunction) is reduced.

13.6.9.5 Suspend Transmission

After an error-passive CAN-controller has transmitted a message, it sends eight recessive bits after the Intermission Field and then checks for Bus-Idle. If during Suspend Transmission another CAN-controller starts transmitting a message the suspended CAN-controller will become the receiver of this message; otherwise being in Bus-Idle it may start to transmit a further message.

13.6.9.6 Start-Up

A CAN-controller which either was switched off or in the Bus-OFF state, must run a Start-Up routine in order to:

- Synchronize with other available CAN-controllers before starting to transmit. Synchronization is achieved, when 11 recessive bits, equivalent to Acknowledge Delimiter, End-Of-Frame and Intermission Field, have been detected (Bus-Free).
- Wait for other CAN-controllers without passing into the Bus-OFF state (due to a missing acknowledge), if there is no other CAN-controller currently available.

13.6.10 AIMS OF ERROR CONFINEMENT

13.6.10.1 Distinction of short and long disturbances

The CPU must be informed when there are long disturbances and when bus activities have returned to normal operation. During long disturbances, a CAN-controller enters the Bus-OFF state and the CPU may use default values.

Minor disturbances of bus activities will not effect a CAN-controller. In particular, a CAN-controller does not enter the Bus-OFF state or inform the CPU of a short bus disturbance.

13.6.10.2 Detection and localization of hardware disturbances and defects

The rules for error confinement are defined by the CAN-protocol specification (and implemented in the P8XC592's on-chip CAN-controller), in such a way that the CAN-controller, being nearest to the error-locus, reacts with a high probability the quickest (i.e. becomes error-passive or Bus-OFF). Hence errors can be localized and their influence on normal bus activities is minimized.

13.6.10.3 Error Confinement

All CAN-controllers contain a Transmit Error Counter and a Receive Error Counter, which registers errors during the transmission and the reception of messages, respectively.

If a message is transmitted or received correctly, the count is decreased. In the event of an error, the count is increased. The Error Counters have an non-proportional method of counting: an error causes a larger counter increase than a correctly transmitted/received message causes the count to decrease. Over a period of time this may result in an increase in error counts, even if there are fewer corrupted messages than uncorrupted ones. The level of the Error Counters reflect the relative frequency of disturbances. The ratio of increase/decrease depends on the acceptable ratio of invalid/valid messages on the bus and is hardware implemented to eight.

If one of the Error Counters exceeds the Warning Limit of 96 error points, indicating a significant accumulation of error conditions, this is signalled by the CAN-controller (Error Status, Error Interrupt).

A CAN-controller operates in the error-active mode until it exceeds 127 error points on one of its Error Counters. At this value it will enter the error-passive state. A transmit error which exceeds 255 error points results in the CAN-controller entering the Bus-OFF state.

14 INTERRUPT SYSTEM

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. Interrupt response latency is from 2.25 µs to 7.5 µs when using a 16 MHz crystal. The latency time strongly depends on the sequence of instructions executed directly after an interrupt request. During a CAN-DMA transfer the interrupt system is disabled (see Section 13.5.17). The P8XC592 acknowledges interrupt requests from fifteen sources as follows:

- $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$: externally via pins 27 and 28 respectively
- Timer 0 and Timer 1: from the two internal counters
  - If the capture function remains unused and the Capture Register contents are 'don't care' then the corresponding input pins 'CTnI', with 'n = 0 ... 3', may be used as positive and/or negative edge triggered external interrupts INT2 to INT5. But note that they can not terminate the Idle mode because the Timer 2 is switched off then
- Timer T2, 8 separate interrupts:
  - 4 capture interrupts
  - 3 compare interrupts
  - an overflow interrupt
- ADC end-of-conversion interrupt
- CAN-controller interrupt
- UART serial I/O port interrupt.

Each interrupt vectors to a separate location in Program Memory for its service program. Each source can be individually enabled or disabled by a corresponding bit in the IEN0 or IEN1 register, moreover each interrupt may be programmed to a HIGH or LOW priority level using a corresponding bit in the IP0 or IP1 register. Also all enabled sources can be globally disabled or enabled. Both external interrupts can be programmed to be level-activated or transition-activated, and an active LOW level allows 'wire-ORing' of several interrupt sources to the input pin.

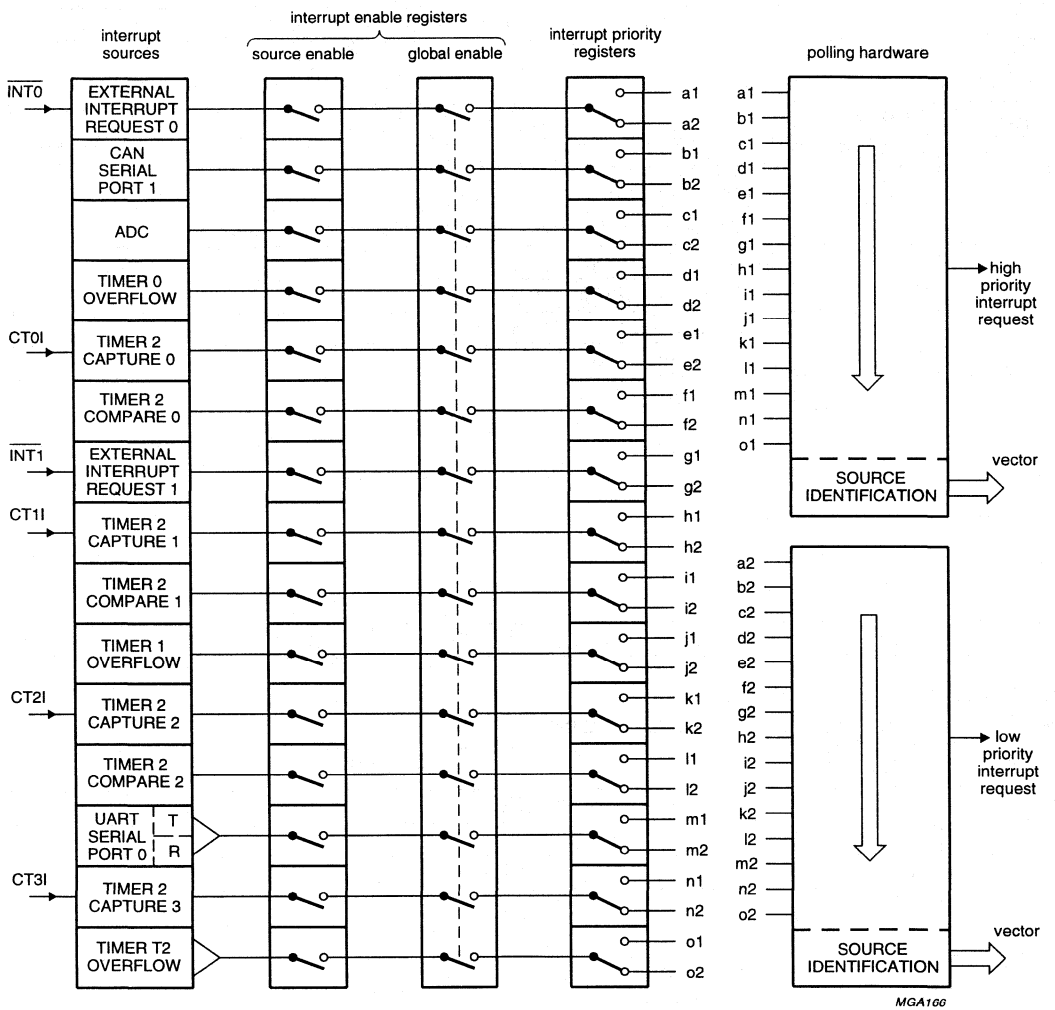


Fig.22 Interrupt system.

14.1 Interrupt Enable and Priority Registers

14.1.1 Interrupt Enable register 0 (IEN0)

Table 71 Interrupt Enable register 0 (address A8H)

7	6	5	4	3	2	1	0
EA	EAD	ES1	ES0	ET1	EX1	ET0	EX0

Table 72 Description of the IEN0 bits

BIT	SYMBOL	FUNCTION
7	EA	**General enable/disable control.** If bit EA is: LOW, then no interrupt is enabled. HIGH, then any individually enabled interrupt will be accepted.
6	EAD	Enable ADC interrupt.
5	ES1	Enable SIO1 (CAN) interrupt.
4	ES0	Enable SIO0 (UART) interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable External 1 interrupt.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable External 0 interrupt.

14.1.2 Interrupt Enable register 1 (IEN1)

Table 73 Interrupt Enable register 0 (address E8H)

7	6	5	4	3	2	1	0
ET2	ECM2	ECM1	ECM0	ECT3	ECT2	ECT1	ECT0

Table 74 Description of the IEN1 bits

Logic 0 = interrupt disabled; Logic 1 = interrupt enabled.

BIT	SYMBOL	FUNCTION
7	ET2	Enable T2 overflow interrupt(s).
6	ECM2	Enable T2 comparator 2 interrupt.
5	ECM1	Enable T2 comparator 1 interrupt.
4	ECM0	Enable T2 comparator 0 interrupt.
3	ECT3	Enable T2 capture register 3 interrupt.
2	ECT1	Enable T2 capture register 2 interrupt.
1	ECT1	Enable T2 capture register 1 interrupt.
0	ECT0	Enable T2 capture register 0 interrupt.

14.1.3 INTERRUPT PRIORITY REGISTER 0 (IP0)

Table 75 Interrupt Priority register 0 (address B8H)

7	6	5	4	3	2	1	0
–	PAD	PS1	PS0	PT1	PX1	PT0	PX0

Table 76 Description of the IP0 bits

BIT	SYMBOL	FUNCTION
7	–	Not used.
6	PAD	ADC interrupt priority level.
5	PS1	SIO1 (CAN) interrupt priority level.
4	PS0	SIO0 (UART) interrupt priority level.
3	PT1	Timer 1 interrupt priority level.
2	PX1	External interrupt 1 priority level.
1	PT0	Timer 0 interrupt priority level.
0	PX0	External interrupt 0 priority level.

14.1.4 INTERRUPT PRIORITY REGISTER 1 (IP1)

Table 77 Interrupt Priority register 1 (address F8H)

7	6	5	4	3	2	1	0
PT2	PCM2	PCM1	PCM0	PCT3	PCT2	PCT1	PCT0

Table 78 Description of the IP1 bits

Logic 0 = low priority; Logic 1 = high priority.

BIT	SYMBOL	FUNCTION
7	PT2	T2 overflow interrupt(s) priority level.
6	PCM2	T2 comparator 2 priority interrupt level.
5	PCM1	T2 comparator 1 priority interrupt level.
4	PCM0	T2 comparator 0 priority interrupt level.
3	PCT3	T2 capture register 3 priority interrupt level.
2	PCT2	T2 capture register 2 priority interrupt level.
1	PCT1	T2 capture register 1 priority interrupt level.
0	PCT0	T2 capture register 0 priority interrupt level.

14.2 Interrupt Vectors

The vector indicates the Program Memory location where the appropriate interrupt service routine starts (see Table 79).

Table 79 Interrupt vectors

SOURCE	BIT	VECTOR
External 0	X0	0003H
Timer 0 overflow	T0	000BH
External 1	X1	0013H
Timer 1 overflow	T1	001BH
Serial I/O 0 (UART)	S0	0023H
Serial I/O 1 (CAN)	S1	002BH
T2 capture 0	CT0	0033H
T2 capture 1	CT1	003BH
T2 capture 2	CT2	0043H
T2 capture 3	CT3	004BH
ADC completion	ADC	0053H
T2 compare 0	CM0	005BH
T2 compare 1	CM1	0063H
T2 compare 2	CM2	006BH
T2 overflow	T2	0073H

14.3 Interrupt Priority

Each interrupt source can be either high priority or low priority. If both priorities are requested simultaneously, the processor will branch to the high priority vector. If there are simultaneous requests from sources of the same priority, then interrupts will be serviced in the following order:

X0, S1, ADC, T0, CT0, CM0, X1, CT1, CM1, T1, CT2, CM2, S0, CT3, T2.

A low priority interrupt routine can only be interrupted by a high priority interrupt. A high priority interrupt routine can not be interrupted.

15 POWER REDUCTION MODES

The P8XC592 has three software-selectable modes to reduce power consumption. These are:

- Sleep mode, affecting the CAN-controller only
- Idle mode, affecting the
  - CPU (halted)
  - Timer 2 (stopped and reset)
  - PWM0, PWM1 (reset, output = HIGH)
  - ADC (aborted if in progress)
- Power-down mode, affecting the whole P8XC592 device.

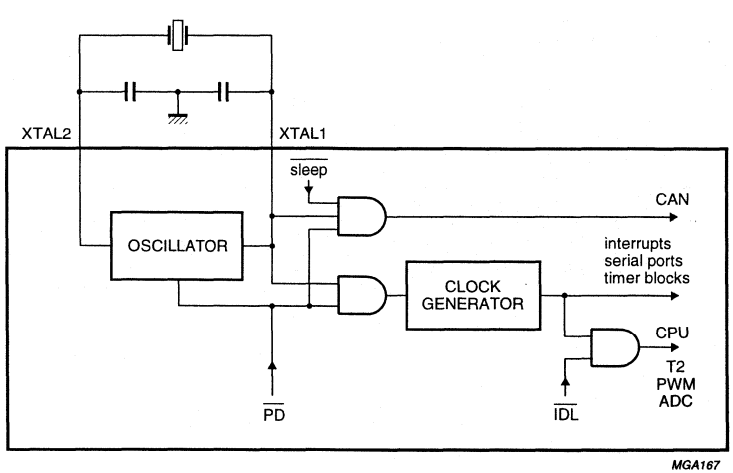


Fig.23 Internal Sleep, Idle and Power-down clock configuration.

15.1 Power Control Register (PCON)

Table 80 Power Control Register (address 87H)

7	6	5	4	3	2	1	0
SMOD	–	–	WLE	GF1	GF0	PD	IDL

Table 81 Description of the PCON bits

BIT	SYMBOL	FUNCTION
7	SMOD	**Double baud rate bit**. When set to logic 1 the baud rate is doubled when the serial port SIO0 is being used in Modes 1, 2 and 3.
6	–	Reserved.
5	–	
4	WLE	**Watchdog Load Enable**. This flag must be set by software prior to loading T3 (Watchdog timer). It is cleared when T3 is loaded.
3	GF1	**General purpose flag bits.**
2	GF0	
1	PD	**Power-down bit**. Setting this bit activates Power-down mode (note 1). It can only be set if input $\overline{EW}$ is HIGH.
0	IDL	**Idle mode bit**. Setting this bit activates the Idle mode (note 1).

Note

1. If PD and IDL are set to HIGH at the same time, PD takes precedence. The reset value of PCON is 0XX00000B.

15.2 CAN Sleep Mode

In order to reduce power consumption of the P8XC592 the CAN-controller may be switched off (disconnecting the internal clock) by setting the CAN Command Register bit 4 (Sleep) HIGH. The CAN-controller leaves this Sleep mode by detecting either activity on the CAN-bus (dominant bit-level on CRX0/CRX1; see Chapter 5, Table 1) or by setting the Sleep bit to LOW. As the CPU can not only write to the Sleep bit, but can also read it, the CAN-controller status can be determined directly.

15.3 Idle Mode

The instruction that sets bit PCON.0 to HIGH is the last one executed in the normal operating mode before Idle mode is activated.

Once in the Idle mode, the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in see Table 82.

There are three ways to terminate the Idle mode:

- Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, provided that the interrupt source is active during Idle mode. After the interrupt is serviced, the program continues with the instruction immediately after the one, at which the interrupt request was detected.
- The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
- Another way of terminating the Idle mode is an external hardware reset. Since the oscillator is still running, the reset signal is required to be active only for two machine cycles (24 oscillator periods) to complete the reset operation.
- The third way is the internally generated watchdog reset after an overflow of Timer 3.

15.4 Power-down Mode

The instruction that sets bit PCON.1 to HIGH, is the last one executed before entering the Power-down mode. In Power-down mode the oscillator of the P8XC592 is stopped. If the CAN-controller is in use, it is recommended to set it into Sleep mode before entering Power-down mode. However, setting PCON.1 to HIGH also sets the Sleep bit (CAN-controller Command Register bit 4) to HIGH.

The P8XC592 leaves Power-down mode either by a hardware reset or by a CAN Wake-Up interrupt (due to activity on the CAN-bus), if the SIO1 (CAN) interrupt source is enabled (contents of register IEN0 = 1X1XXXXXB).

A hardware reset affects the whole P8XC592, but leaves the contents of the on-chip RAM unchanged (CAN-controller-and CPU's SFRs are reset, see Section 13.5.2, Chapter 17 and Table 40). A CAN Wake-Up interrupt during Power-down mode causes a reset output pulse with a width of 6144 machine cycles (4.6 ms with f_{CLK} = 16 MHz). All hardware except that for the CAN-controller of the P8XC592 is reset (i.e. the contents of all CAN-controller registers are preserved).

A capacitance connected to the RST pin can be used to lengthen the internally generated reset pulse. If the pulse exceeds 8192 machine cycles, the CAN-controller part is reset too.

Table 82 Status of external pins during Idle and Power-down modes

MODE	PROGRAM	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1[1]	PORT2	PORT3	PORT4	PWM0/ PWM1
Idle	internal	1	1	port data	port data	port data	port data	port data	1
	external	1	1	floating	port data	address	port data	port data	1
Power-down	internal	0	0	port data	port data	port data	port data	port data	1
	external	0	0	floating	port data	port data	port data	port data	1

Note

1. If the port pins P1.6 and P1.7 are used as the CAN transmitter outputs (CTX0 and CTX1), then during Sleep and Power-down mode these pins output a 'recessive' level (see Sections 13.5.2 and 13.5.11).

16 OSCILLATOR CIRCUITRY

The oscillator circuitry of the P8XC592 is a single-stage inverting amplifier in a Pierce oscillator configuration. The circuitry between XTAL1 and XTAL2 is basically an inverter biased to the transfer point. Either a crystal or ceramic resonator can be used as the feedback element to complete the oscillator circuitry. Both are operated in parallel resonance. XTAL1 (pin 34) is the high gain amplifier input, and XTAL2 (pin 33) is the output (see Fig.24). If XTAL1 is driven from an external source, XTAL2 must be left open (see Fig.25).

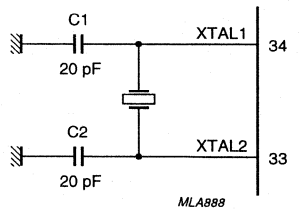


Fig.24 P8XC592 oscillator circuit.

17 RESET CIRCUITRY

The reset pin RST is connected to a Schmitt trigger for noise rejection (see Fig.26). A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods). The CPU responds by executing an internal reset. During reset ALE and $\overline{PSEN}$ output a HIGH level. In order to perform a correct reset, this level must not be affected by external elements.

Also with the P8XC592, the RST line can be pulled HIGH internally by a pull-up transistor activated by the Watchdog timer T3. The length of the output pulse from T3 is 3 machine cycles. A pulse of such short duration is necessary in order to recover from a processor or system fault as fast as possible.

During Power-down a reset could be generated internally via the CAN Wake-Up interrupt. Then the RST pin is pulled HIGH for 6144 machine cycles. In this case the CAN-controller is not reset.

If the Watchdog timer or the CAN Wake-Up interrupt is used to reset external devices, the usual capacitor arrangement for Power-on reset (see Fig.27) should not be used.

However, the internal reset is forced, independent of the external level on the RST pin.

The MAIN RAM and AUXILIARY RAM are not affected. When V_{DD} is turned on, the RAM content is indeterminate. A reset leaves the internal registers as shown in Table 83.

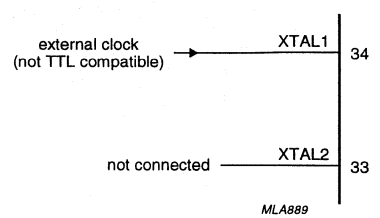


Fig.25 Driving P8XC592 from an external source.

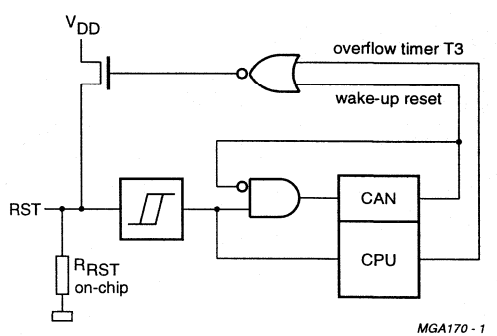


Fig.26 On-chip reset configuration.

Table 83 Internal registers' contents after a reset

X = undefined state.

REGISTER	7	6	5	4	3	2	1	0
CPU part								
ACC	0	0	0	0	0	0	0	0
ADC0	X	X	0	0	0	0	0	0
ADCH	X	X	X	X	X	X	X	X
B	0	0	0	0	0	0	0	0
CML0 to CML2	0	0	0	0	0	0	0	0
CMH0 to CMH2	0	0	0	0	0	0	0	0
CTCON	0	0	0	0	0	0	0	0
CTL0 to CTL3	X	X	X	X	X	X	X	X
CTH0 to CTH3	X	X	X	X	X	X	X	X
DPL	0	0	0	0	0	0	0	0
DPH	0	0	0	0	0	0	0	0
IEN0	0	0	0	0	0	0	0	0
IEN1	0	0	0	0	0	0	0	0
IP0	X	0	0	0	0	0	0	0
IP1	0	0	0	0	0	0	0	0
PCH	0	0	0	0	0	0	0	0
PCL	0	0	0	0	0	0	0	0
PCON	0	X	X	0	0	0	0	0
PSW	0	0	0	0	0	0	0	0
PWM0	0	0	0	0	0	0	0	0
PCWM1	0	0	0	0	0	0	0	0
PCWMP	0	0	0	0	0	0	0	0
P0 to P4	1	1	1	1	1	1	1	1
P5	X	X	X	X	X	X	X	X
RTE	0	0	0	0	0	0	0	0
S0BUF	X	X	X	X	X	X	X	X
S0CON	0	0	0	0	0	0	0	0

REGISTER	7	6	5	4	3	2	1	0
CANSTA	0	0	0	0	1	1	0	0
CANCON	X	X	X	0	0	0	0	0
CANDAT	X	X	X	X	X	X	X	X
CANADR	0	X	1	0	0	1	0	0
SP	0	0	0	0	0	1	1	1
STE	1	1	0	0	0	0	0	0
TCON	0	0	0	0	0	0	0	0
TH0, TH1	0	0	0	0	0	0	0	0
TMH2	0	0	0	0	0	0	0	0
TL0, TL1	0	0	0	0	0	0	0	0
TML2	0	0	0	0	0	0	0	0
TMOD	0	0	0	0	0	0	0	0
TM2CON	0	0	0	0	0	0	0	0
TM2IR	0	0	0	0	0	0	0	0
T3	0	0	0	0	0	0	0	0
CAN part								
CR	0	X	1	X	X	X	X	1
CMR	1	1	X	0	X	X	X	X
SR	0	0	0	0	1	1	0	0
IR	X	X	X	0	0	0	0	0
ACR	X	X	X	X	X	X	X	X
AMR	X	X	X	X	X	X	X	X
BTR0	X	X	X	X	X	X	X	X
BTR1	X	X	X	X	X	X	X	X
OCR	X	X	X	X	X	X	X	X
TR	X	X	X	X	X	X	X	X
TXB 10 to 19	X	X	X	X	X	X	X	X
RXB 20 to 29	X	X	X	X	X	X	X	X

17.1 Power-on Reset

If the RST pin is connected to V_{DD} via a 2.2 µF capacitor, as shown in Fig.27, an automatic reset can be obtained by switching on V_{DD} (provided its rise time is <10 ms). The decrease of the RST pin voltage depends on the capacitor and the internal resistor R_{RST}. That voltage must remain above the lower threshold for at minimum the oscillator start-up time plus 2 machine cycles.

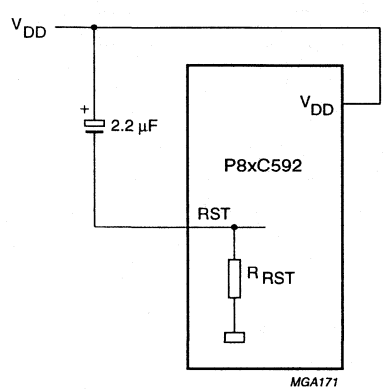


Fig.27 Power-on reset.

18 INSTRUCTION SET

The P8XC592 uses the powerful instruction set of the P80C51. It consists of 49 single-byte, 45 two-byte and 17 three-byte instructions. Using a 16 MHz quartz, 64 of the instructions are executed in 0.75 µs, 45 in 1.5 µs and the multiply, divide instructions in 3 µs. A summary of the instruction set is given in Tables 84, 85, 86, 87 and 88.

18.1 Addressing Modes

Most instructions have a 'destination/source' field that specifies the data type, addressing modes and operands involved. For all these instructions, except from MOVs, the destination operand is also a source operand (e.g. ADD A, R7).

Five types of addressing modes are used:

- Register Addressing,
  - R0 to R7 (4 banks)
  - A,B,C (bit), AB (2 bytes), DPTR (double byte).
- Direct Addressing,
  - lower 128 bytes of internal MAIN RAM (including the 4 R0 to R7 register banks)
  - Special Function Registers (SFRs)
  - 128 bits in a subset of the internal MAIN RAM (see Fig.6)
  - 128 bits in a subset of the Special Function Registers (see Figs 7 and 8).
- Register-Indirect Addressing,
  - internal RAM (@R0, @R1, @SP [PUSH/POP])
  - internal AUXILIARY RAM (@R0, @R1, @DPTR)
  - external Data Memory (@DPTR).
- Immediate Addressing,
  - Program Memory (in-code 8 bit or 16 bit constant).
- Base-Register-plus Index-Register-Indirect Addressing,
  - Program Memory look-up table (@DPTR+A, @PC+A).

The first three addressing modes are usable for destination operands.

18.2 Instruction Set

For the description of the **Data Addressing Modes** and **Hexadecimal opcode cross-reference** see Table 88.

Table 84 Instruction set description: Arithmetic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Arithmetic operations					
ADD	A,Rr	Add register to A	1	1	2*
ADD	A,direct	Add direct byte to A	2	1	25
ADD	A,@Ri	Add indirect RAM to A	1	1	26, 27
ADD	A,#data	Add immediate data to A	2	1	24
ADDC	A,Rr	Add register to A with carry flag	1	1	3*
ADDC	A,direct	Add direct byte to A with carry flag	2	1	35
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A,#data	Add immediate data to A with carry flag	2	1	34
SUBB	A,Rr	Subtract register from A with borrow	1	1	9*
SUBB	A,direct	Subtract direct byte from A with borrow	2	1	95
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A,#data	Subtract immediate data from A with borrow	2	1	94
INC	A	Increment A	1	1	04
INC	Rr	Increment register	1	1	0*
INC	direct	Increment direct byte	2	1	05
INC	@Ri	Increment indirect RAM	1	1	06, 07
DEC	A	Decrement A	1	1	14
DEC	Rr	Decrement register	1	1	1*
DEC	direct	Decrement direct byte	2	1	15
DEC	@Ri	Decrement indirect RAM	1	1	16, 17
INC	DPTR	Increment data pointer	1	2	A3
MUL	AB	Multiply A and B	1	4	A4
DIV	AB	Divide A by B	1	4	84
DA	A	Decimal adjust A	1	1	D4

Table 85 Instruction set description: Logic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Logic operations					
ANL	A,Rr	AND register to A	1	1	5*
ANL	A,direct	AND direct byte to A	2	1	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	1	54
ANL	direct,A	AND A to direct byte	2	1	52
ANL	direct,#data	AND immediate data to direct byte	3	2	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	1	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	1	44
ORL	direct,A	OR A to direct byte	2	1	42
ORL	direct,#data	OR immediate data to direct byte	3	2	43
XRL	A,Rr	Exclusive-OR register to A	1	1	6*
XRL	A,direct	Exclusive-OR direct byte to A	2	1	65
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	Exclusive-OR immediate data to A	2	1	64
XRL	direct,A	Exclusive-OR A to direct byte	2	1	62
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2	63
CLR	A	Clear A	1	1	E4
CPL	A	Complement A	1	1	F4
RL	A	Rotate A left	1	1	23
RLC	A	Rotate A left through the carry flag	1	1	33
RR	A	Rotate A right	1	1	03
RRC	A	Rotate A right through the carry flag	1	1	13
SWAP	A	Swap nibbles within A	1	1	C4

Table 86 Instruction set description: Data transfer

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Data transfer					
MOV	A,Rr	Move register to A	1	1	E*
MOV	A,direct (note 1)	Move direct byte to A	2	1	E5
MOV	A,@Ri	Move indirect RAM to A	1	1	E6, E7
MOV	A,#data	Move immediate data to A	2	1	74
MOV	Rr,A	Move A to register	1	1	F*
MOV	Rr,direct	Move direct byte to register	2	2	A*
MOV	Rr,#data	Move immediate data to register	2	1	7*
MOV	direct,A	Move A to direct byte	2	1	F5
MOV	direct,Rr	Move register to direct byte	2	2	8*
MOV	direct,direct	Move direct byte to direct	3	2	85
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	Move immediate data to direct byte	3	2	75
MOV	@Ri,A	Move A to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1	76, 77
MOV	DPTR,#data16	Load data pointer with a 16-bit constant	3	2	90
MOVC	A,@A+DPTR	Move code byte relative to DPTR to A	1	2	93
MOVC	A,@A+PC	Move code byte relative to PC to A	1	2	83
MOVX	A,@Ri	Move external RAM (8-bit address) to A	1	2	E2, E3
MOVX	A,@DPTR	Move external RAM (16-bit address) to A	1	2	E0
MOVX	@Ri,A	Move A to external RAM (8-bit address)	1	2	F2, F3
MOVX	@DPTR,A	Move A to external RAM (16-bit address)	1	2	F0
PUSH	direct	Push direct byte onto stack	2	2	C0
POP	direct	Pop direct byte from stack	2	2	D0
XCH	A,Rr	Exchange register with A	1	1	C*
XCH	A,direct	Exchange direct byte with A	2	1	C5
XCH	A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD	A,@Ri	Exchange LOW-order digit indirect RAM with A	1	1	D6, D7

Note

1. MOV A,ACC is not permitted.

Table 87 Instruction set description: Boolean variable manipulation, Program and machine control

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Boolean variable manipulation					
CLR	C	Clear carry flag	1	1	C3
CLR	bit	Clear direct bit	2	1	C2
SETB	C	Set carry flag	1	1	D3
SETB	bit	Set direct bit	2	1	D2
CPL	C	Complement carry flag	1	1	B3
CPL	bit	Complement direct bit	2	1	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C,bit	OR direct bit to carry flag	2	2	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C,bit	Move direct bit to carry flag	2	1	A2
MOV	bit,C	Move carry flag to direct bit	2	2	92
Program and machine control					
ACALL	addr11	Absolute subroutine call	2	2	•1
LCALL	addr16	Long subroutine call	3	2	12
RET		Return from subroutine	1	2	22
RETI		Return from interrupt	1	2	32
AJMP	addr11	Absolute jump	2	2	♦1
LJMP	addr16	Long jump	3	2	02
SJMP	rel	Short jump (relative address)	2	2	80
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2	73
JZ	rel	Jump if A is zero	2	2	60
JNZ	rel	Jump if A is not zero	2	2	70
JC	rel	Jump if carry flag is set	2	2	40
JNC	rel	Jump if carry flag is not set	2	2	50
JB	bit,rel	Jump if direct bit is set	3	2	20
JNB	bit,rel	Jump if direct bit is not set	3	2	30
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2	10
CJNE	A,direct,rel	Compare direct to A and jump if not equal	3	2	B5
CJNE	A,#data,rel	Compare immediate to A and jump if not equal	3	2	B4
CJNE	Rr,#data,rel	Compare immediate to register and jump if not equal	3	2	B*
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	2	B6, B7
DJNZ	Rr,rel	Decrement register and jump if not zero	2	2	D*
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2	D5
NOP		No operation	1	1	00

Table 88 Description of the mnemonics in the Instruction set

MNEMONIC	DESCRIPTION
Data addressing modes	
Rr	Working register R0-R7.
direct	128 internal RAM locations and any special function register (SFR).
@Ri	Indirect internal RAM location addressed by register R0 or R1 of the actual register bank.
#data	8-bit constant included in instruction.
#data 16	16-bit constant included as bytes 2 and 3 of instruction.
bit	Direct addressed bit in internal RAM or SFR.
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 kbytes Program Memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 kbytes page of Program Memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is –128 to +127 bytes relative to first byte of the following instruction.
Hexadecimal opcode cross-reference	
*	8, 9, A, B, C, D, E, F.
•	1, 3, 5, 7, 9, B, D, F.
◆	0, 2, 4, 6, 8, A, C, E.

Table 89 Instruction map

First hexadecimal character of opcode ↓	← Second hexadecimal character of opcode → 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC direct	INC @Ri 0	1	INC Rr 0	1	2	3	4	5	6	7
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC direct	DEC @Ri 0	1	DEC Rr 0	1	2	3	4	5	6	7
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,direct	ADD A,@Ri 0	1	ADD A,Rr 0	1	2	3	4	5	6	7
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,direct	ADDC A,@Ri 0	1	ADDC A,Rr 0	1	2	3	4	5	6	7
4	JC rel	AJMP addr11	ORL direct,A	ORL direct,#data	ORL A,#data	ORL A,direct	ORL A,@Ri 0	1	ORL A,Rr 0	1	2	3	4	5	6	7
5	JNC rel	ACALL addr11	ANL direct,A	ANL direct,#data	ANL A,#data	ANL A,direct	ANL A,@Ri 0	1	ANL A,Rr 0	1	2	3	4	5	6	7
6	JZ rel	AJMP addr11	XRL direct,A	XRL direct,#data	XRL A,#data	XRL A,direct	XRL A,@Ri 0	1	XRL A,Rr 0	1	2	3	4	5	6	7
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV direct,#data	MOV @Ri,#data 0	1	MOV Rr,#data 0	1	2	3	4	5	6	7
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV direct,direct	MOV direct,@Ri 0	1	MOV direct,Rr 0	1	2	3	4	5	6	7
9	MOV DTPR,#data16	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,direct	SUBB A,@Ri 0	1	SUB A,Rr 0	1	2	3	4	5	6	7
A	ORL C,/bit	AJMP addr11	MOV bit,C	INC DPTR	MUL AB		MOV @Ri,direct 0	1	MOV Rr,direct 0	1	2	3	4	5	6	7
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A,#data,rel	CJNE A,direct,rel	CJNE @Ri,#data,rel 0	1	CJNE Rr,#data,rel 0	1	2	3	4	5	6	7
C	PUSH direct	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,direct	XCH A,@Ri 0	1	XCH A,Rr 0	1	2	3	4	5	6	7
D	POP direct	ACALL addr11	SETB bit	SETB C	DA A	DJNZ direct,rel	XCHD A,@Ri 0	1	DJNZ Rr,rel 0	1	2	3	4	5	6	7
E	MOVX A,@DTPR	AJMP addr11	MOVX A,@Ri 0	1	CLR A	MOV A,direct (1)	MOV A,@Ri 0	1	MOV A,Rr 0	1	2	3	4	5	6	7
F	MOVX @DTPR,A	ACALL addr11	MOVX @Ri,A 0	1	CPL A	MOV direct,A	MOV @Ri,A 0	1	MOV Rr,A 0	1	2	3	4	5	6	7

Note

1. MOV A, ACC is not a valid instruction.

19 ABSOLUTE MAXIMUM RATINGS (note 1)

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	voltage on V_{DD} pin	−0.5	+6.5	V
V_{I1}	input voltage on any pin (except CTX0, CTX1, CRX0, CRX1 and $\overline{EA}/V_{PP}$)	−0.5	V_{DD} + 0.5	V
V_{I2}	input voltage on $\overline{EA}/V_{PP}$ to V_{SS}	−0.5	+13	V
I_I, I_O	input/output current on any single I/O pin (except from CTX0 and CTX1)	–	±10	mA
I_{OT}	sink current of CTX0, CTX1 together	–	30	mA
	source current of CTX0, CTX1 together	–	−20	mA
P_{tot}	total power dissipation (note 2)	–	1.0	W
T_{stg}	storage temperature range	−65	+150	°C
T_{amb}	operating ambient temperature range:			
	P87C592 EFx	−40	+85	°C
	P8XC592 FFA	−40	+85	°C
	P8XC592 FHA	−40	+125	°C

Notes

1. The following applies to the Absolute Maximum Ratings:
   a) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Chapters 20 "DC characteristics" and 21 "AC characteristics" of this specification is not implied.
   b) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effect of exessive static charge. However, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
   c) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
2. This value is based on the maximum allowable die temperature and the thermal resistance of the package, not on device power consumption.

20 DC CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified.
T_{amb} = −40 to +125 °C for the **P8XC592FHA**; T_{amb} = −40 to +85 °C for the **P8XC592FFA and P87C592EFx**.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply (digital part)					
V_{DD}	supply voltage		4.5	5.5	V
I_{DD}	operating supply current	f_{CLK} = 16 MHz; note 1	–	50	mA
$I_{DD(ID)}$	supply current Idle mode	f_{CLK} = 16 MHz; note 2	–	15	mA
$I_{DD(IS)}$	supply current Idle & Sleep mode	f_{CLK} = 16 MHz; note 3	–	10	mA
$I_{DD(PD)}$	supply current Power-down mode:	note 4			
	P8XC592 FHA		–	150	µA
	P8XC592 xFx		–	50	µA
Inputs					
V_{IL}	LOW level input voltage (except $\overline{EA}$, CRX0 and CRX1)		−0.5	$0.2V_{DD}$ − 0.1	V
V_{IL1}	LOW level input voltage $\overline{EA}$		−0.5	$0.2V_{DD}$ − 0.3	V
V_{IH}	HIGH level input voltage (except RST, XTAL1, CRX0,CRX1)		$0.2V_{DD}$ + 0.9	V_{DD} + 0.5	V
V_{IH1}	HIGH level input voltage (RST and XTAL1)		$0.7V_{DD}$	V_{DD} + 0.5	V
I_{IL}	LOW level input current Ports 1, 2, 3 and 4	V_I = 0.45 V	–	−50	µA
I_{TL}	input current HIGH-to-LOW transition Ports 1, 2, 3 and 4 (except P1.6 and P1.7)	V_I = 2.0 to 0.45 V	–	−650	µA
I_{LI1}	input leakage current Port 0, $\overline{EA}$, STADC, $\overline{EW}$, P1.6, P1.7	0.45 V < V_I < V_{DD}	–	±10	µA
I_{LI2}	input leakage current Port 5	0.45 V < V_I < V_{DD}	–	±1	µA
Outputs					
V_{OL}	LOW level output voltage Ports 1, 2, 3 and 4 (except P1.6 and P1.7)	I_{OL} = 1.6 mA; note 5	–	0.45	V
V_{OL1}	LOW level output voltage Port 0, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$, P1.6, P1.7	I_{OL} = 3.2 mA; note 5	–	0.45	V
V_{OH}	HIGH level output voltage Ports 1, 2, 3 and 4 (except P1.6 and P1.7)	I_{OH} = −60 µA	2.4	–	V
		I_{OH} = −25 µA	$0.75V_{DD}$	–	V
		I_{OH} = −10 µA	$0.9V_{DD}$	–	V
V_{OH1}	HIGH level output voltage Port 0 in external bus mode, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$	I_{OH} = −400 µA	2.4	–	V
		I_{OH} = −150 µA	$0.75V_{DD}$	–	V
		I_{OH} = −40 µA; note 6	$0.9V_{DD}$	–	V

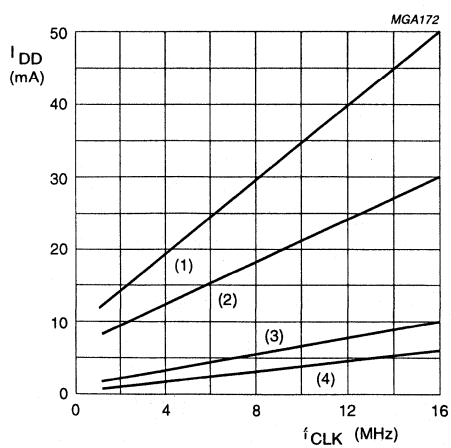
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{OH2}	HIGH level output voltage RST	I_{OH} = –400 µA I_{OH} = –120 µA	2.4 $0.8V_{DD}$	– –	V V
R_{RST}	RST pull-down resistor		50	150	kΩ
$C_{I/O}$	I/O pin capacitance	test frequency = 1 MHz; T_{amb} = 25 °C	–	10	pF
Supply (analog part)					
AV_{DD}	supply voltage	$AV_{DD} = V_{DD} \pm 0.2$ V	4.5	5.5	V
AI_{DD}	operating supply current	Port 5 = AV_{DD}; note 1	–	2.5	mA
$AI_{DD(ID)}$	supply current Idle mode	note 2	–	2.5	mA
$AI_{DD(IS)}$	supply current Idle and Sleep mode: P83C592 FHA P8XC592 xFx	note 3	 – –	 400 350	 µA µA
$AI_{DD(PD)}$	supply current Power-down mode: P83C592 FHA P8XC592 xFx	note 4	 – –	 400 350	 µA µA
Analog inputs					
AV_{IN}	analog input voltage		AV_{SS} – 0.2	AV_{DD} + 0.2	V
AV_{REF-}	reference voltage		AV_{SS} – 0.2	–	V
AV_{REF+}			–	AV_{DD} + 0.2	V
R_{REF}	resistance between AV_{REF+} and AV_{REF-}		10	50	kΩ
C_{IA}	analog input capacitance		–	15	pF
t_{ADS}	sampling time	note 7	–	$8t_{CY}$	µs
t_{ADC}	conversion time (including sample time)	note 7	–	$50t_{CY}$	µs
DL_e	differential non-linearity	notes 8, 9 and 10	–	±1	LSB
IL_e	integral non-linearity	notes 8 and 11	–	±2	LSB
OS_e	offset error	notes 8 and 12	–	±2	LSB
G_e	gain error	notes 8 and 13	–	±0.4	%
A_e	absolute voltage error	notes 8 and 14	–	±3	LSB
M_{ctc}	channel to channel matching		–	±1	LSB
C_t	crosstalk between P5 inputs	0 to 100 kHz	–	–60	dB
CAN input comparator (CRX0, CRX1)					
V_{DIF}	differential input voltage (note 15)	AV_{DD} = 5 V ± 5%; 1.4 V < V_I < AV_{DD}–1.4 V	±32	–	mV
V_{HYST}	hysteresis voltage (note 15)		8	30	mV
I_I	input current		–	±400	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
CAN output driver (V_{DD} = 5 V ± 5%)					
V_{OLT}	LOW level output voltage (CTX0 and CTX1)	I_o = 1.2 mA; note 15 I_o = 10 mA	– –	0.1 0.6	V V
V_{OHT}	High level output voltage (CTX0 and CTX1)	I_o = –1.2 mA; note 15 I_o = –10 mA; note 16	V_{DD} – 0.1 V_{DD} – 0.6	– –	V V
Reference (AV_{DD} = 5 V ± 5%; note 17)					
V_{REFOUT}	REF output voltage	–0.1 mA < I_L < 0.1 mA; C_L = 10 nF; note 15; bit Reference Active = HIGH	½AV_{DD}–0.1	½AV_{DD}+0.1	V
I_{REFIN}	REF input current	1.5 V < V_{REFIN} < AV_{DD}–1.5 V; bit Reference Active = LOW	–	±10	µA

Notes to the DC characteristics

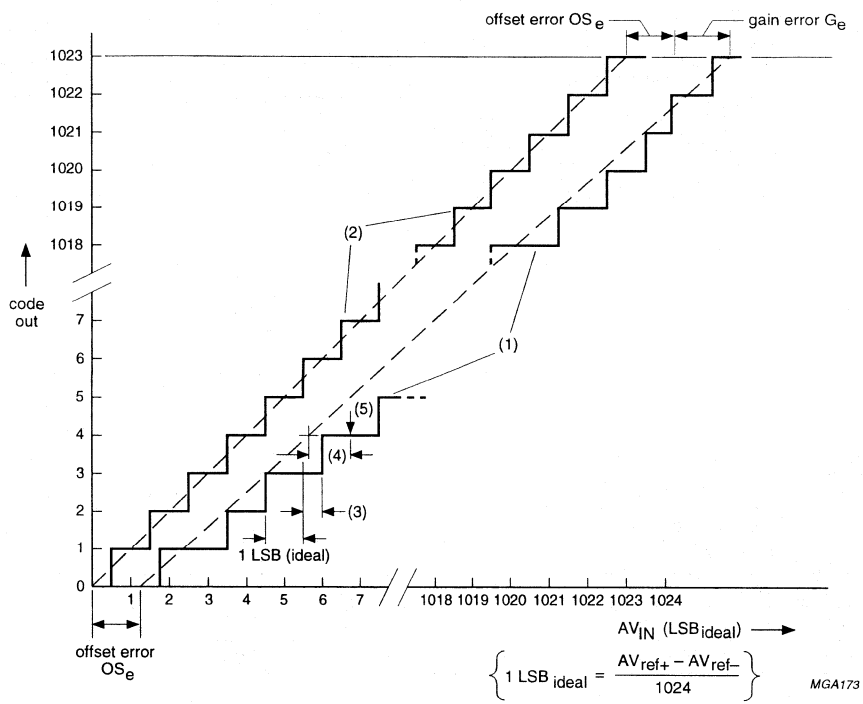
1. Conditions for:
   a) The **digital** operating current measurement: all output pins disconnected; XTAL1 is driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$ + 0.5 V; $V_{IH} = V_{DD}$ – 0.5 V; $\overline{EA}$ = RST = Port 0 = P1.6 = P1.7 = $\overline{EW}$ = V_{DD}; STADC = V_{SS}; CRX0 = 2.7 V; CRX1 = 2.3 V.
   b) The **analog** operating current measurement: Port 5 = AV_{DD}; CAN: register 6: = 00H; load current reference voltage source 100 µA.
2. Conditions for:
   a) The **digital** Idle mode supply current measurement: all output pins disconnected; XTAL1 is driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$ + 0.5 V; $V_{IH} = V_{DD}$ – 0.5 V; Port 0 = P1.6 = P1.7 = $\overline{EW}$ = V_{DD}; $\overline{EA}$ = RST = STADC = V_{SS}; CRX0 = 2.7 V; CRX1 = 2.3 V.
   b) The **analog** Idle mode current measurement: Port 5 = AV_{DD}; CAN: register 6: = 00H; load current reference voltage source 100 µA.
3. Conditions for:
   a) The **digital** Idle and Sleep mode supply current measurement: all output pins disconnected; XTAL1 is driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$ + 0.5 V; $V_{IH} = V_{DD}$ – 0.5 V; Port 0 = P1.6 = P1.7 = $\overline{EW}$ = CRX0 = V_{DD}; $\overline{EA}$ = RST = STADC = CRX1 = V_{SS}; CAN: register 6: = 00H, register 7: = 12H, register 8: = 02H, register 0: = 20H, wait 15t_{CY}, register 1: = 10H, wait for bit Sleep = 1.
   b) The **analog** Idle and Sleep mode current measurement: Port 5 = AV_{DD}; load current reference voltage source 100 µA.
4. Window devices have to be covered. Conditions for:
   a) The **digital** Power-down mode supply current measurement: all output pins and Port 5 disconnected; Port 0 = P1.6 = P1.7 = $\overline{EW}$ = CRX0 = V_{DD}; $\overline{EA}$ = RST = STADC = CRX1 = XTAL1 = AV_{REF+} = AV_{REF-} = CV_{SS} = V_{SS}; AV_{DD} = V_{DD}, but current into AV_{DD} pin is not comprised in digital Power-down current.
   b) The **analog** Power-down mode supply current measurement: Port 5 = AV_{DD}.
5. Capacitive loads on Port 0 and Port 2 may degrade the LOW level output voltage of ALE, Port 1 and Port 3. During a HIGH-to-LOW transition on the Port 0 and Port 2 pins and a capacitive load >100 pF, the ALE LOW level may exceed 0.8 V. In the case that it is necessary to connect ALE to a Schmitt trigger input respectively use an address latch with a Schmitt trigger STROBE input.

6. Capacitive loads on Port 0 and Port 2 may cause a HIGH level voltage degradation of ALE and $\overline{PSEN}$ below $0.9V_{DD}$ during the address bits are stabilizing.
7. $t_{CY} = 12\ t_{CLK}$ is the machine cycle time.
8. $AV_{REF+} = 5.12$ V; $AV_{REF-} = 0$ V; $AV_{DD} = 5.0$ V.
9. The differential non-linearity (DL_e) is the difference between the actual step width and the ideal step width.
10. The ADC is monotonic, there are no missing codes.
11. The integral non-linearity (IL_e) is the peak difference between the centre of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset error.
12. The offset error (OS_e) is the absolute difference between the straight line which fits the actual transfer curve after removing gain error, and a straight line which fits the ideal transfer curve. The offset error is constant at every point of the actual transfer curve.
13. The gain error (G_e) is relative difference in percent between the straight line fitting the actual transfer curve after removing offset error and the straight line which fits the ideal transfer curve. The gain error is constant at every point on the transfer curve.
14. The absolute voltage error (A_e) is the maximum difference between the centre of the steps of the actual transfer curve of the not calibrated ADC and the ideal transfer curve.
15. Not tested during production.
16. Source current for the CTX0, CTX1 outputs together.
17. For the **P87C592V1** the input current is not tested, see Chapter 25 "P87C592 specification differences" (usage of the pin).



(1) Maximum Operating mode (I_{DD}); $V_{DD} = 5.5$ V
(2) Maximum Operating mode (I_{DD}); $V_{DD} = 4.5$ V
(3) Maximum Idle and Sleep mode ($I_{DD(IS)}$); $V_{DD} = 5.5$ V
(4) Maximum Idle and Sleep mode ($I_{DD(IS)}$); $V_{DD} = 4.5$ V

Fig.28 Supply current (I_{DD}) as a function of frequency at XTAL1 (f_{CLK}).



(1) Example of an actual transfer curve.
(2) The ideal transfer curve.
(3) Differential non-linearity (DL_e).
(4) Integral non-linearity (IL_e).
(5) Centre of a step of the actual transfer curve.

Fig.29 ADC conversion characteristic.

21 AC CHARACTERISTICS

See note 1 and 2; C_L = 100 pF for Port 0, ALE and $\overline{PSEN}$; C_L = 80 pF for all other outputs unless otherwise specified.

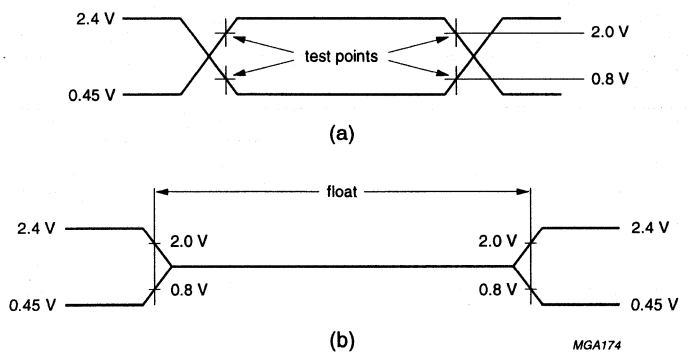
SYMBOL	PARAMETER	f_{CLK} = 16 MHz		f_{CLK} = 12 MHz		VARIABLE CLOCK 1.2 to 16 MHz		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
External Program Memory								
t_{LHLL}	ALE pulse width	85	–	127	–	$2t_{CLK} - 40$	–	ns
t_{AVLL}	address valid to ALE LOW	23	–	43	–	$t_{CLK} - 40$	–	ns
t_{LLAX}	address hold after ALE LOW	33	–	53	–	$t_{CLK} - 30$	–	ns
t_{LLIV}	ALE LOW to valid instruction in	–	150	–	233	–	$4t_{CLK} - 100$	ns
t_{LLPL}	ALE LOW to $\overline{PSEN}$ LOW	33	–	53	–	$t_{CLK} - 30$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	143	–	205	–	$3t_{CLK} - 45$	–	ns
t_{PLIV}	$\overline{PSEN}$ LOW to valid instruction in	–	83	–	145	–	$3t_{CLK} - 105$	ns
t_{PXIX}	input instruction hold after $\overline{PSEN}$	0	–	0	–	0	–	ns
t_{PXIZ}	input instruction float after $\overline{PSEN}$	–	38	–	59	–	$t_{CLK} - 25$	ns
t_{AVIV}	address to valid instruction in	–	208	–	312	–	$5t_{CLK} - 105$	ns
t_{PLAZ}	$\overline{PSEN}$ LOW to address float	–	10	–	10	–	10	ns
External data memory								
t_{RLRH}	$\overline{RD}$ pulse width	275	–	400	–	$6t_{CLK} - 100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	275	–	400	–	$6t_{CLK} - 100$	–	ns
t_{AVLL}	address valid to ALE LOW	8	–	28	–	$t_{CLK} - 55$	–	ns
t_{LLAX}	address hold after ALE LOW	33	–	53	–	$t_{CLK} - 30$	–	ns
t_{RLDV}	$\overline{RD}$ LOW to valid data in	–	148	–	252	–	$5t_{CLK} - 165$	ns
t_{RHDX}	data hold after $\overline{RD}$	0	–	0	–	0	–	ns
t_{RHDZ}	data float after $\overline{RD}$	–	55	–	97	–	$2t_{CLK} - 70$	ns
t_{LLDV}	ALE LOW to valid data in	–	350	–	517	–	$8t_{CLK} - 150$	ns
t_{AVDV}	address to valid data in	–	398	–	585	–	$9t_{CLK} - 165$	ns
t_{LLWL}	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW	138	238	200	300	$3t_{CLK} - 50$	$3t_{CLK} + 50$	ns
t_{AVWL}	address valid to $\overline{RD}$ or $\overline{WR}$ LOW	120	–	203	–	$4t_{CLK} - 130$	–	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	23	103	43	123	$t_{CLK} - 40$	$t_{CLK} + 40$	ns
t_{QVWX}	data valid to $\overline{WR}$ transition	13	–	33	–	$t_{CLK} - 50$	–	ns
t_{QVWH}	data valid time $\overline{WR}$ HIGH	288	–	433	–	$7t_{CLK} - 150$	–	ns
t_{WHQX}	data hold after $\overline{WR}$	13	–	33	–	$t_{CLK} - 50$	–	ns
t_{RLAZ}	$\overline{RD}$ LOW to address float	–	0	–	0	–	0	ns

Notes

1. For the AC Characteristics the following conditions are valid:
   a) **P8XC592 FFA (FHA)**: V_{DD} = 5 V ± 10%; T_{amb} = –40 to +85 °C (125 °C); f_{CLK} = 1.2 to 16 MHz.
   b) **P87C592 EFx**: V_{DD} = 5 V ± 10%; T_{amb} = –40 to +85 °C; f_{CLK} = 3.5 to 16 MHz.
2. $t_{CLK} = \frac{1}{f_{CLK}}$ = one oscillator clock period ; t_{CLK} = 62.5 ns at f_{CLK} = 16 MHz.

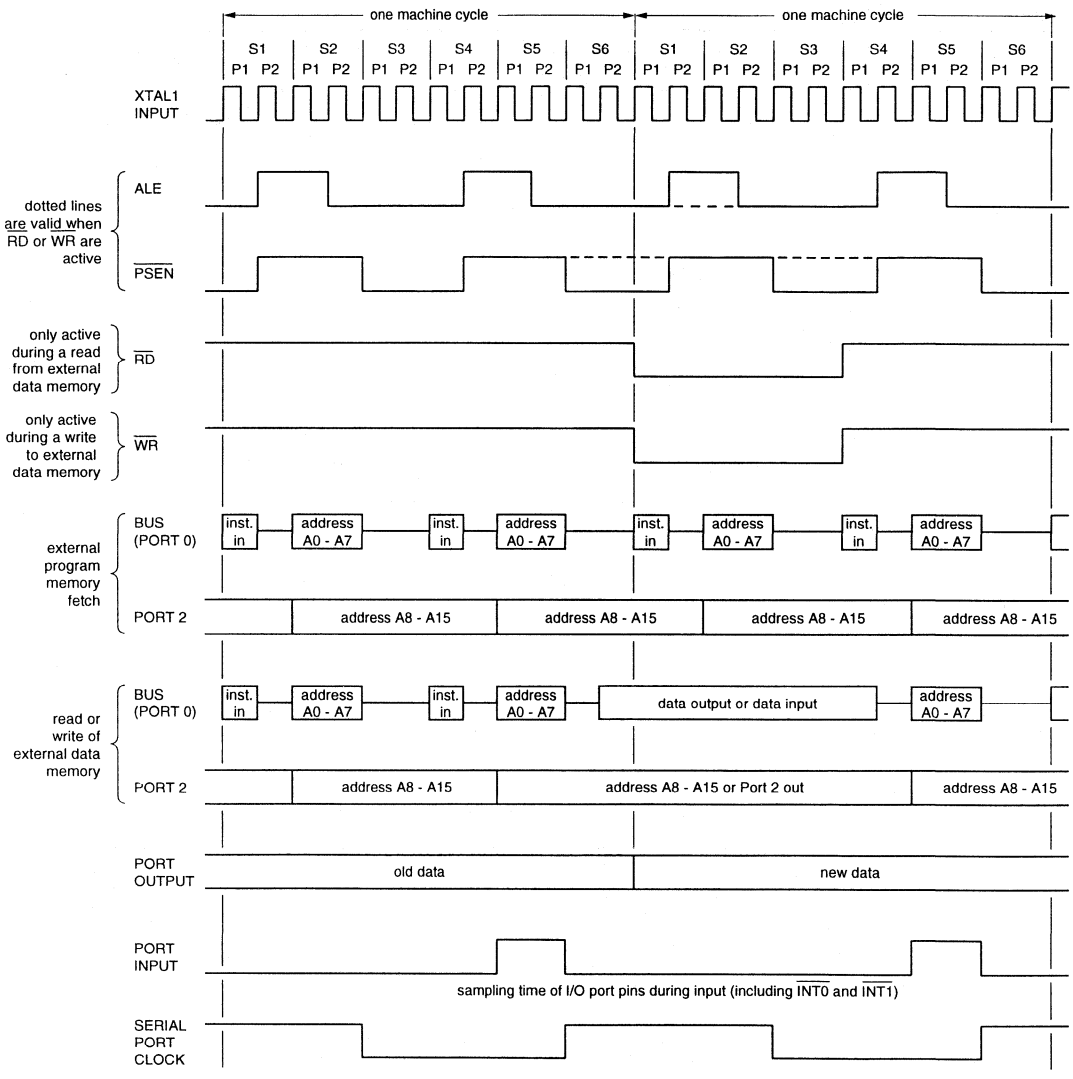
Table 90 CAN characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
CAN input comparator/output driver					
t_{sd}	sum of input and output delay	AV_{DD} = 5 V ± 5%; V_{DIF} = ± 32 mV; 1.4 V < V_I < AV_{DD} − 1.4 V	–	60	ns



AC testing inputs are driven at 2.4 V for a HIGH and 0.45 V for a LOW.
Timing measurements are taken at 2.0 V for a HIGH and 0.8 V for a LOW, see Fig.30 (a).
The float state is defined as the point at which a Port 0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels, see Fig.30 (b).

Fig.30 AC testing input, output waveform (a) and float waveform (b).



The Port 5 input buffers have a maximum propagation delay of 300 ns. As a result Port 5 sample time begins 300 ns before state S5 and ends when S5 has finished.

Fig.31 Instruction cycle timing.

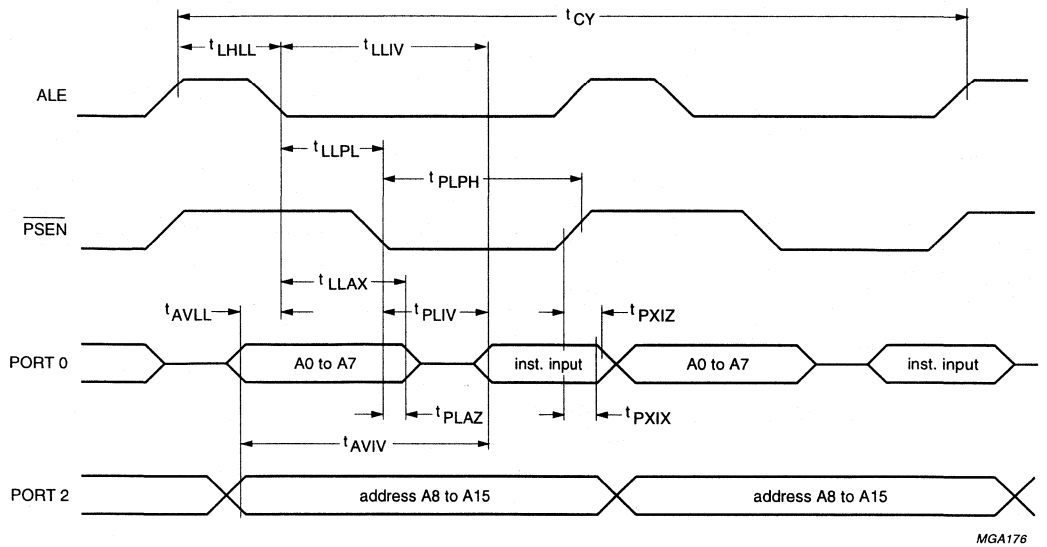


Fig.32 Read from external Program Memory.

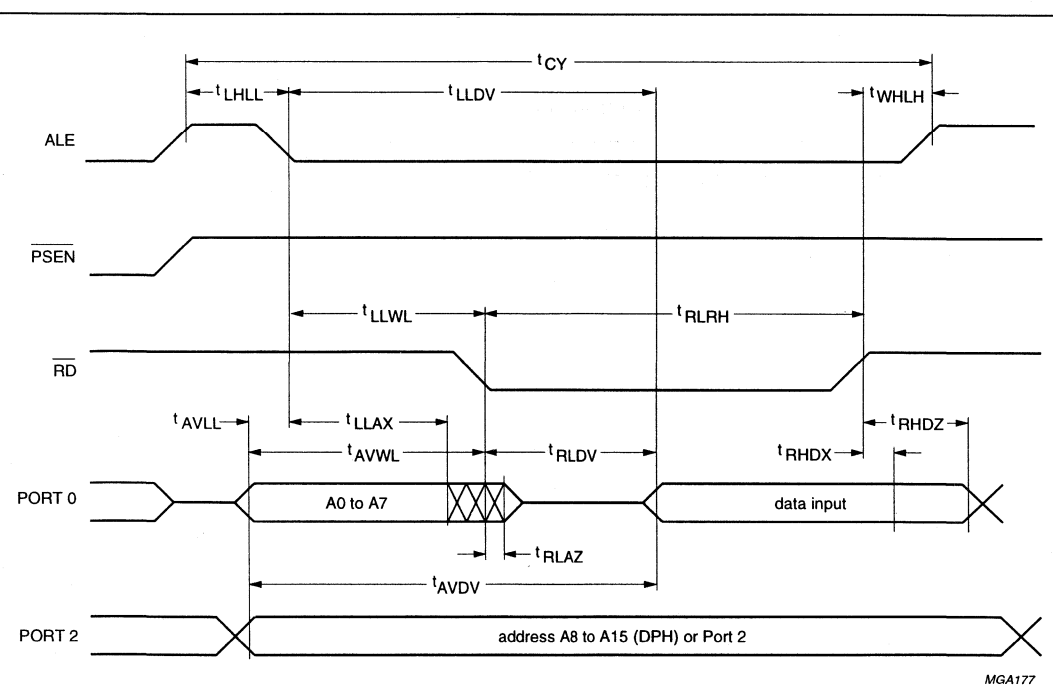


Fig.33 Read from external Data Memory.

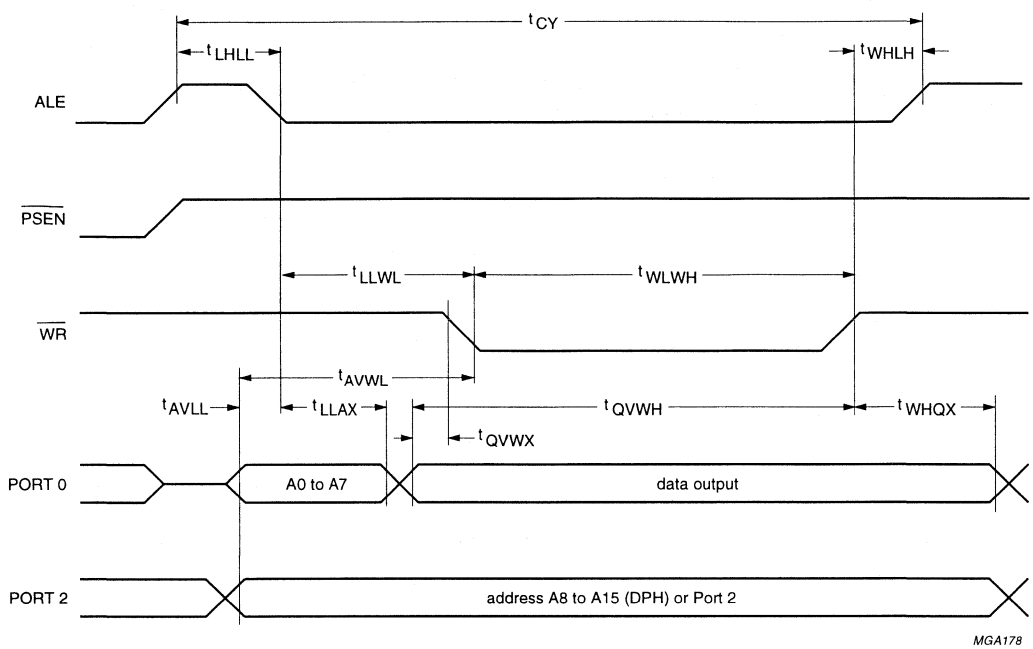


Fig.34 Write to external Data Memory.

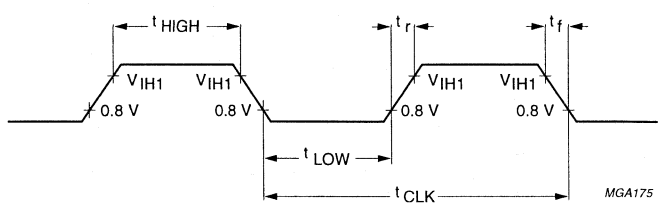


Fig.35 External clock drive XTAL1(see Table 91).

Table 91 External clock drive XTAL1

SYMBOL	PARAMETER	VARIABLE CLOCK (f_{CLK} = 1.2/3.5 to 16 MHz)		UNIT
		MIN.	MAX.	
t_{CLK}	oscillator clock period			
	P83C592	62.5	833.3	ns
	P87C592	62.5	285.7	ns
t_{HIGH}	HIGH time	20	$t_{CLK} - t_{LOW}$	ns
t_{LOW}	LOW time	20	$t_{CLK} - t_{HIGH}$	ns
t_r	rise time	–	20	ns
t_f	fall time	–	20	ns
t_{CY}	cycle time ($12 \times t_{CLK}$)	0.75	10	µs

Table 92 UART Timing in Shift Register Mode

SYMBOL	PARAMETER	f_{CLK}						UNIT
		16 MHz		12 MHz		VARIABLE CLOCK		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{XLXL}	Serial Port clock cycle timing	0.75	–	1.0	–	$12t_{CLK}$	–	ms
t_{QVXH}	output data setup to clock rising edge	492	–	700	–	$10t_{CLK} - 133$	–	ns
t_{XHQX}	output data hold after clock rising edge	8.0	–	50	–	$2t_{CLK} - 117$	–	ns
t_{XHDX}	input data hold after clock rising edge	0	–	0	–	0	–	ns
t_{XHDV}	clock rising edge to input data valid	–	492	–	700	–	$10t_{CLK} - 133$	ns

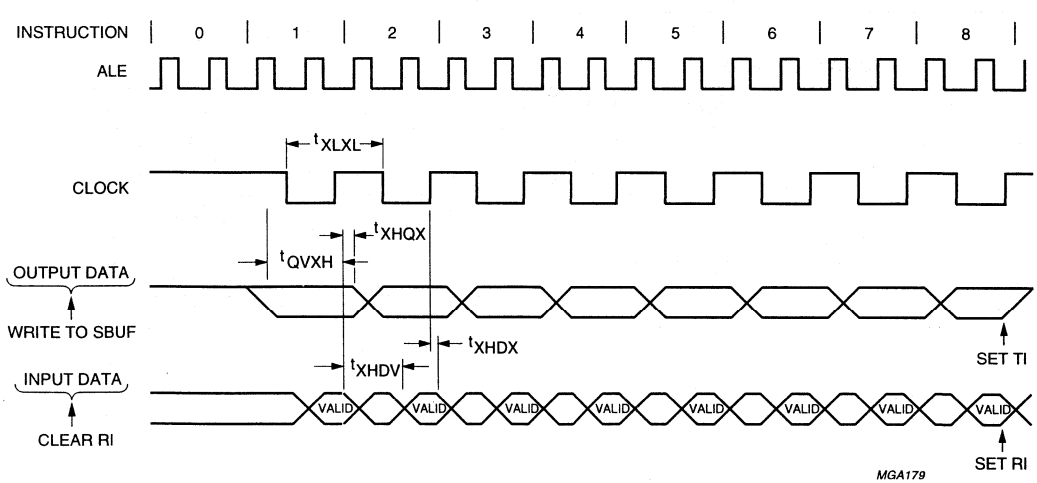


Fig.36 UART waveforms in Shift Register Mode.

22 EPROM CHARACTERISTICS

The P87C592 has an on-chip 16 kbytes EPROM for fast and flexible controller software development.
Two versions are available:

- A ceramic LCC package with a window for UV-erasure, P87C592 EFL
- A low-cost OTP-version in a PLCC package, which is not erasable, P87C592 EFA.

22.1 Programming and Verification

The P87C592 is programmed by using a modified Quick-Pulse Programming algorithm (Trademark algorithm of Intel Corporation).
In Table 94, the logic levels for reading the Signature bytes and for programming the Program Memory, the Encryption Table and the Lock bits are listed.

The circuit configuration and waveforms for programming are shown in the Figures 37 and 38. Fig.39 shows the circuit configuration for code data verification.
Note that programming and verification is carried out with an oscillator frequency of 4 to 6 MHz. The two Signature bytes identifying the device as an P87C592 manufactured by Philips are located as shown in Table 93.

Table 93 Programming and Verification

ADDRESS	CONTENT	MEANING
30H	15H	Philips
31H	9CH	P87C592

22.2 Security

For code protection the P87C592 has an Encryption table and two Lock bits. After programming the Encryption table from addresses 00H to 1FH, a verification sequence will present the data at Port 0 as a logical EXNOR of the program byte with one of the Encryption bytes. The Encryption table is not readable. The purpose of Lock bit 1 is to inhibit programming. It is impossible to fetch code bytes from the internal Program Memory with MOVC instructions executed from external memory. However, verification of the EPROM and programming of the second Lock bit is still possible. Lock bit 2 additionally disables verification of the program code. Note that for further security the $\overline{EA}$ input level of the P8XC592 is latched during Reset.

22.3 Erasure

A controlled erasure is done by exposing the EPROM window to an ultraviolet lamp of 12 $\mu W/cm^2$ for 20 to 39 minutes at a distance of about 2.5 cm.
The integrated dose of the ultraviolet light (2537 Å) must be at least 15 Ws/cm^2. Erasure leaves the array in an all 'logic 1' state.

To avoid inadvertent erasure of the EPROM in sunlight or fluorescent lighting it is recommended to cover the window with an opaque label.

Table 94 EPROM programming modes

MODE	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.7	P2.6	P3.7	P3.6
Read Signature	HIGH	LOW	HIGH	HIGH	LOW	LOW	LOW	LOW
Program code data	HIGH	LOW	LOW (note 1)	V_{PP} (note 2)	HIGH	LOW	HIGH	HIGH
Verify code data	HIGH	LOW	HIGH	HIGH	LOW	LOW	HIGH	HIGH
Program Encryption table	HIGH	LOW	LOW (note 1)	V_{PP} (note 2)	HIGH	LOW	HIGH	LOW
Program Lock bit 1	HIGH	LOW	LOW (note 1)	V_{PP} (note 2)	HIGH	HIGH	HIGH	HIGH
Program Lock bit 2	HIGH	LOW	LOW (note 1)	V_{PP} (note 2)	HIGH	HIGH	LOW	LOW

Notes

1. Each programming pulse is:
   a) LOW for 100 ± 10 µs.
   b) HIGH for at least 10 µs.
2. ALE/$\overline{PROG}$ receives 25 programming pulses while V_{PP} is held at 12.75 V ± 0.25 V.

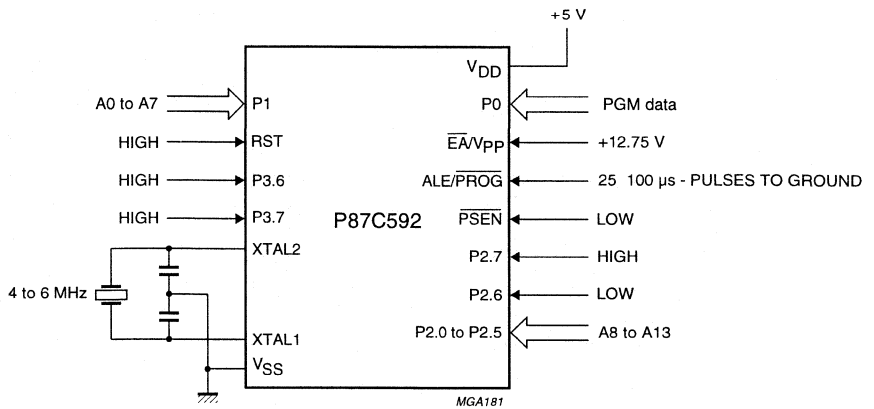


Fig.37 Programming configuration.

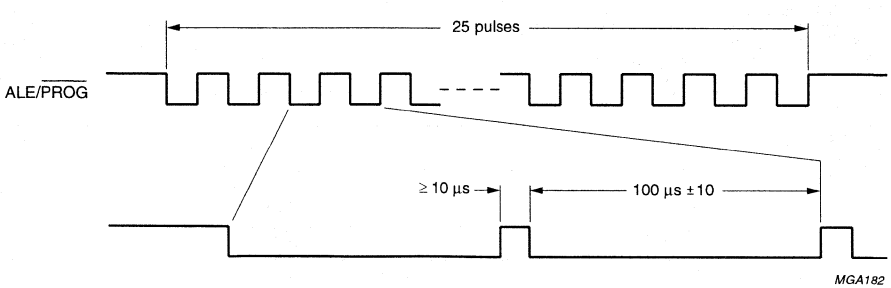


Fig.38 PROG waveform.

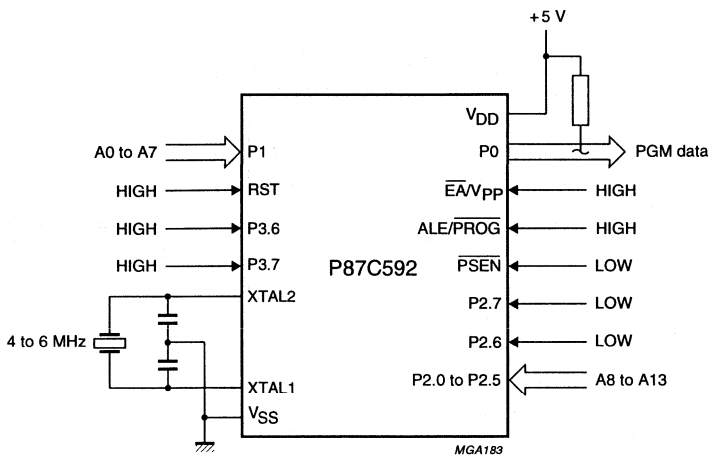
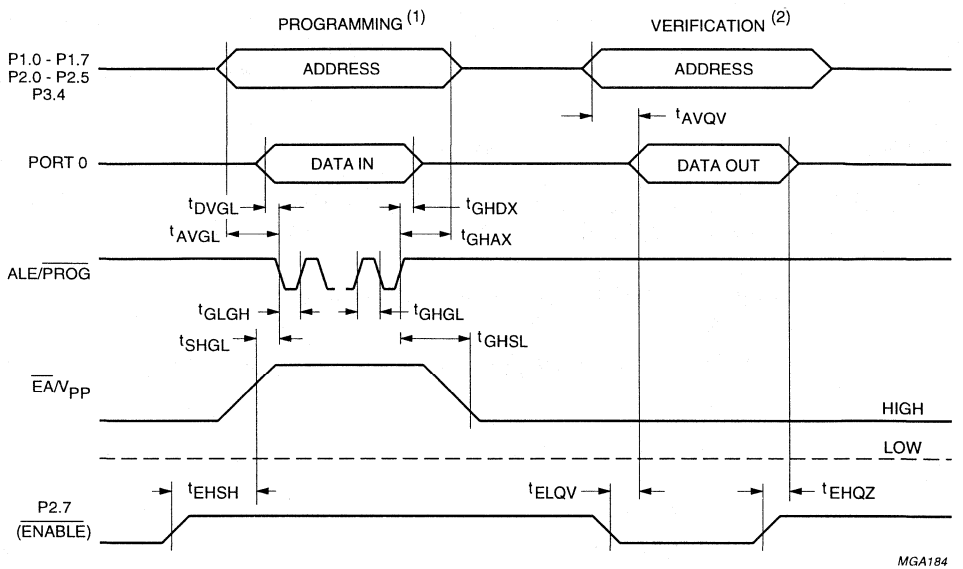


Fig.39 Program verification.

Table 95 EPROM programming and verification characteristics

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = 21 °C to 27 °C.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{PP}	programming supply voltage	12.5	13.0	V
I_{PP}	programming supply current	–	50	mA
f_{CLK}	oscillator frequency	4	6	MHz
t_{AVGL}	address set-up to $\overline{PROG}$ LOW	$48t_{CLK}$	–	
t_{GHAX}	address hold after $\overline{PROG}$ HIGH	$48t_{CLK}$	–	
t_{DVGL}	data set-up to $\overline{PROG}$ LOW	$48t_{CLK}$	–	
t_{GHDX}	data hold after $\overline{PROG}$ HIGH	$48t_{CLK}$	–	
t_{EHSH}	P2.7 ($\overline{ENABLE}$) HIGH to V_{pp}	$48t_{CLK}$	–	
t_{SHGL}	V_{pp} set-up to $\overline{PROG}$ LOW	10	–	µs
t_{GHSL}	V_{pp} hold after $\overline{PROG}$ HIGH	10	–	µs
t_{GLGH}	$\overline{PROG}$ pulse width	90	110	µs
t_{AVQV}	address to data valid	–	$48t_{CLK}$	
t_{ELQV}	P2.7 ($\overline{ENABLE}$) LOW to data valid	–	$48t_{CLK}$	
t_{EHQZ}	data float after P2.7 ($\overline{ENABLE}$) HIGH	0	$48t_{CLK}$	
t_{GHGL}	$\overline{PROG}$ HIGH to $\overline{PROG}$ LOW	10	–	µs



(1) For programming see Fig.37.
(2) For verification conditions see Fig.39.

Fig.40 EPROM Programming and Verification.

23 CAN APPLICATION INFORMATION

23.1 Latency time requirements

Real-time applications require the ability to process and transfer information in a limited and predetermined period of time. If knowing this total time and the time required to process the information, the (maximum allowed) transfer delay time is given.

It is measured from the initiation of the transfer up to the signalling of reception.
For instance, this is the period of time between programming the CAN Command Register bit 0 (Transmission Request) to HIGH and the time getting an interrupt at a receiving CAN-device (due to the reception of the respective message).

23.1.1 MAXIMUM ALLOWED BIT-TIME CALCULATION

The maximum allowed bit-time (t_{BIT}) due to latency time requirements can be calculated as:

$$t_{BIT} \leq \frac{t_{MAX\ TRANSFER\ TIME}}{(n_{BIT,\ MAX\ LATENCY} + n_{BIT,\ MESSAGE})} \quad (1)$$

Where:

- $t_{MAX\ TRANSFER\ TIME}$:
  the maximum allowed transfer delay time (application-specific).
- $n_{BIT,\ MAX\ LATENCY}$:
  the maximum latency time (in terms of number of bits), which depends on the actual state of the CAN network (e.g. another message already on the network);
- $n_{BIT,\ MESSAGE}$:
  the number of bits of a message; it varies with the number of transferred data bytes $n_{DATA\ BYTES}$ (0..8) and Stuffbits like:

$$44 + 8.n_{DATA\ BYTES} \leq n_{BIT,\ MESSAGE} \leq 52 + 10.n_{DATABYTES} \quad (2)$$

Example:

For the calculation of $n_{BIT,\ MAX\ LATENCY}$ the following is assumed (the term 'our message' refers to that one the latency time is calculated for):

- since at maximum one-bit-time ago another CAN-controller is transmitting.
- a single error occurs during the transmission of that message preceding ours, leading to the additional transfer of one Error Frame
- 'our message' has the highest priority,

giving:

$$n_{BIT,\ MAX\ LATENCY} \geq 44 + 8.n_{DATA\ BYTES,\ WORST\ CASE} + 18 \quad (3)$$

$$n_{BIT,\ MAX\ LATENCY} \leq 52 + 10.n_{DATA\ BYTES,\ WORST\ CASE} + 18 \quad (4)$$

Where:

- The additional 18 bits are due to the Error Frame and the Intermission Field preceding 'our message'.
- $n_{DATA\ BYTES,\ WORST\ CASE}$ denotes the number of data bytes contained by the longest message being used in a given CAN network.

23.1.2 CALCULATING THE MAXIMUM BIT-TIME

Table 96 Example for calculating the maximum bit-time

STATEMENT	COMMENTS
$t_{MAX\ TRANSFER\ TIME} = 10$ ms	assumption
$n_{DATA\ BYTES,\ WORST\ CASE} = 6$	longest message in that network; assumption
$n_{DATA\ BYTES} = 4$	'our message'; assumption
$n_{BIT\ MAX\ LATENCY} \leq 130$	using Equation (3) and (4)
$n_{MESSAGE} \leq 92$	using Equation (2)
$t_{BIT} \leq \frac{10\ ms}{(130 + 92)} = 0.045$ ms $= 45\ \mu s$	using Equation (1)

23.2 Connecting a P8XC592 to a bus line (physical layer)

23.2.1 On-Chip Transceiver

The P8XC592 features an on-chip differential transceiver including output driver and input comparator both being configurable (see Fig.41). Therefore it supports many types of common transmission media such as:

- Single-wire bus line
- Two-wire bus line (differential)
- Optical cable bus line.

The P8XC592 can directly drive a differential bus line. An example is given in Fig.42 for a bus line having a characteristic impedance of 120 Ω. Direct interfacing to the bus line is well suited for applications with limited requirements concerning electromagnetic susceptibility, wiring failure tolerance and protection against transients.

23.2.2 Transceiver for In-vehicle Communication

Fig.43 shows a versatile transceiver implementation designed for automotive applications. It features a bit rate of up to 1 Mbit/s and dissipates low power during standby (1.4 mA). Thus it is suitable also for applications requiring a Sleep mode function with system activation via the bus line. The transceiver provides and extended common mode range for high electromagnetic susceptibility performance.

Two external driver transistors amplify the output current to 35 mA typically and provide protection against overvoltage conditions on the bus line (e.g. due to an accidental short-circuit between a bus wire and battery voltage). The serial diodes prevent in combination with the transistors the bus from being blocked in case of a bus not powered. More than 32 nodes may be connected to the bus line.

23.2.3 Detection and Handling of Bus Wiring Failures

Using the P8XC592 a superior wiring failure tolerance and detection performance can be achieved. This requires both bus lines to be mutually decoupled as shown in Fig.44. Each bus wire is based separately to a reference voltage of $\frac{1}{2}AV_{DD}$.

The diodes suppress reverse current in case of a termination circuit being not properly powered or a bus line being short i.e. to a voltage higher than 5 V. Applying this bus termination circuit the following wiring failures on the bus are detectable and can be handled:

- Interruption of one bus wire at any location.
- Short-circuit of one bus wire to ground or battery voltage.
- Short-circuit between the bus wires.

A bus failure can be detected e.g. by a drop out of a status message, regularly being transmitted on the bus. If a bus wire is corrupted the following actions have to be taken:

- Switch the corresponding comparator input over to a reference voltage of $\frac{1}{2}AV_{DD}$.
- Disable the corresponding output driver stage.

As a consequence communication will continue on that bus wire not being corrupted. The required reference voltage and the switches for the comparator inputs are provided on-chip. An output driver stage can be disabled by reconfiguration of the on-chip output driver (reprogramming of the Output Control Register of the P8XC592; see Section 13.5.11, Table 51). To find out which of the bus wires is corrupted a heuristic method is applied.

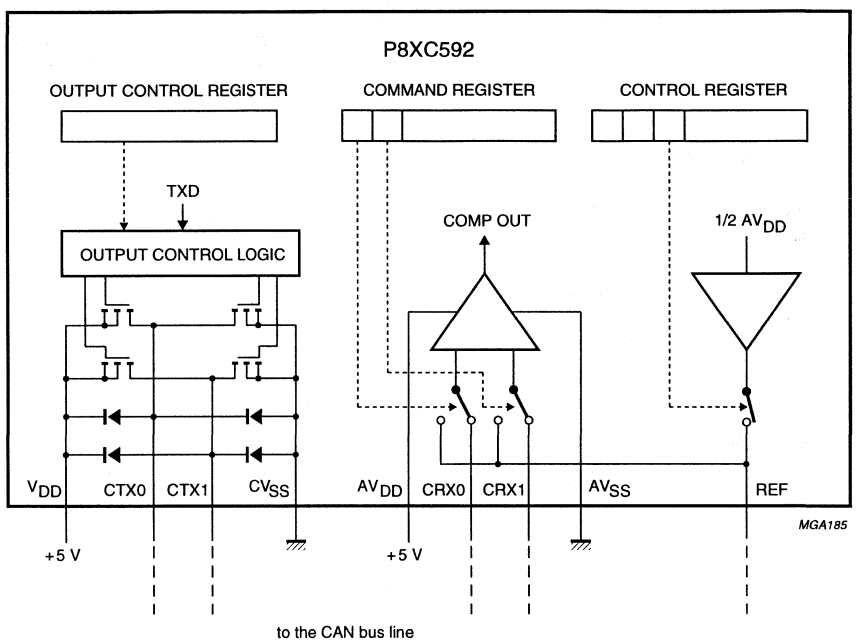


Fig.41 Structure of on-chip CAN-Transceiver.

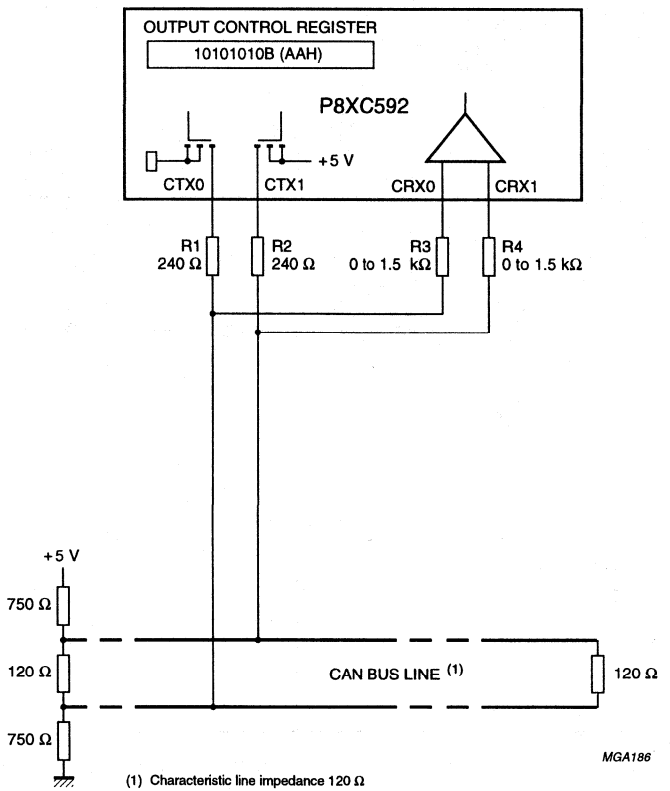


Fig.42 Direct interface to a two-wire differential bus.

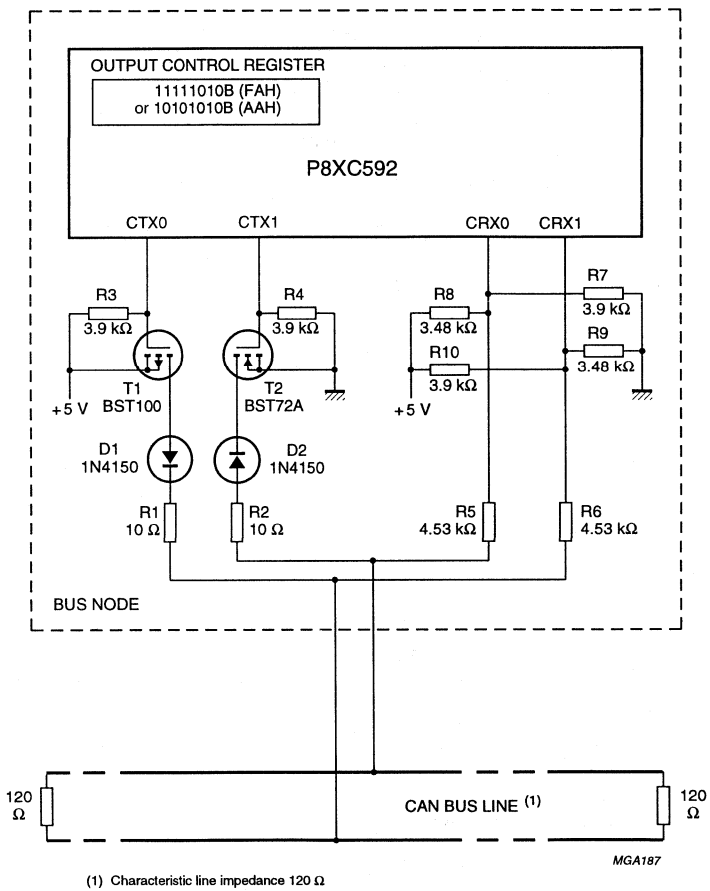


Fig.43 In-vehicle Transceiver.

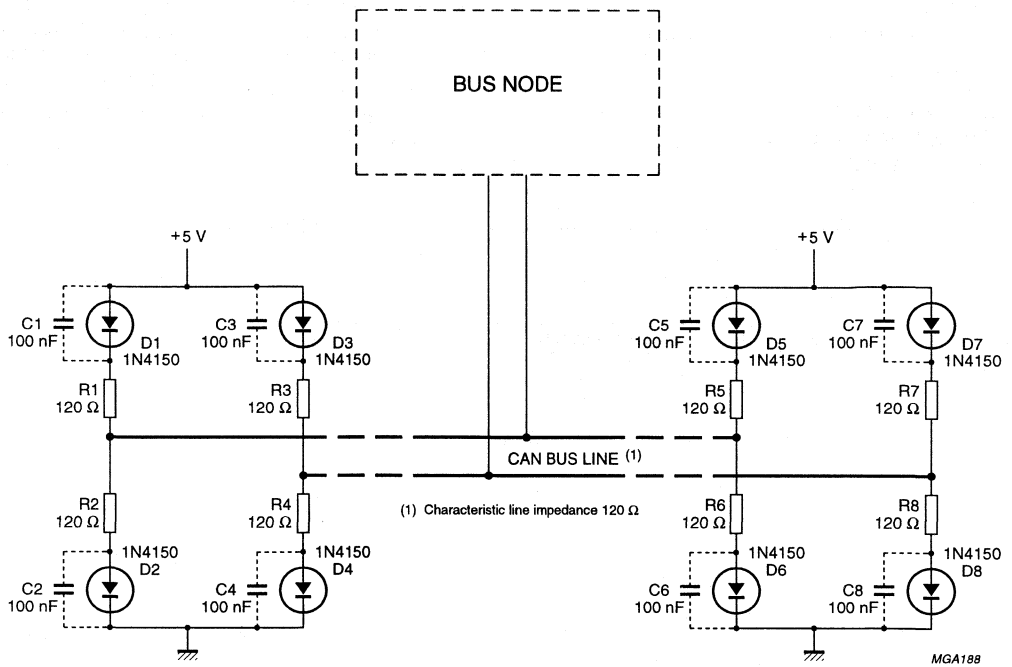


Fig.44 Bus termination with decoupled wires.

23.2.4 Connection to an Optical Bus Line

Using an optical medium provides the following advantages:

- Bus nodes are galvanically decoupled.
- Optical cable features very high noise immunity.
- No noise emission by the bus cable.

An example for an interface to an optical connector is given in Fig.45. In most cases a transistor is required to amplify the TX-output current.

Thus more optical power is provided to compensate for losses in the optical connectors and the optical star. The P8XC592 features an on-chip $\frac{1}{2}AV_{DD}$ reference voltage output so only a capacitor is required for the receiver part. Two optical fibres are used to connect the bus nodes. The TX-fibre transfers the output signal of the CAN-controller to the optical star. The optical star transfers the TX-fibre input signal over to all the RX-fibres. The RX-fibres transfer the resulting optical signal over to the receivers of all the bus nodes.

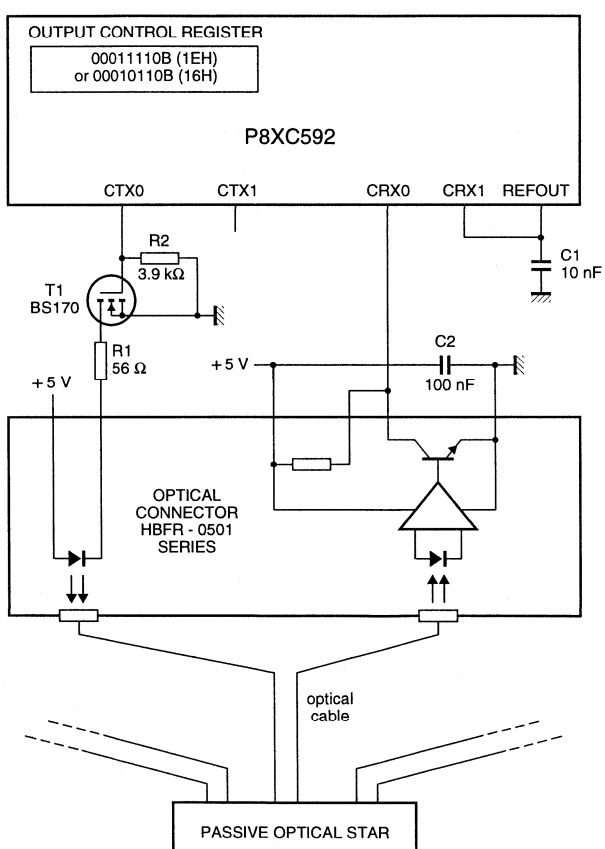


Fig.45 Optical Transceiver.

23.2.5 P8XC592 CAN INTERRUPT HANDLER SOFTWARE EXAMPLE (INCLUDING FAST DMA TRANSFER).

MCS-51 MACRO ASSEMBLER P8XC592 CAN interrupt-handler

```
LOC  OBJ   LINE  SOURCE

           1     $TITLE (8xC592 CAN interrupt-handler)
00A0       2     $NOSYMBOLS NOPAGING
00A1       3
           4     ;*******************************************************************************************************
           5     ;
           6     ;Very fast receive-routine for the 8xC592. It:
           7     • is embedded in the interrupt-handler for the CAN-controller,
           8     • uses the DMA-logic and
           9     • handles up to eight different messages
00A2       10    ;(if these have the same leading 8 identifier-bits).
           11    ;
           12    ;To allow for faster receive-routine, it is assumed that all other routines
           13    ;accessing the CAN-controller, disable the interrupt of the CAN-controller
           14    ;(IEN0.5) during their execution.
00A5       15    ;
00A7       16    ;Version:    1.0
           17    ;Date:       12-April-90
           18    ;Author:     Bernhard Reckels
           19    ;at:         Philips Components Application Lab., Hamburg (PCALH)
00A9       20
00AB       21    ;*******************************************************************************************************
00AD       22
           23    ;*******************************************************************************************************
           24    ;initial stuff
           25    ;*******************************************************************************************************
           26
           27    ;equatas
           28
           29              ;addresses of Special Function Registers
00AE       30              CANADR      EQU     0DBH
00AF       31              CANDAT      EQU     0DAH
           32              CANCON      EQU     0D9H
00B0       33              CANSTA      EQU     0D8H
           34
```

```
LOC    OBJ      LINE  SOURCE
                   35          ;commands for the CAN-controller / DMA logic
                   36          CAN_REF_REL     EQU     00000100B   ;Release Receive Buffer
00A0               37          CAN_RX_DMA      EQU     80H + 22    ;Rx DMA-transfer
00A1               38
                   39          ; addresses of CAN-controller internal registers
                   40          CAN_REF         EQU     20          ;1st address of Rx-buffer
                   41
                   42          ; masks
                   43          INT_FLAG_MASK   EQU     00011111B   ;all CAN's interrupt-flags
                   44          ID2_0_MASK      EQU     11100000B   ;only ID.2 ... ID.0 bits
00A2               45      ; jump-address for a CAN-controller interrupt
                   46
                   47
                   48      CSEG at 2BH
         020080    49          LJMP            CAN_INT_HANDLER     ; CAN's interrupt-vector
00A5               50
00A7               51      ; data storage
                   52
                   53      DSEG at 20H
                   54          CAN_INT_IMAGE:  DS      1
00A9               55
00AB               56      BSEG at 00H
00AD               57          CAN_INT_RX:     DBIT    1           ; = CAN_INT_IMAGE.0
                   58          CAN_INT_TX:     DBIT    1           ; = CAN_INT_IMAGE.1
                   59          CAN_INT_KR:     DBIT    1           ; = CAN_INT_IMAGE.2
                   60          CAN_INT_OV:     DBIT    1           ; = CAN_INT_IMAGE.3
                   61          CAN_INT_WK:     DBIT    1           ; = CAN_INT_IMAGE.4
                   62
                   63      ;*******************************************************************************************************
                   64      ;CAN-controller interrupt-handler
00AE               65      ;
00AF               66      ;Only the receive-interrupt is coded.
                   67      ;
00B0               68      ;*******************************************************************************************************
                   69
                   70      CSEG at 080H
                   71
```

```
LOC  OBJ     LINE  SOURCE
00A0         72    CAN_INT_HANDLER:
00A1         73
             74            ; first save used registers
     C0D0    75            PUSH    PSW
     C0E0    76            PUSH    ACC
             77
             78            ; store the CAN-controller's Interrupt Register contents
             79            ; (here: at a bit-addressable location).
00A2         80            ; This is necessary because after reading the Interrupt Register
             81            ; its contents is cleared, but – on the other hand – several flags
             82            ; may be set in coincidence.
     E5D9    83            MOV     A, CANON
     541F    84            ANL     A, #INT_FLAG_MASK      ; only interrupt-flags
00A5 F520    85            MOV     CAN_INT_IMAGE, A
00A7         86
             87
             88    ;dispatcher----------------------------------------------------------------------------------------
             89    INT_TEST0:
00A9 100000  90            JBC     CAN_INT_RX,CAN_RX_SERV      ;receive-interrupt?
00AB         91
00AD         92    INT_TEST1:
             93            ; here the dispatcher has to be completed according
             94            ; to the application-specific requirements
             95            ; ...
             96            ; ...
             97    ; end of dispatcher--------------------------------------------------------------------------------
             98
             99    ;Rx-serve------------------------------------------------------------------------------------------
00AE         100   ; copy message (Data-Field only) from CAN- to CPU memory
00AF         101
             102   CAN_RX_SERVE
00B0         103           ; read 2nd Descriptor-Byte from the Rx-Buffer (address 21)
     75DB15  104           MOV     CANADR, #CAN_REF + 1
     E5DA    105           MOV     A, CANDAT
             106
```

```
LOC   OBJ      LINE  SOURCE
00A0           107          ; determine the destination address in data-memory for the
00A1           108          ; message's Data-Field
      54E0     109          ANL     A, #ID2_0_MASK      ; use ID.2 ... ID.0 only
      C4       110          SWAP    A
      03       111          RR      A                   ; A = 4*ID.2 + 2*ID.1 + ID.0
               112          ; this value is used as an index for an array of 8 bytes
               113          ; containing the destination-addresses for the 8 different
               114          ; messages. Note, that the #RX_ARRAY_OFFSET is due to the
00A2           115          ; program counter-relative access to the array.
      2415     116          ADD     A, #RX_ARRAY_START - RX_ARRAY_OFFSET
      83       117          MOVC    A, @A + PC
               118          RX_ARRAY_OFFSET:
               119
00A5           120          ; if a message passes the acceptance-filter of the CAN
00A7           121          ; Controller, but the CPU doesn't need it, the array
               122          ; entry's value may be set to zero indicating this.
               123          ; The following <jz> instruction cares for this.
      6007     124          JZ      CAN_RX_READY
00A9           125
00AB           126          ; now copy the Data-Field (only) from CAN- to CPU memory
00AD           127          ; with the aid of the DMA-logic. Note, that a TX-DMA is
               128          ; performed when writing 8AH (DMA + address 10) into CANADR
               129          ; and a RX-DMA is performed when writing 94H (DMA + address 20)
               130          ; ... 9DH (DMA + address 29) into CANADR. Here address 22 is
               131          ; used to copy just the Data-Field.
      F5D8     132          MOV     CANSTA, A           ; data-memory address
      75DB96   133          MOV     CANADR, #CAN_RX_DMA ; starts RX-DMA at address 22
               134
00AE           135          ; the DMA-transfer is done in at maximum 2 instruction cycles.
00AF           136          ; During the transfer, neither the data-memory (RAM) nor one
               137          ; of the SFRs CANADR, CANDAT, CANCON and
00B0           138          ; CANSTA may be accessed by the CPU.
               139          ; For simplicity, two NOPs are used here.
      00       140          NOP
      00       141          NOP
00A0           142
```

```
LOC  OBJ     LINE  SOURCE
00A1         143           ; after reading the Rx-Buffer it must be released back to
             144           ; the CAN-controller. In coincidence, the Clear Overrun bit
             145           ; (CANCON.3) may be set, regardless of an existing or
             146           ; non-existing data overrun.
             147   CAN_RX_READY:
     75D904  148           MOV         CANCON, #CAN_RBF_REL
             149
00A2         150           ; if no other interrupt-flag is set, the interrupt-handler
             151           ; for the CAN-controller can be left. Otherwise further
             152           ; services are required.
     E520    153           MOV         A, CAN_INT_IMAGE
     70E4    154           JNZ         INT_TEST1
00A5         155
00A7         156           ; no other service is required, so the interrupt-handler
             157           ; is left.
     D0E0    158           POP         ACC
     D0D0    159           POP         PSW
00A9 32      160           RETI
00AB         161   ; end of Rx-serve----------------------------------------------------------------------------------
00AD         162
             163           ; here the array follows containing 8 destination-addresses
             164           ; for up to 8 different messages to be received. The values
             165           ; are fully application-specific (the values below show an
             166           ; example only).
             167   RX_ARRAY_START:
     E0      168           DB          0E0H    ; Rx-message #0
     00      169           DB          000H    ; this message is not used
00AE         170           ; ...
00AF FA      171           DB          0FAH    ; RX-message #7, containing 6 data bytes
             172
00B0         173           END

REGISTER BANK(S) USED: 0

ASSEMBLY COMPLETE, NO ERRORS FOUND
```

24 EPROM/OTP DEVELOPMENT SUPPORT

For sophisticated real-time in-circuit emulation, evaluation purposes and programming of the EPROM/OTP version, tools are available as described in the following sections.

24.1 In-circuit Emulation

24.1.1 PHILIPS SEMICONDUCTORS DEVELOPMENT SUPPORT TOOLS

TYPE	TYPE NUMBER FOR ORDERING
Hardware Tools	
SDS 80C51 real-time emulator	OM4120S
8xC592 probe	OM4110 (universal probe base) + OM4112 (emulation head for P8XC592)
Software Tools	
80C51 cross-assembler & PL/M-Compiler package for MS/DOS	OM4144
80C51 cross-assembler & C-Compiler package for MS/DOS	OM4285
CROSS VIEW debugger for MS/DOS-WINDOWS (for SDS 80C51)	OM4286

24.1.2 THIRD-PARTY VENDORS DEVELOPMENT SUPPORT TOOLS

In addition to the tools provided by Philips, the 8xC592 is also supported by several third party development tool vendors. For a more complete list and additional information:

- Contact your local Philips office for actual and detailed Development Support Tools offers from third-party vendors
- See *"Data Handbook IC20", Development Support Tools"*.
- See Philips brochure *"Microcontrollers and Microprocessors for embedded control applications"* ordering code 9398 374 90011.

24.2 Evaluation

For evaluation and simulation (especially for the CAN interface) purposes the following tools are available.

24.2.1 Philips Semiconductors Evaluation Support Tools; P8XC592 evaluation board

For evaluation of the P8XC592 microcontrollers's CAN-bus interface, Philips Semiconductors offers the OM4239 board. It is a low-cost prototyping board providing powerful monitor functions for interactive development of programs for full access to the CAN-bus.

24.2.1.1 Targets

- Ready to use on-board demonstration application.
- Aid user in understanding CAN and P8XC592.
- Support rapid proto-typing of specific applications.

24.2.1.2 Features

Major features of the OM4239 include:

- Evaluation of the P8XC592 microcontroller's CAN interface.
- Full support of the CAN communication utilities:
  - Demonstration and monitor software for the CAN-bus system supports CAN communication of up to 1 Mbit/s
  - Interactive configuration of the CAN-controller
  - CAN physical layer circuitry for balanced bus wires
  - Detachable LED display.
- Interactive software development with up/down-loading of user-specific hex files.
- On-board monitor software (EPROM).
- RS232C interface for connection to a PC, a terminal such as a VT100 or a workstation with terminal emulation.
- Wire-wrap area for prototyping, an application interface and two-wire CAN-bus connector
- Supply voltage: 7.5 to 18 V.
- Dimensions: 100 × 160 mm.
- P87C592 microcontroller:
  - 48 kbytes EPROM (16 kbytes on-chip, 32 kbytes external)
  - 2 × 256 bytes on-chip RAM; 32 kbytes external SRAM.
- Off-chip transceiver circuit designed to meet ISO/TC22/SC3/N608E (high-speed) with two selectable options:
  - Option 1: very low standby power consumption.
  - Option 2: support of single wire communication to recover from wiring failures.
- Power-down mode:
  - Small power consumption
  - Wake-Up via CAN-bus possible.

24.2.2 I+ME CAN Evaluation Design Tools

CAN Evaluation design tools offered by I+ME (Philips subcontractor):

- CAN/Net Sim
- CAN/Net Emu
- CAN/Net Ana.

Based on a PC System (Board + Monitor) a standard PC can be confirmed as a complete mode in CAN network.

For further information contact:

I+ME GmbH

Germany

Phone: +49-5331-72066

Fax: +49-5331-32455

For a detailed Development Support Tools list, please refer to *"Data Handbook IC20, Development Support Tools"*.

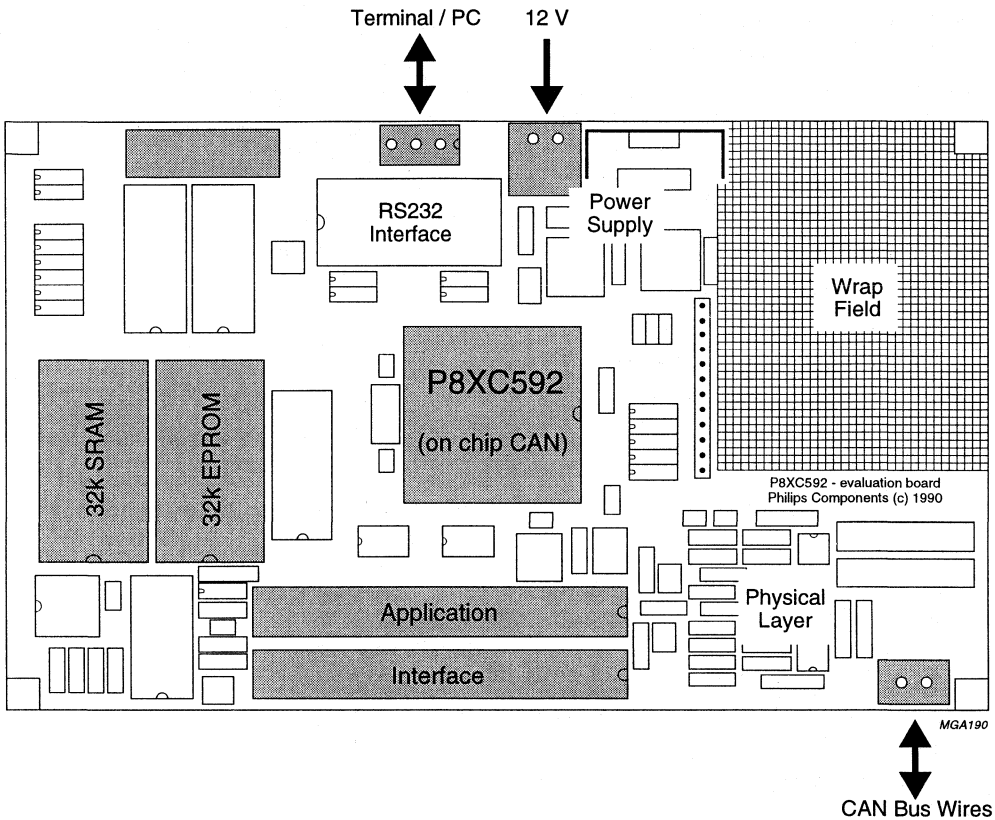


Fig.46 Top view of the P8XC592 Evaluation Board.

25 P87C592 SPECIFICATION DIFFERENCES

25.1 Control Register (CR)

The bit Reference Active (CR.5) is not provided in the P87C592V1. When reading this bit a HIGH is returned. This means it is not possible to set the input function of pin REF. The solution for using this pin is described in the following section.

25.2 Solution

In the case that the REF pin (pin 55) shall be used in the application for tolerating physical bus errors (opens and shorts of the bus wires) a simple external circuit has to be connected to it as illustrated in Fig.47.

Table 97 Components and characteristics for the solution
Supply voltage range 4.5 V to 5.5 V.

MODE	COMPONENTS (see Fig.47)			CHARACTERISTICS[2]		
	R1	C1	IC1[1]	I_R (typ.)	I_O	
					source	sink
High-Speed Transceiver	1 kΩ	–	• LM285Z-2.5 (–40 °C ... +85 °C; 1.5%)	2.5 mA	–1.9 mA	5 mA
Low-Speed Transceiver	16 kΩ	1 nF	• LM382BZ-2.5 (0 °C ... +70 °C; 1.5%) • KM385Z-2.5 (0 °C ... +70 °C; 3%)	160 µA	–70 µA	5 mA

Notes

1. Precise voltage regulation:
   a) ±3.4% LM285Z (over temperature).
   b) ±2.6% LM385BZ (over temperature).
2. The input current into the REF pin is negligible.

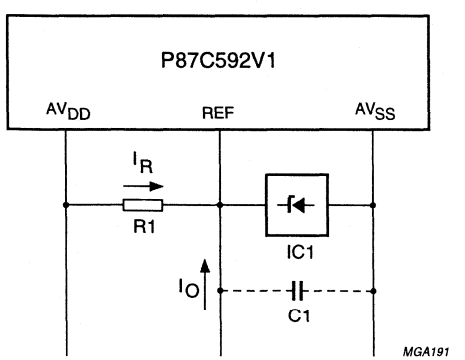


Fig.47 Application hint for 2.5 V reference voltage.

P8xC592 microcontroller with CAN interface

Application report HKI/AN 91 014

Summary:

The integrated circuit P8xC592 from Philips is a single-chip high performance microcontroller designed for use in automotive and general industrial applications. It is a high-end derivative of the 80C51 family CMOS microcontrollers.

In addition to the 80C51 standard features the P8xC592 provides a number of dedicated hardware features for sophisticated control applications. It includes timers, A/D converter, PWM output, UART and a CAN protocol controller (CAN = Controller Area Network) for serial communication.

The P8xC592 covers the complete CAN specification, offering important features such as multi-master serial communication capability with a high number of participating network nodes, programmable data transmission rate up to 1 Mbit/s and powerful error handling.

This technical publication puts special emphasis on CAN applications of the P8xC592. The application note provides a simple circuit example for a CAN module built with a P8xC592. Furthermore flowcharts are discussed to let the reader become familiar with the software aspects of CAN communication. A practical example shows that there is very little CPU load for the control of CAN communication.

P8xC592 microcontroller with CAN interface

Application report
HKI/AN 91 014

Table of Contents:

1. Introduction

CAN (Controller Area Network) is an advanced serial communication protocol, which efficiently supports distributed real-time control with a very high safety level. CAN allows the flexible configuration of networks with different types of microprocessors and microcontrollers. Typical applications of CAN-based networks can be found in automotive and industrial environment:

- o Automotive Systems:
  - multiplex wiring (< 125kbit/s)
  - engine control, ABS etc. (up to 1 Mbit/s)
- o Industrial Systems:
  - field bus applications
  - robotics, numeric machine control

Fig.1 shows a schematic network using the P8xC592 for distributed control applications. The kernel of each module is a Module Controller (CPU) that communicates via the Bus Controller (i.e. CAN controller) with the other modules. CPU and CAN controller can also be implemented on the very same chip, as it is in the P8xC592.

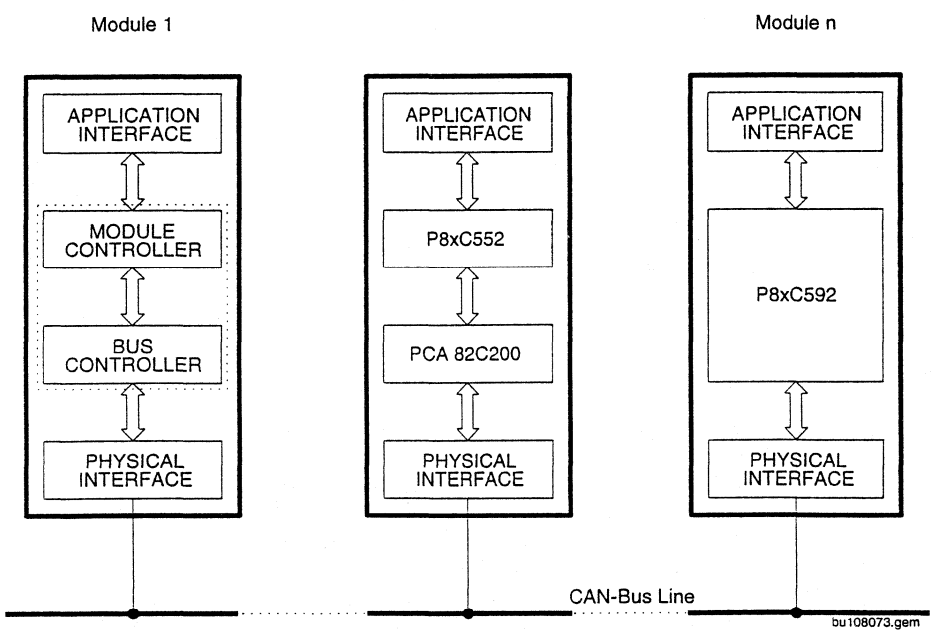


Fig. 1 Example of a "Controller Area Network"

The P8xC592 is a stand-alone high performance microcontroller designed for use in automotive and general industrial applications. In addition to the 80C51 standard features this device provides a number of dedicated hardware functions for these applications. It basically combines the functions of the well-known P8xC552 microcontroller [9] (without I^2C hardware) and the PCA 82C200 (Philips Stand-alone CAN-controller [3]), with some enhanced features.

The CAN-part of the P8xC592 fulfills the complete CAN specification, to provide the following important features:

- o multi-master operation in a serial communication network with an unlimited number of active network nodes,
- o programmable data transmission rate, up to 1 Mbit/s,
- o very low probability of undetected errors, due to powerful error handling,
- o 40 m maximum distance between two bus nodes at a data transmission rate of 1 Mbit/s, lower transmission rates allow even longer distances,
- o guaranteed latency time supporting real-time applications.

This Application Note covers the CAN related items of P8xC592 applications. It describes a simple circuit example for a module in a CAN network. To apply and understand the application examples given in this document, the reader should be familiar with the Philips P8xC592 data sheet [2].

2. P8xC592 Features

Fig.2 shows the block diagram of the P83C592 (ROM) or the P87C592 (EPROM) versions. There is also a ROM-less version labeled P80C592 without on-chip program memory. Except the three blocks "CAN controller", "DMA" and "256 Bytes Aux. RAM", the blocks shown are not different from those which are present in other 80C51 derivatives like in the well-known Philips **P8xC552**. The use of the CPU, the memory access modes, the timers, A/D converter and PWM outputs have already been described in detail in the User Manual for the P8xC552 [9], which shall not be repeated in this application note again. Please refer to that document for information about these topics.

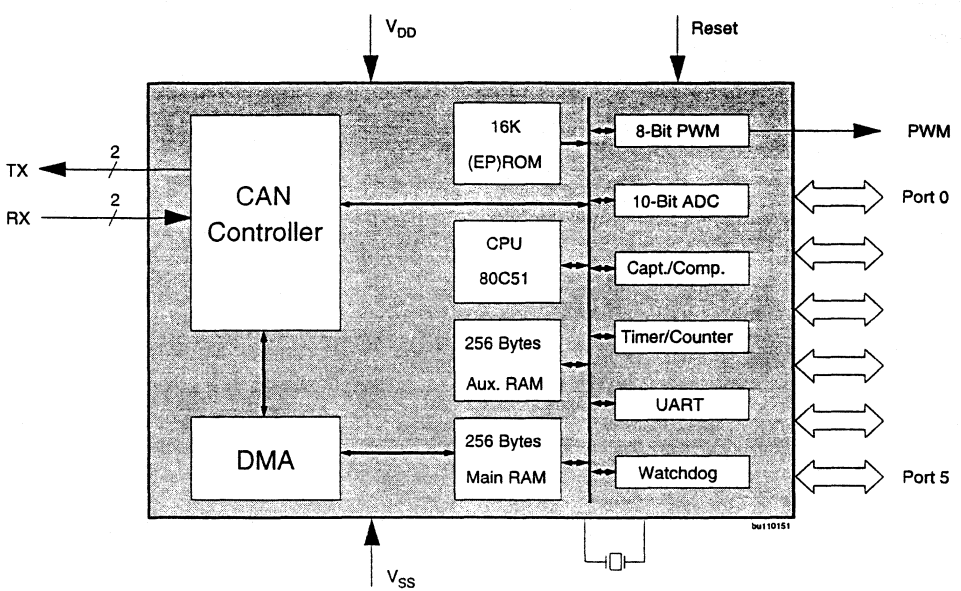


Fig. 2 Block diagram of the P8xC592

The **CAN controller** on the P8xC592 is mainly an on-chip implementation of the Philips Stand-alone CAN-controller **PCA 82C200** [3]. The access to the internal CAN registers now is given via 4 Special Function Registers (**SFR**). The transfer of the messages between the CAN controller and the P8xC592's main RAM can be done in extremely short time by using Direct Memory Access (**DMA**). More information about this feature is given in chapter 4.2.3 .

The P8xC592 has a 256 bytes **on-chip auxiliary RAM**, which is indirectly addressable in the same way as external data memory. This doubling of internal RAM capacity satisfies the rising demand for parameter storage in distributed control applications.

Summarizing the P8xC592 is a single-chip 8-bit microcontroller featuring:

- o 80C51 CPU
- o CAN controller with DMA
- o 16K bytes ROM / EPROM
- o 2 * 256 bytes RAM
- o 10-bit A/D converter, 8 channels
- o 3 * 16 bit timer/counters
  - 4 capture registers
  - 3 comparators controlling 8 outputs
- o 6 * 8-bit I/O ports
- o 2 * PWM outputs
- o full-duplex UART
- o interrupt controller (15 sources)
- o watchdog timer

3. Hardware Aspects

This section covers hardware considerations of a CAN-based module in a network. The first part describes the minimum circuitry required for the P83C592 / P87C592. The second part gives suggestions for the connection of the controller to the CAN bus wires.

3.1 Main Circuitry

The P8xC592 is designed to work with a minimum of external components. Fig.3 shows the circuitry of a CAN node using the ROM- or EPROM- version P83C592 or P87C592. The only additional components that are required are a crystal (Q1) plus two small capacitors (C1, C2) to drive the on-chip oscillator, a reset circuit to provide the power-on RESET and a transceiver circuit (see section 3.2) for the connection to the bus wires.

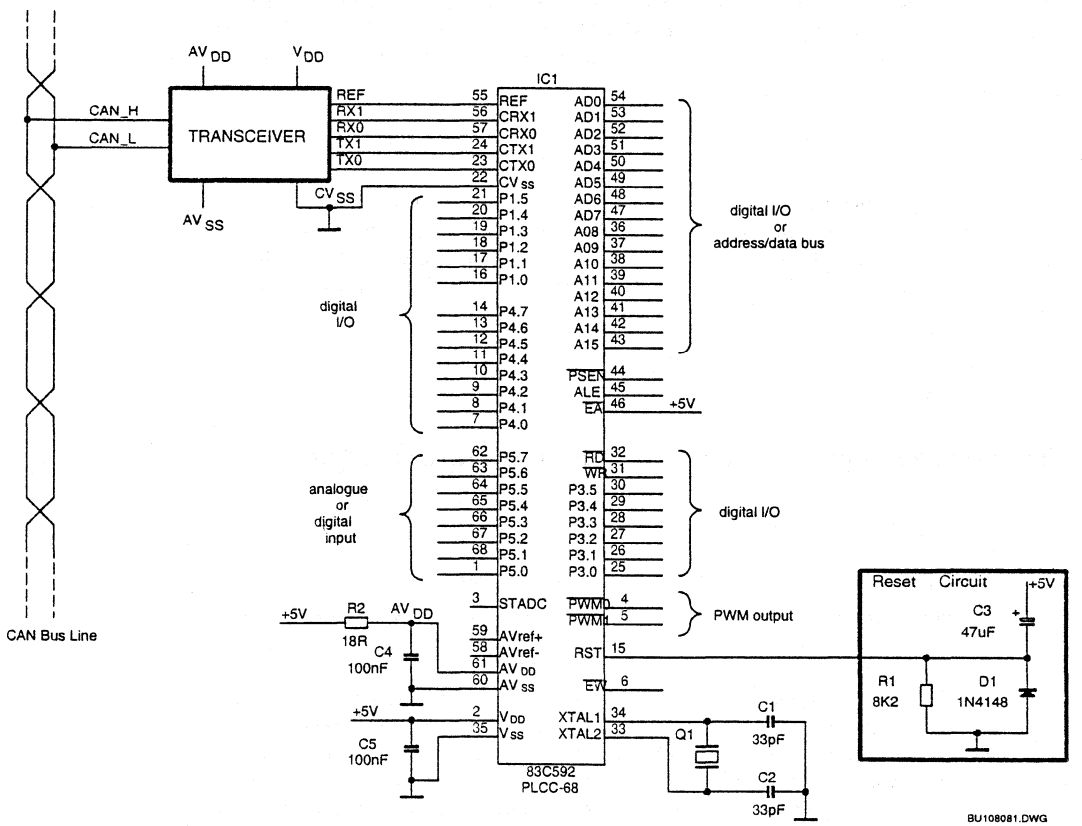


Fig. 3 P87C592 / P83C592 circuitry for a CAN application

Power Supply

The 5V power supply is split on the different power input pins of the µC. The main supply for the (digital part of the) CPU is fed to the V_{DD} / V_{SS} pins, buffered by capacitor C5.

It is recommended that the supply AV_{DD} / AV_{SS} for the analogue parts is derived from the main supply by the filter R2 / C4. The AV_{DD} / AV_{SS} supply is used to drive the on-chip A/D converter and the receiver section of the CAN controller; it shall also be used for optional biasing of the RX0 / RX1 pins in the off-chip transceiver.

The pin CV_{SS} is the ground pin belonging to the CAN on-chip transmitter output stages (cf. chapter 3.2.1), which shall also be used for optional ground potential of the off-chip transceiver.

Program Fetch

The schematics of fig.3 present the circuitry for microcontrollers with on-chip program memory (ROM or EPROM). Therefore the pin $\overline{EA}$ is connected to +5V for program being fetched from internal memory. Note that the EA-pin is only read by the CPU during RESET, that means, switching it during program execution is not possible. This can give an additional protection against unauthorized copying of the on-chip program.

Reset Circuit

The schematics of fig.3 present a proposal for a discrete circuit that provides the necessary RESET signal to the CPU during power-up. The Reset Circuit can be replaced by a connection of the RST-pin to the power-on/power-fail reset output of the power supply, if available. Note that internal RESET conditions of the CPU (e.g. watchdog or recover from power-down) may cause the output of a short pulse on the RST pin, which the Reset Circuit has to tolerate.

3.2 Transceiver: Physical Interface to the Transmission Medium

The transceiver circuit performs the following functions:

- o it converts signals TX0, TX1 into the voltage levels for the bus wires,
- o it converts the voltage levels on the bus wires to be compatible with the CRX0, CRX1 inputs of the P8xC592.

How this connection actually is implemented, is application-specific. Depending on the requirements for the bus signals, the transceiver can be realized with more or less effort, the cheapest solution consists only of a couple of resistors, more expensive ones need some more discrete components or an extra IC. In principle the very same transceiver circuits can be used as for the stand-alone CAN controller PCA 82C200 [3]. Three examples for cheap discrete transceivers have been described in the Application Note [4] for the PCA 82C200, for instance.

In order to get to an international standard for CAN communication (including the transceiver), the International Standardization Organization (ISO) has prepared two standards, one for lower bit rates (up to 125 kbit/s) [6], one for higher ones [7]. They also define the electrical parameters for the transceiver. Application hints for implementation of an ISO-compatible transceiver circuit are given in [10].

3.2.1 On-chip Transceiver Components

The off-chip transceiver circuit connects the bus wires to the on-chip transceiver components. The on-chip transceiver provides the transmitter output stage and the receiver input comparator, see fig.4.

Transmitter

The transmitter provides two output lines (CTX0, CTX1); their characteristics can be programmed individually with the OUTPUT CONTROL register. Each line can work as open-drain or open-source or push-pull output, with positive or negative polarity. Thus the transmitter is well prepared to drive any kind of differential bus lines.

The connections of the transmitter outputs to the bus wires have to be done in such a way, that the resulting level on the bus is:

- o recessive level, when all nodes transmit a logical 1 or do not transmit,
- o dominant level, when one or more nodes transmit a logical 0.

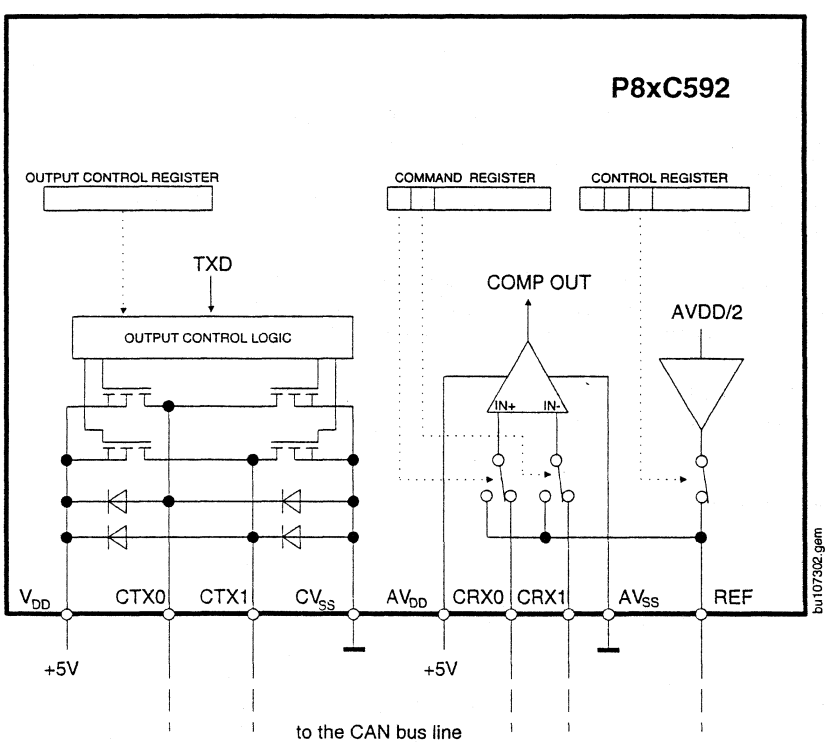


Fig. 4 Structure of the on-chip CAN transceiver

Receiver

The on-chip receiver is a differential input comparator with the input lines CRX0 and CRX1. It decodes

- o the recessive level to a logical 1, when the voltage at the CRX0-pin is higher than at the CRX1-pin,
- o the dominant level to a logical 0, when the voltage at the CRX0-pin is lower than at the CRX1-pin.

Instead of decoding the **differential** bus signal, the comparator inputs can also be switched by software to decode the signal of only one of the two bus lines, comparing it to the reference voltage at the REF pin. The reference voltage can either be provided by the internal on-chip voltage generator (= default), or, if desired, it is fed to the REF pin by an external source, with the internal source being switched off by software. The use of **single wire** decoding is beneficial to continue communication, when one of the two bus lines has a wiring failure (open or short circuit), please refer to [8].

4. Software Aspects

4.1 CAN Registers

The P8xC592's on-chip CAN controller is a full implementation of the CAN protocol. It contains all necessary features required for a high performance communication protocol.

The CAN controller appears to the CPU as a memory- mapped I/O device which is arranged as Control Segment, Transmit (Tx) Buffer and Receive (Rx) Buffer (see fig.5).

Exchange of status, control and command signals between the CPU and the CAN controller is done by the control segment which contains 10 bytes. It is programmed during initialization for configuration of the communication parameters. Additionally the CPU controls the CAN communication via this segment.

Data to be transmitted are loaded into the Transmit Buffer by the CPU. The buffer contains the descriptor (Identifier, RTR-bit and DLC) and up to eight data bytes.

After a successful reception messages are read from the Receive Buffer. It consists of two 10 byte memories which are alternatively used to store messages. The CPU can process one message while another is being received.

4.2 On-chip Interface Between CPU and CAN Controller

To access the described CAN controller registers, four special function registers CANADR, CANDAT, CANCON and CANSTA are implemented. All CAN registers of the Control Segment which are used during communication now appear as being directly addressable as they are represented by these four special function registers. The Status Register represented by CANSTA now is even bit-addressable. With the help of these registers and the DMA logic, data transfer between Transmit/Receive Buffers and internal main RAM is also done very effectively (see fig. 6).

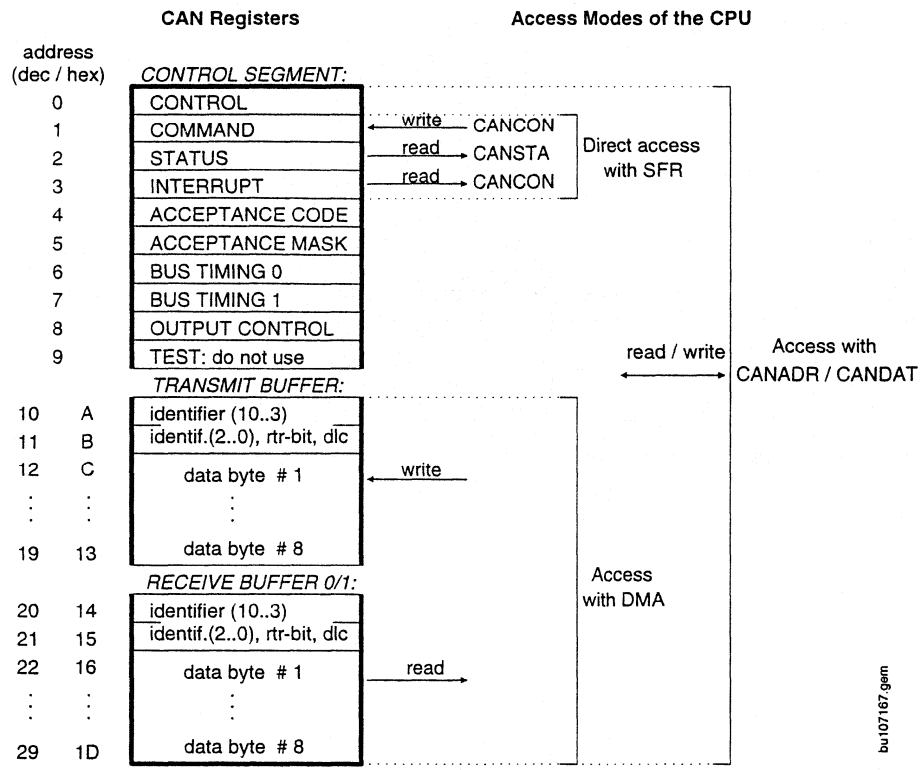


Fig. 5 CAN register mapping

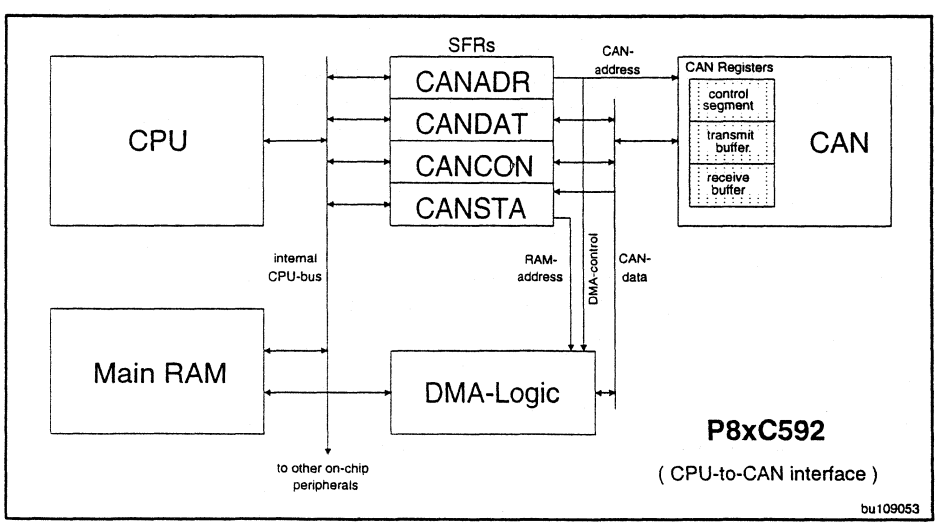


Fig. 6 Block diagram of the CPU - to - CAN interface

4.2.1 CAN Related Special Function Registers

Table 1 shows the special function register arrangement. Note that CANCON and CANSTA have different meanings for a read and write access.

SFR	ADR	ACS	MSB 7	6	5	4	3	2	1	LSB 0
CANADR	D8H	R/W	DMA	reserved	AutoInc	CANA4	CANA3	CANA2	CANA1	CANA0
CANDAT	DAH	R/W	CAND7	CAND6	CAND5	CAND4	CAND3	CAND2	CAND1	CAND0
CANCON	D9H	R	reserved	reserved	reserved	Wake up Int	Overrun Int	Error Int	Transmit Int	Receive Int
		W	RX0 active	RX1 active	Wake up Mode	Sleep	Clear Overrun	Release Rx Buffer	Abort Transm.	Transmit Request
CANSTA	D8H	R	Bus Status	Error Status	Transmit Status	Receive Status	TX compl. Status	Tx Buffer Access	Data Overrun	Rx Buffer Status
		W	RAMA7	RAMA6	RAMA5	RAM4	RAMA3	RAMA2	RAMA2	RAMA1

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Table 1: CAN Special Function Registers

CANADR

With the least significant bits CANA4...CANA0 each of the CAN controller internal registers can be addressed by a write access to CANADR. Reading or modification of the particular CAN register then is done by reading or writing to CANDAT. CANADR is implemented as a read/write register which also contains control bits to select auto increment addressing and to start a DMA transfer.

CANDAT

When reading or writing CANDAT, access to the CAN registers addressed by CANADR is possible. The way of accessing CAN registers via CANADR/CANDAT normally is only necessary for the registers Acceptance Code, Acceptance Mask, Bus Timing 0, Bus Timing 1, Output Control, which the CPU has to access during initialization only.

CANCON

CANCON is a register with different meaning for write and read operation. Writing to CANCON is a direct access to the command register and reading from it is a direct access to the interrupt register.

CANSTA

The bit addressable register allows a direct read access to the Status Register of the CAN Controller. Writing to CANSTA sets the address of the on-chip main RAM for a subsequent DMA transfer.

4.2.2 Auto Address Increment

Fast reading and writing of consecutive CAN Controller internal registers is possible by setting the AutoInc bit of CANADR and the concerning register address simultaneously. A first access to CANDAT refers to the register specified in CANADR. After any read or write access to CANDAT the contents of CANADR are incremented automatically in this mode.

Incrementing CANADR beyond XX111111B resets the AutoInc bit automatically to XX000000B.

4.2.3 High Speed DMA

The DMA logic provides a very fast transfer of complete messages between receive/transmit buffers and internal data memory (Main RAM) within 2 instruction cycles. The transfer process operates in the background and therefore the CPU can continue with the next instruction. However, an access to the Main RAM or to the CAN special function registers is not allowed during this time.

A DMA transfer action is achieved by first writing the RAM address into CANSTA and then writing the Tx- or Rx-Buffer address and the DMA bit simultaneously into CANADR.

The DMA automatically recognizes the transfer direction (see table 2). For the Rx Buffer DMA there is the option to copy a whole message or only a part of it.

CANADR	subject to transfer	transfer direction
8AH	whole message	RAM -> Tx Buffer
94H	whole message	Rx Buffer -> RAM
95H	whole message without first byte	
96H	data bytes only *)	
97H	last data bytes *)	
.	.	
.	.	
9DH	only the last data byte *)	

*) data bytes are copied as far as they are available (DLC!)

Table 2: DMA Modes

Setting the DMA bit causes an automatic evaluation of the data length and subsequent transfer. For a Tx Buffer DMA transfer the data length is always expected at "RAM address + 1".

After the DMA transfer has been finished, the DMA bit and the AutoInc bit are reset.

4.3 Basic Functions for CAN Communication

4.3.1 Initialization

During Initialization the P8xC592's CAN Controller is configured according to the required communication parameters. Before setting the registers in the Control Segment (see fig.5) first the Reset Request bit in the Control Register has to be set to "present" (high). An initialization procedure should include definitions of the following items:

- o Acceptance Filter
- o Bus Timing
- o Output Mode
- o Interrupts
- o Reference Voltage Mode

A flow chart of the initialization procedure is shown in table 4.

When the configuration of the P8xC592 is finished the Reset Request bit has to be set to "absent" to allow receive- or transmit operations.

4.3.2 Transmission

The CPU may write a message into the transmit buffer whenever the transmit buffer access bit (Status Register) is set. After writing the message to the transmit buffer and setting the transmission request bit high (Command Register), the CAN Controller begins with the transmission process.

If the CPU cannot access the transmit buffer because a previously requested message is still waiting for transmission, it is possible to abort the current process. A transmission already in progress is not stopped.

```
+-------------------------------------------------------------------------------+
|if (status bit TRANSMIT BUFFER ACCESS = "released")                            |
+------------then--------------+--------------------else-----------------------+
| write message into           |if (<high priority message to be transmitted>) |
| TRANSMIT BUFFER              +---------------then--------------+----else---+
+------------------------------+ set command bit                 |           |
|set command bit TRANSMISSION  | ABORT TRANSMISSION:= "present"  |           |
|REQUEST := "present"          +---------------------------------+-----------+
|                              |(* the next transmission is delayed until      |
|                              |   TRANSMIT BUFFER ACCESS = "released" is      |
|                              |   signalled by a TRANSMIT INTERRUPT or by     |
|                              |   polling the STATUS REGISTER *)              |
+------------------------------+-----------------------------------------------+
```

Table 3: Flow chart of a transmission procedure

```
+-------------------------------------------------------------------------------+
|(* start initialization; write CONTROL REGISTER *)                             |
|                                                                               |
|        - set RESET_REQUEST := "present"                                       |
|        - set TEST_MODE     := "disabled"                                      |
+-------------------------------------------------------------------------------+
|(* write acceptance filter *)                                                  |
|                                                                               |
|        - write ACCEPTANCE CODE REGISTER                                       |
|        - write ACCEPTANCE MASK REGISTER                                       |
|                                                                               |
|(* example: contents of ACCEPTANCE CODE REGISTER   =   01110010B               |
|            contents of ACCEPTANCE MASK REGISTER   =   00111000B               |
|            allows for messages with following IDs:    01xxx010xxxB            |
|*)                                                                             |
+-------------------------------------------------------------------------------+
|(* define bus timing (baud rate on the CAN Bus) *)                             |
|                                                                               |
|        - write BUS TIMING 0 REGISTER                                          |
|        - write BUS TIMING 1 REGISTER                                          |
|                                                                               |
|(* example: contents of BUS TIMING 0 REGISTER = 10001001B                      |
|            contents of BUS TIMING 1 REGISTER = 11101011B                      |
|            results in:                                                        |
|               tSCL     = (9 + 1) * 2 * tOSC   (with fOSC = 16 MHz: 1.25 us)  |
|               tSJW     = (2 + 1) * tSCL                            (3.75 us) |
|               SAM      = 1                      (three samples / bit taken)  |
|               tSYNC    = 1 * tSCL                                  (1.25 us) |
|               tTSEG2   = (6 + 1) * tSCL                            (8.75 us) |
|               tTSEG1   = (11 + 1) * tSCL                          (15.00 us) |
|               tBIT     = tSYNCSEG + tTSEG1 + tTSEG2 = 20 * tSCL    (25.00 us) |
|               variation of bit time due to resynchronization:                 |
|                   tBITmin  = tBIT - tSJW = 17 tSCL                  (21.25 us) |
|                   tBITmax  = tBIT + tSJW = 23 tSCL                  (28.75 us) |
|*)                                                                             |
+-------------------------------------------------------------------------------+
|(* define bus driver characteristics *)                                        |
|                                                                               |
|        - write OUTPUT CONTROL REGISTER                                        |
|                                                                               |
|(* example: contents of OUTPUT CONTROL REGISTER = 10101010B                    |
|            results in:                                                        |
|               output mode: normal 1 (bit sequence on TX0 and TX1 pins)       |
|               TX0 configuration: bit-state 0 (1) -> output-state low  (float)|
|               TX1 configuration: bit-state 0 (1) -> output-state high (float)|
|*)                                                                             |
+-------------------------------------------------------------------------------+
|(* end initialization; write to CONTROL REGISTER *)                            |
|                                                                               |
|        - enable interrupt sources             (* bits 4 .. 1  *)             |
|        - define mode of reference voltage     (* bit 5        *)             |
|        - define the resynchronization mode    (* SYNCH; bit 6 *)             |
|        - set RESET REQUEST := "absent"        (* bit 0        *)             |
+-------------------------------------------------------------------------------+
(* = start of comment       *) = end of comment
```

Table 4: Flow chart of an initialization procedure

4.3.3 Reception

Whenever the status bit 'Receive Buffer Status' is set, a new message is available in the Rx Buffer. Polling the Status Register enables the information of new message data in the Rx Buffer to be coordinated and controlled by the CPU.

When the Receive Interrupt is enabled the according bit in the interrupt register is set simultaneously with the Receive Buffer Status bit and the interrupt service can start with reading of message data from the Rx Buffer.

After Reading the buffer contents the CPU has to release this buffer by setting the Release Receive Buffer command bit. This may result in another message becoming immediately available.

```
+-------------------------------------------------------------------------------+
|read message from RECEIVE BUFFER                                               |
+-------------------------------------------------------------------------------+
|set command bit RELEASE RECEIVE BUFFER := "released"                           |
+-------------------------------------------------------------------------------+
```

Table 5: Flow chart of a reception procedure

4.3.4 Sleep Mode

If the Sleep Bit of the Command Register is set high the CAN controller enters the Sleep Mode, requiring that there is no bus activity and no interrupt is pending. A network enters the 'Sleep Mode' when all its nodes enter the Sleep Mode.

The CAN Controller wakes up after setting the Sleep bit of the Command Register low or when there is any bus activity. Upon wake up a wake up interrupt is generated. It is not necessary to enable the wake up interrupt.

After the CAN Controller entered Sleep Mode the CPU may be set into the 'Power Down Mode' (oscillator stopped). Upon wake up, the oscillator is started again. The wake up interrupt will wake up a CPU from 'Power Down Mode' by generating a Reset pulse, if the SIO1 (CAN) interrupt source was enabled. A CAN Controller that wakes up because of bus activity is not able to receive this message until it detects a bus free signal.

Reading of the Sleep bit reflects the status of the CAN Controller.

```
+-------------------------------------------------------------------------------+
|Set command bit SLEEP := "sleep"                                               |
+-------------------------------------------------------------------------------+
```

Table 6: Flow chart of a "go to sleep" procedure

4.3.5 Comparator Switches

Data communication between the nodes of a network is disturbed or stopped when the bus wires are short-circuited (global failures) or interrupted (local failures). With the P8xC592 precautions have been taken to continue data communication despite of a bus failure.

With the help of the comparator switches, implemented in the CAN Controller, it is possible to tolerate the following single wiring failures:

- o one of the bus lines is short-circuited with VBAT or GND
- o one bus line is short-circuited against the other
- o interruption of one of the bus lines

The structure of the on-chip CAN Transceiver in fig.4 shows that in case of a short circuit it is possible to disconnect a blocked bus wire from the CAN receivers of all network nodes and replace this faulty bus line potential by a local reference level at one of the comparator inputs. In some cases it might be necessary to disconnect the bias voltage of one bus wire from the power supply terminal, additionally, to continue with communication.

Bus line interruptions are solved similar to the short circuit failures by replacing the potential of one bus line with a local reference potential.

The positions of the switches are defined via the Command Register bits RX0A and RX1A (see table 7). Reading of RX0A/RX1A reflects the status of the switches.

RX0A	RX1A	Result
0	0	unchanged
0	1	IN+ = REF, IN- = CRX1
1	0	IN+ = CRX0, IN- = REF
1	1	IN+ = CRX0, IN- = CRX1

Table 7: Results of setting RX0A/RX1A

With the help of the described comparator switches three configurations can be selected:

- o two wire communication (differential signal)
- o single wire communication using CAN_H
- o single wire communication using CAN_L

Thereby a test of the bus wires can be implemented easily by software: if single wire communication is possible in the network with each of the bus lines as well as differential communication, then there is no wiring failure. Otherwise the faulty wire is detected (**diagnosis**) and the network may continue to communicate on the other wire till the faulty wire is repaired.

For more details on CAN Bus failure management please refer to [8].

4.4 Control of CAN Communication

Information about the reception of messages, the completion of a transmission, data overrun, error status etc. can be signalled to the CPU either with interrupt processing, described in chapter 4.4.1 or with polling, described in chapter 4.4.2. It can be of advantage to mix both, polling and interrupt control. Note, that the wake up event can only be processed by interrupt.

4.4.1 Interrupts

The P8xC592 controls five different CAN related interrupt sources. These are the Receive-, Transmit-, Overrun-, Error- and the Wake up Interrupt. All interrupts can be enabled/disabled via the Control Register except of the Wake up Interrupt which is always enabled. Setting of the interrupt sources is usually done during initialization (see also table 4). Do not forget to enable the CPU's SIO1 interrupt (by ES1 bit) and the global interrupt (by EA bit).

Upon the occurrence of one or more (enabled) interrupts the according bits are set in the **Interrupt Register** and a CAN interrupt (SIO1) for the CPU is performed. After reading this register, that appears to the CPU as a read only memory, all bits are reset by the CAN Controller. Therefore, the Interrupt Register should be stored in a bitaddressable part of the CPU memory for later interrupt evaluation.

Table 8 shows the procedure for an Interrupt Register data evaluation. In this example it is assumed that all interrupt sources are enabled to present a complete description.

The following summary gives a short overview of the CAN related interrupts and their occurrences.

Receive Interrupt:	If a new message is available in the Receive Buffer, the Receive Interrupt is given.
Transmit Interrupt:	A Transmit Interrupt is signalled, when a transmission has been completed or aborted.
Error Interrupt:	If the Bus Status or the Error Status changes, an Error Interrupt is given.
Overrun Interrupt:	When both Receive Buffers contain a message and the first byte of the next message should be stored, the Overrun Interrupt is signalled.
Wake up Interrupt:	Whenever the Sleep Mode is left, a Wake up Interrupt is signalled.

When CAN communication is controlled partly in the interrupt service routine and partly in the main program, care has to be taken about the use of CANADR/CANDAT (indirect addressing of the CAN Registers) or CANADR/CANSTA (use of DMA), respectively. If they are used as well in main program level as in interrupt level, it might be necessary to save the address of CANADR (push/pop) during interrupt processing, or disable the CAN interrupt during DMA transfer at main level, respectively. For the latter, if required, the interrupt has to be disabled right before the RAM address is written into CANSTA, and can be re-enabled just after the start of the DMA transfer.

Table 8: Flow chart of Interrupt Register data evaluation

4.4.2 Polling

Analysing the contents of the Status Register, as shown in table 9, is very similar to analysing the contents of the Interrupt Register. With the following overview the concerning Status bits are described:

Receive Buffer Status: This bit is set when a new message is available.

Transmit Buffer Access: The CPU may write a message to the Tx Buffer when this bit is set.

Error Status: The Error Status bit is set when at least one of the Error Counters has reached the warning limit.

Data Overrun: When both Receive Buffers are full and the first byte of a new message should be stored, this bit is set.

if (**TRANSMIT BUFFER ACCESS** = "released")			
then			else
a next message may be written into the TRANSMIT BUFFER			
if (<using the ABORT TRANSMISSION command>)			
then		else	
if (TRANSMISSION COMPLETE STATUS = "complete")		(* last requested transmission has been completed *)	
then	else		
(* last requested transmission has been completed, no ABORT TRANSMISSION command has been exec. *)	(* last requested transmission has not been completed due to an ABORT TRANSMISSION command *)		
if (**RECEIVE BUFFER STATUS** = "full")			
then			else
read RECEIVE BUFFER into CPU memory			
set command bit RELEASE RECEIVE BUFFER := "released"			
if (**DATA OVERRUN** = "overrun")			
then		else	
an application may use this information to change its behaviour (e.g. faster reaction on a RECEIVE INTERRUPT)			
set command bit CLEAR OVERRUN := "clear"			
if (**BUS STATUS** = "on-bus")			
then		else	
(* P8xC592 takes part in bus activities *)		(* P8xC592 does not take part in bus activities *)	
if (**ERROR STATUS** = "ok")		if (<restart CAN hardware required>)	
then	else	then	else
(* the CAN-bus is presently not severely disturbed *)	(* the CAN-bus is presently severely disturbed *) some application-specific actions may be necessary	set control bit RESET REQUEST := "absent" (* now the P8xC592 waits for 128 * 11 consecutive recessive bits before going "on-bus" again *)	perform application-specific default-mode operation

Table 9: Flow chart of Status Register data evaluation (polling)

4.5 CPU Load for CAN - a Real Example

In a CAN system data transfer can be done with a very high level of safety with the CAN controller part of the P8xC592. The CPU has only the task of post-processing the received data and pre-processing the data to be transmitted. Communication between CPU and CAN controller is easily done via the Special Function Registers described in chapter 4.2.1. Using the DMA transfer facility, data exchange between CPU and Rx/Tx buffer is very effective.

That means that the resulting CPU load for CAN communication is very low, as the analysis of the following communication example proves. Simulations with "NetSim" (a simulator for CAN communication, see chapter 5.4) have been done with a real communication example of 7 nodes. At a data rate of 500kbit/s, 12 different messages M are transferred on the bus. Fig.7 shows the structure of the network. M3_2 means: 2nd type of message that is transmitted by node number 3, for instance.

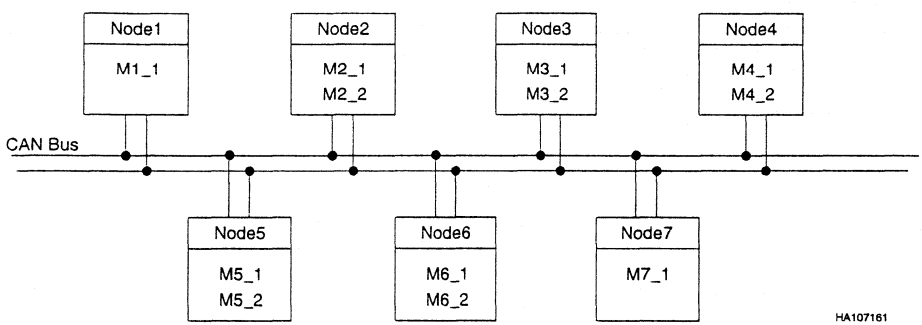


Fig. 7 Network example

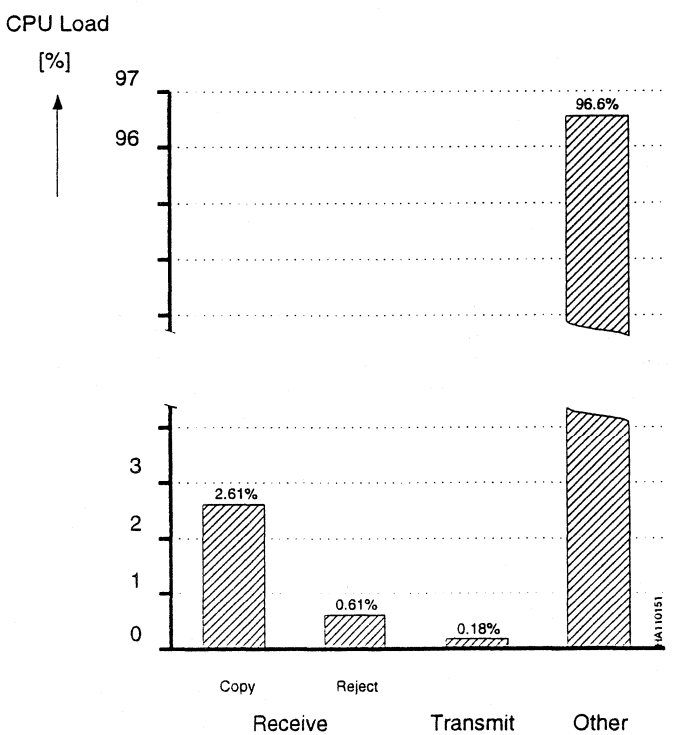
The communication matrix and information about message length, repetition time and node numbers are given in table 10, whereby the described communication of the example with the according messages results in a total bus load of about 23%.

The CPU load for CAN communication is defined as the percentage of time the CPU is serving the CAN communication; its calculation is described in detail in chapter 4.6.

The diagram of figure 8 shows the CPU load of nodes 1...7, split up in receive and transmit actions of the CPU. Receive actions are executed for all messages that pass the acceptance filter. These messages are **copied** into the CPU RAM except they are not of interest for the CPU, the latter means they are **rejected**. The result of this simulation is that the CPU spends only 3.4% of the time for CAN related procedures. In this example 96.6% of the time is free for other CPU activities.

Transmitting node / message		DLC	ID	Repetition Time [ms]	receiving node						
					1	2	3	4	5	6	7
1	M1_1	4	10	2	-	x	x	x	-	-	x
2	M2_1	7	11	2	x	-	x	x	x	x	x
2	M2_2	2	30	100	-	-	-	-	-	-	x
3	M3_1	5	15	20	x	x	-	-	x	-	x
3	M3_2	3	31	100	-	-	-	-	-	-	x
4	M4_1	5	32	20	-	x	-	-	-	x	x
4	M4_2	3	33	100	-	-	-	-	-	-	x
5	M5_1	8	20	100	x	x	x	-	-	x	x
5	M5_2	8	34	100	-	-	-	-	-	-	x
6	M6_1	8	21	100	-	x	-	x	x	-	x
6	M6_2	8	35	100	-	-	-	-	-	-	x
7	M71	8	36	100	-	-	-	-	x	x	-

Table 10: Communication Matrix of the network example. (ID = Identifier, DLC = data length code)



4.6 Calculation of the CPU Load for CAN Communication

In chapter 4.5 a practical example was presented for which the CPU load for CAN communication had been investigated. The figures were obtained for a real set-up using 7 nodes. In this chapter the details of such a CPU load calculation are presented.

The following calculations and diagrams give hints and ideas to the user of the P8xC592 about the receive interrupt service execution time and CPU load when serving the CAN controller. To get results as reliable as possible all figures are calculated for worst case. As shown in fig.8 both reception of messages and transmission of messages result in CPU load, but the partial CPU load for transmission obviously is almost negligible. Therefore the considerations in the next sections have been focussed on the reception of messages. Reception of messages is normally initiated by interrupt. The according interrupt service routine copies the Rx buffer contents to an internal CPU RAM location. Its execution time should be as short as possible in order to achieve a low CPU load.

The **CPU load** for CAN communication is defined as the percentage of time the CPU is serving the CAN communication, measured in a time interval of interest.

In case the time interval is shorter than the duration of a message transfer on the bus, the Spare Time should be considered instead of the CPU load. The **Spare Time** is defined as the amount of coherent CPU time the CPU may reserve for non-CAN activities between the reception of consecutive messages.

The next section presents the software which meets the requirements for a fast execution of the receive interrupt service.

Receive Interrupt Service Routine

Base of all the following calculations is a simple receive interrupt service routine for the P8xC592 (table 11, see also Appendix A.1). The calculations of CPU load have been investigated by using a reference software (fig.9, Appendix A.1) that uses the receive interrupt service routine. It also checks the data overrun condition in order to evaluate the Spare Time. The described software and the results are an example and transformation to user specific requirements is very easy.

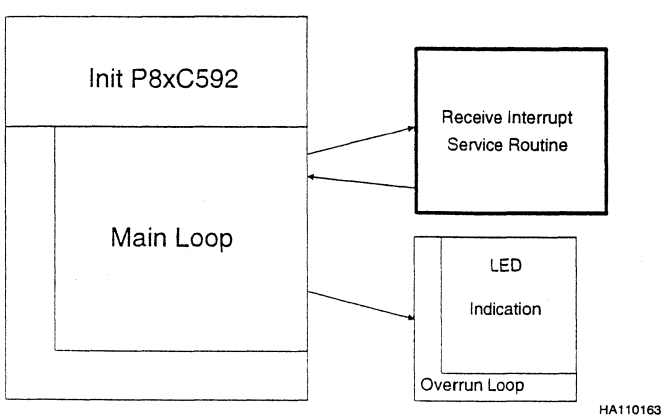


Fig. 9 Reference software with Receive Interrupt Service Routine

First of all the arrangement of the reference software is given in a short summary:

Identifier:	ID10,ID9,ID8,ID7 are fixed by acceptance filter,e.g. ID = 0101 XXXX XXX
Interrupts:	Receive Interrupt enabled
Data Copy:	data bytes according data length code and a part of the identifier (as an indication for a new message) are copied into the internal µC Main RAM
Remote Frames:	in case of remote frame reception the data length code is deleted and only a part of the identifier is copied as an indication of its reception.
Overrun:	the overrun status bit is checked in the main loop. Whenever an overrun condition would be detected, indication would be done via LED. The program remains in the overrun loop until reset.
Reject:	Messages which pass the acceptance filter, but are useless for the µC, are rejected by the software automatically.

CAN_INTERRUPT:

context switch save Accu & PSW select register bank
clear interrupt bits (read Interrupt Register)
calculate table address fetch target address from table
if target address ≠ 0, then copy Rx Buffer to int. µC RAM starting at target address
release Receive Buffer (Acknowledge)
restore context

Table 11: Flowchart of the Receive Interrupt Service Routine

Receive Interrupt Execution Time

Table 12 shows the interrupt execution time for the used receive interrupt service routine. The routine is split up into different macros, for each of them the according processing time has been calculated.

The receive interrupt execution time is shorter, when a message has to be rejected. Therefore two columns are shown, the particular processing time for the copy and the reject case. Another column shows the time passing until the Receive Buffer is released, for evaluation of the CPU Spare Time (see chapter 4.6.2).

Times are given in units of machine cycles and one cycle consists of 12 oscillator periods. The used oscillator frequency of the P8xC592 is 16 MHz resulting in a cycle time of 0.75µs.

Fig. 10 shows the receive interrupt execution time ("copy" and "reject") as a function of the message data length code (DLC). For purpose of comparison also the message transfer time on the bus is given for the data rates: 250kbit/s, 500kbit/s and 1Mbit/s.

Macro Name	Machine Cycles	Copy	Reject	Rx Buff Release
Max. Interrupt Response Time	5	x	x	x
Long Jump to Interrupt Service Routine	2	x	x	x
Context Switch	6	x	x	x
Clear Int. Bits	1	x	x	x
Calculate Target Address	15	x	x	x
Copy rx buffer	8	x	-	x
Acknowledge	2	x	x	x
Restore Context	6	x	x	-
Sum of cycles		45	37	39

Table 12: Summary of receive interrupt execution times (machine cycles)

Fig. 10 shows that due to the DMA function of the P8xC592 the receive interrupt execution time is always independent of the length of the received message. It is very important that the receive interrupt execution time is much shorter than the time the message itself spends on the bus. This clearly shows that a data overrun caused by a burst of messages can be excluded.

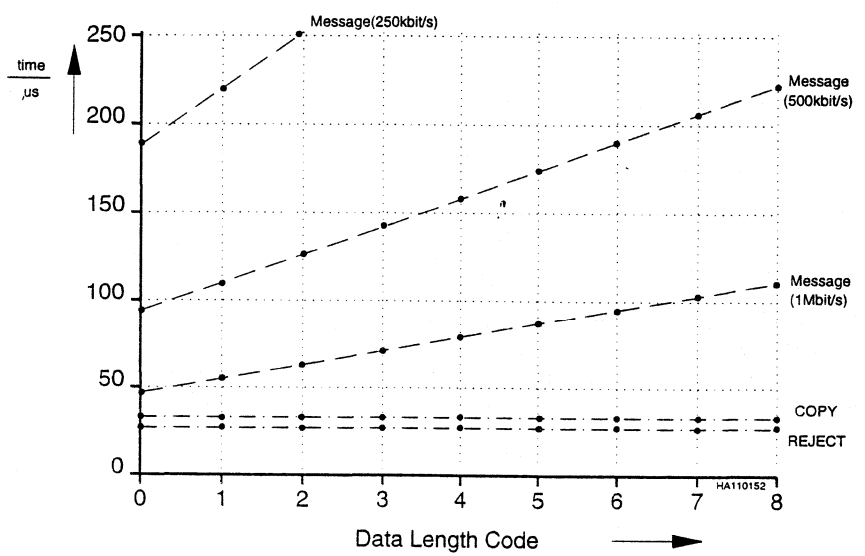


Fig.10 Receive interrupt execution time ("copy" and "reject") and message transfer time ("Message") for 16MHz CPU as a function of Data Length Code

4.6.1 CPU Load

Three parameters are important for the calculation of the CPU load while receiving messages: The used receive interrupt execution time (see tables 11/12), the bit rate and the bus load.

The **bus load** is the percentage of time the bus is occupied (active) by transferring messages. Therefore it has to be calculated how many messages are transferred in a time interval, and how long a message transfer is on the bus. The latter is the message length (=number of bits) multiplied by the time of one bit. The message length depends on the data length code. For the following calculations a data length code estimation has to be made.

$$bus\ load = \frac{bus\ active\ time}{time\ interval} = \frac{number\ of\ messages \cdot message\ length \cdot bit\ time}{time\ interval}$$

In order to get a direct relation between CPU Load, bit rate and bus load, from the formula for the bus load the formula for the number of messages is derived, which can be inserted into the definition of the CPU load:

$$number\ of\ messages = \frac{bus\ load \cdot time\ interval}{message\ length \cdot bit\ time}$$

$$CPU\ load = \frac{number\ of\ messages \cdot receive\ interrupt\ execution\ time}{time\ interval}$$

$$CPU\ Load = \frac{bus\ load \cdot time\ interval \cdot receive\ interrupt\ execution\ time}{message\ length \cdot bit\ time \cdot time\ interval}$$

With the definition of $bit\ rate = 1 / bit\ time$ we get

$$CPU\ load = bus\ load \cdot bit\ rate \cdot \frac{receive\ interrupt\ execution\ time}{message\ length} = bus\ load \cdot bit\ rate \cdot \tau$$

The result is, that the CPU load is proportional to the bus load and bit rate. The term $\tau := receive\ interrupt\ execution\ time\ /\ message\ length$ only depends on the data length code, as it is shown in fig. 11.

Using this formula the CPU load can be calculated for any bit rate at any bus load: for example, a bus load of 10% at 400kbit/s with only one-byte messages (copy all of them) means 10% · 0.4 Mbit/s · 0.6 µs/bit = 2.4% of CPU load. For the example of 4-byte messages (DLC=4) the CPU load has been calculated for different bit rates and different bus loads, the result is shown in table 13.

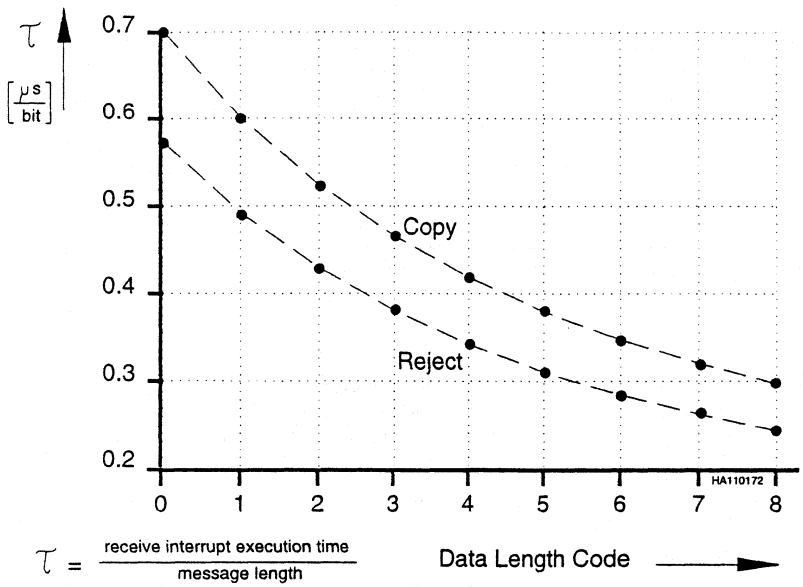


Fig. 11 Diagram for calculation of the CPU load while receiving messages

bit rate	10 % bus load	20 % bus load	50 % bus load
100 kbit/s	0.4 %	0.8 %	2.1 %
250 kbit/s	1.0 %	2.1 %	5.2 %
500 kbit/s	2.1 %	4.2 %	10 %
1 Mbit/s	4.2 %	8.4 %	21 %

Table 13: CPU load when 4-byte messages (DLC=4) are used, for worst case (copy all of them)

4.6.2 Spare Time

But, what happens when the CAN interrupt is delayed or interrupted (e.g. by other interrupt service routines with same or higher priority) ? The first statement is, that the CAN receive interrupt can be delayed for at least that amount of time that is the difference between message transfer time and the receive interrupt execution time.

The actual time that a CAN receive interrupt service may be delayed without risk of loosing a message ("data overrun") is even longer: In fig.12 the execution of the receive interrupt service routine has been delayed so that the routine is not yet finished when the next message comes in, but the 'Release Receive Buffer' command comes just in time before the first byte of the next message is to be stored in the Receive Buffer. No message is lost, but of course that long delay must be compensated by faster response for subsequent reception.

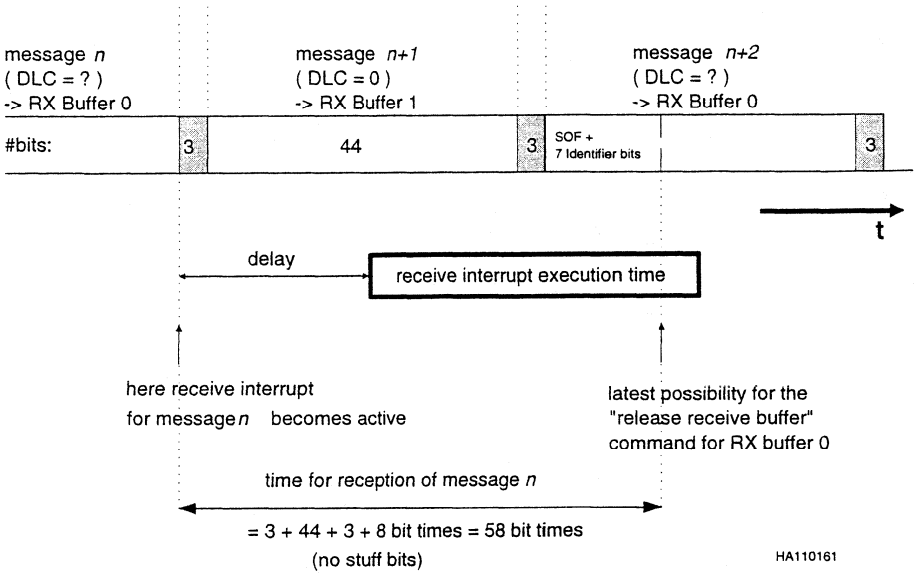
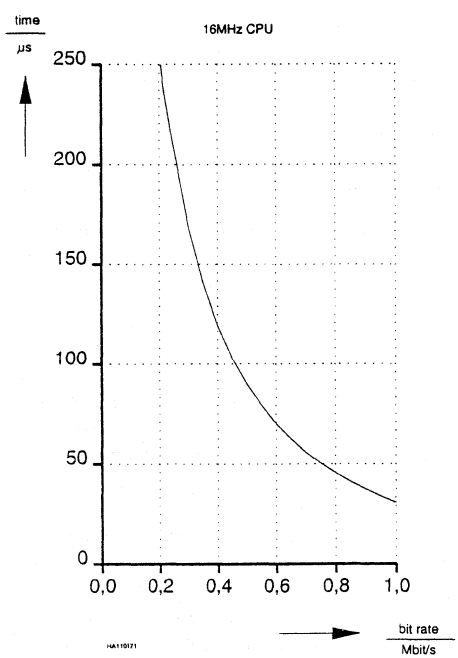


Fig. 12 Delay of receive interrupt service. The worst case is, when a message is followed by a 0-byte message plus another message of any DLC.

The resulting allowed spare time (worst case) is shown in fig.13 for different bit rates. It has been calculated by relating the Receive Buffer Release time of table 12 (39 cycles) to the transmission time of a 0-byte message plus the first byte of a next message (58 bits).



5. Development Tools

For the P8xC592 several powerful support tools can be supplied to assist during the design and test phase. These tools are:

- o the P8xC592 Evaluation Board
- o P8xC592 In-Circuit Emulators
- o P87C592 EPROM programmers
- o debug tools for CAN communication
  NetSim NetAna NetEmu

5.1 Philips P8xC592 Evaluation Board

The P8xC592 evaluation board (OM4239) is a most versatile aid consisting of a ready-to-use hardware and software module very similar to a real CAN bus node. The P8xC592 evaluation board can be used in a car since it has its own 5V supply. An RS232 interface allows the P8xC592 evaluation board to be connected to a terminal or to a PC with terminal emulating software.

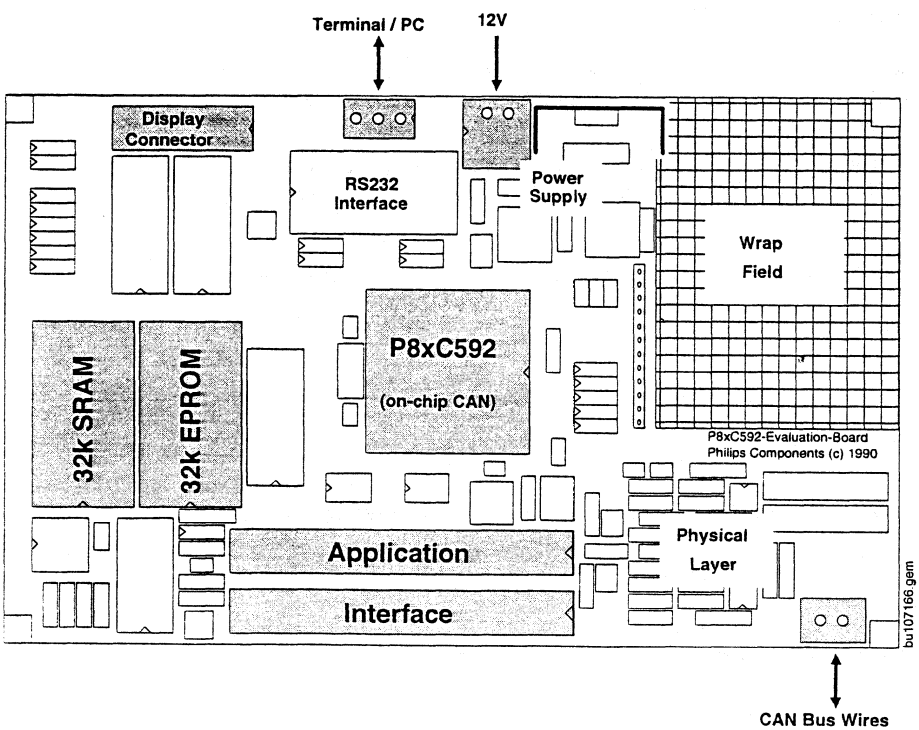


Fig. 14 P8xC592 Evaluation Board

5.1.1 P8xC592 Evaluation Board Hardware

The P8xC592 evaluation board hardware (single EURO format size) is shown in figure 14. It consists of:

- o P87C592 microcontroller with an external memory capacity of 32 KBytes for RAM and 32 KBytes for ROM storage. Together with the on-chip EPROM there are 48 KBytes of continuous program memory
- o 5V power supply with protection against car battery voltage fluctuations
- o off-chip transceiver circuit, designed to meet ISO/TC 22/SC 3 N608E, with two selectable options:
  - very low standby power consumption
  - support of single wire communication to recover from wiring failures.
- o RS232 interface
- o removable LED unit for demonstration purposes
- o wrap field for the user's specific circuitry

5.1.2 P8xC592 Evaluation Board Software

The software for the P8xC592 evaluation board is stored in the on-board EPROM. The software is designed to assist users with different experience in CAN-based networks:

- o A user with little experience is able to activate the demonstration software. A menu-driven software monitor allows the contents of the P87C592's CAN-registers to be altered and thereby enables the user to gain experience. For the latter an RS232-terminal (e.g. VT100) is required.
- o A user with more experience will use the "download" facility; this allows the user to load new software on to the P8xC592 evaluation board. Download requires a PC with terminal emulating software.

The P8xC592 evaluation board is also ready to be used as a bus monitor, receiving messages from the bus for display on a terminal.

5.2 In-Circuit-Emulators

For the software development on the P8xC592 several in-circuit-emulators (ICE) are available.

5.2.1 Philips Stand-alone Debug System (SDS)

Philips' well known and well accepted stand-alone debug station (SDS) for the real-time development of 8-bit µCs is already prepared for future probes > 16MHz. Three configurations are possible:

- o stand-alone operation together with a terminal
- o connected to a terminal plus a host computer (download/upload)
- o connected to a PC/AT (IBM or compatible) with terminal emulation software.

Features of the SDS:

- o fully transparent real-time emulation
- o allows optimal emulation according to the exact specification of the target controller
- o emulation memory: 64 KBytes with no wait states
- o interfaces to external equipment
- o full assembly-level debugging
- o HLL debugging possible
- o single step and breakpoint setting
- o trace and triggering with hardware qualifiers
- o trace memory 2048 lines
- o new improved handbook
- o probes for
  - optimal connection to the target system
  - optimal emulation of the target µC.

For emulation of the P8xC592 the user needs the following parts:

- o SDS80C51 stand-alone debug system (OM4120S)
- o probe base (OM4110)
- o emulation head "592" (OM4112)

Software for development support with the SDS (assembler, PL/M-compiler, C-compiler, HLL debugger) is offered and supported by

Tasking B.V.
Plotterweg 31
3821 BB Amersfoort, Netherlands

their products can also be ordered via Philips.

5.2.2 ICE from Other Vendors

Philips supports all major third-party ICE suppliers with emulating chips for the P8xC592. Most of them already announced to support the P8xC592.

5.3 Programming Support for P87C592 (EPROM)

Philips offers a low-cost programmer for microcontrollers inclusively the P87C592:

- o LCPX5X40 programmer (OM4232)
  - 87C592-PLCC68 adaptor (OM4235)

5.4 Debug Tools for CAN Communication

In addition to the P8xC592 evaluation board three other sophisticated development and debug tools for CAN communication can be supplied. These are offered and supported by

Gesellschaft für Informatik und Mikro-Elektronik
Prof. Dr.-Ing. W.Lawrenz mbH
Ferdinandstr. 15 A
3340 Wolfenbüttel
Germany

NetSim

NetSim (Network Simulator) is a software simulator for use with a Personal Computer. The CAN network is described using NetSim on the PC by:

- o number of network nodes
- o data transmission rate
- o message identifiers / message length / message transmission repetition rate
- o noise

The simulation is then started. NetSim provides information for various parameters, such as:

- o message delays
- o bus load

NetSim assists during the design phase to investigate these parameters.

NetAna

NetAna (Network Analyzer) is a combined hardware / software tool, operating in conjunction with a PC.

NetAna has two basic functions:

- o to monitor the bus traffic and store the data on the hard disk in the PC for subsequent analysis
- o an event is triggered (identifier, bus error, etc.) and the messages around the trigger point are recorded.

NetAna assists to trace communication failures in an existing CAN network

NetEmu

NetEmu (Network Emulator) enables the user to transmit defined messages into an operational CAN network. The resultant network response can then be analyzed by NetAna.

6. References

[1] CAN Specification Version 1.2, Philips Components 1990

[2] P8xC592 target device specification, Version 2.2, Philips Export B.V. 1991

[3] Data sheet PCA 82C200 Stand-alone CAN-controller, Philips Export B.V. 1990, 12NC: 9397 285 30011

[4] Application of the PCA 82C200 CAN Controller (PSCC), Philips Export B.V. 1990, 12NC: 9398 373 50011

[5] Bit Timing Parameters for CAN Networks, Application Note KIE07/91ME, Philips Components PCALH 1991

[6] Road vehicles - Serial data communication for automotive application. Part 1: Controller Area Network (CAN). ISO/DIS 11519 part 1, International Organization for Standardization 1992

[7] Road vehicles - Interchange of digital information - Controller Area Network (CAN) for high speed communication. ISO/DIS 11898, International Organization for Standardization 1992

[8] CAN bus failure management using the P8xC592 microcontroller, Application Note HKI/AN 91 020, Philips Semiconductors PCALH 1991

[9] Single-chip 8-bit microcontrollers: PCB83C552 - User Manual, Philips Export B.V. 1988, 12NC: 9398 637 90011

[10] CAN Physical Layer Concepts for the P8xC592 Microcontroller, Application Note HKI/AN 91 027, Philips Semiconductors PCALH 1991

Appendix

A. Reference software for investigation of the CPU load

A.1 Receiver part

This module is a program including a very fast, versatile receive interrupt service routine which is able to handle up to 128 identifiers. It runs on the P8xC592 Evaluation Board (OM4239), for instance. With only little modifications it can be adapted to other applications.

The receive interrupt execution time is less than 34µs and every software reject is done within 28µs.

The acceptance filter of the CAN part is set to 0101 XXXX XXX. Upon reception of a message which passes the acceptance filter, the data bytes (plus the second byte of the Rx buffer for signalling the reception of new data to the main program) are copied into the internal RAM of the P8xC592, according to a table. In this table for each message the corresponding RAM address can be found or a "0", telling that the message is not of interest and shall be rejected.

In case of an overrun condition, indication is done via LED.

```
CONTROL          EQU     0H
COMMAND          EQU     1H
STATUS           EQU     2H
INTERRUPT        EQU     3H
ACCEPTANCE_CODE  EQU     4H
ACCEPTANCE_MASK  EQU     5H
BUS_TIMING_0     EQU     6H
BUS_TIMING_1     EQU     7H
OUTPUT_CONTROL   EQU     8H

CANADR           EQU     0DBH
CANDAT           EQU     0DAH
CANCON           EQU     0D9H
CANSTA           EQU     0D8H

AUTO_RX_BUFFER   EQU     34H
RX_BUFFER        EQU     14H
DMA_RX_BUFFER    EQU     94H

INT_MASK         EQU     00000010B       ; Rx Interrupt enabled

ES1              BIT     0ADH

DSEG AT 30H
    ARRAY_LONG: DS       9               ; space for Rx of an 8-byte message
    ARRAY_SHORT:DS       1               ; space for Rx of a 0-byte message

BIT_VAR SEGMENT DATA BITADDRESSABLE
RSEG    BIT_VAR
    INT_SAVE:   DS       1
    RX_INT BIT INT_SAVE.0

CSEG AT RESET
    LJMP         MAIN_PROG

CSEG AT 2BH
    LJMP         CAN_INTERRUPT
```

```
MAIN SEGMENT CODE
RSEG    MAIN

MAIN_PROG:

------------------------ Initialization -------------------------------

    MOV         SP,#7FH                 ; set stackpointer

    CLR         EA                      ; disable all interrupts
    SETB        ES1                     ; CAN Controller interrupt enabled

    MOV         DPTR,#4000H
    MOV         A,#0FFH
    MOVX        @DPTR,A                 ; LEDs - dark

    MOV         ARRAY_LONG,#0           ; delete RAM position
    MOV         ARRAY_LONG+1,#0

    MOV         INT_SAVE,#0             ; delete interrupt save register

INIT_CAN:
    MOV         CANADR,#CONTROL         ; reset request
    MOV         CANDAT,#00000001B

    MOV         A,CANDAT
    JNB         ACC.0,INIT_CAN          ; repeat reset, if reset request is

                                        ; absent

    MOV         CANADR,#ACCEPTANCE_MASK
    MOV         CANDAT,#0FH

    MOV         CANADR,#ACCEPTANCE_CODE ; ID = 0101 XXXX XXX
    MOV         CANDAT,#05FH

    MOV         CANADR,#BUS_TIMING_0
    MOV         CANDAT,#80H

    MOV         CANADR,#BUS_TIMING_1
    MOV         CANDAT,#23H

    MOV         CANADR,#OUTPUT_CONTROL
    MOV         CANDAT,#0FAH

    MOV         CANADR,#CONTROL
    MOV         A,CANDAT

    ORL         A,#INT_MASK             ; enable receive interrupt
    ANL         A,#11111110B            ; reset request bit = 0
    MOV         CANDAT,A

    SETB        EA                      ; enable all interrupts

LOOP:
    JB          CANSTA.1,OVERRUN
    SJMP        LOOP

OVERRUN:
    MOV         A,ARRAY_LONG
    MOV         DPTR,#4100H
    MOVX        @DPTR,A                 ; first byte of message to green LED

    MOV         A,ARRAY_LONG+1
    MOV         DPTR,#4200H
    MOVX        @DPTR,A                 ; second byte of message to red LED

    SJMP        $
```

```
---------------- Receive Interrupt Service Routine ---------------------
CAN_INTERRUPT:

---------------------------- CONTEXT_SWITCH ----------------  6 cycles -

    PUSH        ACC
    PUSH        PSW
USING 1
    SETB        RS0
    CLR         RS1

---------------------------- CLEAR_INTERRUPT ---------------  1 cycle  -

CLR_INT:
    MOV         A,CANCON        ; clear interrupt bits

-------------------------- RX_INT_TARGET_ADDR --------------- 15 cycles -

BEGIN_RX:
    MOV         CANADR,#AUTO_RX_BUFFER  ; set auto incr. and CANA = 20dec
    MOV         A,CANDAT                ; fetch RX buffer
    ANL         A,#0FH                  ; upper 4 bits masked per
                                        ; acceptance filter
    MOV         R1,A
    MOV         A,CANDAT                ; fetch RX buffer+1
    MOV         R5,A                    ; temp. save of RX buffer+1
    ANL         A,#0E0H                 ; ID2,ID1,ID0,0,0,0,0,0
    RR          A                       ; 0,ID2,ID1,ID0,0,0,0,0
    ORL         A,R1                    ; 0,ID2,ID1,ID0,ID6,ID5,ID4,ID3
    ADD         A,#TABLE-TABLE_BASE
    MOVC        A,@A+PC                 ; accu contains the target address
TABLE_BASE:
    JZ          RELEASE_BUF             ; software reject - no data copying

---------------------- RX_INT_COPY_DATA_LOOP_DMA ------------  8 cycles -

    MOV         CANSTA,A                ; target address for DMA
    MOV         A,R5                    ; get RX Buffer+1
    JNB         ACC.4,DMA_START         ; test of RTR bit
    MOV         CANADR,#RX_BUFFER+1     ; in case of a Remote Frame:
    ANL         CANDAT,#0F0H            ; delete data length code,
                                        ; only the descriptor byte is copied
DMA_START:
    MOV         CANADR,#DMA_RX_BUFFER+1
    NOP                                 ; wait for data transfer
    NOP

---------------------------- RX_INT_ACKN ------------------- 2  cycles -

RELEASE_BUF:
    MOV         CANCON,#4               ; release receive buffer

------------------------- RESTORE_CONTEXT ----------------- (6) cycles -

END_RX:
    POP         PSW
    POP         ACC
    RETI

-------------------- RX_INT_TARGET_ADDRESS_TABLE -----------------------

TABLE:          ; copy data of message 01010101000 to ARRAY_LONG (8+1 bytes)
                ; copy data of message 01010101010 to ARRAY_SHORT (0+1 byte)
    DB          0,0,0,0,0,ARRAY_LONG,0,0,0,0,0,0,0,0,0 ; ID2=0,ID1=0,ID0=0
    DB          0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0         ; ID2=0,ID1=0,ID0=1
    DB          0,0,0,0,0,ARRAY_SHORT,0,0,0,0,0,0,0,0,0; ID2=0,ID1=1,ID0=0
    DB          0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0         ; ID2=0,ID1=1,ID0=1
    DB          0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0         ; ID2=1,ID1=0,ID0=0
    DB          0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0         ; ID2=1,ID1=0,ID0=1
    DB          0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0         ; ID2=1,ID1=1,ID0=0
    DB          0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0         ; ID2=1,ID1=1,ID0=1
END
```

A.2 Transmitter part

```
------------------------------ Tx Procedure --------------------------------

This module is a program including a transmit procedure using a loop that copies
data from the internal µC RAM to the Tx buffer of the P8xC592. It runs on the
P8xC592 Evaluation Board, for instance. Whenever the controller gets bus access,
the contents of the buffer is transmitted on the CAN bus. Therefore it generates
a very high bus load. The Identifier of the message has been chosen such, that
it will be received by the reference software (see Appendix A.1).

CONTROL          EQU     0H
COMMAND          EQU     1H
STATUS           EQU     2H
INTERRUPT        EQU     3H
ACCEPTANCE_CODE  EQU     4H
ACCEPTANCE_MASK  EQU     5H
BUS_TIMING_0     EQU     6H
BUS_TIMING_1     EQU     7H
OUTPUT_CONTROL   EQU     8H

CANADR           EQU     0DBH
CANDAT           EQU     0DAH
CANCON           EQU     0D9H
CANSTA           EQU     0D8H

DMA_TX_BUFFER    EQU     8AH

DSEG AT 30H
    ARRAY:       DS      10

CSEG AT RESET
    LJMP         MAIN_PROG

MAIN SEGMENT CODE
RSEG    MAIN

MAIN_PROG:

---------------------------- Initialization -------------------------------

    MOV          SP,#7FH                ; set stackpointer

    CLR          EA                     ; disable all interrupts

    MOV          DPTR,#4000H
    MOV          A,#0FFH
    MOVX         @DPTR,A                ; LEDs - dark

    MOV          ARRAY+0,#01010101B     ; ID10,ID9,ID8,ID7,ID6,ID5,ID4,ID3
    MOV          ARRAY+1,#00001000B     ; ID2,ID1,ID0,RTR,DLC3,DLC2,
                                        ; DLC1,DLC0
    MOV          ARRAY+2,#011H          ; 1st data byte
    MOV          ARRAY+3,#022H          ; 2nd data byte
    MOV          ARRAY+4,#033H          ;       .
    MOV          ARRAY+5,#044H          ;       .
    MOV          ARRAY+6,#055H          ;       .
    MOV          ARRAY+7,#066H          ;       .
    MOV          ARRAY+8,#077H          ;       .
    MOV          ARRAY+9,#088H          ; last data byte
```

```
INIT_CAN:
    MOV         CANADR,#CONTROL          ; reset request
    MOV         CANDAT,#00000001B
    MOV         A,CANDAT
    JNB         ACC.0,INIT_CAN           ; repeat reset, if reset request is
                                         ; absent

    MOV         CANADR,#ACCEPTANCE_MASK ; acceptance filter not used for Tx
    MOV         CANDAT,#0FFH

    MOV         CANADR,#BUS_TIMING_0
    MOV         CANDAT,#80H

    MOV         CANADR,#BUS_TIMING_1
    MOV         CANDAT,#23H

    MOV         CANADR,#OUTPUT_CONTROL
    MOV         CANDAT,#0FAH

    MOV         CANADR,#CONTROL
    MOV         A,CANDAT
    ANL         A,#11111110B             ; reset request bit = 0
    MOV         CANDAT,A

---------------------------- Tx Loop -----------------------------------

BEGIN_TX:
    MOV         CANSTA,#ARRAY            ; target RAM address

WAIT:
    JNB         CANSTA.2,WAIT            ; wait until Transmit Buffer access

    MOV         CANADR,#DMA_TX_BUFFER    ; Transmit Buffer = 10H
    NOP                                  ; set DMA bit
    NOP

    MOV         CANCON,#00000001B        ; transmission request

    SJMP        BEGIN_TX

END
```

CONTENTS

1 FEATURES

- 80C51 central processing unit (CPU)
- 32 kbytes on-chip ROM (EPROM), externally expandible to 64 kbytes
- 2 × 256 bytes on-chip RAM, externally expandible to 64 kbytes
- Two standard 16-bit timers/counters
- One additional 16-bit timer/counter coupled to four capture and three compare registers
- 10-bit ADC with 8 multiplexed analog inputs
- Two 8-bit resolution Pulse Width Modulated outputs
- 15 interrupt sources with 2 priority levels (2 to 6 external interrupt sources possible)
- Five 8-bit I/O ports, plus one 8-bit input port shared with analog inputs
- CAN-controller (CAN = Controller Area Network) with DMA data transfer facility to internal RAM
- 1 Mbit/s CAN-controller with bus failure management facility
- $\frac{1}{2}AV_{DD}$ reference voltage
- Full-duplex UART compatible with the standard 80C51
- On-chip Watchdog Timer (WDT)
- 1.2 to 16 MHz clock frequency (3.5 to 16 MHz for EPROM/OTP version)
- Improved Electromagnetic Compatibility (EMC).

2 GENERAL DESCRIPTION

The P8XCE598 is a single-chip 8-bit high-performance microcontroller with on-chip CAN-controller, derived from the 80C51 microcontroller family.
It uses the powerful 80C51 instruction set.
Figure 1 shows a block diagram of the P8XCE598.

The P8XCE598 is manufactured in an advanced CMOS process, and is designed for use in automotive and general industrial applications. In addition to the 80C51 standard features, the device provides a number of dedicated hardware functions for these applications.

Three versions of the P8XCE598 will be offered:

- P80CE598 (without ROM)
- P83CE598 (with ROM)
- P87CE598 (EPROM/OTP).
  OTP = One Time Programmable.

Hereafter these versions will be referred to as P8XCE598.

The temperature range includes (max. f_{CLK} = 16 MHz):

- –40 to +85 °C version, for general applications
- –40 to +125 °C version for automotive applications.

The P8XCE598 combines the functions of P8XC552 (microcontroller) and the PCA82C200 (Philips CAN-controller) with the following enhanced features:

- 32 kbytes Program Memory
- 2 × 256 bytes Data Memory
- DMA between CAN Transmit/Receive Buffer and internal RAM.

The main differences to the P8XC552 microcontroller are:

- 32 kbytes programmable ROM resp. EPROM (P8XC552 has 8 kbytes)
- Additional 256 bytes RAM
- A CAN-controller instead of the I^2C-serial interface.

2.1 Electromagnetic Compatibility (EMC)

Primary attention is paid to the reduction of electromagnetic emission of the microcontroller P8XCE598. The following features reduce the electro-magnetic emission and additionally improve the electromagnetic susceptibility:

- One analog part power supply pin (AV_{DD}) and one analog part ground pin (AV_{SS}), placed as a pair of pins on one side of the package (see Fig.3), providing power supply (+5V) and ground for ADC, CAN receiver and reference voltage.
- Four digital part supply voltage pins (V_{DD1} to V_{DD4}) and four digital part ground pins (V_{SS1} to V_{SS4}) are provided on the package. These pins, one V_{DD} and one V_{SS} as a pair of pins are placed on each of the four sides of the package to provide:
  - V_{DD1}/V_{SS1} for internal logic (CPU, Timers/counters, Memory, CAN, UART, ADC)
  - V_{DD2}/V_{SS2} for Port 1, Port 3 and Port 4, and $\overline{PWM0}$ and $\overline{PWM1}$ outputs
  - V_{DD3}/V_{SS3} for the on-chip oscillator
  - V_{DD4}/V_{SS4} for the Port 0, Port 2, ALE output and PSEN output.
- External capacitors should be connected across associated V_{DDx} and V_{SSx} pins (i.e. V_{DD1} and V_{SS1}). Lead length should be as short as possible. Ceramic chip capacitors are recommended (100 nF).

- One CAN supply voltage pin (CV_{DD}) and one CAN ground pin (CV_{SS}) as a pair of pins placed on one side of the package providing (digital part) power supply (+5V) and ground for the CAN transmitter outputs.
- On the P87CE598 version, the additional supply voltage pin (V_{PP}) providing:
  - The programming supply voltage V_{PP}
  - The alternative function for pin 65 ($\overline{EA}/V_{PP}$) on the P87CE598 EPROM/OTP version (see Fig.2 and Fig.37).
- Internal decoupling capacitance improves the EMC radiation behaviour and the EMC immunity.

2.2 Recommendation on ALE

For application that require no external memory or temporarily no external memory: the ALE output signal (pulses at a frequency of $\frac{1}{6} f_{OSC}$) can be disabled under software control (bit 5 in PCON SFR: **'RFI'**); if disabled, no ALE pulse will occur. ALE pin will be pulled down internally, switching an external address latch to a quiet state. The MOVX instruction will still toggle ALE as a normal MOVX. ALE will retain its normal HIGH value during Idle mode and a LOW value during Power-down mode while in the **'RFI** reduction mode'.

Additionally during internal access ($\overline{EA}$ = 1) ALE will toggle normally when the address exceeds the internal Program Memory size. During external access ($\overline{EA}$ = 0) ALE will always toggle normally, whether the flag **'RFI'** is set or not.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE (°C)	FREQ. (MHz)
	NAME	DESCRIPTION	VERSION		
Without ROM					
P80CE598FFB	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.7 mm; high stand-off height	SOT318-1	–40 to +85	1.2 to 16
P80CE598FHB				–40 to +125	
With ROM					
P83CE598FFB	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.7 mm; high stand-off height	SOT318-1	–40 to +85	1.2 to 16
P83CE598FHB				–40 to +125	
With EPROM/OTP					
P87CE598EFQ	CQFP80	ceramic quad flat package; 80 leads	SOT351-1	–40 to +85	3.5 to 16
P87CE598EFB	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.7 mm; high stand-off height	SOT318-1		

4 BLOCK DIAGRAM

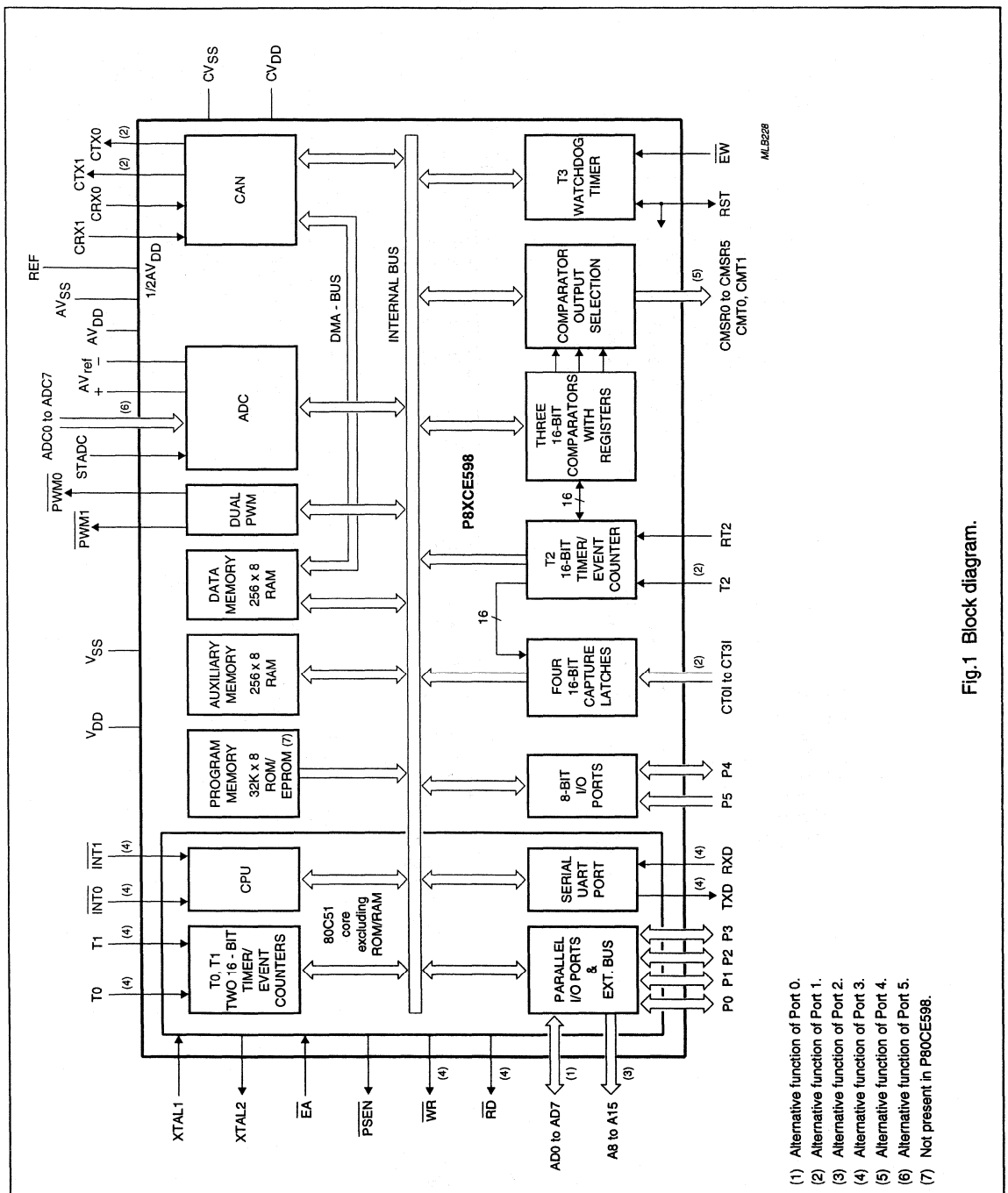
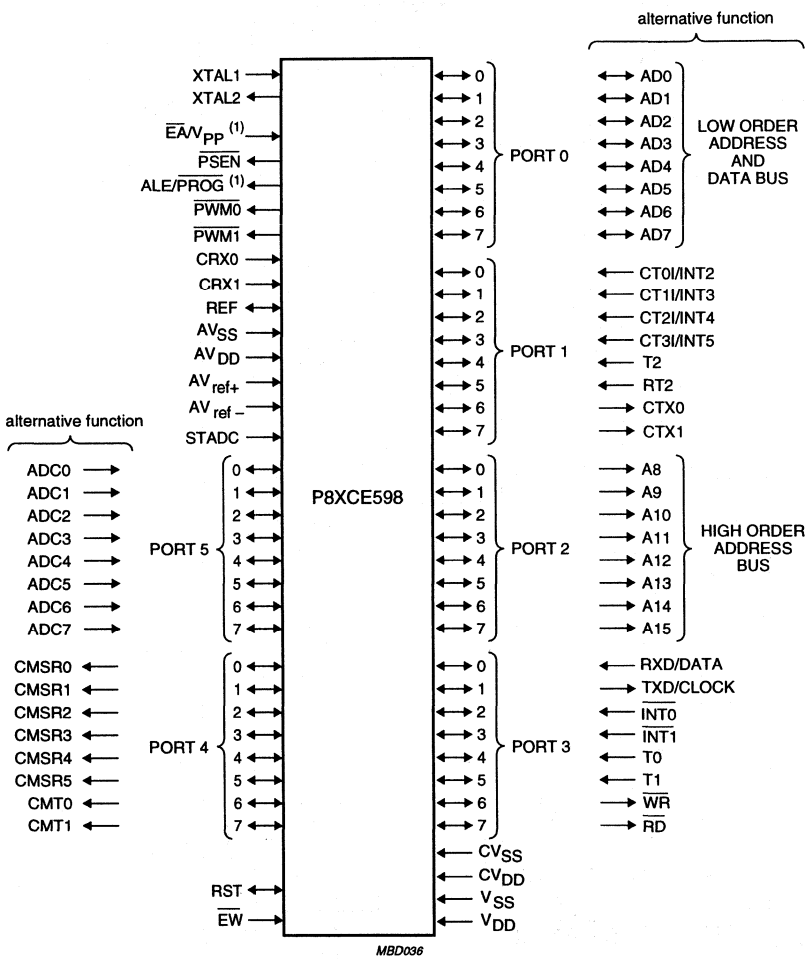


Fig.1 Block diagram.

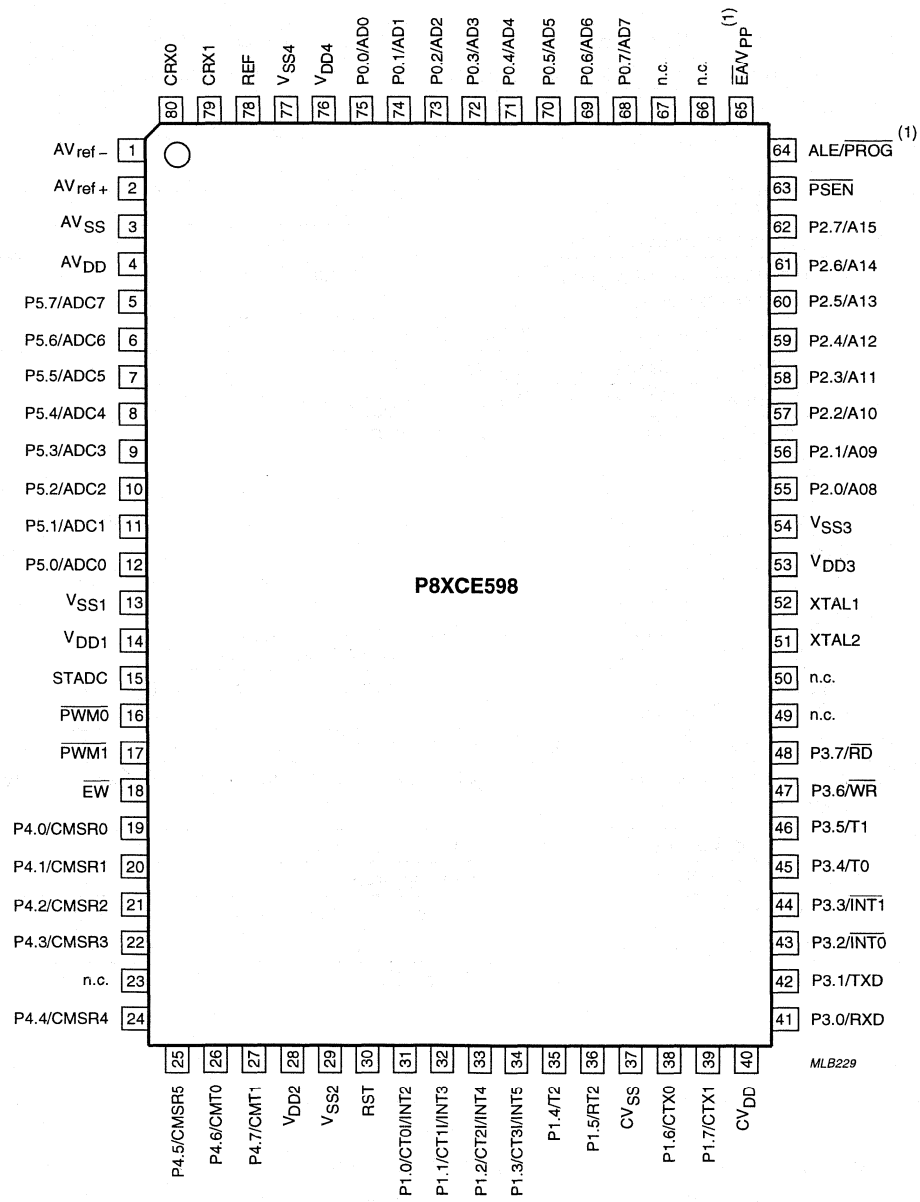
(1) Alternative function of Port 0.
(2) Alternative function of Port 1.
(3) Alternative function of Port 2.
(4) Alternative function of Port 3.
(5) Alternative function of Port 4.
(6) Alternative function of Port 5.
(7) Not present in P80CE598.

5 PINNING



(1) Only the **P87CE598** with an alternative function.

Fig.2 Pin functions.



(1) Only **P87CE598** with an alternative function.

Fig.3 Pin configuration QFP80/SOT318-1 and CQFP80/SOT351-1.

Table 1 Pin description for **single function** pins (SOT318-1 and SOT351-1; see note 1)

SYMBOL	PIN	DESCRIPTION
V_{DD1}	14	**Power supply, digital part:** for internal logic (CPU, Timers/counters, Memory, CAN, UART, ADC).
V_{DD2}	28	**Power supply, digital part:** for Port 1, Port 3, Port 4, $\overline{PWM0}$ and $\overline{PWM1}$ outputs.
V_{DD3}	53	**Power supply, digital part:** for the on-chip oscillator.
V_{DD4}	76	**Power supply, digital part:** for Port 0, Port 2, ALE output and $\overline{PSEN}$ output.
STADC	15	**Start ADC operation.** Input starting analog-to-digital conversion (note 2). This pin must not float.
$\overline{PWM0}$	16	**Pulse width modulation** output 0.
$\overline{PMW1}$	17	**Pulse width modulation** output 1.
$\overline{EW}$	18	**Enable Watchdog Timer (WDT):** enable for T3 Watchdog Timer and disable Power-down mode. This pin must not float.
RST	30	**Reset:** input to reset the P8XCE598 (note 3).
CV_{SS}	37	**Ground** potential for the CAN transmitter outputs.
CV_{DD}	40	**Power supply** (+5V) for the CAN transmitter outputs.
XTAL2	51	**Crystal pin 2:** output of the inverting amplifier that forms the oscillator. When an external clock oscillator is used this pin is left open-circuit.
XTAL1	52	**Crystal pin 1:** input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external clock oscillator signal, when an external oscillator is used.
V_{SS1}	13	**Ground, digital part:** for internal logic (CPU, Timers/Counters, Memory, CAN, UART, ADC).
V_{SS2}	29	**Ground, digital part:** for Port 1, Port 3 and Port 4, and $\overline{PWM0}$ and $\overline{PWM1}$ outputs.
V_{SS3}	54	**Ground, digital part:** for the on-chip oscillator.
V_{SS4}	77	**Ground, digital part:** for the Port 0, Port 2, ALE output and $\overline{PSEN}$ output.
$\overline{PSEN}$	63	**Program Store Enable:** Read strobe to external Program Memory (active LOW). Drive: 8 × LSTTL inputs.
REF	78	**$\frac{1}{2}AV_{DD}$ reference voltage** output respectively input (note 4).
CRX1	79	**Inputs from the CAN-bus line** to the differential input comparator of the on-chip CAN-controller (note 5).
CRX0	80	
AV_{REF-}	1	**Low-end of ADC** (analog-to-digital conversion) reference resistor.
AV_{REF+}	2	**High-end of ADC** (analog-to-digital conversion) reference resistor (note 6).
AV_{SS}	3	**Ground, analog part.** For ADC, CAN receiver and reference voltage.
AV_{DD}	4	**Power supply, analog part** (+5 V). For ADC, CAN receiver and reference voltage.
n.c.	23, 49, 50, 66, 67	**No connection** (both SOT318-2 and SOT351-1).

Notes

1. To avoid a 'latch up' effect at power-on: $V_{SS} - 0.5\ V <$ 'voltage on any pin at any time' $< V_{DD} + 0.5\ V$.
2. Triggered by a rising edge. ADC operation can also be started by software.
3. RST also provides a reset pulse as output when timer T3 overflows or after a CAN wake-up from Power-down.

4. Pin 78, REF:
   a) Selection of input respectively output dependent of CAN Control Register bit 5 (CR.5; see Section 13.5.3 Table 32).
   b) If the internal reference is used, then REF should be connected to AV_{SS} via a capacitor with a value of $\geq$ 10 nF.
   c) After an external reset (RST = HIGH) the internal $\frac{1}{2}AV_{DD}$ source is activated and, REF is a reference output.
   d) If the CAN-controller is in the reset state, e.g. after an external reset, then the $\frac{1}{2}AV_{DD}$ source is switched off during Power-down mode.
5. CAN Bus line:
   a) CRX0 level > CRX1 level is interpreted as a logic 1 (recessive).
   b) CRX0 level < CRX1 level is interpreted as a logic 0 (dominant).
6. The level of AV_{REF+} must be higher than that of AV_{REF-}.

Table 2 Pin description for pins with **alternative functions** (SOT318-2 and SOT351-1; see note 1)

SYMBOL		PIN	DESCRIPTION
DEFAULT	**ALTERNATIVE**		
Port 4			
P4.0 to P4.7		19 to 22, 24 to 27	**8-bit quasi-bidirectional I/O port.**
	CMSR0	19	**Compare and Set/Reset outputs** for Timer T2.
	CMSR1	20	
	CMSR2	21	
	CMSR3	22	
	CMSR4	24	
	CMSR5	25	
	CMT0	26	**Compare and toggle outputs** for Timer T2.
	CMT1	27	
Port 1			
P1.0 to P1.7		31 to 36, 38 to 39	**8-bit quasi-bidirectional I/O port.**
	CT0I/INT2	31	**Capture timer inputs** for Timer T2, or **External interrupt inputs** 2 to 5.
	CT1I/INT3	32	
	CT2I/INT4	33	
	CT3I/INT5	34	
	T2	35	**T2 event input** (rising edge triggered).
	RT2	36	**T2 timer reset input** (rising edge triggered).
	CTX0	38	**CAN transmitter** output 0 (note 2).
	CTX1	39	**CAN transmitter** output 1 (note 2).

SYMBOL		PIN	DESCRIPTION
DEFAULT	ALTERNATIVE		
Port 3			
P3.0 to P3.7		41 to 48	**8-bit quasi-bidirectional I/O port.**
	RXD	41	**Serial Input Port.**
	TXD	42	**Serial Output Port.**
	$\overline{INT0}$	43	**External interrupt input 0.**
	$\overline{INT1}$	44	**External interrupt input 1.**
	T0	45	**Timer 0 external input.**
	T1	46	**Timer 1 external input.**
	$\overline{WR}$	47	**External Data Memory Write strobe.**
	$\overline{RD}$	48	**External Data Memory Read strobe.**
Port 2 (Sink/source: 1 × TTL = 4 × LSTTL inputs)			
P2.0 to P2.7		55 to 62	**8-bit quasi-bidirectional I/O port.**
	A08 to A15		**High-order address byte for external memory.**
ALE/$\overline{PROG}$ (Drive: 8 × LSTTL inputs; handles CMOS inputs without an external pull-up)			
ALE		64	**Address Latch Enable:** latches the Low-byte of the address during accesses to external memory (note 3).
	$\overline{PROG}$		**Programming-pulse input for P87CE598.**
$\overline{EA}$/V_{PP}			
$\overline{EA}$		65	**External Access input.** See note 4.
	V_{PP}		**Programming supply voltage for P87CE598.**
Port 0 (Sink/source: 8 × LSTTL inputs)			
P0.7 to P0.0		68 to 75	**8-bit open drain bidirectional I/O port.**
	AD7 to AD0		**Multiplexed Low-order address and Data bus for external memory.**
Port 5			
P5.7 to P5.0		5 to 12	**8-bit input port.**
	ADC7 to ADC0		**8 input channels to ADC.**

Notes

1. To avoid a 'latch up' effect at power-on: $V_{SS} - 0.5\ V <$ 'voltage on any pin at any time' $< V_{DD} + 0.5\ V$.
2. If the CAN-controller is in the reset state (e.g. after a power-up reset; CAN Control Register bit CR.0; see Section 13.5.3 Table 32, the CAN transmitter outputs are floating and the pins P1.6 and P1.7 can be used as open-drain port pins. After a power-up reset the port data is HIGH, leaving the pins P1.6 and P1.7 floating.
3. ALE is activated every six oscillator periods. During an external data memory access one ALE pulse is skipped.
4. See Section 7.1, Table 3 for $\overline{EA}$ operation. For P83CE598 microcontrollers specified with the option 'ROM-code protection', the $\overline{EA}$ pin is latched during reset and is 'don't care' after reset, regardless of whether the ROM-code protection is selected or not.

6 FUNCTIONAL DESCRIPTION

The P8XCE598 functions will be described as shown in the following overview:

- Memory organization
- I/O Port structure
- Pulse Width Modulated outputs
- Analog-to-Digital Converter
- Timers/Counters
- Serial I/O Ports
- Interrupt system
- Power reduction modes
- Oscillator circuitry
- Reset circuitry
- Instruction Set
- EMC (see Section 2.1).

7 MEMORY ORGANIZATION

The Central Processing Unit (CPU) manipulates operands in three memory spaces (see Fig.4) as follows:

- 32 kbytes internal, resp. 64 kbytes external Program Memory
- 512 bytes internal Data Memory MAIN- and AUXILIARY RAM.
- Up to 64 kbytes external Data Memory (with 256 bytes residing in the internal AUXILIARY RAM).

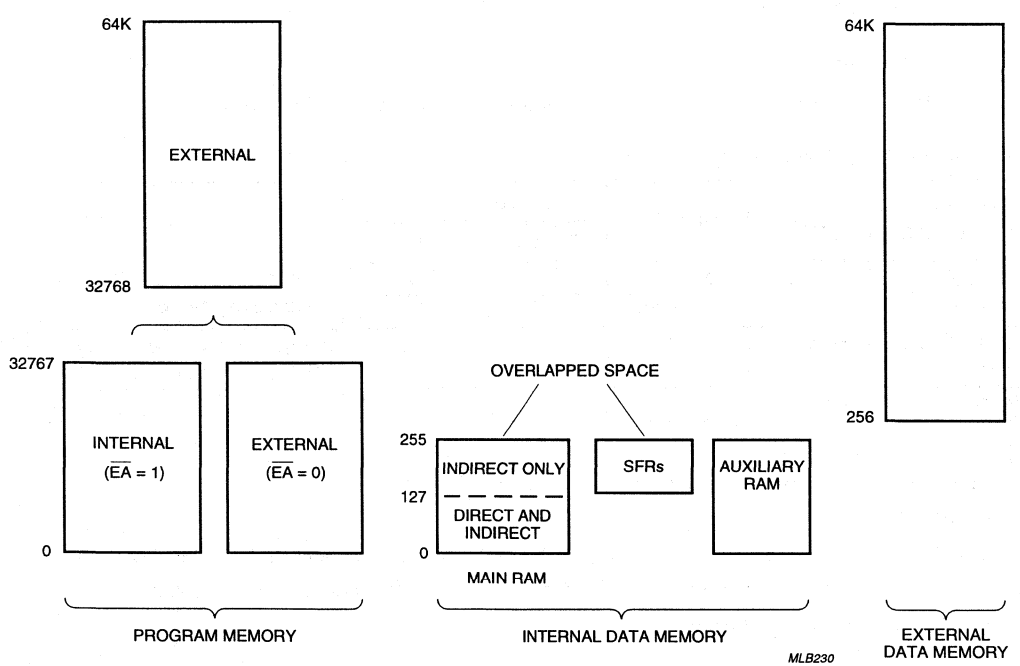


Fig.4 Memory map.

7.1 Program Memory

The Program Memory of the P8XCE598 consists of 32 kbytes ROM resp. EPROM on-chip, externally expandible up to 64 kbytes.

Table 3 Instruction fetch controlled by $\overline{EA}$

PIN $\overline{EA}$ (note 1)		INSTRUCTIONS FETCHED FROM:	ADDRESS LOCATION
DURING RESET LATCHED TO:	AFTER RESET		
H	–	internal Program Memory (note 2)	0000H → 7FFFH
H	–	external Program Memory	8000H → FFFFH
L	–		0000H → FFFFH
–	'don't care'	–	–

Notes

1. This implementation prevents reading of the internal program code by switching from external Program Memory during a MOVC instruction.
2. By setting a security bit the internal Program Memory content is protected, which means it cannot be read out. If the security bit has been set to LOW there are no restrictions for the MOVC instruction. For code protection of the P87CE598 see Section 22.2 "Security".

7.2 Internal Data Memory

The internal Data Memory is physically built-up and accessible as shown in Table 4 (see Fig.5).

Table 4 Internal Data Memory size and address mode

INTERNAL DATA MEMORY	SIZE	LOCATION	ADDRESS MODE		POINTERS
			DIRECT	INDIRECT	
MAIN RAM (note 1)	256 bytes	0 to 127	X	X	Address pointers are R0 and R1 of the selected register bank.
		128 to 255	–	X	
AUXILIARY RAM (note 2)	256 bytes	0 to 255	–	X	Address pointers are R0 and R1 of the selected register bank and the DPTR.
SFRs (note 3)	128 bytes	128 to 255	X	–	–

Notes

1. MAIN RAM can be addressed directly and indirectly as in the 80C51.
2. AUXILIARY RAM (0 to 255):
   a) Is indirectly addressable in the same way as the external Data Memory with MOVX instructions.
   b) Access will not affect the ports P0, P2, P3.6 and P3.7 during internal program execution.
3. SFRs = Special Function Registers.

7.2.1 MAIN RAM

Four 8-bit register banks occupy the lower RAM area,

- BANK 0: location 0 to 7
- BANK 1: location 8 to 15
- BANK 2: location 16 to 23
- BANK 4: location 24 to 31.

Only one of these banks may be enabled at the same time.

The next 16 bytes, locations 32 through 45, contains 128 directly addressable bit locations.

The stack can be located anywhere in the internal Main RAM address space. The stack depth is only limited by the internal RAM space available. All registers except the program counter and the four 8-bit register banks reside in the SFR address space.

7.3 External Data Memory

An access to external Data Memory locations higher than 255 will be performed with the MOVX @DPTR instructions in the same way as in the 80C51 structure, i.e.with P0 and P2 as data/address bus and P3.6 and P3.7 as Write and Read strobe signals.

Note that these external Data Memory locations cannot be accessed with R0 or R1 as address pointer.

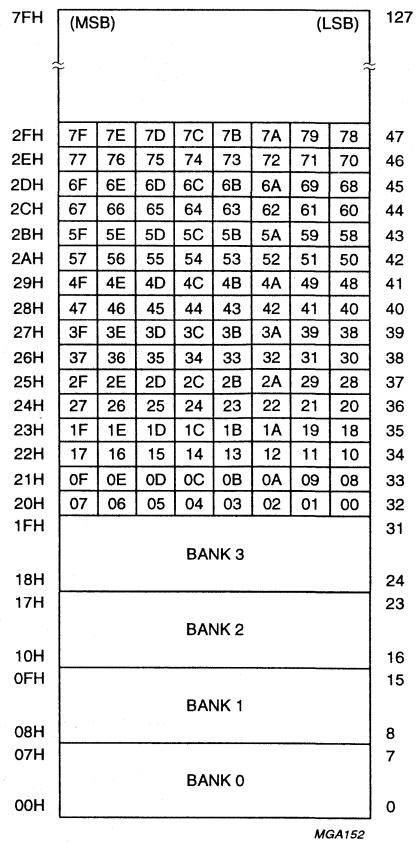


Fig.5 Internal MAIN RAM bit addresses.

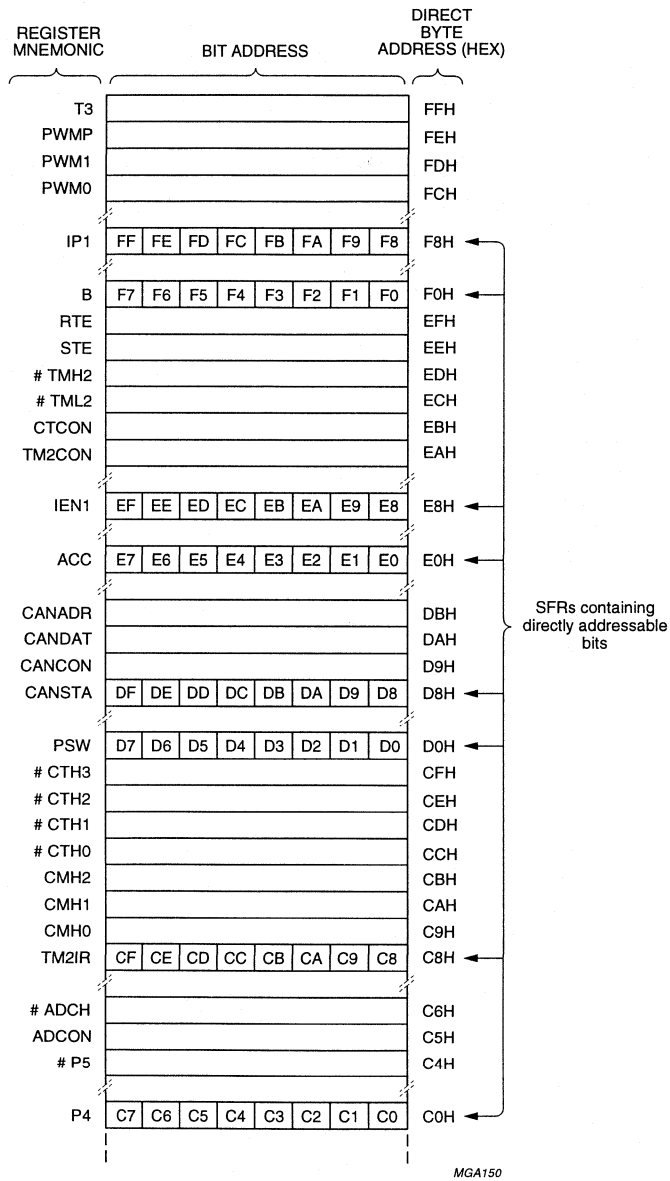


Fig.6 Special Function Register memory map (a).

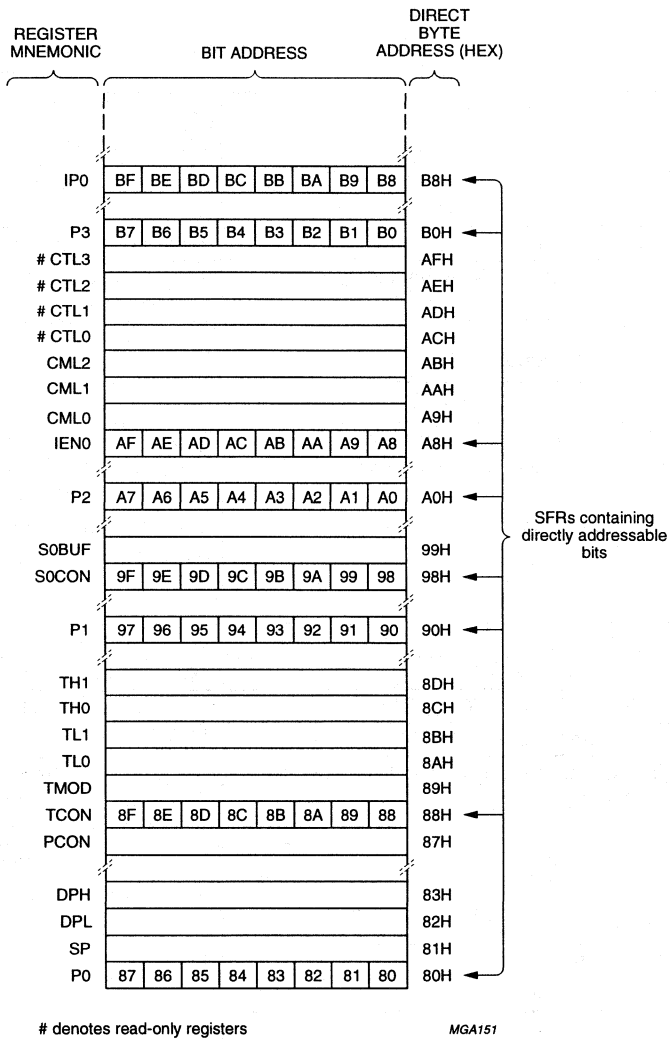


Fig.7 Special Function Register memory map (b).

8 I/O PORT STRUCTURE

The P8XCE598 has six 8-bit parallel ports: Port 0 to Port 5. In addition to the standard 8-bit parallel ports, the I/O facilities also include a number of special I/O lines. The use of a Port 1, Port 3 or Port 4 pins as an alternative function is carried out automatically provided the associated SFR bit is set HIGH.

Table 5 Default Port functions

PORT	TYPE	FUNCTION	REMARKS
Port 0	I/O	The same as in the 80C51	Except for the additional functions of P1.6 and P1.7.
Port 1	I/O		
Port 2	I/O		
Port 3	I/O		
Port 4	I/O	Parallel I/O port	Parallel I/O function is identical to Port1, 2 and 3.
Port 5	I	Parallel input port with an input function only	May be used as normal inputs if the ADC function is inoperative.

Table 6 Alternative Port functions

PORT	TYPE	FUNCTION	REMARKS
Port 0	I/O	Multiplexed Low-order address and Data bus for external memory (AD7 to AD0)	Provides the multiplexed Low-order address and data bus used for expanding the P8XCE598 with standard memories and peripherals.
Port 1	I/O	Capture timer inputs for Timer T2 (CT0I to CT3I), or External interrupt request inputs (INT2 to INT5)	External interrupt request inputs, if capture information is not utilized.
		T2 event input (T2)	External counter input.
		T2 timer reset input (RT2)	External counter reset input.
		CAN transmitter output 0 (CTX0)	CTX0 and CTX1 outputs of the CAN interface (note 1).
		CAN transmitter output 1 (CTX1)	
Port 2	I/O	High-order address byte for external memory (A08 to A15)	Port 2 provides the High-order address bus when the P8XCE598 is expanded with external Program Memory and/or external Data Memory.
Port 3	I/O	Serial Input Port (RXD)	Receiver input of serial port SIO0 (UART).
		Serial Output Port (TXD)	Transmitter output of serial port SIO0 (UART).
		External interrupt ($\overline{\text{INT0}}$)	External interrupt request inputs.
		External interrupt ($\overline{\text{INT1}}$)	
		Timer 0 external input (T0)	Counter inputs.
		Timer 1 external input (T1)	
		External data memory Write strobe ($\overline{\text{WR}}$)	Control signal to write to external Data Memory.
		External data memory Read strobe ($\overline{\text{RD}}$)	Control signal to read from external Data Memory.
Port 4	I/O	Compare and Set/Reset outputs (CMSR0 to CMSR5)	Can be configured to provide signals indicating a match between Timer counter T2 and its compare registers.
		Compare and toggle outputs (CMT0, CMT1)	
Port 5	I	Input channels to ADC (ADC7 to ADC0)	Port 5 may be used in conjunction with the ADC interface (note 2).

Notes to the Alternative Port functions

1. Port lines P1.6 and P1.7 may be selected as CTX0 and CTX1 outputs of the serial port SIO1 (CAN). After reset P1.6 and P1.7 may be used as normal I/O ports, if the CAN interface is not used.
2. Unused analog inputs can be used as digital inputs. As Port 5 lines may be used as inputs to the ADC, these digital inputs have an inherent hysteresis to prevent the input logic from drawing too much current from the power lines when driven by analog signals.
   Channel-to-channel crosstalk should be taken into consideration when both digital and analog signals are simultaneously input to Port 5 (see Chapter 20).

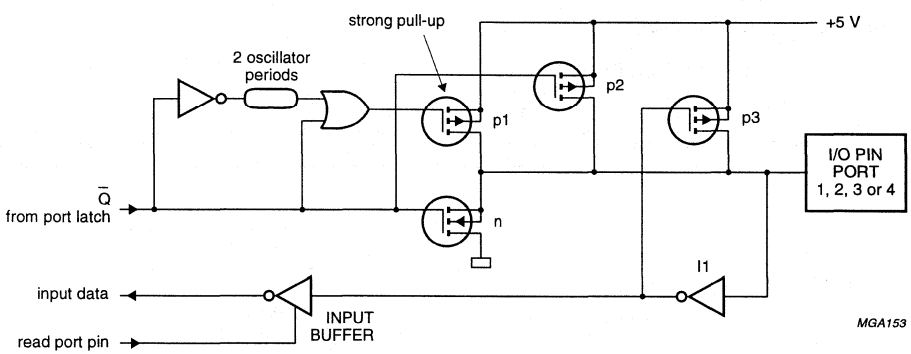


Fig.8 I/O buffers in the P8XCE598 (P1.0 to P1.5, Ports 2, 3, and 4).

9 PULSE WIDTH MODULATED OUTPUTS (PWM)

Two Pulse Width Modulated (PWM) output channels are available with the P8XCE598. These channels provide output pulses of programmable length and interval. The repetition frequency is defined by an 8-bit prescaler PWMP which generates the clock for the counter. Both the prescaler and counter are common to both PWM channels. The 8-bit counter counts modulo 255 i.e. from 0 to 254 inclusive. The value of the 8-bit counter is compared to the contents of two registers: PWM0 and PWM1.

Provided the contents of either of these registers is greater than the counter value, the output of $\overline{\text{PWM0}}$ or $\overline{\text{PWM1}}$ is set LOW. If the contents of these register are equal to, or less than the counter value, the output will be HIGH. The pulse-width-ratio is therefore defined by the contents of the register PWM0 and PWM1. The pulse-width-ratio is in the range of 0 to $^{255}/_{255}$ and may be programmed in increments of $^{1}/_{255}$.

The repetition frequency f_{PWM}, at the $\overline{\text{PWMn}}$ outputs is given by: $f_{PWM} = \frac{f_{CLK}}{2 \times (PWMP + 1) \times 255}$

When using an oscillator frequency of 16 MHz, for example, the above formula would give a repetition frequency range of 123 Hz to 31.4 kHz.

By loading the PWM registers with either 00H or FFH, the PWM outputs can be retained at a constant HIGH or LOW level respectively. When loading FFH to the PWM registers, the 8-bit counter will never actually reach this (FFH) value.
Both output pins $\overline{\text{PWMn}}$ are driven by push-pull drivers, and are not shared with any other function.

9.1 Prescaler frequency control register (PWMP)

Table 7 Prescaler frequency control register (address FEH)

7	6	5	4	3	2	1	0
PWMP.7	PWMP.6	PWMP.5	PWMP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.0

Table 8 Description of PWMP bits

BIT	SYMBOL	FUNCTION
7 to 0	PWMP.7 to PWMP.0	**Prescaler division factor.** The Prescaler division factor = (PWMP) + 1

9.2 Pulse Width Register 0 (PWM0)

Table 9 Pulse Width Register (address FCH)

7	6	5	4	3	2	1	0
PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0

Table 10 Description of PWM0 bits

BIT	SYMBOL	FUNCTION
7 to 0	PWM0.7 to PWM0.0	**Pulse width ratio.** LOW/HIGH ratio of $\overline{PWMn}$ signals $= \frac{(PWMn)}{255 - (PWMn)}$

9.3 Pulse Width Register 1 (PWM1)

Table 11 Pulse width register (address FDH)

7	6	5	4	3	2	1	0
PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0

Table 12 Description of PWM1 bits

BIT	SYMBOL	FUNCTION
7 to 0	PWM1.7 to PWM1.0	**Pulse width ratio.** LOW/HIGH ratio of $\overline{PWMn}$ signals $= \frac{(PWMn)}{255 - (PWMn)}$

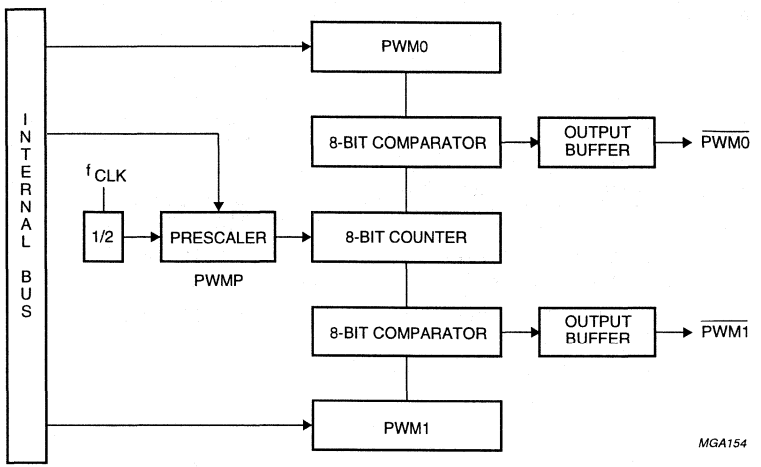


Fig.9 Functional diagram of Pulse Width Modulated outputs.

10 ANALOG-TO-DIGITAL CONVERTER (ADC)

The analog input circuitry consists of an 8-input analog multiplexer and an ADC with 10-bit resolution. The analog reference voltage and analog power supplies are connected via separate input pins. The conversion takes 50 machine cycles i.e. 37.5 µs at 16 MHz oscillator frequency. The input voltage swing is from 0 V to AV_{DD}. The ADC is controlled using the ADCON control register. Register bits ADCON.0 to ADCON.2 select the input channels of the analog multiplexer (see Fig.10).
The completion of the 10-bit analog-to-digital conversion is flagged by ADCI in the ADCON register and the result is stored in the SFR ADCH (upper 8-bits) and the 2 lower bits (ADC.1 and ADC.0) in register ADCON.

An analog-to-digital conversion in progress is unaffected by an external or software ADC start. The result of a completed conversion remains unchanged provided ADCI = HIGH. While ADCI or ADCS are HIGH, a new ADC START will be blocked and consequently lost. An analog-to-digital conversion already in progress is aborted when the Idle or Power-down mode is entered.

The result of a completed conversion (ADCI = HIGH) remains unaffected during the Idle mode.
The LOW-to-HIGH transition of STADC is recognized at the end of a machine cycle and the conversion commences at the beginning of the next cycle. When a conversion is initiated by software, the conversion starts at the beginning of the machine cycle following the instruction that sets ADCS.

The next two machine cycles are used to initiate the converter. At the end of this first cycle, the ADCS status flag is set to HIGH while the conversion is in progress. Sampling of the analog input commences at the end of the second cycle.

During the next eight machine cycles, the voltage at the previously selected pin of Port 5 is sampled and this input voltage should be stable in order to obtain a useful sample. In any case, the input voltage slew rate must be less than 10 V/ms (5 V conversion range) in order to prevent an undefined result. The conversion takes four machine cycles per bit.

10.1 ADC Control register (ADCON)

Table 13 ADC Control register (address C5H)

7	6	5	4	3	2	1	0
ADC.1	ADC.0	ADEX	ADCI	ADCS	AADR2	AADR1	AADR0

Table 14 Description of the ADCON bits

BIT	SYMBOL	FUNCTION
7	ADC.1	Bit 1 of ADC converted value.
6	ADC.0	Bit 0 of ADC converted value.
5	ADEX	Enable external start of conversion by STADC. If ADEX is: LOW, then conversion cannot be started externally by STADC (only by software by setting ADCS) HIGH, then conversion can be started externally by a rising edge on STADC or externally.
4	ADCI	**ADC interrupt flag.** This flag is set when an analog-to-digital conversion result is ready to be read. If enabled, an interrupt is invoked. The flag must be cleared by software. It cannot be set by software (see Table 15).
3	ADCS	**ADC start and status.** Setting this bit starts an analog-to-digital conversion. It may be set by software or by the external signal STADC. The ADC logic ensures that this signal is HIGH while the ADC is busy. On completion of the conversion, ADCS is reset at the same time the interrupt flag ADCI is set. ADCS can not be reset by software (see Table 15).
2	AADR2	**Analog input select.** This binary coded address selects one of the eight analog port pins of P5 to be input to the converter. It can only be changed when ADCI and ADCS are both LOW. AADR2 is the MSB (e.g. 100B selects the analog input channel ADC4).
1	AADR1	
0	AADR0	

Table 15 ADCI and ADCS operating modes

If ADCI is cleared by software while ADCS is set at the same time a new analog-to-digital conversion with the same channel-number may be started. It is recommended to reset ADCI before ADCS is set.

ADCI	ADCS	OPERATION
0	0	ADC not busy, a conversion can be started.
0	1	ADC busy, start of a new conversion is blocked.
1	X (don't care)	Conversion completed (note 1).

Note

1. Start of a new conversion requires ADCI = 0.

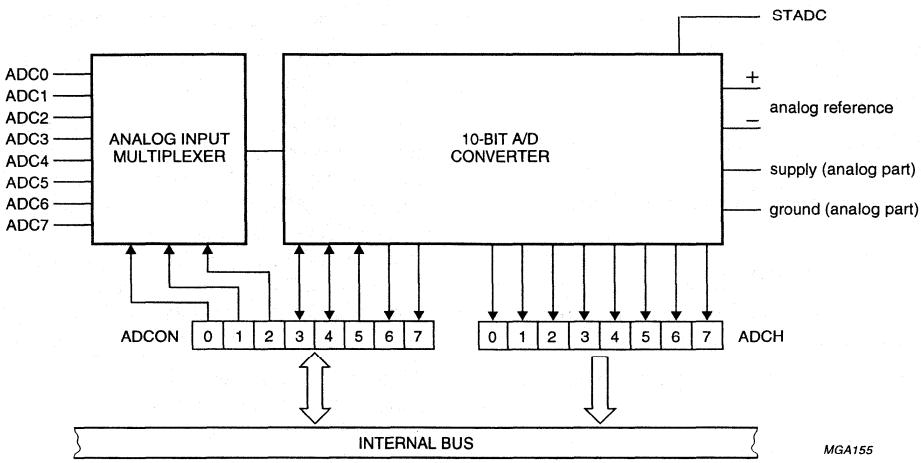


Fig.10 Functional diagram of analog input.

11 TIMERS/COUNTERS

The P8XCE598 contains:

- Three 16-bit timer/event counters: Timer 0, Timer 1 and Timer 2
- One 8-bit timer, T3 (Watchdog WDT).

11.1 Timer 0 and Timer 1

Timer 0 and Timer 1 may be programmed to carry out the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests.

Timer 0 and Timer 1 can be programmed independently to operate in 3 modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.

Mode 1 16-bit timer-interval or event counter.

Mode 2 8-bit timer-interval or event counter with automatic reload upon overflow.

Timer 0 can be programmed to operate in an additional mode as follows:

Mode 3 one 8-bit time-interval or event counter and one 8-bit timer-interval counter.

When Timer 0 is in Mode 3, Timer 1 can be programmed to operate in Modes 0, 1 or 2 but cannot set an interrupt flag or generate an interrupt. However, the overflow from Timer 1 can be used to pulse the Serial Port baud-rate generator.

The frequency handling range of these counters with a 16 MHz crystal is as follows:

- In the timer function, the timer is incremented at a frequency of 1.33 MHz ($1/12$ of the oscillator frequency)
- 0 Hz to an upper limit of 0.66 MHz ($1/24$ of the oscillator frequency) when programmed for external inputs.

Both internal and external inputs can be gated to the counter by a second external source for directly measuring pulse durations. When configured as a counter, the register is incremented on every falling edge on the corresponding input pin, T0 or T1.

The earliest moment, when the incremented register value can be read is during the second machine cycle following the machine cycle within which the incrementing pulse occurred.The counters are started and stopped under software control. Each one sets its interrupt request flag when it overflows from all HIGHs to all LOWs (or automatic reload value), with the exception of Mode 3 as previously described.

11.2 Timer T2 Capture and Compare Logic

Timer T2 is a 16-bit timer/counter which has capture and compare facilities (see Fig.11).

The 16-bit timer/counter is clocked via a prescaler with a programmable division factor of 1, 2, 4 or 8. The input of the prescaler is clocked with $1/12$ of the oscillator frequency, or by an external source connected to the T2 input, or it is switched off. The maximum repetition rate of the external clock source is $1/12 f_{CLK}$, twice that of Timer 0 and Timer 1. The prescaler is incremented on a rising edge. It is cleared if its division factor or its input source is changed, or if the timer/counter is reset.

T2 is readable 'on the fly', without any extra read latches; this means that software precautions have to be taken against misinterpretation at overflow from least to most significant byte while T2 is being read. T2 is not loadable and is reset by the RST signal or at the positive edge of the input signal RT2, if enabled. In the Idle mode the timer/counter and prescaler are reset and halted.

T2 is connected to four 16-bit Capture Registers: CT0, CT1, CT2 and CT3. A rising or falling edge on the inputs CT0I, CT1I, CT2I or CT3I (alternative function of Port 1) results in loading the contents of T2 into the respective Capture Registers and an interrupt request.

Using the Capture Register CTCON, these inputs may invoke capture and interrupt request on a positive edge, a negative edge or on both edges. If neither a positive nor a negative edge is selected for capture input, no capture or interrupt request can be generated by this input.

The contents of the Compare Registers CM0, CM1 and CM2 are continually compared with the counter value of Timer T2. When a match occurs, an interrupt may be invoked. A match of CM0 sets the bits 0 to 5 of Port 4, a CM1 match resets these bits and a CM2 match toggles bits 6 and 7 of Port 4, provided these functions are enabled by the STE/RTE registers. A match of CM0 and CM1 at the same time results in resetting bits 0 to 5 of Port 4. CM0, CM1 and CM2 are reset by the RST signal.

Port 4 can be read and written by software without affecting the toggle, set and reset signals. At a byte overflow of the least significant byte, or at a 16-bit overflow of the timer/counter, an interrupt sharing the same interrupt vector is requested. Either one or both of these overflows can be programmed to request an interrupt. All interrupt flags must be reset by software.

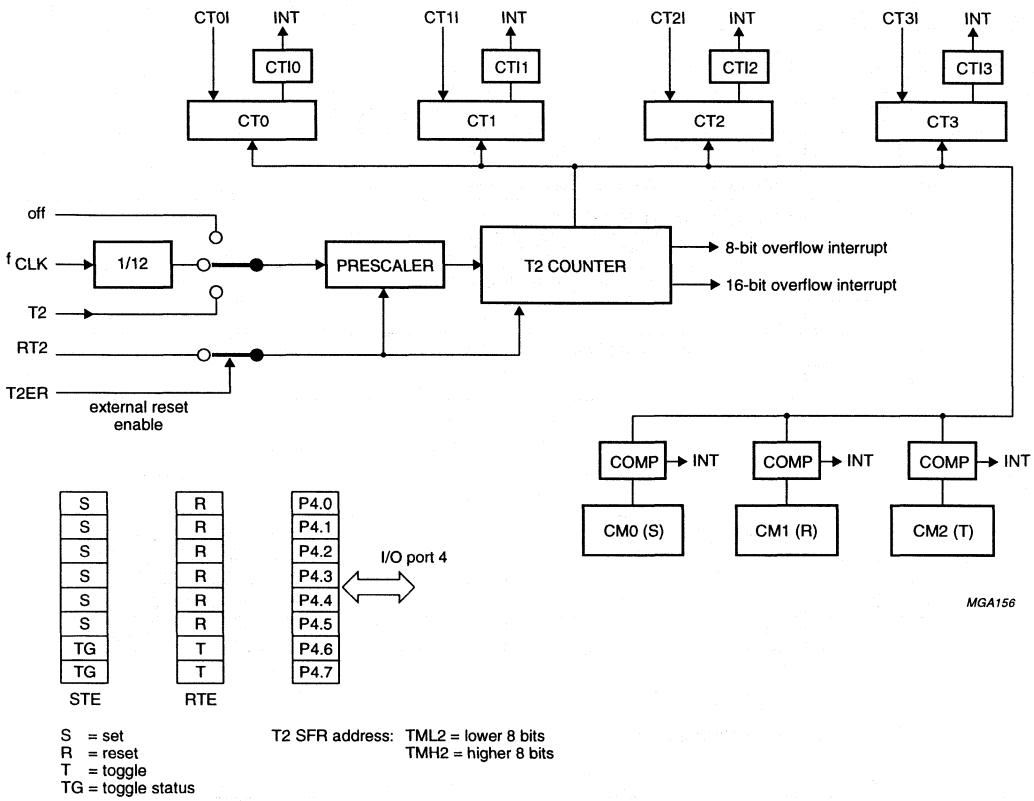


Fig.11 Block diagram of Timer T2 configuration.

11.2.1 Counter Control register (TM2CON)

Table 16 Counter Control register (address EAH)

7	6	5	4	3	2	1	0
T2IS1	T2IS0	T2ER	T2B0	T2P1	T2P0	T2MS1	T2MS0

Table 17 Description of the TM2CON bits

BIT	SYMBOL	FUNCTION
7	T2IS1	Timer 2 16-bit overflow interrupt select.
6	T2IS0	Timer 2 byte overflow interrupt select.
5	T2ER	Timer 2 external reset enable.
4	T2B0	Timer 2 byte overflow interrupt flag.
3	T2P1	Timer 2 prescaler select (see Table 18).
2	T2P0	
1	T2MS1	Timer 2 mode select (see Table 19).
0	T2MS0	

Table 18 Timer 2 prescaler select

T2P1	T2P0	T2 CLOCK
0	0	Clock source
0	1	$\frac{1}{2}$ Clock source
1	0	$\frac{1}{4}$ Clock source
1	1	$\frac{1}{8}$ Clock source

Table 19 Timer 2 mode select

T2MS1	T2MS0	MODE
0	0	Timer T2 is halted
0	1	T2 clock source = $\frac{1}{12}f_{CLK}$
1	0	Test mode; do not use
1	1	T2 clock source = pin T2

11.2.2 Capture Control register (CTCON)

Table 20 Capture Control register (address EBH)

7	6	5	4	3	2	1	0
CTN3	CTP3	CTN2	CTP2	CTN1	CTP1	CTN0	CTP0

Table 21 Description of the CTCON bits

BIT	SYMBOL	FUNCTION	
		CAPTURE	INTERRUPT ON
7	CTN3	CT3I	negative edge
6	CTP3	CT3I	positive edge
5	CTN2	CT2I	negative edge
4	CTP2	CT2I	positive edge
3	CTN1	CT1I	negative edge
2	CTP1	CT1I	positive edge
1	CTN0	CT0I	negative edge
0	CTP0	CT0I	positive edge

11.2.3 TIMER INTERRUPT FLAG REGISTER (TM2IR)

Table 22 Timer Interrupt Flag register (address C8H)

7	6	5	4	3	2	1	0
T2OV	CMI2	CMI1	CMI0	CTI3	CTI2	CTI1	CTI0

Table 23 Description of the TM2IR bits (see notes 1 and 2)

BIT	SYMBOL	FUNCTION
7	T2OV	T2: 16-bit overflow interrupt flag.
6	CMI2	CM2: interrupt flag.
5	CMI1	CM1: interrupt flag.
4	CMI0	CM0: interrupt flag.
3	CTI3	CT3: interrupt flag.
2	CTI2	CT2: interrupt flag.
1	CTI1	CT1: interrupt flag.
0	CTI0	CT0: interrupt flag.

Notes

1. Interrupt Enable IEN1 is used to enable/disable Timer 2 interrupts (see Section 14.1.2).
2. Interrupt Priority Register IP1 is used to determine the Timer 2 interrupt priority (see Section 14.1.4).

11.2.4 SET ENABLE REGISTER (STE)

Table 24 Set Enable register (address EEH)

7	6	5	4	3	2	1	0
TG47	TG46	SP45	SP44	SP43	SP42	SP41	SP40

Table 25 Description of the STE bits (see notes 1 and 2)

BIT	SYMBOL	FUNCTION
7	TG47	if HIGH then P4.7 is reset on the next toggle, if LOW P4.7 is set on the next toggle.
6	TG46	if HIGH then P4.6 is reset on the next toggle, if LOW P4.6 is set on the next toggle.
5	SP45	if HIGH then P4.5 is set on a match of CM0 and T2.
4	SP44	if HIGH then P4.4 is set on a match of CM0 and T2.
3	SP43	if HIGH then P4.3 is set on a match of CM0 and T2.
2	SP42	if HIGH then P4.2 is set on a match of CM0 and T2.
1	SP41	if HIGH then P4.1 is set on a match of CM0 and T2.
0	SP40	if HIGH then P4.0 is set on a match of CM0 and T2.

Notes

1. If STE.n is LOW then P4.n is not affected by a match of CM0 and T2 (n = 0, 1, 2, 3, 4, 5).
2. STE.6 and STE.7 are read only.

11.2.5 RESET/TOGGLE ENABLE REGISTER (RTE)

Table 26 Reset/Toggle Enable register (address EFH)

7	6	5	4	3	2	1	0
TP47	TP46	RP45	RP44	RP43	RP42	RP41	RP40

Table 27 Description of the RTE bits (note 1)

BIT	SYMBOL	FUNCTION
7	TP47	if HIGH then P4.7 toggles on a match of CM2 and T2.
6	TP46	if HIGH then P4.6 toggles on a match of CM2 and T2.
5	RP45	if HIGH then P4.5 is reset on a match of CM1 and T2.
4	RP44	if HIGH then P4.4 is reset on a match of CM1 and T2.
3	RP43	if HIGH then P4.3 is reset on a match of CM1 and T2.
2	RP42	if HIGH then P4.2 is reset on a match of CM1 and T2.
1	RP41	if HIGH then P4.1 is reset on a match of CM1 and T2.
0	RP40	if HIGH then P4.0 is reset on a match of CM1 and T2.

Note

1. If RTE.n is LOW then P4.n is not affected by a match of CM1 and T2 or CM2 and T2.
   For more information, refer to the 8051-based *"8-bit Microcontrollers Data Handbook IC20"*.

11.3 Watchdog Timer (T3)

In addition to Timer T2 and the standard timers (Timer 0 and Timer 1), a Watchdog Timer (WDT) comprising an 11-bit prescaler and an 8-bit timer (T3) is also provided (see Fig.12).

The timer T3 is incremented every 1.5 ms, derived from the oscillator frequency of 16 MHz by the following formula: $f_{timer} = \frac{f_{CLK}}{12 \times 2048}$

When a timer T3 overflow occurs, the microcontroller is reset and a reset-output-pulse is generated at pin RST. This short output pulse (3 machine cycles) may be suppressed if the RST pin is connected to a capacitor.

To prevent a system reset (by an overflow of the WDT), the user program has to reload T3 within periods that are shorter than the programmed Watchdog time interval.

If the processor suffers a hardware/software malfunction, the software will fail to reload the timer. This failure will produce a reset upon overflow thus preventing the processor running out of control.

The Watchdog Timer can only be reloaded if the condition flag WLE = PCON.4 has been previously set by software. At the moment the counter is loaded the condition flag is automatically cleared.

The timer interval between the timer's reloading and the occurrence of a reset depends on the reloaded value. For example, this may range from 1.5 ms to 0.375 s when using an oscillator frequency of 16 MHz.

In the Idle state the Watchdog Timer and reset circuitry remain active.

The Watchdog Timer (WDT) is controlled by the Enable Watchdog pin ($\overline{EW}$); see Table 28.

Table 28 $\overline{EW}$ controlling WDT and Power-down mode

PIN $\overline{EW}$	WDT	POWER-DOWN MODE
LOW	enabled	disabled
HIGH	disabled	enabled

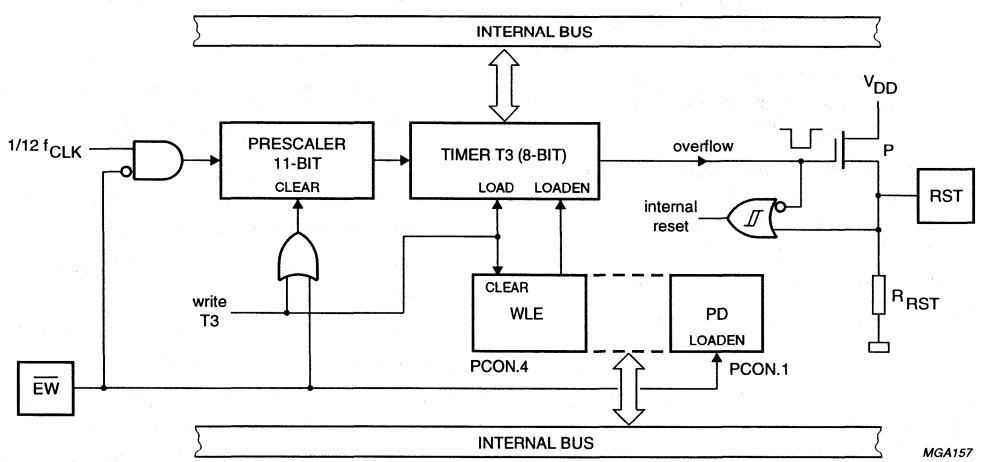


Fig.12 Functional diagram of T3 Watchdog Timer.

12 SERIAL I/O PORT: SIO0 (UART)

The Serial Port SIO0 is a full duplex (UART) serial I/O port i.e. it can transmit and receive simultaneously. This Serial Port is also receive-buffered. It can commence reception of a second byte before the previously received byte has been read from the receive register. However, if the first byte has still not been read by the time reception of the second byte is complete, one of these (first or second) bytes will be lost. The SIO0 receive and transmit registers are both accessed via the S0BUF SFR. Writing to S0BUF loads the transmit register, and reading S0BUF accesses to a physically separate receive register. SIO0 can operate in 4 modes:

Mode 0 Serial data is transmitted and received through RXD. TXD outputs the shift clock. 8 data bits are transmitted/received (LSB first). The baud rate is fixed at $1/12$ of the oscillator frequency.

Mode 1 10 bits are transmitted via TXD or received through RXD: a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit is put into RB8 of the S0CON SFR. The baud rate is variable.

Mode 2 11 bits are transmitted through TXD or received through RXD: a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8 in S0CON) can be assigned the value of 0 or 1. With nominal software, TB8 can be the parity bit (P in PSW). During a receive, the 9th data bit is stored in RB8 (S0CON), and the stop bit is ignored. The baud rate is programmable to either $1/32$ or $1/64$ of the oscillator frequency.

Mode 3 11 bits are transmitted through TXD or received through RXD: a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is the same as Mode 2 except for the baud rate which is variable in Mode 3.

In all four modes, transmission is initiated by any instruction that writes to the S0BUF SFR.
Reception is initiated in Mode 0 when RI = 0 and REN = 1. In the other three modes, reception is initiated by the incoming start bit provided that REN = 1.

Modes 2 and 3 are provided for multiprocessor communications. In these modes, 9 data bits are received with the 9th bit written to RB8 (S0CON). The 9th bit is followed by the stop bit. The port can be programmed so that with receiving the stop bit, the Serial Port interrupt will be activated if, and only if RB8 = 1.

This feature is enabled by setting bit SM2 in S0CON. This feature may be used in multiprocessor systems.

For more information about how to use the UART in combination with the registers S0CON, PCON, IE, SBUF and the Timer register, refer to the 8051-based *"8-bit Microcontrollers Data Handbook IC20"*.

13 SERIAL I/O PORT: SIO1 (CAN)

SIO1 (CAN) provides the CAN (Controller Area Network) serial-bus data communication interface. SIO1 (CAN) replaces the SIO1 (I^2C) serial interface as provided in the microcontroller derivative P8XC552.

13.1 On-chip CAN-controller

CAN is the definition of a high performance communication protocol for serial data communication. The P8XCE598 on-chip CAN-controller is a full implementation of the CAN 2.0A protocol. With the P8XCE598 powerful local networks can be built, both for automotive and general industrial environments. This results in a much reduced wiring harness and enhanced diagnostic and supervisory capabilities.

13.2 CAN Features

- Multi-master architecture
- Bus access priority determined by the message identifier
- 2032 message identifier (2^{11} standard frame CAN 2.0A)
- Guaranteed latency time for high priority messages
- Powerful error handling capability
- Data length from 0 up to 8 bytes
- Multicast and broadcast message facility
- Non destructive bit-wise arbitration
- Non-return-to-zero (NRZ) coding/decoding with bit-stuffing
- Programmable transfer rate (up to 1 Mbit/s)
- Programmable output driver configuration
- Suitable for use in a wide range of networks including the SAE's network classes A, B and C
- DMA providing high-speed on-chip data exchange
- Bus failure management facility
- $1/2AV_{DD}$ reference voltage.

13.3 Interface between CPU and CAN

The internal interface between the P8XCE598's CPU and on-chip CAN-controller is achieved via the following four SFRs (see Fig.13):

- CANADR, to point to a register of the CAN-controller
- CANDAT, to read or write data
- CANCON, to read interrupt flags and to write commands
- CANSTA, to read status information and to write DMA pointer.

Additionally, the DMA-logic allows a high-speed data exchange between the CAN-controller and the CPU's on-chip Main RAM. For more information, see Section 13.5.15 "Handling of the CPU-CAN interface".

13.4 Hardware blocks of the CAN-controller

The P8XCE598 CAN-controller contains all necessary hardware for high performance serial network communications (see Fig.14 and Table 29).

It controls the communication flow through the area network using the CAN-protocol. The CAN-controller meets the following requirements:

- Short message length
- Bus access priority, determined by the message identifier
- Powerful error handling capability
- Configuration flexibility to allow area network expansion
- Guaranteed latency time for urgent messages;
  - The **latency time** defines the period between the initiation (Transmission Request) and the start of the transmission on the bus. The latency time strongly depends on a large variety of bus-related conditions. In the case of a message being transmitted on the bus and one distortion, the latency time can be up to 149 bit times (worst case). For more information see Chapter 23, "CAN application information".

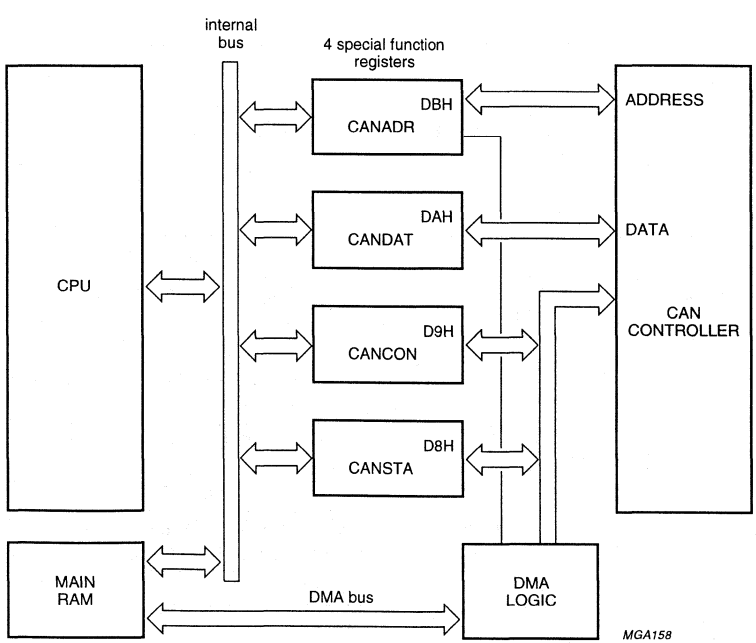


Fig.13 Interface between CPU and CAN-controller.

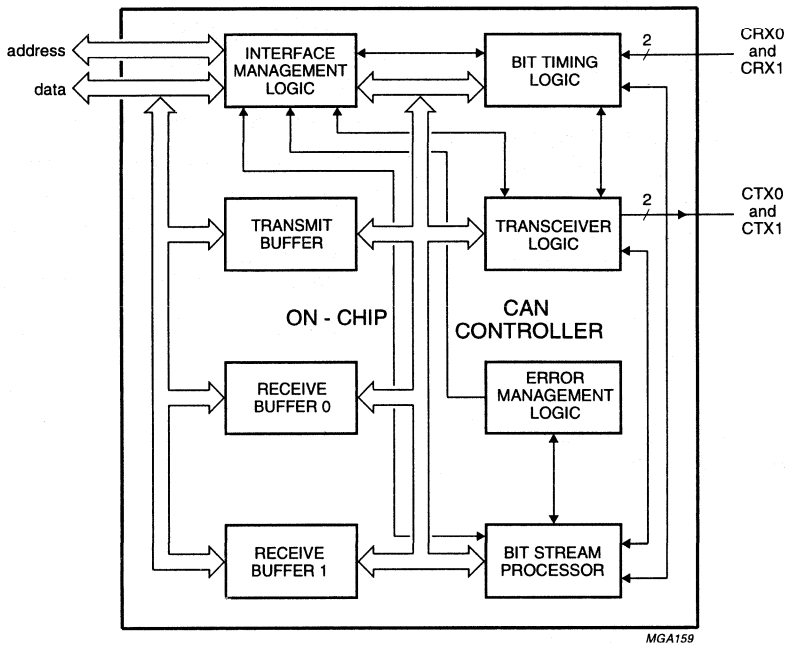


Fig.14 Block diagram of the P8XCE598 on-chip CAN-controller.

Table 29 Hardware blocks of the CAN-controller (see Fig.14)

NAME	BLOCK	DESCRIPTION
Interface Management Logic	IML	Interprets commands from the CPU, allocates the message buffers (TBF, RBF0 and RBF1) and provides interrupts and status information to the microcontroller.
Transmit Buffer	TBF	10 bytes memory into which the CPU writes messages which are to be transmitted over the CAN network.
Receive Buffers (0 and 1)	RBF0 RBF1	RBF0 and RBF1 are each 10 bytes memories which are alternatively used to store messages received from the CAN network. The CPU can process one message while another is being received.
Bit Stream Processor	BSP	Is a sequencer, controlling the data stream between the Transmit Buffer, Receive Buffers (parallel data) and the CAN-bus (serial data).
Bit Timing Logic	BTL	Synchronizes the CAN-controller to the bitstream on the CAN-bus.
Transceiver Control Logic	TCL	Controls the output driver.
Error Management Logic	EML	Performs the error confinement according to the CAN-protocol.

13.5 Control Segment and Message Buffer description

The CAN-Controller appears to the CPU as a memory-mapped peripheral, guaranteeing the independent operation of both parts.

13.5.1 Address allocation

The address area of the CAN-controller consists of the Control Segment and the message buffers. The Control Segment is programmed during an initialization down-load in order to configure communication parameters (e.g. bit timing). The communication over the CAN-bus is also controlled via this segment by the CPU. A message which is to be transmitted, must be written to the Transmit Buffer. After a successful reception the CPU may read the message from the Receive Buffer and then release it for further use.

13.5.2 Control Segment layout

The exchange of status, control and command signals between the CPU and the CAN-controller is performed in the control segment. The layout of this segment is shown in Fig.15. After an initial down-load, the contents of the registers Acceptance Code, Acceptance Mask, Bus Timing 0, Bus Timing 1 and Output Control should not be changed. These registers may only be accessed when the Reset Request bit in the Control Register is set HIGH (see Tables 30, 31 and 32).

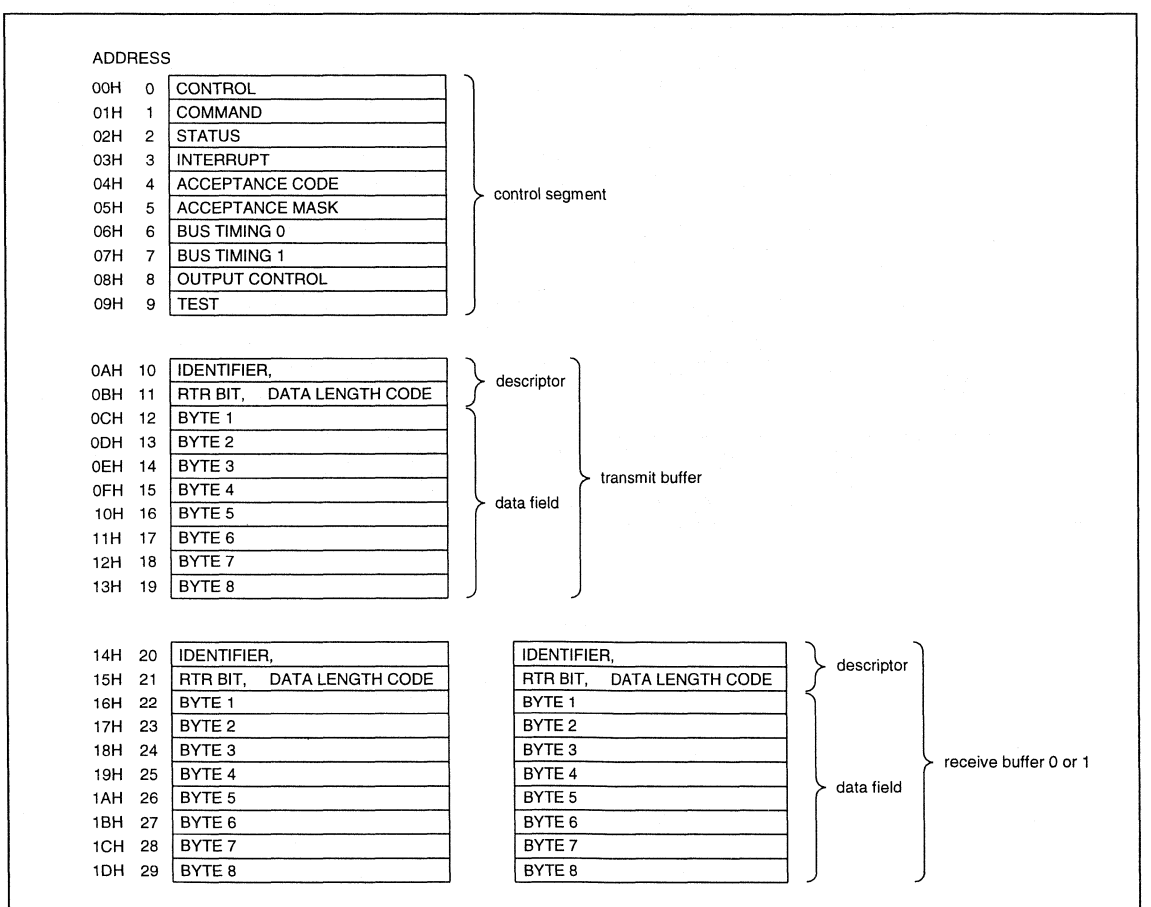


Fig.15 CAN-controller internal address allocation.

Table 30 CPU/CAN Register map

BIT							
7	6	5	4	3	2	1	0
Control Segment							
ADDRESS 0: CONTROL REGISTER							
TM	S	RA	OIE	EIE	TIE	RIE	RR
ADDRESS 1: COMMAND REGISTER							
RX0A	RX1A	WUM	SLP	COS	RRB	AT	TR
ADDRESS 2: STATUS REGISTER							
BS	ES	TS	RS	TCS	TBS	DO	RBS
ADDRESS 3: INTERRUPT REGISTER							
Reserved	Reserved	Reserved	WUI	OI	EI	TI	RI
ADDRESS 4: ACCEPTANCE CODE REGISTER							
AC.7	AC.6	AC.5	AC.4	AC.3	AC.2	AC.1	AC.0
ADDRESS 5: ACCEPTANCE MASK REGISTER							
AM.7	AM.6	AM.5	AM.4	AM.3	AM.2	AM.1	AM.0
ADDRESS 6: BUS TIMING REGISTER 0							
SJW.1	SJW.0	BRP.5	BRP.4	BRP.3	BRP.2	BRP.1	BRP.0
ADDRESS 7: BUS TIMING REGISTER 1							
SAM	TSEG2.2	TSEG2.1	TESG2.0	TSEG1.3	TSEG1.2	TSEG1.1	TSEG1.0
ADDRESS 8: OUTPUT CONTROL REGISTER							
OCTP1	OCTN1	OCPOL1	OCTP0	OCTN0	OCPOL0	OCMODE1	OCMODE0
ADDRESS 9: TEST REGISTER (note 1)							
Reserved	Reserved	Map Internal Register	Connect RX Buffer 0 CPU	Connect TX Buffer CPU	Access Internal Bus	Normal RAM Connect	Float Output Driver

BIT							
7	6	5	4	3	2	1	0
Transmit Buffer							
ADDRESS 10: IDENTIFIER							
ID.10	ID.9	ID.8	ID.7	ID.6	ID.5	ID.4	ID.3
ADDRESS 11: RTR, DATA LENGTH CODE							
ID.2	ID.1	ID.0	RTR	DLC.3	DLC.2	DLC.1	DLC.0
ADDRESS 12 TO 19: BYTES 1 TO 8							
Data	Data	Data	Data	Data	Data	Data	Data
Receive Buffer 0 and 1							
ADDRESS 20: IDENTIFIER							
ID.10	ID.9	ID.8	ID.7	ID.6	ID.5	ID.4	ID.3
ADDRESS 21: RTR, DATA LENGTH CODE							
ID.2	ID.1	ID.0	RTR	DLC.3	DLC.2	DLC.1	DLC.0
ADDRESS 22 TO 29: BYTES 1 TO 8							
Data	Data	Data	Data	Data	Data	Data	Data

Note

1. The Test Register is used for production testing only.

13.5.3 CONTROL REGISTER (CR)

The contents of the Control Register are used to change the behaviour of the CAN-controller. Control bits may be set or reset by the CPU which uses the Control Register as a read/write memory.

Table 31 Control Register (address 0)

7	6	5	4	3	2	1	0
TM	S	RA	OIE	EIE	TIE	RIE	RR

Table 32 Description of the CR bits

BIT	SYMBOL	FUNCTION
7	TM	**Test Mode** (note 1).If the value of TM is: HIGH (enabled), then the CAN-controller enters Test Mode (normal operations impossible). LOW (disabled), then the CAN-controller is in normal operating mode.
6	7	**Sync** (note 2). If the value of S is: HIGH (2 edges), then bus-line transitions from recessive-to-dominant and vice-versa are used for resynchronization (see Sections 13.5.20 and 13.6). LOW (1 edge), then the only transitions from recessive-to-dominant are used for resynchronization.
5	RA	**Reference Active** (note 2). If the value of RA is: HIGH (output), then the pin REF is an $\frac{1}{2}AV_{DD}$ reference output. LOW (input), then a reference voltage may be input.
4	OIE	**Overrun Interrupt Enable**. If the value of OIE is: HIGH (enabled) and the Data Overrun bit is set (see Section 13.5.5) then the CPU receives an Overrun Interrupt signal. LOW (disabled), then the CPU receives no Overrun Interrupt signal from the CAN-controller.
3	EIE	**Error Interrupt Enable**. If the value of EIE is: HIGH (enabled) and the Error or Bus Status change (see Section 13.5.5) then the CPU receives an Error Interrupt signal. LOW (disabled), then the CPU receives no Error Interrupt signal.
2	TIE	**Transmit Interrupt Enable**. If the value of TIE is: HIGH (enabled) and when a message has been successfully transmitted or the Transmit Buffer is accessible again, (e.g. after an Abort Transmission command), then the CAN-controller transmits a Transmit Interrupt signal to the CPU. LOW (disabled), then there is no transmission of the Transmit Interrupt signal by the CAN-controller to the CPU.
1	RIE	**Receive Interrupt Enable**. If the value of RIE is: HIGH (enabled) and when a message has been received without errors, then the CAN-controller transmits a Receive Interrupt signal to the CPU. LOW (disabled), then there is no transmission of the Receive Interrupt signal by the CAN-controller to the CPU.
0	RR	**Reset Request** (note 3). If the value of RR is: HIGH (present), then detection of a Reset Request results in the CAN-controller aborting the current transmission/reception of a message entering the reset state. LOW (absent), on the HIGH-to-LOW transition of the Reset Request bit, the CAN-controller returns to its normal operating state.

Notes to the description of the CR bits

1. The test mode is intended for factory testing and not for customer use.
2. A modification of the bits Reference Active and Sync is only possible with Reset Request = HIGH (present). It is allowed to set these bits while Reset Request is changed from a HIGH level to a LOW level. After an external reset (pin RST = HIGH) the Reference Active bit is set HIGH (output), the Sync bit is undefined.
3. During an external reset (RST = HIGH) or when the Bus Status bit is set HIGH (Bus-OFF), the IML forces the Reset Request HIGH (present). After the Reset Request bit is set LOW (absent) the CAN-controller will wait for:
   a) One occurrence of the Bus-Free signal (11 recessive bits, see Section 13.6.9.6), if the preceding reset (Reset Request = HIGH) has been caused by an external reset or a CPU initiated reset.
   b) 128 occurrences of Bus-Free, if the preceding reset (Reset Request = HIGH) has been caused by a CAN-controller initiated Bus-OFF, before re-entering the Bus-On mode, see Section 13.6.9.
   c) When Reset Request is set HIGH (present), for whatever reason, the Control, Command, Status and Interrupt bits are affected, see Table 40. The registers at addresses 4 to 8 are only accessible when the Reset Request is set HIGH (present).

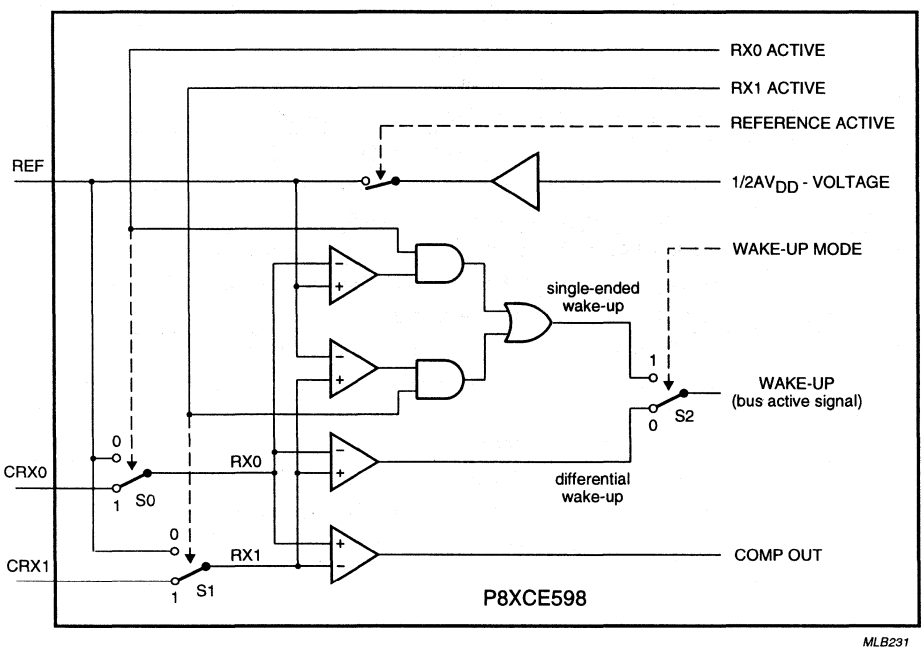


Fig.16 Configurable CAN receiver.

13.5.4 Command Register (CMR)

A command bit initiates an action within the transfer layer of the CAN-controller. The Command Register appears to the CPU as a read/write memory, except for the bits CMR.0 (TR) to CMR.3 (COS), which return a HIGH if being read.

Table 33 Command Register (address 1)

7	6	5	4	3	2	1	0
RX0A	RX1A	WUM	SLP	COS	RRB	AT	TR

Table 34 Description of the CMR bits

BIT	SYMBOL	FUNCTION
7	RX0A	**RX0 Active**. See Table 35; note 1.
6	RX1A	**RX1 Active**. See Table 35; note 1.
5	WUM	**Wake-up Mode** (note 2). If the value of WUM is: HIGH (single ended), then the difference of the RX signals to the internal reference voltage $\frac{1}{2}AV_{DD}$ is used for wake up. LOW (differential), then the differential signal between RX0 and RX1 is used for wake up.
4	SLP	**Sleep** (note 3). If the value of SLP is: HIGH (sleep), then the CAN-controller enters sleep mode if no CAN interrupt is pending and there is no bus activity. LOW (wake up), then the CAN-controller functions normally.
3	COS	**Clear Overrun Status** (note 4). If the value of COS is: HIGH (clear), then the Data Overrun status bit is set to LOW (see Table 37). LOW (no action), then there is no action.
2	RRB	**Release Receive Buffer** (note 5). If the value of RRB is: HIGH (released), then the Receive Buffer attached to the CPU is released. LOW (no action), then there is no action.
1	AT	**Abort Transmission** (note 6). If the value of AT is: HIGH (present) and if not already in progress, a pending Transmission Request is cancelled. LOW (absent), then there is no action.
0	TR	**Transmission Request** (note 7). If the value of TR is: HIGH (present), then a message shall be transmitted. LOW (absent), then there is no action.

Notes to the description of the CMR bits

1. The RX0/RX1 Active bits, if being read, reflect the status of the respective switches (see Fig.16). It is recommended to change the switches only during the reset state (Reset Request = HIGH).
2. The Wake-Up Mode bit should be set at the same time as the Sleep bit. The differential wake up mode is useful if both bus wires are fully functioning; it minimizes the amount of wake ups due to noise. The single ended wake up mode is recommended if a wake up must be possible even if one bus wire is already or may become disturbed (see Fig.16).
3. The CAN-controller will enter sleep mode, if the Sleep bit is set HIGH (sleep) there is no bus activity and no interrupt is pending. The CAN-controller will wake up after the Sleep bit is set LOW (wake up) or when there is bus activity. On wake up, a Wake-Up Interrupt (see Section 13.5.6) is generated (see also Chapter 15). A CAN-controller which is sleeping and then awaken by bus activity will not be able to receive this message until it detects a Bus-Free signal (see Section 13.6.9.6). The Sleep bit, if read, reflects the status of the CAN-controller.
4. This command bit is used to acknowledge the Data Overrun condition signalled by the Data Overrun status bit. It may be given or set at the same time as a Release Receive Buffer command bit.
5. After reading the contents of the Receive Buffer (RBF0 or RBF1) the CPU must release this buffer by setting Release Receive Buffer bit HIGH (released). This may result in another message becoming immediately available.
6. The Abort Transmission bit is used when the CPU requires the suspension of the previously requested transmission, e.g. to transmit an urgent message. A transmission already in progress is not stopped. In order to see if the original message had been either transmitted successfully or aborted, the Transmission Complete Status bit should be checked. This should be done after the Transmit Buffer Access bit has been set HIGH (released) or a Transmit Interrupt has been generated (see Section 13.5.6).
7. If the Transmission Request bit was set HIGH in a previous command, it cannot be cancelled by setting the Transmission Request bit LOW (absent). Cancellation of the requested transmission may be performed by setting the Abort Transmission bit HIGH (present).

Table 35 Combination of bits RX0A and RX1A (see Fig.16)

CONTROL		RX0	RX1
RX0ACTIVE	RX1ACTIVE		
1	1	CRX0	CRX1
1	0	CRX0	$\frac{1}{2}AV_{DD}$
0	1	$\frac{1}{2}AV_{DD}$	CRX1
0	0	No action	

13.5.5 STATUS REGISTER (SR)

The contents of the Status Register reflects the status of the CAN-controller. The Status Register appears to the CPU as a read only memory.

Table 36 Status Register (address 2)

7	6	5	4	3	2	1	0
BS	ES	TS	RS	TCS	TBS	DO	RBS

Table 37 Description of the SR bits

BIT	SYMBOL	FUNCTION
7	BS	**Bus Status** (note 1). If the value of BS is: HIGH (Bus-OFF), then the CAN-controller is not involved in bus activities. LOW (Bus-ON), then the CAN-controller is involved in bus activities.
6	ES	**Error Status**. If the value of ES is: HIGH (error), then at least one of the Error Counters (see Section 13.6.10) has reached the CPU Warning limit. LOW (ok), then both Error Counters have not reached the warning limit.
5	TS	**Transmit Status** (note 2). If the value of TS is: HIGH (transmit), then the CAN-controller is transmitting a message. LOW (idle), then no message is transmitted.
4	RS	**Receive Status** (note 2). If the value of RS is: HIGH (receive), then the CAN-controller is receiving a message. LOW (idle), then no message is received.
3	TCS	**Transmission Complete Status** (note 3). If the value of TCS is: HIGH (complete), then last requested transmission has been successfully completed. LOW (incomplete), then previously requested transmission is not yet completed.
2	TBS	**Transmit Buffer Access** (note 3). If the value of TBS is: HIGH (released), then the CPU may write a message into the TBF. LOW (locked), then the CPU cannot access the Transmit Buffer. A message is either waiting for transmission or is in the process of being transmitted.
1	DO	**Data Overrun** (note 4). If the value of DO is: HIGH (overrun), then this bit is set HIGH (Overrun), when both Receive Buffers are full and the first byte of another message should be stored. LOW (absent), then no data overrun has occurred since the Clear Overrun command was given.
0	RBS	**Receive Buffer Status** (note 5). If the value of RBS is: HIGH (full), then this bit is set when a new message is available. LOW (empty), then no message has become available since the last Release Receive Buffer command bit was set.

Notes to the description of the SR bits

1. When the Bus Status bit is set HIGH (Bus-OFF), the CAN-controller will set the Reset Request bit HIGH (present). It will stay in this state until the CPU sets the Reset Request bit LOW (absent). Once this is completed the CAN-controller will wait the minimum protocol-defined time (128 occurrences of the Bus-Free signal) before setting the Bus Status bit LOW (Bus-ON), the Error Status bit LOW (ok) and resetting the Error Counters. During Bus-OFF the output drivers are switched off (floating); external transceiver circuits should output a recessive level in this case.
2. If both the Receive Status and Transmit Status bits are LOW (idle) the CAN-bus is idle.
3. If the CPU tries to write to the Transmit Buffer when the Transmit Buffer Access bit is LOW (locked), the written bytes will not be accepted and will be lost without this being signalled. The Transmission Complete Status bit is set LOW (incomplete) whenever the Transmission Request bit is set HIGH (present). If an Abort Transmission command is issued, the Transmit Buffer will be released. If the message, which was requested and then aborted, was not transmitted, the Transmission Complete Status bit will remain LOW.
4. If Data Overrun = HIGH (overrun) is detected, the currently received message is dropped. A transmitted message, granted acceptance, is also stored in a Receive Buffer. This occurs because it is not known if the CAN-controller will lose arbitration and so become a receiver of the message. If no Receive Buffer is available, Data Overrun is signalled. However, this transmitted and accepted message does neither cause a Receive Interrupt nor set the Receive Buffer Status bit to HIGH (full). Also, a Data Overrun does not cause the transmission of an Overload Frame (see Sections 13.6.1 and 13.6.5).
5. If the command bit Release Receive Buffer is set HIGH (released) by the CPU, the Receive Buffer Status bit is set LOW (empty) by IML. When a new message is stored in any of the receive buffers, the Receive Buffer Status bit is set HIGH (full) again.

13.5.6 INTERRUPT REGISTER (IR)

The Interrupt Register allows the identification of an interrupt source. When one or more bits of this register are set, a CAN interrupt (SI01) will be indicated to the CPU. All bits are reset by the CAN-controller after this register is read by the CPU. This register appears to the CPU as a read only memory.

Table 38 Interrupt Register (address 3)

7	6	5	4	3	2	1	0
–	–	–	WUI	OI	EI	TI	RI

Table 39 Description of the IR bits

BIT	SYMBOL	FUNCTION
7	–	Reserved.
6	–	Reserved.
5	–	Reserved.
4	WUI	**Wake-Up Interrupt**. The value of WUI is set to: HIGH (set), when the sleep mode is left. See Section 13.5.4. LOW (reset), by a read access of the Interrupt Register by the CPU.
3	OI	**Overrun Interrupt** (note 1). The value of OI is set to: HIGH (set), if both Receive Buffers contain a message and the first byte of another message should be stored (passed acceptance), and the Overrun Interrupt Enable is HIGH (enabled). LOW (reset), by a read access of the Interrupt Register by the CPU.
2	EI	**Error Interrupt**. The value of EI is set to: HIGH (set), on a change of either the Error Status or Bus Status bits, if the Error Interrupt Enable is HIGH (enabled). See Section 13.5.5. LOW (reset), by a read access of the Interrupt Register by the CPU.
1	TI	**Transmit Interrupt**. The value of TI is set to: HIGH (set), on a change of the Transmit Buffer Access from LOW to HIGH (released) and Transmit Interrupt Enable is HIGH (enabled). LOW (reset), after a read access of the Interrupt Register by the CPU.
0	RI	**Receive Interrupt** (note 2). The value of RBS is set to: HIGH (set), when a new message is available in the Receive Buffer and the Receive Interrupt Enable bit is HIGH (enabled). LOW (reset) automatically by a read access of Interrupt Register by the CPU.

Notes

1. Overrun Interrupt bit (if enabled) and Data Overrun bit (see Section 13.5.5) are set at the same time.
2. Receive Interrupt bit (if enabled) and Receive Buffer Status bit (see Section 13.5.5) are set at the same time.

Table 40 Effects of setting the Reset Request bit HIGH (present)

TYPE	BIT	SYMBOL	FUNCTION	EFFECT
Control	CR.7	TM	Test Mode	LOW (disabled)
	CR.5	RA	Reference Active	HIGH (output); note 1
Command	CMR.7	RX0A	RX0 Active	HIGH (RX0 = CRX0); note 1
	CMR.6	RX1A	RX1 Active	HIGH (RX1 = CRX1); note 1
	CMR.4	SLP	Sleep	LOW (wake-up)
	CMR.3	COS	Clear Overrun Status	HIGH (clear)
	CMR.2	RRB	Release Receive Buffer	HIGH (released)
	CMR.1	AT	Abort Transmission	LOW (absent)
	CMR.0	TR	Transmission Request	LOW (absent)
Status	SR.7	BS	Bus Status	LOW (Bus-On); note 1
	SR.6	ES	Error Status	LOW (no error); note 1
	SR.5	TS	Transmit Status	LOW (idle)
	SR.4	RS	Receive Status	LOW (idle)
	SR.3	TCS	Transmission Complete Status	HIGH (complete)
	SR.2	TBS	Transmit Buffer Access	HIGH (released)
	SR.1	DO	Data Overrun	LOW (absent)
	SR.0	RBS	Receive Buffer Status	LOW (empty)
Interrupt	IR.3	OI	Overrun Interrupt	LOW (reset)
	IR.1	TI	Transmit Interrupt	LOW (reset)
	IR.0	RI	Receive Interrupt	LOW (reset)

Note

1. Only after an external reset; see note 5 to Table 37 "Description of the SR bits".

13.5.7 Acceptance Code Register (ACR)

The Acceptance Code Register is part of the acceptance filter of the CAN-controller. This register can be accessed (read/write), if the Reset Request bit is set HIGH (present).

When a message is received which passes the acceptance test and if there is an empty Receive Buffer, then the respective Descriptor and Data Field (see Fig.15) are sequentially stored in this empty buffer.

In the event that there is no empty Receive Buffer, the Data Overrun bit is set HIGH (overrun); see Sections 13.5.5 and 13.5.6.

When the complete message has been correctly received the following occurs:

- The Receive Buffer Status bit is set HIGH (full)
- If the Receive Interrupt Enable bit is set HIGH (enabled), the Receive Interrupt is set HIGH (set).

During transmission of a message which passes the acceptance test, the message is also written to its own Receive Buffer. If no Receiver Buffer is available, Data Overrun is signalled because it is not known at the start of a message whether the CAN-controller will lose arbitration and so become a receiver of the message.

Table 41 Acceptance Code Register (address 4)

7	6	5	4	3	2	1	0
AC.7	AC.6	AC.5	AC.4	AC.3	AC.2	AC.1	AC.0

Table 42 Description of the ACR bits

BIT	SYMBOL	FUNCTION
7 to 0	AC.7 to AC.0	**Acceptance Code.** The Acceptance Code bits (AC.7 to AC.0) and the eight most significant bits of the message's Identifier (ID.10 to ID.3) must be equal to those bit positions which are marked relevant by the Acceptance Mask bits (AM.7 to AM.0). The acceptance is given, if the following equation is satisfied: (ID10 ... ID.3) = [(AC.7 ... AC.0) or (AM.7 ... AM.0)] = 1111 1111 B

13.5.8 Acceptance Mask Register (AMR)

The Acceptance Mask Register is part of the acceptance filter of the CAN-controller.
This register can be accessed (read/write) if the Reset Request bit is set HIGH (present).

The Acceptance Mask Register qualifies which of the corresponding bits of the acceptance code are 'relevant' or 'don't care' for acceptance filtering.

Table 43 Acceptance Mask Register (address 5)

7	6	5	4	3	2	1	0
AM.7	AM.6	AM.5	AM.4	AM.3	AM.2	AM.1	AM.0

Table 44 Description of the AMR bits

BIT	SYMBOL	FUNCTION
7 to 0	AM.7 to AM.0	**Acceptance Mask.** If the Acceptance Mask bit is: HIGH (don't care), then this bit position is 'don't care' for the acceptance of a message. LOW (relevant), then this bit position is 'relevant' for acceptance filtering.

13.5.9 Bus Timing Register 0 (BTR0)

The contents of Bus Timing Register 0 defines the values of the Baud Rate Prescaler (BRP) and the Synchronization Jump Width (SJW).

This register can be accessed (read/write) if the Reset Request bit is set HIGH (present).
For further information on bus timing, see Sections 13.5.10 and 13.5.18.

Table 45 Bus Timing Register 0 (address 6)

7	6	5	4	3	2	1	0
SJW.1	SJW.0	BRP.5	BRP.4	BRP.3	BRP.2	BRP.1	BRP.0

Table 46 Description of the BTR0 bits

BIT	SYMBOL	FUNCTION
7	SJW.1	**Synchronization Jump Width.** To compensate for phase shifts between clock oscillators of different bus controllers, any bus controller must resynchronize on any relevant signal edge of the current transmission. The synchronization jump width defines the maximum number of clock cycles a bit period may be shortened or lengthened by one resynchronization: $t_{SJW} = t_{SCL}(2SJW.1 + SJW.0 + 1)$
6	SJW.0	
5	BRP.5	**Baud Rate Prescaler.** The period of the system clock t_{SCL} is programmable and determines the individual bit timing.The system clock is calculated using the following equation: $t_{SCL} = 2t_{CLK}(32BRP.5 + 16BRP.4 + 8BRP.3 + 4BRP.2 + 2BRP.1 + BRP.0 + 1)$ Where t_{CLK} = time period of the P8XCE598 oscillator.
4	BRP.4	
3	BRP.3	
2	BRP.2	
1	BRP.1	
0	BRP.0	

13.5.10 Bus Timing Register 1(BTR1)

The contents of Bus Timing Register 1 defines the length of the bit period, the location of the sample point and the number of samples to be taken at each sample point.

This register can be accessed (read/write) if the Reset Request bit is set HIGH (present).For further information on bus timing, see Sections 13.5.9 and 13.5.18.

Table 47 Bus Timing Register 1 (address 7)

7	6	5	4	3	2	1	0
SAM	TSEG2.2	TSEG2.1	TSEG2.0	TSEG1.3	TSEG1.2	TSEG1.1	TSEG1.0

Table 48 Description of the BTR1 bits

BIT	SYMBOL	FUNCTION
7	SAM	**Sampling.** If the bit SAM is: HIGH (3 samples), then three samples are taken. This is recommended for slow/medium speed buses (SAE class A and B) where filtering of spikes on the bus-line is beneficial (see Section 13.5.19.6). LOW (1 sample), the bus is sampled once. This is recommended for high speed buses (SAE class C).
6	TSEG2.2	**Time Segment 1 (TSEG1) and Time Segment 2 (TSEG2).** TSEG1 determines the number of clock cycles per bit period and the location of the sample point: $t_{TSEG1} = t_{SCL}(8TSEG1.3 + 4TSEG1.2 + 2TSEG1.1 + TSEG1.0 + 1)$ TSEG2 determines the number of clock cycles per bit period and the location of the sample point: $t_{TSEG2} = t_{SCL}(4TSEG2.2 + 2TSEG2.1 + TSEG2.0 + 1)$
5	TSEG2.1	
4	TSEG2.0	
3	TSEG1.3	
2	TSEG1.2	
1	TSEG1.1	
0	TSEG1.0	

13.5.11 Output Control Register (OCR)

The Output Control Register allows, under software control, the set-up of different output driver configurations. This register can be accessed (read/write) if the Reset Request bit is set HIGH (present). If the CAN-controller is in the sleep mode (Sleep = HIGH) a recessive level is output on the CTX0 and CTX1 pins. If the CAN-controller is in the reset state (Reset Request = HIGH) the output drivers are floating.

Tables 50 and 51, show the relationship between the bits of the Output Control Register and the two serial output pins CTX0 and CTX1 of the P8XCE598 CAN-controller, connected to the serial bus (see Fig.14).

Table 49 Output Control Register (address 8)

7	6	5	4	3	2	1	0
OCTP1	OCTN1	OCPOL1	OCTP0	OCTN0	OCPOL0	OCMODE1	OCMODE0

Table 50 Description of the OCR bits

BIT	SYMBOL	FUNCTION
7	OCTP1	See Tables 51 and 52.
6	OCTN1	
5	OCPOL1	
4	OCTP0	
3	OCTN0	
2	OCPOL0	
1	OCMODE1	**Output Mode.** These bits select the output mode; see Table 51.
0	OCMODE0	

Table 51 Description of the Output Mode bits

OCMODE1	OCMODE0	DESCRIPTION
1	0	**Normal Output Mode.** The bit sequence (TXD) is sent via CTX0, CTX1. TXD is the data bit to be transmitted. The voltage levels on the output driver pins CTX0 and CTX1 depend on both the driver characteristic programmed by OCTPx, OCTNx (float, pull-up, pull-down, push-pull) and the output polarity programmed by OCPOLx (see Fig.17).
1	1	**Clock Output Mode.** For the CTX0 pin this is the same as in Normal Output Mode (CTX0: bit sequence). However, the data stream to CTX1 is replaced by the transmit clock (TXCLK). The rising edge of the transmit clock (non-inverted) marks the beginning of a bit period. The clock pulse width is t_{SCL}.
0	0	**Bi-phase Output Mode.** In contrast to Normal Output Mode the bit representation is time variant and toggled. If the bus controllers are galvanically decoupled from the bus-line by a transformer, the bit stream is not allowed to contain a DC component. This is achieved by the following scheme. During recessive bits all outputs are deactivated (floating). Dominant bits are sent alternately on CTX0 and CTX1, i.e. the first dominant bit is sent on CTX0, the second is sent on CTX1, and the third one is sent on CTX0 again, etc.
0	1	**Test Output Mode.** For the CTX0 pin this is the same as in Normal Output Mode (CTX0: bit sequence). To measure the delay time of the transmitter and receiver this mode connects the output of the input comparator (COMP OUT) with the input of the output driver CTX1. This mode is used for production testing only.

Table 52 Output pin set-up

DRIVE	OCTPx	OCTNx	OCPOLx	TXD	TPx(1)	TNx(2)	CTXx(3)
Float	0	0	0	0	OFF	OFF	float
	0	0	0	1	OFF	OFF	float
	0	0	1	0	OFF	OFF	float
	0	0	1	1	OFF	OFF	float
Pull-down	0	1	0	0	OFF	ON	LOW
	0	1	0	1	OFF	OFF	float
	0	1	1	0	OFF	OFF	float
	0	1	1	1	OFF	ON	LOW
Pull-up	1	0	0	0	OFF	OFF	float
	1	0	0	1	ON	OFF	HIGH
	1	0	1	0	ON	OFF	HIGH
	1	0	1	1	OFF	OFF	float
Push/Pull	1	1	0	0	OFF	ON	LOW
	1	1	0	1	ON	OFF	HIGH
	1	1	1	0	ON	OFF	HIGH
	1	1	1	1	OFF	ON	LOW

Notes

1. TPx is the on-chip output transistor x, connected to CV_{DD}; x = 0 or 1.
2. TNx is the on-chip output transistor x, connected to CV_{SS}; x = 0 or 1.
3. CTXx is the serial output level on CTX0 or CTX1. It is required that the output level on the CAN-bus is dominant with TXD = 0 and recessive with TXD = 1, see Section 13.6.1.1 "Bit representation".

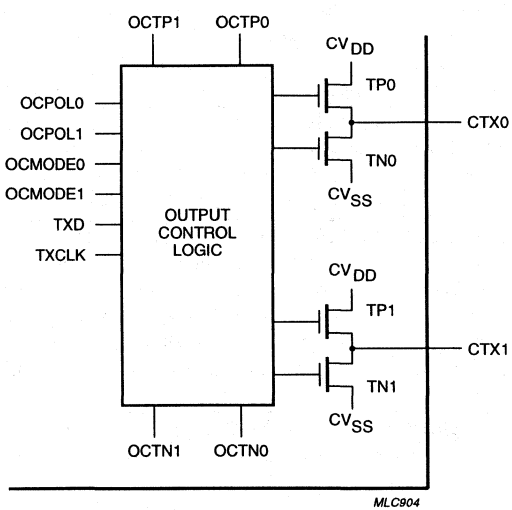


Fig.17 Configurable CAN Transmitter.

13.5.12 Test Register (TR)

The Test Register is used for production testing only.

Table 53 Test Register (address 9)

7	6	5	4	3	2	1	0
Reserved	Reserved	Map Internal Register	Connect RX Buffer 0 CPU	Connect TX Buffer CPU	Access Internal Bus	Normal RAM Connect	Float Output Driver

13.5.13 Transmit Buffer layout

The global layout of the Transmit Buffer is shown in Fig.15. This buffer serves to store a message from the CPU to be transmitted by the CAN-controller. It is subdivided into Descriptor and Data Field. The Transmit Buffer can be written to and read from by the CPU.

13.5.13.1 Descriptor

Table 54 Descriptor Byte 1 Register (DSCR1, address 10)

7	6	5	4	3	2	1	0
ID.10	ID.9	ID.8	ID.7	ID.6	ID.5	ID.4	ID.3

Table 55 Descriptor Byte 2 Register (DSCR2, address 11)

7	6	5	4	3	2	1	0
ID.2	ID.1	ID.0	RTR	DLC.3	DLC.2	DLC.1	DLC.0

Table 56 Description of the ID.n bits in DSCR1 and DSCR2

BIT	SYMBOL	FUNCTION
DSCR1		
7	ID.10	**Identifier.** The Identifier consists of 11 bits (ID.10 to ID.0). ID.10 is the most significant bit, which is transmitted first on the bus during the arbitration process. The Identifier acts as the messages' name, used in a receiver for acceptance filtering, and also determines the bus access priority during the arbitration process. The lower the binary value of the Identifier the higher the priority. This is due to the larger number of leading dominant bits during arbitration (see Section 13.6.7).
6	ID.9	
5	ID.8	
4	ID.7	
3	ID.6	
2	ID.5	
1	ID.4	
0	ID.3	
DSCR2		
7	ID.2	**Identifier**. See DSCR1.
6	ID.1	
5	ID.0	

Table 57 Description of the other DSCR2 bits

BIT	SYMBOL	FUNCTION
4	RTR	**Remote Transmission Request.** If the RTR bit is: HIGH (remote), then the Remote Frame will be transmitted by the CAN-controller. LOW (data), then the Data Frame will be transmitted by the CAN-controller.
3	DLC.3	**Data Length Code (DLC).** The number of bytes (Data Byte Count) in the Data Field of a message is coded by the Data Length Code. At the start of a Remote Frame transmission the Data Length Code is not considered due to the RTR bit being HIGH (remote). This forces the number of transmitted/received data bytes to be a logic 0. Nevertheless, the Data Length Code must be specified correctly to avoid bus errors, if two CAN-controllers start a Remote Frame transmission simultaneously. The range of the Data Byte Count is 0 to 8 bytes and coded as follows: Data Byte Count = 8DLC.3 + 4DLC.2 + 2DLC.1 + DLC.0 For reasons of compatibility no Data Byte Counts other than 0,1,2,....,8 should be used.
2	DLC.2	
1	DLC.1	
0	DLC.0	

13.5.13.2 Data Field

The number of transferred data bytes is determined by the Data Length Code. The first bit transmitted is the most significant bit of data byte 1 at address 12.

13.5.14 RECEIVE BUFFER LAYOUT

The layout of the Receive Buffer and the individual bytes correspond to the definitions given for the Transmit Buffer layout, except that the addresses start at 20 instead of 10 (see Fig.15).

13.5.15 HANDLING OF THE CPU-CAN INTERFACE

Via the four special registers CANADR, CANDAT, CANCON and CANSTA the CPU has access to the CAN-controller and also to the DMA-logic. Note that CANCON and CANSTA have different meanings for a Read and Write access.

Table 58 The SFRs between CPU and CAN

Reserved bits are read as HIGH. R = Read; W = Write; R/W = Read/Write.

ADDRESS	ACCESS	BIT							
		7	6	5	4	3	2	1	0
CANADR									
DBH	R/W	DMA	Reserved	AutoInc	CANA4	CANA3	CANA2	CANA1	CANA0
CANDAT									
DAH	R/W	CAND7	CAND6	CAND5	CAND4	CAND3	CAND2	CAND1	CAND0
CANCON; Do not use a RMW instruction									
D9H	R	Reserved	Reserved	Reserved	WUI	OI	EI	TI	RI
	W	RX0A	RX1A	WUM	SLP	COS	RRB	AT	TR
CANSTA; The bit addresses of CANSTA (7 to 0) are DFH to D8H; do not use a RMW instruction									
DFH to D8H	R	BS	ES	TS	RS	TCS	TBS	DO	RBS
	W	RAMA7	RAMA6	RAMA5	RAMA4	RAMA3	RAMA2	RAMA1	RAMA0

13.5.15.1 Special Function Register CANADR

CANADR is implemented as a read/write register.

Table 59 SFR CANADR (address DBH)

7	6	5	4	3	2	1	0
DMA	–	AutoInc	CANA4	CANA3	CANA2	CANA1	CANA0

Table 60 Description of the CANADR bits

BIT	SYMBOL	FUNCTION
7	DMA	DMA-logic controlled via bit CANADR.7 (see Section 13.5.17).
6	–	Reserved.
5	AutoInc	Auto Address Increment mode controlled via bit CANADR.5 (see Section 13.5.16).
4	CANA4	The five least significant bits CANADR.4 to CANADR.0 define the address of one of the CAN-controller internal registers to be accessed via CANDAT. For instance, after an external hardware (e.g. power-on) reset CANADR contains the value 64H, and hence the CPU accesses (read/write) the Acceptance Code register of the CAN-controller, via the SFR CANDAT.
3	CANA3	
2	CANA2	
1	CANA1	
0	CANA0	

13.5.15.2 Special Function Register CANDAT

CANDAT is implemented as a read/write register.

Table 61 SFR CANDAT (address DAH)

7	6	5	4	3	2	1	0
CAND7	CAND6	CAND5	CAND4	CAND3	CAND2	CAND1	CAND0

Table 62 Description of the CANADR bits

BIT	SYMBOL	FUNCTION
7 to 0	CAND7 to CAND0	The SFR CANDAT appears as a port to the CAN-controller internal register (memory location) being selected by CANADR. Reading or writing CANDAT is effectively an access to that CAN-controller internal register, which is selected by CANADR.

13.5.15.3 Special Function Register CANCON

Table 63 SFR CANCON in **Read** access (address D9H)

7	6	5	4	3	2	1	0
–	–	–	WUI	OI	EI	TI	RI

Table 64 Description of the CANCON bits in **Read** access

When reading CANCON the Interrupt Register of the CAN-controller is accessed.

BIT	SYMBOL	FUNCTION
7	–	Reserved; bits are read as HIGH.
6	–	
5	–	
4	WUI	Wake-Up Interrupt (see Table 39).
3	OI	Overrun Interrupt (see Table 39).
2	EI	Error Interrupt (see Table 39).
1	TI	Transmit Interrupt (see Table 39).
0	RI	Receive Interrupt (see Table 39).

Table 65 SFR CANCON in **Write** access (address D9H)

7	6	5	4	3	2	1	0
RX0A	RX1A	WUM	SLP	COS	RRB	AT	TR

Table 66 Description of the CANCON bits in **Write** access

When writing to CANCON then the Command Register of the CAN-controller is accessed.

BIT	SYMBOL	FUNCTION
7	RX0A	RX0 Active (see Table 34).
6	RX1A	RX1 Active (see Table 34).
5	WUM	Wake-Up Mode (see Table 34).
4	SLP	Sleep (see Table 34).
3	COS	Clear Overrun Status (see Table 34).
2	RRB	Release Receive Buffer (see Table 34).
1	AT	Abort Transmission (see Table 34).
0	TR	Transmission Request (see Table 34).

13.5.15.4 Special Function Register CANSTA

CANSTA is implemented as a bit-addressable read/write register.
The bit addresses of CANSTA (7 to 0) are DFH to D8H.

Table 67 SFR CANCON in **Read** access (address DFH to D8H)

7	6	5	4	3	2	1	0
BS	ES	TS	RS	TCS	TBS	DO	RBS

Table 68 Description of the CANCON bits in **Read** access
When reading CANSTA the Status Register of the CAN-controller is accessed.

BIT	SYMBOL	FUNCTION
7	BS	Bus Status (see Table 37).
6	ES	Error Status (see Table 37).
5	TS	Transmit Status (see Table 37).
4	RS	Receive Status (see Table 37).
3	TCS	Transmission Complete Status (see Table 37).
2	TBS	Transmit Buffer Access (see Table 37).
1	DO	Data Overrun (see Table 37).
0	RBS	Receive Buffer Status (see Table 37).

Table 69 SFR CANCON in **Write** access (address DFH to D8H)

7	6	5	4	3	2	1	0
RAMA7	RAMA6	RAMA5	RAMA4	RAMA3	RAMA2	RAMA1	RAMA0

Table 70 Description of the CANSTA bits in **Write** access
Writing to CANSTA sets the address of the on-chip MAIN RAM (internal Data Memory) for a subsequent DMA transfer.

BIT	SYMBOL	FUNCTION
7 to 0	RAMA7 to RAMA0	–

13.5.16 Auto address increment

With the Auto Address Increment mode a fast stack-like reading and writing of CAN-controller internal registers is provided. If the bit CANADR.5 (AutoInc) is HIGH, the content of CANADR is incremented automatically after any read or write access to CANDAT. For instance, loading a message into the Transmit Buffer can be done by writing 2AH into CANADR and then moving byte by byte of the message to CANDAT. Incrementing CANADR beyond XX111111B resets the bit CANADR.5 (AutoInc) automatically (CANADR = XX000000B).

13.5.17 High speed DMA

The DMA-logic allows you to transfer a complete message (up to 10 bytes) between CAN-controller and Main RAM in 2 instruction cycles at maximum; up to 4 bytes are transferred in 1 instruction cycle. The performance of the CPU is strongly enhanced because this very fast transfer is carried out in the background.

A DMA transfer is achieved by first writing the RAM address (00H to FFH) into CANSTA and then setting the TX- or RX-Buffer address in CANDR and the bit CANADR.7 (DMA) simultaneously; the RAM address points to the location of the first byte to be transferred. Setting the DMA bit causes an automatic evaluation of the Data Length Code and then the transfer; for a TX-DMA transfer the Data Length Code is expected at the location 'RAM address + 1'.

In order to program a TX-DMA transfer the value 8AH (address 10) has to be written into CANADR. Then a complete message, consisting of the 2-byte Descriptor and the Data Field (0 to 8 bytes), starting at location 'RAM address' is transferred to the TX-Buffer.

The RX-DMA transfer is very versatile. By writing a value in the range of 94H (address 20) up to 9DH (address 29) into CANADR the whole or a part of the received message, starting at the specified address, is transferred to the internal Data Memory. This allows e.g. to transfer the bytes of the Data Field only.

After a successful DMA transfer the DMA-bit is reset.

During a DMA transfer the CPU can process the next instruction. However, an access to the Data Memory, CANADR, CANDAT, CANCON or CANSTA is not allowed. After having set the DMA-bit, every interrupt is disabled until the end of the transfer. Note, that disadvantageous programming may lead to an interrupt response time of at most 10 instruction cycles. The shortest interrupt response time is achieved by using 2 consecutive 1-cycle instructions directly after setting the DMA-bit.

During the reset state (bit Reset Request is HIGH) a DMA transfer is not possible.

13.5.18 Bus timing/synchronization

The Bus Timing Logic (BTL) monitors the serial bus-line via the on-chip input comparator and performs the following functions (see Section 13.4 "Hardware blocks of the CAN-controller"):

- Monitors the serial bus-line level
- Adjusts the sample point, within a bit period (programmable)
- Samples the bus-line level using majority logic (programmable, 1 or 3 samples)
- Synchronization to the bit stream:
  - hard synchronization at the start of a message
  - resynchronization during transfer of a message.

The configuration of the BTL is performed during the initialization of the CAN-controller. The BTL uses the following three registers:

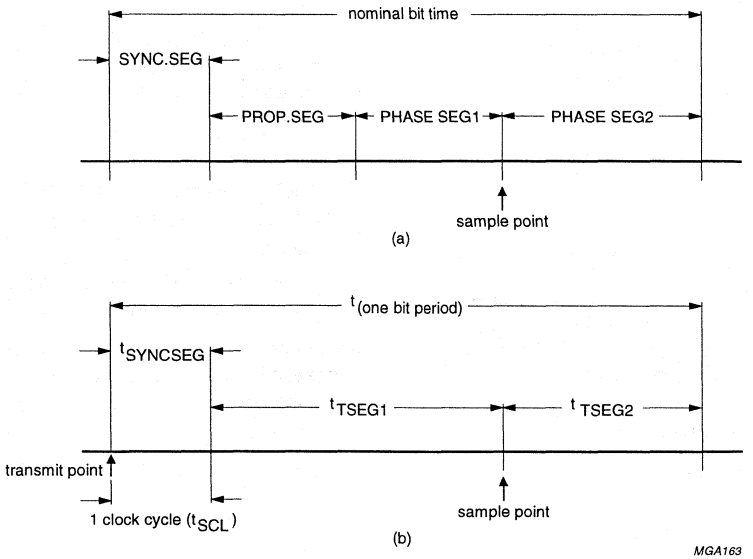
- Control Register (Sync)
- Bus Timing Register 0
- Bus Timing Register 1.

13.5.19 Bit timing

A bit period is built up from a number of system clock cycles (t_{SCL}), see Section 13.5.9.
One bit period is the result of the addition of the programmable segments TSEG1 and TSEG2 and the general segment SYNCSEG.

13.5.19.1 Synchronization Segment (SYNCSEG)

The incoming edge of a bit is expected during this state; this state corresponds to one system clock cycle ($1 \times t_{SCL}$).



(a) As defined by the CAN-protocol.
(b) As implemented in the P8XCE598's on-chip CAN-controller.

Fig.18 Bit period.

13.5.19.2 Time Segment 1 (TSEG1)

This segment determines the location of the sampling point within a bit period, which is at the end of TSEG1. TSEG1 is programmable from 1 to 16 system clock cycles (see Section 13.5.10).

The correct location of the sample point is essential for the correct functioning of a transmission. The following points must be taken into consideration:

- A Start-Of-Frame (see Section 13.6.2) causes all CAN-controllers to perform a 'hard synchronization' (see Section 13.5.20) on the first recessive-to-dominant edge. During arbitration, however, several CAN-controllers may simultaneously transmit. Therefore it may require twice the sum of bus-line, input comparator and the output driver delay times until the bus is stable. This is the propagation delay time.
- To avoid sampling at an incorrect position, it is necessary to include an additional synchronization buffer on both sides of the sample point. The main reasons for incorrect sampling are:
  - incorrect synchronization due to spikes on the bus-line
  - slight variations in the oscillator frequency of each CAN-controller in the network, which results in a phase error.
- Time Segment 1 consists of the segment for compensation of propagation delays and the synchronization buffer segment directly before the sample point (see Fig.18).

13.5.19.3 Time Segment 2 (TSEG2)

This time segment provides:

- additional time at the sample point for calculation of the subsequent bit levels (e.g. arbitration)
- synchronization buffer segment directly after the sample point.

TSEG2 is programmable from 1 to 8 system clock cycles (see Section 13.5.10.

13.5.19.4 Synchronisation Jump Width (SJW)

SJW defines the maximum number of clock cycles (t_{SCL}) a period may be reduced or increased by one resynchronization. SJW is programmable from 1 to 4 system clock cycles, see Section 13.5.2.

13.5.19.5 Propagation Delay Time (t_{prop})

The Propagation Delay Time is:

$t_{prop} = 2 \times$ (physical bus delay + input comparator delay + output driver delay).

t_{prop} is rounded up to the nearest multiple of t_{SCL}.

13.5.19.6 Bit Timing Restrictions

Restrictions on the configuration of the bit timing are based on internal processing. The restrictions are:

- $t_{TSEG2} \geq 2t_{SCL}$
- $t_{TSEG2} \geq t_{SJW}$
- $t_{TSEG1} \geq t_{SEG2}$
- $t_{TSEG1} \geq t_{SJW} + t_{prop}$.

The three sample mode (SAM = HIGH) has the effect of introducing a delay of one system clock cycle on the bus-line. This must be taken into account for the correct calculation of TSEG1 and TSEG2:

- $t_{TSEG1} \geq t_{SJW} + t_{prop} + 2t_{SCL}$
- $t_{TSEG2} \geq 3t_{SCL}$.

13.5.20 SYNCHRONIZATION

Synchronization is performed by a state machine which compares the incoming edge with its actual bit timing and adapts the bit timing by hard synchronization or resynchronization.

This type of synchronization occurs only at the beginning of a message.

The CAN-controller synchronizes on the first incoming recessive-to-dominant edge of a message (being the leading edge of a message's Start-Of-Frame bit; see Section 13.6.2.

Resynchronization occurs during the transmission of a message's bit stream to compensate for:

- Variations in individual CAN-controller oscillator frequencies
- Changes introduced by switching from one transmitter to another (e.g. during arbitration).

As a result of resynchronization either t_{TSEG1} may be increased by up to a maximum of t_{SJW} or t_{TSEG2} may be decreased by up to a maximum of t_{SJW}:

- $t_{TSEG1} \leq t_{SCL}$ [(TSEG1 + 1) + (SJW + 1)]
- $t_{TSEG2} \geq t_{SCL}$ [(TSEG2 + 1) – (SJW + 1)].

TSEG1, TSEG2 and SJW are the programmed numerical values.

The phase error (e) of an edge is given by the position of the edge relative to SYNCSEG, measured in system clock cycles (t_{SCL}).

The value of the phase error is defined as:

- e = 0, if the edge occurs within SYNCSEG
- e > 0, if the edge occurs within TSEG1
- e < 0, if the edge occurs within TSEG2.

The effect of resynchronization is:

- The same as that of a hard synchronization, if the magnitude of the phase error (e) is less or equal to the programmed value of t_{SJW}
- To increase a bit period by the amount of t_{SJW},if the phase error is positive and the magnitude of the phase error is larger than t_{SJW}
- To decrease a bit period by the amount of t_{SJW} if the phase error is negative and the magnitude of the phase error is larger than t_{SJW}.

13.5.20.1 Synchronization Rules

The synchronization rules are as follows:

- Only one synchronization within one bit time is used.
- An edge is used for synchronization only if the value detected at the previous sample point differs from the bus value immediately after the edge.
- Hard synchronization is performed whenever there is a recessive-to-dominant edge during Bus-Idle (see Section 13.6.6).
- All other edges (recessive-to-dominant and optionally dominant-to recessive edges if the Sync bit is set HIGH (see Section 13.5.3) which are candidates for resynchronization will be used with the following exception:
  - A transmitting CAN-controller will not perform a resynchronization as a result of a recessive-to-dominant edge with positive phase error, if only these edges are used for resynchronization. This ensures that the delay times of the output driver and input comparator do not cause a permanent increase in the bit time.

13.6 CAN 2.0A Protocol description

13.6.1 FRAME TYPES

The P8XCE598's CAN-controller supports the four different CAN-protocol frame types for communication:

- Data Frame, to transfer data
- Remote Frame, request for data
- Error Frame, globally signal a (locally) detected error condition
- Overload Frame, to extend delay time of subsequent frames (an Overload Frame is not initiated by the P8XCE598 CAN-Controller).

13.6.1.1 Bit representation

There are two logical bit representations used in the CAN-protocol:

- A recessive bit on the bus-line appears only if all connected CAN-controllers send a recessive bit at that moment.
- Dominant bits always overwrite recessive bits i.e. the resulting bit level on the bus-line is dominant.

13.6.2 DATA FRAME

A Data Frame carries data from a transmitting CAN-controller to one or more receiving ones.
A Data Frame is composed of seven different bit-fields:

- Start-Of-Frame
- Arbitration Field
- Control Field
- Data Field (may have a length of zero)
- CRC Field
- Acknowledge Field
- End-Of-Frame.

13.6.2.1 Start-Of-Frame bit

Signals the start of a Data Frame or Remote Frame. It consists of a single dominant bit use for hard synchronization of a CAN-controller in receive mode.

13.6.2.2 Arbitration Field

Consists of the message Identifier and the RTR bit. In the case of simultaneous message transmissions by two or more CAN-controllers the bus access conflict is solved by bit-wise arbitration, which is active during the transmission of the Arbitration Field.

13.6.2.3 Identifier

This 11-bit field is used to provide information about the message, as well as the bus access priority. It is transmitted in the order ID.10 to ID.0 (LSB). The situation that the seven most significant bits (ID.10 to ID.4) are all recessive must not occur.

An Identifier does not define which particular CAN-controller will receive the frame because a CAN based communication network does not differentiate between a point-to-point, multicast or broadcast communication.

13.6.2.4 RTR bit

A CAN-controller, acting as a receiver for certain information may initiate the transmission of the respective data by transmitting a Remote Frame to the network, addressing the data source via the Identifier and setting the RTR bit HIGH (remote; recessive bus level). If the data source simultaneously transmits a Data Frame containing the requested data, it uses the same Identifier. No bus access conflict occurs due to the RTR bit being set LOW (data; dominant bus level) in the Data Frame.

13.6.2.5 Control Field

This field consists of six bits. It includes two reserved bits (for future expansions of the CAN-protocol), transmitted with a dominant bus level, and is followed by the Data Length Code (4 bits).
The number of bytes (destuffed; number of data bytes to be transmitted/received) in the Data Field is indicated by the Data Length Code. Admissible values of the Data Length Code, and hence the number of bytes in the (destuffed) Data Field, are {0, 1, ..., 8}. A logic 0 (logic 1) in the Data Length Code is transmitted as dominant (recessive) bus level, respectively.

13.6.2.6 Data Field

The data, stored within the Data Field of the Transmit Buffer, are transmitted according to the Data Length Code. Conversely, data of a received Data Frame will be stored in the Data Field of a Receive Buffer. The Data Field can contain from 0 up to 8 bytes. The most significant bit of the first data byte (lowest address) is transmitted/received first.

13.6.2.7 Cyclic Redundancy Code Field (CRC)

The CRC Field consists of the CRC Sequence (15 bits) and the CRC Delimiter (1 recessive bit). The Cyclic Redundancy Code (CRC) encloses the destuffed bit stream of the Start-Of-Frame, Arbitration Field, Data Field and CRC Sequence. The most significant bit of the CRC Sequence is transmitted/received first. This frame check sequence, implemented in the CAN-controller is derived from a cyclic redundancy code best suited for frames with a total bit count of less than 127 bits, see Section 13.6.8.3. With Start-Of-Frame (dominant bit) included in the code word, any rotation of the code word can be detected by the absence of the CRC Delimiter (recessive bit).

13.6.2.8 Acknowledge Field (ACK)

The Acknowledge Field consists of two bits, the Acknowledge Slot and the Acknowledge Delimiter, which are transmitted with a recessive level by the transmitter of the Data Frame. All CAN-controllers having received the matching CRC Sequence, report this by overwriting the transmitter's recessive bit in the Acknowledge Slot with a dominant bit. Thereby a transmitter, still monitoring the bus level recognizes that at least one receiver within the network has received a complete and correct message (i.e. no error was found). The Acknowledge Delimiter (recessive bit) is the second bit of the Acknowledge Field. As a result, the Acknowledge Slot is surrounded by two recessive bits: the CRC Delimiter and the Acknowledge Delimiter.

All nodes within a CAN network may use all the information coming to the network by all CAN-controllers (shared memory concept). Therefore, acknowledgement and error handling are defined to provide all information in a consistent way throughout this shared memory. Hence, there is no reason to discriminate different receivers of a message in the acknowledge field. If a node is disconnected from the network due to bus failure, this particular node is no longer part of the shared memory. To identify a 'lost node' additional and application specific precautions are required.

13.6.2.9 End-Of-Frame

Each Data Frame or Remote Frame is delimited by the End-Of-Frame bit sequence which consists of seven recessive bits (exceeds the bit stuff width by two bits). Using this method a receiver detects the end of a frame independent of a previous transmission error because the receiver expects all bits up to the end of the CRC Sequence to be coded by the method of bit-stuffing, see Section 13.6.7.3. The bit-stuffing logic is deactivated during the End-Of-Frame sequence.

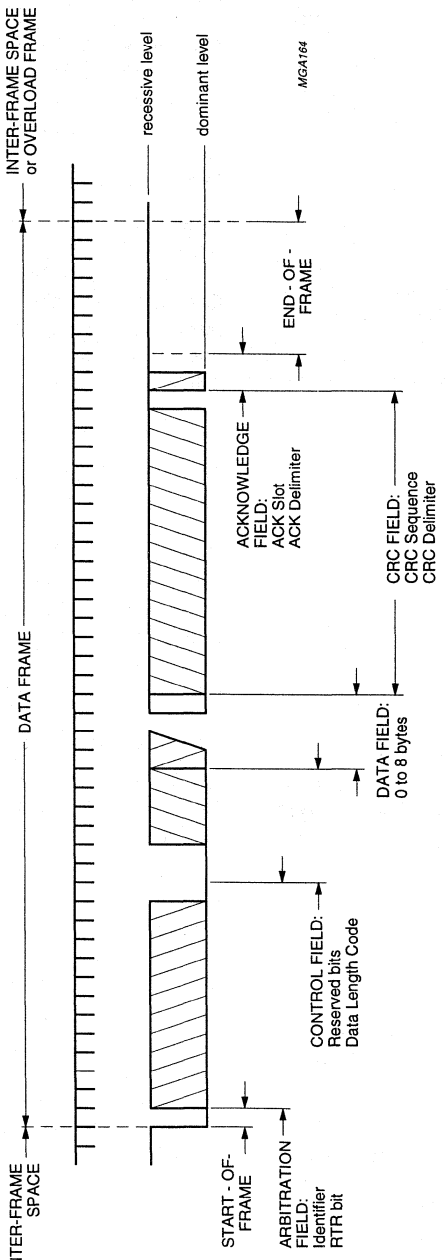


Fig.19 Data Frame.

13.6.3 REMOTE FRAME

A CAN-controller acting as a receiver for certain information may initiate the transmission of the respective data by transmitting a Remote Frame to the network, addressing the data source via the Identifier and setting the RTR bit HIGH (remote; recessive bus level). The Remote Frame is similar to the Data Frame with the following exceptions:

- RTR bit is set HIGH
- Data Length Code is ignored
- no Data Field contained.

Note that the value of the Data Length Code should be the one of the corresponding Data Frame, although it is ignored for a Remote Frame.

A Remote Frame is composed of six different bit fields:

- Start-of-Frame
- Arbitration Field
- Control Field
- CRC Field
- Acknowledge Field
- End-Of-Frame.

See Section 13.6.2 for more detailed explanation of the Remote Frame bit fields.

13.6.4 ERROR FRAME

The Error Frame consists of two different fields:

- The first field, accomplished by the superimposing of Error Flags contributed from different CAN-controllers
- The second field is the Error Delimiter.

13.6.4.1 Error Flag

There are two forms of an Error Flag:

- Active Error Flag, consists of six consecutive dominant bits
- Passive Error Flag, consists of six consecutive recessive bits unless it is overwritten by dominant bits from other CAN-controllers.

An error-active CAN-controller (see Section 13.6.9) detecting an error condition signals this by transmission of an Active Error Flag. This Error Flag's form violates the bit-stuffing rule (see Section 13.6.7) applied to all fields, from Start-Of-Frame to CRC Delimiter, or destroys the fixed form of the fields Acknowledge Field or End-Of-Frame (see Fig.20). Consequently, all other CAN-controllers detect an error condition and start transmission of an Error Flag. Therefore the sequence of dominant bits, which can be monitored on the bus, results from the superimposing of different Error Flags transmitted by individual CAN-controllers. The total length of this sequence varies between six (minimum) and twelve (maximum) bits.

An error-passive CAN-controller (see Section 13.6.9) detecting an error condition tries to signal this by transmission of a Passive Error Flag. The error-passive CAN-controller waits for six consecutive bits with identical polarity, beginning at the start of the Passive Error Flag. The Passive Error Flag is complete when these six identical bits have been detected.

13.6.4.2 Error Delimiter

The Error Delimiter consists of eight recessive bits and has the same format as the Overload Delimiter. After transmission of an Error Flag, each CAN-controller monitors the bus-line until it detects a transition from a dominant-to-recessive bit level. At this point in time, every CAN-controller has finished sending its Error Flag and has additionally sent the first out of the 8 recessive bits of the Error Delimiter. Afterwards all CAN-controllers transmit the remaining recessive bits. After this event and an Intermission Field all error-active CAN-controllers within the network can start a transmission simultaneously.

If a detected error is signalled during transmission of a Data Frame or Remote Frame, the current message is spoiled and a retransmission of the message is initiated.

If a CAN-controller monitors any deviation of the Error Frame, a new Error Frame will be transmitted. Several consecutive Error Frames may result in the CAN-controller becoming error-passive and leaving the network unblocked.

In order to terminate an Error Flag correctly, an error-passive CAN-controller requires the bus to be Bus-Idle (see Section 13.6.6) for at least three bit periods (if there is a local error at an error-passive-receiver). Therefore a CAN-bus should not be 100% permanently loaded.

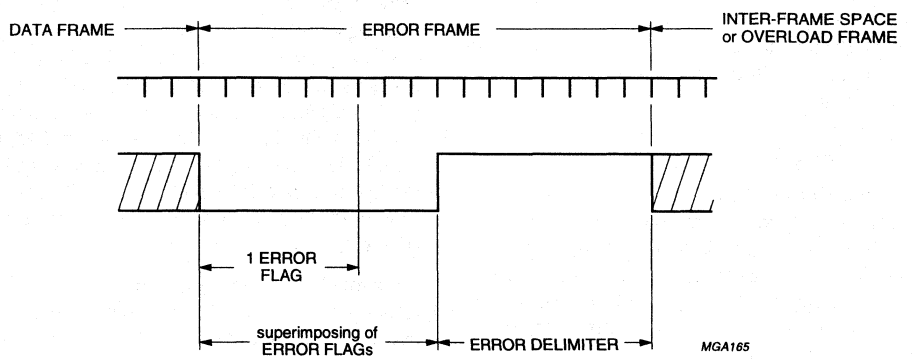


Fig.20 Error Frame.

13.6.5 OVERLOAD FRAME

The Overload Frame consists of two fields:

- The Overload Flag
- The Overload Delimiter.

The transmission of an Overload Frame may only start:

- Condition 1; during the first bit period of an expected Intermission Field.
- Condition 2; one bit period after detecting the dominant bit during Intermission Field.

The P8XCE598's on-chip CAN-controller will never initiate transmission of a condition 1 Overload Frame and will only react on a transmitted condition 2 Overload Frame, according to the CAN-protocol. No more than two Overload Frames are generated to delay a Data Frame or a Remote Frame. Although the overall form of the Overload Frame corresponds to that of the Error Frame, an Overload Frame does not initiate or require the retransmission of the preceding frame.

13.6.5.1 Overload Flag

The Overload Flag consists of six dominant bits and has a similar format to the Error Flag.

There are two conditions in the CAN-protocol which lead to the transmission of an Overload Flag:

- Condition 1; receiver circuitry requires more time to process the current data before receiving the next frame (receiver not ready).
- Condition 2; detection of a dominant bit during Intermission Field (see Section 13.6.6).

The Overload Flag's form corrupts the fixed form of the Intermission Field. All other CAN-controllers detecting the overload condition also transmit an Overload Flag (condition 2).

13.6.5.2 Overload Delimiter

The Overload Delimiter consists of eight recessive bits and takes the same form as the Error Delimiter. After transmission of an Overload Flag, each CAN-controller monitors the bus-line until it detects a transition from a dominant-to-recessive bit level. At this point in time, every CAN-controller has finished sending its Overload Flag and all CAN-controllers start simultaneously transmitting seven more recessive bits.

13.6.6 Inter-Frame Space

Data Frames and Remote Frames are separated from preceding frames (all types) by an Inter-Frame Space, consisting of an Intermission Field and a Bus-Idle. Error-passive CAN-controllers also send a Suspend Transmission (see Section 13.6.9) after transmission of a message. Overload Frames and Error Frames are not preceded by an Inter-Frame Space.

13.6.6.1 Intermission Field

The Intermission Field consists of three recessive bits. During an Intermission period, no frame transmissions will be started by the P8XCE598's on-chip CAN-controller. An Intermission is required to have a fixed time period to allow a CAN-controller to execute internal processes prior to the next receive or transmit task.

13.6.6.2 Bus-Idle

The Bus-Idle time may be of arbitrary length (min. 0 bit). The bus is recognized to be free and a CAN-controller having information to transmit may access the bus. The detection of a dominant bit level during Bus-Idle on the bus is interpreted as the Start-Of-Frame.

13.6.7 Bus organization

Bus organization is based on five basic rules described in the following subsections.

13.6.7.1 Bus Access

CAN-controllers only start transmission during the Bus-Idle state. All CAN-controllers synchronize on the leading edge of the Start-Of-Frame (hard synchronization).

13.6.7.2 Bus Arbitration

If two or more CAN-controllers simultaneously start transmitting, the bus access conflict is solved by a bit-wise arbitration process during transmission of the Arbitration Field.

During arbitration every transmitting CAN-controller compares its transmitted bit level with the monitored bus level. Any CAN-controller which transmits a recessive bit and monitors a dominant bus level immediately becomes the receiver of the higher-priority message on the bus without corrupting any information on the bus. Each message contains an unique Identifier and a RTR bit describing the type of data within the message. The Identifier together with the RTR bit implicitly define the message's bus access priority. During arbitration the most significant bit of the Identifier is transmitted first and the RTR bit last. The message with the lowest binary value of the Identifier and RTR bit has the highest priority. A Data Frame has higher priority than a Remote Frame due to its RTR bit having a dominant level.

For every Data Frame there is an unique transmitter. For reasons of compatibility with other CAN-bus controllers, use of the Identifier bit pattern ID = 1111111XXXXB (X being bits of arbitrary level) is forbidden.

The number of available different Identifiers:
$(2^{11} - 2^4) = 2032$.

13.6.7.3 Coding/Decoding

The following bit fields are coded using the bit-stuffing technique:

- Start-Of-Frame
- Arbitration Field
- Control Field
- Data Field
- CRC Sequence.

When a transmitting CAN-controller detects five consecutive bits of identical polarity to be transmitted, a complementary (stuff) bit is inserted into the transmitted bit-stream.

When a receiving CAN-controller has monitored five consecutive bits with identical polarity in the received bit streams of the above described bit fields, it automatically deletes the next received (stuff) bit. The level of the deleted stuff bit has to be the complement of the previous bits; otherwise a Stuff Error will be detected and signalled (see Section 13.6.8).

The remaining bit fields or frames are of fixed form and are not coded or decoded by the method of bit-stuffing.

The bit-stream in a message is coded according to the Non-Return-to-Zero (NRZ) method, i.e. during a bit period, the bit level is held constant, either recessive or dominant.

13.6.7.4 Error Signalling

A CAN-controller which detects an error condition, transmits an Error Flag. Whenever a Bit Error, Stuff Error, Form Error or an Acknowledgement Error is detected, transmission of an Error Flag is started at the next bit. Whenever a CRC Error is detected, transmission of an Error Flag starts at the bit following the Acknowledge Delimiter, unless an Error Flag for another error condition has already started. An Error Flag violates the bit-stuffing law or corrupts the fixed form bit fields. A violation of the bit-stuffing law affects any CAN-controller which detects the error condition. These devices will also transmit an Error Flag.

An error-passive CAN-controller (see Section 13.6.9) which detects an error condition, transmits a Passive Error Flag. A Passive Error Flag is not able to interrupt a current message at different CAN-controllers but this type of Error Flag may be ignored (overwritten) by other CAN-controllers. After having detected an error condition, an error-passive CAN-controller will wait for six consecutive bits with identical polarity and when monitoring them, interpret them as an Error Flag.

After transmission of an Error Flag, each CAN-controller monitors the bus-line until it detects a transition from a dominant-to-recessive bit level. At this point in time, every CAN-controller has finished transmitting its Error Flag and all CAN-controllers start transmitting seven additional recessive bits (Error Delimiter, see Section 13.6.4).

The message format of a Data Frame or Remote Frame is defined in such a way that all detectable errors can be signalled within the message transmission time and therefore it is very simple for the CAN-controllers to associate an Error Frame to the corresponding message and to initiate retransmission of the corrupted message. If a CAN-controller monitors any deviation of the fixed form of an Error Frame, it transmits a new Error Frame.

13.6.7.5 Overload Signalling

Some CAN-controllers (but not the one on-chip of the P8XCE598) require to delay the transmission of the next Data Frame or Remote Frame by transmitting one or more Overload Frames. The transmission of an Overload Frame must start during the first bit of an expected Intermission Field. Transmission of Overload Frames which are reactions on a dominant bit during an expected Intermission Field, start one bit after this event.

Though the format of Overload Frame and Error Frame are identical, they are treated differently. Transmission of an Overload Frame during Intermission Field does not initiate the retransmission of any previous Data Frame or Remote Frame. If a CAN-controller which transmitted an Overload Frame monitors any deviation of its fixed form, it transmits an Error Frame.

13.6.8 Error Detection

The processes described in the following sub-sections are implemented in the P8XCE598's on-chip CAN-controller for error detection.

13.6.8.1 Bit Error

A transmitting CAN-controller monitors the bus on a bit-by-bit basis. If the bit level monitored is different from the transmitted one, a Bit Error is signalled. The exceptions being:

- During the Arbitration Field, a recessive bit can be overwritten by a dominant bit. In this case, the CAN-controller interprets this as a loss of arbitration.
- During the Acknowledge Slot, only the receiving CAN-controllers are able to recognize a Bit Error.

13.6.8.2 Stuff Error

The following bit fields are coded using the bit-stuffing technique:

- Start-Of-Frame
- Arbitration Field
- Control Field
- Data Field
- CRC Sequence.

There are two possible ways of generating a Stuff Error:

- A disturbance generates more than the allowed five consecutive bits with identical polarity. These errors are detected by all CAN-controllers.
- A disturbance falsifies one or more of the five bits preceding the stuff bit. This error situation is not recognized as a Stuff Error by the receivers. Therefore, other error detection processes may detect this error condition such as:
  - CRC check, format violation at the receiving CAN-controllers, or
  - Bit Error detection by the transmitting CAN-controller.

13.6.8.3 CRC Error

To ensure the validity of a transmitted message all receivers perform a CRC check. Therefore, in addition to the (destuffed) information digits (Start-Of-Frame up to Data Field), every message includes some control digits (CRC Sequence; generated by the transmitting CAN-controller of the respective message) used for error detection.

The code used by all CAN-controllers is a (shortened) BCH code, extended by a parity check and has the following attributes:

- 127 bits as maximum length of the code.
- 112 bits as maximum number of information digits (max. 83 bits are used by the CAN-controller).
- Length of the CRC Sequence amounts to 15 bits.
- Hamming distance d = 6.

As a result, '(d–1)' random errors are detectable (some exceptions exist).

The CRC Sequence is determined (calculated) by the following procedure:

1. The destuffed bit stream consisting of Start-Of-Frame up to the Data Field (if present) is interpreted as polynomial with coefficients 0 or 1.
2. This polynomial is divided (modulo-2) by the following generator polynomial, which includes a parity check:
   $f(x) = (x^{14} + x^9 + x^8 + x^6 + x^5 + x^4 + x^2 + x + 1)$
   $(x + 1) = 1100010110011001$ B.
3. The remainder of this polynomial division is the CRC sequence.

Burst errors are detected up to a length of 15 [degree of f(x)]. Multiple errors (number of disturbed bits at least d = 6) are not detected with a residual error probability of 2^{-15} (3×10^{-5}) by CRC check only.

13.6.8.4 Form Error

Form Errors result from violations of the fixed form of the following bit fields:

- CRC Delimiter
- Acknowledge Delimiter
- End-Of-Frame
- Error Delimiter
- Overload Delimiter.

During the transmission of these bit fields an error condition is recognized if a dominant bit level instead of a recessive one is detected.

13.6.8.5 Acknowledgement Error

This is detected by a transmitter whenever it does not monitor a dominant bit during the Acknowledge Slot.

13.6.8.6 Error detection by an Error Flag from another CAN-controller

The detection of an error is signalled by transmitting an Error Flag. An Active Error Flag causes a Stuff Error, a Bit Error or a Form Error at all other CAN-controllers.

13.6.8.7 Error Detection Capabilities

Errors which occur at all CAN-controllers (global errors) are 100% detected. For local errors, i.e. for errors occurring at some CAN-controllers only, the shortened BCH code, extended by a parity check, has the following error detection capabilities:

- Up to five single Bit Errors are 100% detected, even if they are distributed randomly within the code.
- All single Bit Errors are detected if their total number (within the code) is odd.
- The residual error probability of the CRC check amounts to (3×10^{-5}). As an error may be detected not only by CRC check but also by other detection processes described above the residual error probability is several magnitudes less than (3×10^{-5}).

13.6.9 Error confinement definitions

13.6.9.1 Bus-OFF

A CAN-controller which has too many unsuccessful transmissions, relative to the number of successful transmissions, will enter the Bus-OFF state. It remains in this state, neither receiving nor transmitting messages until the Reset Request bit is set LOW (absent) and both Error Counters set to 0 (see Section 13.6.10).

13.6.9.2 Acknowledge

A CAN-controller which has received a valid message correctly, indicates this to the transmitter by transmitting a dominant bit level on the bus during the Acknowledge Slot, independent of accepting or rejecting the message.

13.6.9.3 Error-Active

An error-active CAN-controller in its normal operating state is able to receive and to transmit normally and also to transmit an Active Error Flag (see Section 13.6.10).

13.6.9.4 Error-Passive

An error-passive CAN-controller may transmit or receive messages normally. In the case of a detected error condition it transmits a Passive Error Flag instead of an Active Error Flag. Hence the influence on bus activities by an error-active CAN-controller (e.g. due to a malfunction) is reduced.

13.6.9.5 Suspend Transmission

After an error-passive CAN-controller has transmitted a message, it sends eight recessive bits after the Intermission Field and then checks for Bus-Idle. If during Suspend Transmission another CAN-controller starts transmitting a message the suspended CAN-controller will become the receiver of this message; otherwise being in Bus-Idle it may start to transmit a further message.

13.6.9.6 Start-Up

A CAN-controller which either was switched off or in the Bus-OFF state, must run a Start-Up routine in order to:

- Synchronize with other available CAN-controllers before starting to transmit. Synchronization is achieved, when 11 recessive bits, equivalent to Acknowledge Delimiter, End-Of-Frame and Intermission Field, have been detected (Bus-Free).
- Wait for other CAN-controllers without passing into the Bus-OFF state (due to a missing acknowledge), if there is no other CAN-controller currently available.

13.6.10 AIMS OF ERROR CONFINEMENT

13.6.10.1 Distinction of short and long disturbances

The CPU must be informed when there are long disturbances and when bus activities have returned to normal operation. During long disturbances, a CAN-controller enters the Bus-OFF state and the CPU may use default values.

Minor disturbances of bus activities will not effect a CAN-controller. In particular, a CAN-controller does not enter the Bus-OFF state or inform the CPU of a short bus disturbance.

13.6.10.2 Detection and localization of hardware disturbances and defects

The rules for error confinement are defined by the CAN-protocol specification (and implemented in the P8XCE598's on-chip CAN-controller), in such a way that the CAN-controller, being nearest to the error-locus, reacts with a high probability the quickest (i.e. becomes error-passive or Bus-OFF). Hence errors can be localized and their influence on normal bus activities is minimized.

13.6.10.3 Error Confinement

All CAN-controllers contain a Transmit Error Counter and a Receive Error Counter, which registers errors during the transmission and the reception of messages, respectively.

If a message is transmitted or received correctly, the count is decreased. In the event of an error, the count is increased. The Error Counters have an non-proportional method of counting: an error causes a larger counter increase than a correctly transmitted/received message causes the count to decrease. Over a period of time this may result in an increase in error counts, even if there are fewer corrupted messages than uncorrupted ones. The level of the Error Counters reflect the relative frequency of disturbances. The ratio of increase/decrease depends on the acceptable ratio of invalid/valid messages on the bus and is hardware implemented to eight.

If one of the Error Counters exceeds the Warning Limit of 96 error points, indicating a significant accumulation of error conditions, this is signalled by the CAN-controller (Error Status, Error Interrupt).

A CAN-controller operates in the error-active mode until it exceeds 127 error points on one of its Error Counters. At this value it will enter the error-passive state. A transmit error which exceeds 255 error points results in the CAN-controller entering the Bus-OFF state.

14 INTERRUPT SYSTEM

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. Interrupt response latency is from 2.25 µs to 7.5 µs when using a 16 MHz crystal. The latency time strongly depends on the sequence of instructions executed directly after an interrupt request. During a CAN-DMA transfer the interrupt system is disabled (see Section 13.5.17). The P8XCE598 acknowledges interrupt requests from fifteen sources as follows:

- $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$: externally via pins 43 and 44 respectively
- Timer 0 and Timer 1: from the two internal counters
  - If the capture function remains unused and the Capture Register contents are 'don't care' then the corresponding input pins 'CTnI', with 'n = 0 ... 3', may be used as positive and/or negative edge triggered external interrupts INT2 to INT5. But note that they can not terminate the Idle mode because the Timer 2 is switched off then.
- Timer T2, 8 separate interrupts:
  - 4 capture interrupts
  - 3 compare interrupts
  - An overflow interrupt.
- ADC end-of-conversion interrupt
- CAN Controller interrupt
- UART serial I/O port interrupt.

Each interrupt vectors to a separate location in Program Memory for its service program. Each source can be individually enabled or disabled by a corresponding bit in the IEN0 or IEN1 register, moreover each interrupt may be programmed to a HIGH or LOW priority level using a corresponding bit in the IP0 or IP1 register. Also all enabled sources can be globally disabled or enabled. Both external interrupts can be programmed to be level-activated or transition-activated, and an active LOW level allows 'wire-ORing' of several interrupt sources to the input pin.

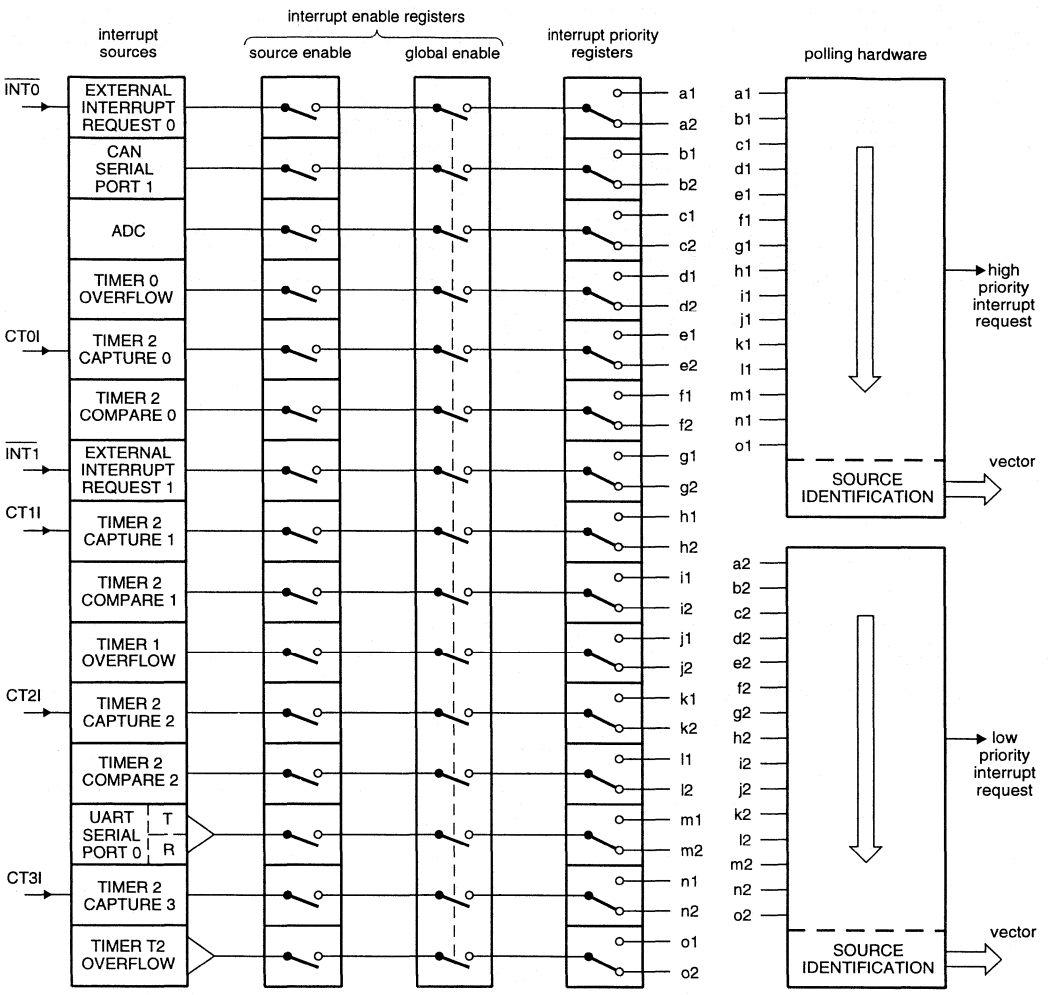


Fig.21 Interrupt system.

14.1 Interrupt Enable and Priority Registers

14.1.1 Interrupt Enable register 0 (IEN0)

Table 71 Interrupt Enable register 0 (address A8H)

7	6	5	4	3	2	1	0
EA	EAD	ES1	ES0	ET1	EX1	ET0	EX0

Table 72 Description of the IEN0 bits

BIT	SYMBOL	FUNCTION
7	EA	**General enable/disable control.** If bit EA is: LOW, then no interrupt is enabled. HIGH, then any individually enabled interrupt will be accepted.
6	EAD	Enable ADC interrupt.
5	ES1	Enable SIO1 (CAN) interrupt.
4	ES0	Enable SIO0 (UART) interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable External 1 interrupt.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable External 0 interrupt.

14.1.2 Interrupt Enable register 1 (IEN1)

Table 73 Interrupt Enable register 0 (address E8H)

7	6	5	4	3	2	1	0
ET2	ECM2	ECM1	ECM0	ECT3	ECT2	ECT1	ECT0

Table 74 Description of the IEN1 bits

Logic 0 = interrupt disabled; logic 1 = interrupt enabled.

BIT	SYMBOL	FUNCTION
7	ET2	Enable T2 overflow interrupt(s).
6	ECM2	Enable T2 comparator 2 interrupt.
5	ECM1	Enable T2 comparator 1 interrupt.
4	ECM0	Enable T2 comparator 0 interrupt.
3	ECT3	Enable T2 capture register 3 interrupt.
2	ECT1	Enable T2 capture register 2 interrupt.
1	ECT1	Enable T2 capture register 1 interrupt.
0	ECT0	Enable T2 capture register 0 interrupt.

14.1.3 Interrupt Priority register 0 (IP0)

Table 75 Interrupt Priority register 0 (address B8H)

7	6	5	4	3	2	1	0
–	PAD	PS1	PS0	PT1	PX1	PT0	PX0

Table 76 Description of the IP0 bits

BIT	SYMBOL	FUNCTION
7	–	Not used.
6	PAD	ADC interrupt priority level.
5	PS1	SIO1 (CAN) interrupt priority level.
4	PS0	SIO0 (UART) interrupt priority level.
3	PT1	Timer 1 interrupt priority level.
2	PX1	External interrupt 1 priority level.
1	PT0	Timer 0 interrupt priority level.
0	PX0	External interrupt 0 priority level.

14.1.4 Interrupt Priority register 1 (IP1)

Table 77 Interrupt Priority register 1 (address F8H)

7	6	5	4	3	2	1	0
PT2	PCM2	PCM1	PCM0	PCT3	PCT2	PCT1	PCT0

Table 78 Description of the IP1 bits

Logic 0 = low priority; logic 1 = high priority.

BIT	SYMBOL	FUNCTION
7	PT2	T2 overflow interrupt(s) priority level.
6	PCM2	T2 comparator 2 priority interrupt level.
5	PCM1	T2 comparator 1 priority interrupt level.
4	PCM0	T2 comparator 0 priority interrupt level.
3	PCT3	T2 capture register 3 priority interrupt level.
2	PCT2	T2 capture register 2 priority interrupt level.
1	PCT1	T2 capture register 1 priority interrupt level.
0	PCT0	T2 capture register 0 priority interrupt level.

14.2 Interrupt Vectors

The vector indicates the Program Memory location where the appropriate interrupt service routine starts (see Table 79).

Table 79 Interrupt vectors

SOURCE	BIT	VECTOR
External 0	X0	0003H
Timer 0 overflow	T0	000BH
External 1	X1	0013H
Timer 1 overflow	T1	001BH
Serial I/O 0 (UART)	S0	0023H
Serial I/O 1 (CAN)	S1	002BH
T2 capture 0	CT0	0033H
T2 capture 1	CT1	003BH
T2 capture 2	CT2	0043H
T2 capture 3	CT3	004BH
ADC completion	ADC	0053H
T2 compare 0	CM0	005BH
T2 compare 1	CM1	0063H
T2 compare 2	CM2	006BH
T2 overflow	T2	0073H

14.3 Interrupt Priority

Each interrupt source can be either high priority or low priority. If both priorities are requested simultaneously, the processor will branch to the high priority vector. If there are simultaneous requests from sources of the same priority, then interrupts will be serviced in the following order:

X0, S1, ADC, T0, CT0, CM0, X1, CT1, CM1, T1, CT2, CM2, S0, CT3, T2.

A low priority interrupt routine can only be interrupted by a high priority interrupt. A high priority interrupt routine can not be interrupted.

15 POWER REDUCTION MODES

The P8XCE598 has three software-selectable modes to reduce power consumption. These are:

- Sleep mode, affecting the CAN Controller only
- Idle mode, affecting the
  - CPU (halted)
  - Timer 2 (stopped and reset)
  - PWM0, PWM1 (reset, output = HIGH)
  - ADC (aborted if in progress)
- Power-down mode, affecting the whole P8XCE598 device.

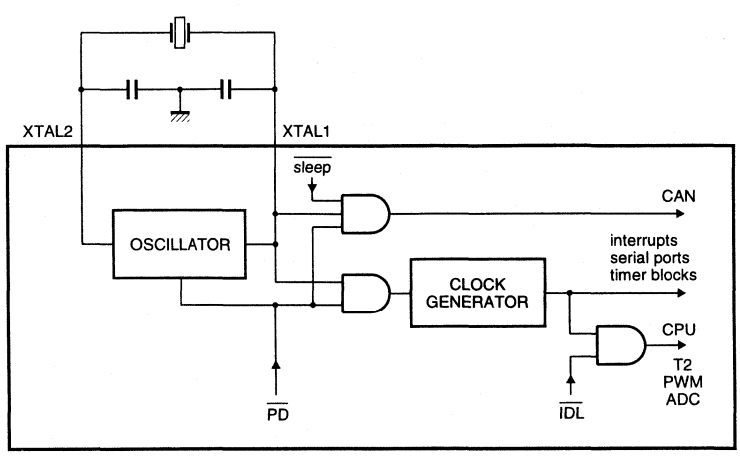


Fig.22 Internal Sleep, Idle and Power-down clock configuration.

15.1 Power Control Register (PCON)

Table 80 Power Control Register (address 87H)

7	6	5	4	3	2	1	0
SMOD	–	RFI	WLE	GF1	GF0	PD	IDL

Table 81 Description of the PCON bits

BIT	SYMBOL	FUNCTION
7	SMOD	**Double Baud rate bit.** When set to logic 1 the baud rate is doubled when the serial port SIO0 is being used in Modes 1, 2 and 3.
6	–	Reserved.
5	RFI	**RFI-Reduction Mode bit.** When set to HIGH the toggling of ALE pin is prohibited. This bit is cleared on RESET; see also ALE/$\overline{\text{PROG}}$ in Sections 2.1 and 2.2.
4	WLE	**Watchdog Load Enable.** This flag must be set by software prior to loading T3 (watchdog timer). It is cleared when T3 is loaded.
3	GF1	**General purpose flag bits.**
2	GF0	
1	PD	**Power-down bit.** Setting this bit activates Power-down mode (note 1). It can only be set if input $\overline{\text{EW}}$ is HIGH.
0	IDL	**Idle mode bit.** Setting this bit activates the Idle mode (note 1).

Note

1. If PD and IDL are set to HIGH at the same time, PD takes precedence. The reset value of PCON is 0X000000B.

15.2 CAN Sleep Mode

In order to reduce power consumption of the P8XCE598 the CAN Controller may be switched off (disconnecting the internal clock) by setting the CAN Command Register bit 4 (Sleep) HIGH. The CAN Controller leaves this Sleep mode by detecting either activity on the CAN-bus (dominant bit-level on CRX0/CRX1; see Chapter 5, Table 1) or by setting the Sleep bit to LOW. As the CPU can not only write to the Sleep bit, but can also read it, the CAN Controller status can be determined directly.

15.3 Idle Mode

The instruction that sets bit PCON.0 to HIGH is the last one executed in the normal operating mode before Idle mode is activated.

Once in the Idle mode, the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in see Table 82.

There are three ways to terminate the Idle mode:

- Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, provided that the interrupt source is active during Idle mode. After the interrupt is serviced, the program continues with the instruction immediately after the one, at which the interrupt request was detected.
- The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
- Another way of terminating the Idle mode is an external hardware reset. Since the oscillator is still running, the reset signal is required to be active only for two machine cycles (24 oscillator periods) to complete to reset operation.
- The third way is the internally generated watchdog reset after an overflow of Timer 3.

15.4 Power-down Mode

The instruction that sets bit PCON.1 to HIGH, is the last one executed before entering the Power-down mode. In Power-down mode the oscillator of the P8XCE598 is stopped. If the CAN Controller is in use, it is recommended to set it into Sleep mode before entering Power-down mode. However, setting PCON.1 to HIGH also sets the Sleep bit (CAN Controller Command Register bit 4) to HIGH.

The P8XCE598 leaves Power-down mode either by a hardware reset or by a CAN Wake-Up interrupt (due to activity on the CAN-bus), if the SIO1 (CAN) interrupt source is enabled (contents of register IEN0 = 1X1XXXXXB).

A hardware reset affects the whole P8XCE598, but leaves the contents of the on-chip RAM unchanged (CAN Controller-and CPU's SFRs are reset, see Section 13.5.2, Chapter 17 and Table 40). A CAN Wake-Up interrupt during Power-down mode causes a reset output pulse with a width of 6144 machine cycles (4.6 ms with f_{CLK} = 16 MHz). All hardware except that for the CAN Controller of the P8XCE598 is reset (i.e. the contents of all CAN Controller registers are preserved).

A capacitance connected to the RST pin can be used to lengthen the internally generated reset pulse. If the pulse exceeds 8192 machine cycles, the CAN Controller part is reset too.

Table 82 Status of external pins during Idle and Power-down modes

MODE	PROGRAM	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1[1]	PORT2	PORT3	PORT4	PWM0/ PWM1
Idle	internal	1	1	port data	port data	port data	port data	port data	1
	external	1	1	floating	port data	address	port data	port data	1
Power-down	internal	0	0	port data	port data	port data	port data	port data	1
	external	0	0	floating	port data	port data	port data	port data	1

Note

1. If the port pins P1.6 and P1.7 are used as the CAN transmitter outputs (CTX0 and CTX1), then during Sleep and Power-down mode these pins output a 'recessive' level (see Sections 13.5.2 and 13.5.11).

16 OSCILLATOR CIRCUITRY

The oscillator circuitry of the P8XCE598 is a single-stage inverting amplifier in a Pierce oscillator configuration. The circuitry between XTAL1 and XTAL2 is basically an inverter biased to the transfer point. Either a crystal or ceramic resonator can be used as the feedback element to complete the oscillator circuitry. Both are operated in parallel resonance. XTAL1 (pin 52) is the high gain amplifier input, and XTAL2 (pin 51) is the output (see Fig.23). If XTAL1 is driven from an external source, XTAL2 must be left open (see Fig.24).

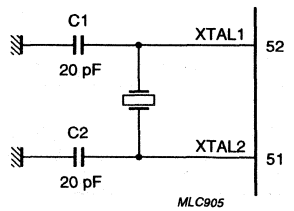


Fig.23 P8XCE598 oscillator circuit.

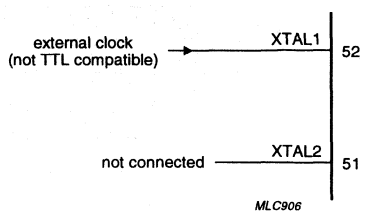


Fig.24 Driving P8XCE598 from an external source.

17 RESET CIRCUITRY

The reset pin RST is connected to a Schmitt trigger for noise rejection (see Fig.25). A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods). The CPU responds by executing an internal reset. During reset ALE and $\overline{PSEN}$ output a HIGH level. In order to perform a correct reset, this level must not be affected by external elements.

Also with the P8XCE598, the RST line can be pulled HIGH internally by a pull-up transistor activated by the Watchdog timer T3. The length of the output pulse from T3 is 3 machine cycles. A pulse of such short duration is necessary in order to recover from a processor or system fault as fast as possible.

During Power-down a reset could be generated internally via the CAN Wake-Up interrupt. Then the RST pin is pulled HIGH for 6144 machine cycles. In this case the CAN Controller is not reset.

If the Watchdog timer or the CAN Wake-Up interrupt is used to reset external devices, the usual capacitor arrangement for Power-on reset (see Fig.26) should not be used.

However, the internal reset is forced, independent of the external level on the RST pin.

The MAIN RAM and AUXILIARY RAM are not affected. When V_{DD} is turned on, the RAM content is indeterminate. A reset leaves the internal registers as shown in Table 83).

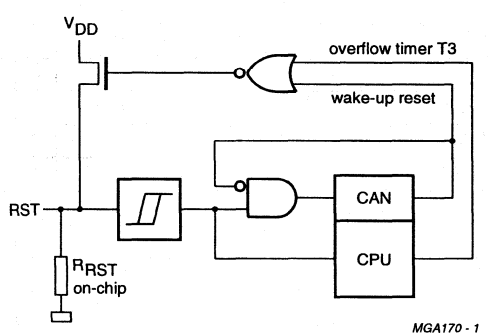


Fig.25 On-chip reset configuration.

Table 83 Internal registers' contents after a reset
X = undefined state.

REGISTER	7	6	5	4	3	2	1	0
CPU part								
ACC	0	0	0	0	0	0	0	0
ADC0	X	X	0	0	0	0	0	0
ADCH	X	X	X	X	X	X	X	X
B	0	0	0	0	0	0	0	0
CML0 to CML2	0	0	0	0	0	0	0	0
CMH0 to CMH2	0	0	0	0	0	0	0	0
CTCON	0	0	0	0	0	0	0	0
CTL0 to CTL3	X	X	X	X	X	X	X	X
CTH0 to CTH3	X	X	X	X	X	X	X	X
DPL	0	0	0	0	0	0	0	0
DPH	0	0	0	0	0	0	0	0
IEN0	0	0	0	0	0	0	0	0
IEN1	0	0	0	0	0	0	0	0
IP0	X	0	0	0	0	0	0	0
IP1	0	0	0	0	0	0	0	0
PCH	0	0	0	0	0	0	0	0
PCL	0	0	0	0	0	0	0	0
PCON	0	X	0	0	0	0	0	0
PSW	0	0	0	0	0	0	0	0
PWM0	0	0	0	0	0	0	0	0
PCWM1	0	0	0	0	0	0	0	0
PCWMP	0	0	0	0	0	0	0	0
P0 to P4	1	1	1	1	1	1	1	1
P5	X	X	X	X	X	X	X	X
RTE	0	0	0	0	0	0	0	0
S0BUF	X	X	X	X	X	X	X	X
S0CON	0	0	0	0	0	0	0	0

REGISTER	7	6	5	4	3	2	1	0
CANSTA	0	0	0	0	1	1	0	0
CANCON	X	X	X	0	0	0	0	0
CANDAT	X	X	X	X	X	X	X	X
CANADR	0	X	1	0	0	1	0	0
SP	0	0	0	0	0	1	1	1
STE	1	1	0	0	0	0	0	0
TCON	0	0	0	0	0	0	0	0
TH0, TH1	0	0	0	0	0	0	0	0
TMH2	0	0	0	0	0	0	0	0
TL0, TL1	0	0	0	0	0	0	0	0
TML2	0	0	0	0	0	0	0	0
TMOD	0	0	0	0	0	0	0	0
TM2CON	0	0	0	0	0	0	0	0
TM2IR	0	0	0	0	0	0	0	0
T3	0	0	0	0	0	0	0	0
CAN part								
CR	0	X	1	X	X	X	X	1
CMR	1	1	X	0	X	X	X	X
SR	0	0	0	0	1	1	0	0
IR	X	X	X	0	0	0	0	0
ACR	X	X	X	X	X	X	X	X
AMR	X	X	X	X	X	X	X	X
BTR0	X	X	X	X	X	X	X	X
BTR1	X	X	X	X	X	X	X	X
OCR	X	X	X	X	X	X	X	X
TR	X	X	X	X	X	X	X	X
TXB 10 to 19	X	X	X	X	X	X	X	X
RXB 20 to 29	X	X	X	X	X	X	X	X

17.1 Power-on Reset

If the RST pin is connected to V_{DD} via a 2.2 µF capacitor, as shown in Fig.26, an automatic reset can be obtained by switching on V_{DD} (provided its rise time is <10 ms). The decrease of the RST pin voltage depends on the capacitor and the internal resistor R_{RST}. That voltage must remain above the lower threshold for at minimum the oscillator start-up time plus 2 machine cycles.

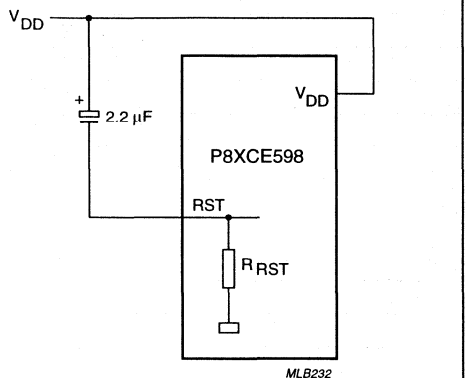


Fig.26 Power-on reset.

18 INSTRUCTION SET

The P8XCE598 uses the powerful instruction set of the P80C51. It consists of 49 single-byte, 45 two-byte and 17 three-byte instructions. Using a 16 MHz quartz, 64 of the instructions are executed in 0.75 µs, 45 in 1.5 µs and the multiply, divide instructions in 3 µs. A summary of the instruction set is given in Tables 84, 85, 86, 87 and 88.

18.1 Addressing Modes

Most instructions have a 'destination/source' field that specifies the data type, addressing modes and operands involved. For all these instructions, except from MOVs, the destination operand is also a source operand (e.g. ADD A, R7).

Five types of addressing modes are used:

- Register Addressing,
  - R0 to R7 (4 banks)
  - A,B,C (bit), AB (2 bytes), DPTR (double byte).
- Direct Addressing,
  - lower 128 bytes of internal Main RAM (including the 4 R0 to R7 register banks)
  - Special Function Registers (SFRs)
  - 128 bits in a subset of the internal Main RAM (see Fig.5)
  - 128 bits in a subset of the Special Function Registers (see Figs 6 and 7).
- Register-Indirect Addressing,
  - internal RAM (@R0, @R1, @SP [PUSH/POP])
  - internal Auxiliary RAM (@R0, @R1, @DPTR)
  - external Data Memory (@DPTR).
- Immediate Addressing,
  - Program Memory (in-code 8 bit or 16 bit constant)
- Base-Register-plus Index-Register-Indirect Addressing,
  - Program Memory look-up table (@DPTR+A, @PC+A).

The first three addressing modes are usable for destination operands.

18.2 Instruction Set

For the description of the **Data Addressing Modes** and **Hexadecimal opcode cross-reference** see Table 88.

Table 84 Instruction set description: Arithmetic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Arithmetic operations					
ADD	A,Rr	Add register to A	1	1	2*
ADD	A,direct	Add direct byte to A	2	1	25
ADD	A,@Ri	Add indirect RAM to A	1	1	26, 27
ADD	A,#data	Add immediate data to A	2	1	24
ADDC	A,Rr	Add register to A with carry flag	1	1	3*
ADDC	A,direct	Add direct byte to A with carry flag	2	1	35
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A,#data	Add immediate data to A with carry flag	2	1	34
SUBB	A,Rr	Subtract register from A with borrow	1	1	9*
SUBB	A,direct	Subtract direct byte from A with borrow	2	1	95
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A,#data	Subtract immediate data from A with borrow	2	1	94
INC	A	Increment A	1	1	04
INC	Rr	Increment register	1	1	0*
INC	direct	Increment direct byte	2	1	05
INC	@Ri	Increment indirect RAM	1	1	06, 07
DEC	A	Decrement A	1	1	14
DEC	Rr	Decrement register	1	1	1*
DEC	direct	Decrement direct byte	2	1	15
DEC	@Ri	Decrement indirect RAM	1	1	16, 17
INC	DPTR	Increment data pointer	1	2	A3
MUL	AB	Multiply A and B	1	4	A4
DIV	AB	Divide A by B	1	4	84
DA	A	Decimal adjust A	1	1	D4

Table 85 Instruction set description: Logic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Logic operations					
ANL	A,Rr	AND register to A	1	1	5*
ANL	A,direct	AND direct byte to A	2	1	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	1	54
ANL	direct,A	AND A to direct byte	2	1	52
ANL	direct,#data	AND immediate data to direct byte	3	2	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	1	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	1	44
ORL	direct,A	OR A to direct byte	2	1	42
ORL	direct,#data	OR immediate data to direct byte	3	2	43
XRL	A,Rr	Exclusive-OR register to A	1	1	6*
XRL	A,direct	Exclusive-OR direct byte to A	2	1	65
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	Exclusive-OR immediate data to A	2	1	64
XRL	direct,A	Exclusive-OR A to direct byte	2	1	62
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2	63
CLR	A	Clear A	1	1	E4
CPL	A	Complement A	1	1	F4
RL	A	Rotate A left	1	1	23
RLC	A	Rotate A left through the carry flag	1	1	33
RR	A	Rotate A right	1	1	03
RRC	A	Rotate A right through the carry flag	1	1	13
SWAP	A	Swap nibbles within A	1	1	C4

Table 86 Instruction set description: Data transfer

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Data transfer					
MOV	A,Rr	Move register to A	1	1	E*
MOV	A,direct (note 1)	Move direct byte to A	2	1	E5
MOV	A,@Ri	Move indirect RAM to A	1	1	E6, E7
MOV	A,#data	Move immediate data to A	2	1	74
MOV	Rr,A	Move A to register	1	1	F*
MOV	Rr,direct	Move direct byte to register	2	2	A*
MOV	Rr,#data	Move immediate data to register	2	1	7*
MOV	direct,A	Move A to direct byte	2	1	F5
MOV	direct,Rr	Move register to direct byte	2	2	8*
MOV	direct,direct	Move direct byte to direct	3	2	85
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	Move immediate data to direct byte	3	2	75
MOV	@Ri,A	Move A to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1	76, 77
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2	90
MOVC	A,@A+DPTR	Move code byte relative to DPTR to A	1	2	93
MOVC	A,@A+PC	Move code byte relative to PC to A	1	2	83
MOVX	A,@Ri	Move external RAM (8-bit address) to A	1	2	E2, E3
MOVX	A,@DPTR	Move external RAM (16-bit address) to A	1	2	E0
MOVX	@Ri,A	Move A to external RAM (8-bit address)	1	2	F2, F3
MOVX	@DPTR,A	Move A to external RAM (16-bit address)	1	2	F0
PUSH	direct	Push direct byte onto stack	2	2	C0
POP	direct	Pop direct byte from stack	2	2	D0
XCH	A,Rr	Exchange register with A	1	1	C*
XCH	A,direct	Exchange direct byte with A	2	1	C5
XCH	A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD	A,@Ri	Exchange LOW-order digit indirect RAM with A	1	1	D6, D7

Note

1. MOV A,ACC is not permitted.

Table 87 Instruction set description: Boolean variable manipulation, Program and machine control

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Boolean variable manipulation					
CLR	C	Clear carry flag	1	1	C3
CLR	bit	Clear direct bit	2	1	C2
SETB	C	Set carry flag	1	1	D3
SETB	bit	Set direct bit	2	1	D2
CPL	C	Complement carry flag	1	1	B3
CPL	bit	Complement direct bit	2	1	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C,bit	OR direct bit to carry flag	2	2	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C,bit	Move direct bit to carry flag	2	1	A2
MOV	bit,C	Move carry flag to direct bit	2	2	92
Program and machine control					
ACALL	addr11	Absolute subroutine call	2	2	•1
LCALL	addr16	Long subroutine call	3	2	12
RET		Return from subroutine	1	2	22
RETI		Return from interrupt	1	2	32
AJMP	addr11	Absolute jump	2	2	♦1
LJMP	addr16	Long jump	3	2	02
SJMP	rel	Short jump (relative address)	2	2	80
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2	73
JZ	rel	Jump if A is zero	2	2	60
JNZ	rel	Jump if A is not zero	2	2	70
JC	rel	Jump if carry flag is set	2	2	40
JNC	rel	Jump if carry flag is not set	2	2	50
JB	bit,rel	Jump if direct bit is set	3	2	20
JNB	bit,rel	Jump if direct bit is not set	3	2	30
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2	10
CJNE	A,direct,rel	Compare direct to A and jump if not equal	3	2	B5
CJNE	A,#data,rel	Compare immediate to A and jump if not equal	3	2	B4
CJNE	Rr,#data,rel	Compare immediate to register and jump if not equal	3	2	B*
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	2	B6, B7
DJNZ	Rr,rel	Decrement register and jump if not zero	2	2	D*
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2	D5
NOP		No operation	1	1	00

Table 88 Description of the mnemonics in the Instruction set

MNEMONIC	DESCRIPTION
Data addressing modes	
Rr	Working register R0-R7.
direct	128 internal RAM locations and any special function register (SFR).
@Ri	Indirect internal RAM location addressed by register R0 or R1 of the actual register bank.
#data	8-bit constant included in instruction.
#data 16	16-bit constant included as bytes 2 and 3 of instruction.
bit	Direct addressed bit in internal RAM or SFR.
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 kbytes Program Memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 kbytes page of Program Memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is –128 to +127 bytes relative to first byte of the following instruction.
Hexadecimal opcode cross-reference	
*	8, 9, A, B, C, D, E, F.
•	1, 3, 5, 7, 9, B, D, F.
♦	0, 2, 4, 6, 8, A, C, E.

Table 89 Instruction map

First hexadecimal character of opcode ↓	← Second hexadecimal character of opcode → 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC direct	INC @Ri 0	1	INC Rr 0	1	2	3	4	5	6	7
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC direct	DEC @Ri 0	1	DEC Rr 0	1	2	3	4	5	6	7
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,direct	ADD A,@Ri 0	1	ADD A,Rr 0	1	2	3	4	5	6	7
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,direct	ADDC A,@Ri 0	1	ADDC A,Rr 0	1	2	3	4	5	6	7
4	JC rel	AJMP addr11	ORL direct,A	ORL direct,#data	ORL A,#data	ORL A,direct	ORL A,@Ri 0	1	ORL A,Rr 0	1	2	3	4	5	6	7
5	JNC rel	ACALL addr11	ANL direct,A	ANL direct,#data	ANL A,#data	ANL A,direct	ANL A,@Ri 0	1	ANL A,Rr 0	1	2	3	4	5	6	7
6	JZ rel	AJMP addr11	XRL direct,A	XRL direct,#data	XRL A,#data	XRL A,direct	XRL A,@Ri 0	1	XRL A,Rr 0	1	2	3	4	5	6	7
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV direct,#data	MOV @Ri,#data 0	1	MOV Rr,#data 0	1	2	3	4	5	6	7
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV direct,direct	MOV direct,@Ri 0	1	MOV direct,Rr 0	1	2	3	4	5	6	7
9	MOV DTPR,#data16	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,direct	SUBB A,@Ri 0	1	SUB A,Rr 0	1	2	3	4	5	6	7
A	ORL C,/bit	AJMP addr11	MOV bit,C	INC DPTR	MUL AB		MOV @Ri,direct 0	1	MOV Rr,direct 0	1	2	3	4	5	6	7
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A,#data,rel	CJNE A,direct,rel	CJNE @Ri,#data,rel 0	1	CJNE Rr,#data,rel 0	1	2	3	4	5	6	7
C	PUSH direct	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,direct	XCH A,@Ri 0	1	XCH A,Rr 0	1	2	3	4	5	6	7
D	POP direct	ACALL addr11	SETB bit	SETB C	DA A	DJNZ direct,rel	XCHD A,@Ri 0	1	DJNZ Rr,rel 0	1	2	3	4	5	6	7
E	MOVX A,@DTPR	AJMP addr11	MOVX A,@Ri 0	1	CLR A	MOV A,direct (1)	MOV A,@Ri 0	1	MOV A,Rr 0	1	2	3	4	5	6	7
F	MOVX @DTPR,A	ACALL addr11	MOVX @Ri,A 0	1	CPL A	MOV direct,A	MOV @Ri,A 0	1	MOV Rr,A 0	1	2	3	4	5	6	7

Note

1. MOV A, ACC is not a valid instruction.

19 ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134); note 1

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	voltage on V_{DD} pins	−0.5	+6.5	V
V_I (note 1)	input voltage on any pin (except CTX0, CTX1, CRX0, CRX1 and $\overline{EA}/V_{PP}$)	−0.5	V_{DD} + 0.5	V
V_I (note 2)	input voltage on $\overline{EA}/V_{PP}$ to V_{SS}	−0.5	+13	V
I_I, I_O	input/output current on any single I/O pin (except from CTX0 and CTX1)	−	±10	mA
I_{OT}	sink current of CTX0, CTX1 together	−	30	mA
	source current of CTX0, CTX1 together	−	−20	mA
P_{tot}	total power dissipation (note 2)	−	1.0	W
T_{stg}	storage temperature range	−65	+150	°C
T_{amb}	operating ambient temperature range:			
	P87CE598 EFQ/EFB	−40	+85	°C
	P83CE598 FFB/P80CE598 FFB	−40	+85	°C
	P83CE598 FHB/P80CE598 FHB	−40	+125	°C

Notes

1. The following applies to the Absolute Maximum Ratings:
   a) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Chapters "AC characteristics" and "DC characteristics" of this specification is not implied.
   b) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effect of exessive static charge. However, its suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
   c) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
2. This value is based on the maximum allowable die temperature and the thermal resistance of the package, not on device power consumption.

20 DC CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified.

T_{amb} = −40 to +125 °C for the **P83CE598/P80CE598**; T_{amb} = −40 to +85 °C for the **P83CE598/P80CE598/ P87CE598.**

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply (digital part)					
V_{DD}	supply voltage		4.5	5.5	V
I_{DD}	operating supply current	f_{CLK} = 16 MHz; note 1	–	50	mA
$I_{DD(ID)}$	supply current Idle mode	f_{CLK} = 16 MHz; note 2	–	15	mA
$I_{DD(IS)}$	supply current Idle & Sleep mode	f_{CLK} = 16 MHz; note 3	–	10	mA
$I_{DD(PD)}$	supply current Power-down mode:	note 4			
	P8XCE598 FHB		–	150	µA
	P8XCE598 FFB		–	50	µA
	P87CE598 EFx		–	70	µA
Inputs					
V_{IL}	LOW level input voltage (except $\overline{EA}$, CRX0 and CRX1)		−0.5	$0.2V_{DD}$ − 0.1	V
V_{IL1}	LOW level input voltage $\overline{EA}$		−0.5	$0.2V_{DD}$ − 0.3	V
V_{IH}	HIGH level input voltage (except RST, XTAL1, CRX0,CRX1)		$0.2V_{DD}$ + 0.9	V_{DD} + 0.5	V
V_{IH1}	HIGH level input voltage (RST and XTAL1)		$0.7V_{DD}$	V_{DD} + 0.5	V
I_{IL}	LOW level input current Ports 1, 2, 3 and 4	V_I = 0.45 V	–	−50	µA
I_{TL}	input current HIGH-to-LOW transition Ports 1, 2, 3 and 4 (except P1.6 and P1.7)	V_I = 2.0 V to 0.45 V	–	−650	µA
I_{LI1}	input leakage current Port 0, $\overline{EA}$, STADC, $\overline{EW}$, P1.6, P1.7	0.45 V < V_I < V_{DD}	–	±10	µA
I_{LI2}	input leakage current Port 5	0.45 V < V_I < V_{DD}	–	±1	µA
Outputs					
V_{OL}	LOW level output voltage Ports 1, 2, 3 and 4 (except P1.6 and P1.7)	I_{OL} = 1.6 mA; note 5	–	0.45	V
V_{OL1}	LOW level output voltage Port 0, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$, P1.6, P1.7	I_{OL} = 3.2 mA; note 5	–	0.45	V
V_{OH}	HIGH level output voltage Ports 1, 2, 3 and 4 (except P1.6 and P1.7)	I_{OH} = −60 µA	2.4	–	V
		I_{OH} = −25 µA	$0.75V_{DD}$	–	V
		I_{OH} = −10 µA	$0.9V_{DD}$	–	V
V_{OH1}	HIGH level output voltage Port 0 in external bus mode, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$	I_{OH} = −400 µA	2.4	–	V
		I_{OH} = −150 µA	$0.75V_{DD}$	–	V
		I_{OH} = −40 µA; note 6	$0.9V_{DD}$	–	V

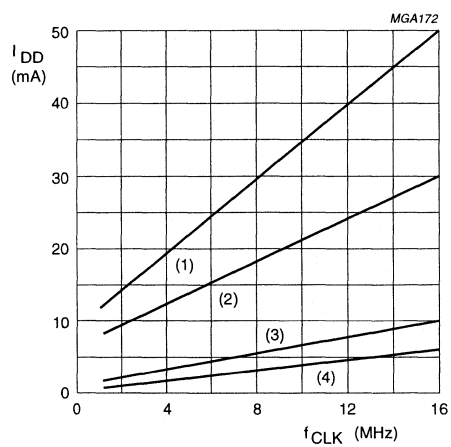
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{OH2}	HIGH level output voltage RST	I_{OH} = –400 µA I_{OH} = –120 µA	2.4 $0.8V_{DD}$	– –	V V
R_{RST}	RST pull-down resistor		50	150	kΩ
$C_{I/O}$	I/O pin capacitance	test frequency = 1 MHz; T_{amb} = 25 °C	–	10	pF
Supply (analog part)					
AV_{DD}	supply voltage	$AV_{DD} = V_{DD} \pm 0.2$ V	4.5	5.5	V
AI_{DD}	supply current operating	Port 5 = AV_{DD}; note 1	–	2.5	mA
$AI_{DD(ID)}$	supply current Idle mode	note 2	–	2.5	mA
$AI_{DD(IS)}$	supply current Idle and Sleep mode: P8XCE598 FHB P8XCE598 xFx	note 3	 – –	 400 350	 µA µA
$AI_{DD(PD)}$	supply current Power-down mode: P8XCE598 FHB P8XCE598 xFx	note 4	 – –	 400 350	 µA µA
Analog inputs					
AV_{IN}	analog input voltage		AV_{SS} – 0.2	AV_{DD} + 0.2	V
AV_{REF-}	reference voltage		AV_{SS} – 0.2	–	V
AV_{REF+}			–	AV_{DD} + 0.2	V
R_{REF}	resistance between AV_{REF+} and AV_{REF-}		10	50	kΩ
C_{IA}	analog input capacitance		–	15	pF
t_{ADS}	sampling time	note 7	–	$8t_{CY}$	µs
t_{ADC}	conversion time (including sample time)	note 7	–	$50t_{CY}$	µs
DL_e	differential non-linearity	notes 8, 9 and 10	–	±1	LSB
IL_e	integral non-linearity	notes 8 and 11	–	±2	LSB
OS_e	offset error	notes 8 and 12	–	±2	LSB
G_e	gain error	notes 8 and 13	–	±0.4	%
A_e	absolute voltage error	notes 8 and 14	–	±3	LSB
M_{ctc}	channel-to-channel matching		–	±1	LSB
C_t	crosstalk between P5 inputs	0 to 100 kHz	–	–60	dB
CAN input comparator (CRX0, CRX1)					
V_{DIF}	differential input voltage (note 15)	AV_{DD} = 5 V ± 5%; 1.4 V < V_I < AV_{DD} – 1.4 V	±32	–	mV
V_{HYST}	hysteresis voltage (note 15)		8	30	mV
I_I	input current		–	±400	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
CAN output driver (V_{DD} = 5 V ± 5%)					
V_{OLT}	output voltage LOW (CTX0 and CTX1)	I_o = 1.2 mA; note 15 I_o = 10 mA	– –	0.1 0.6	V V
V_{OHT}	output voltage HIGH (CTX0 and CTX1)	I_o = –1.2 mA; note 15 I_o = –10 mA; note 16	V_{DD}–0.1 V_{DD}–0.6	– –	V V
Reference (AV_{DD} = 5 V ± 5%)					
V_{REFOUT}	REF output voltage	–0.1 mA < I_L < 0.1 mA; C_L = 10 nF; note 15; bit Reference Active = HIGH	$\frac{1}{2}AV_{DD}$–0.1	$\frac{1}{2}AV_{DD}$+0.1	V
I_{REFIN}	REF input current	1.5 V < V_{REFIN} < AV_{DD}–1.5 V; bit Reference Active = LOW	–	±10	µA

Notes to the DC characteristics

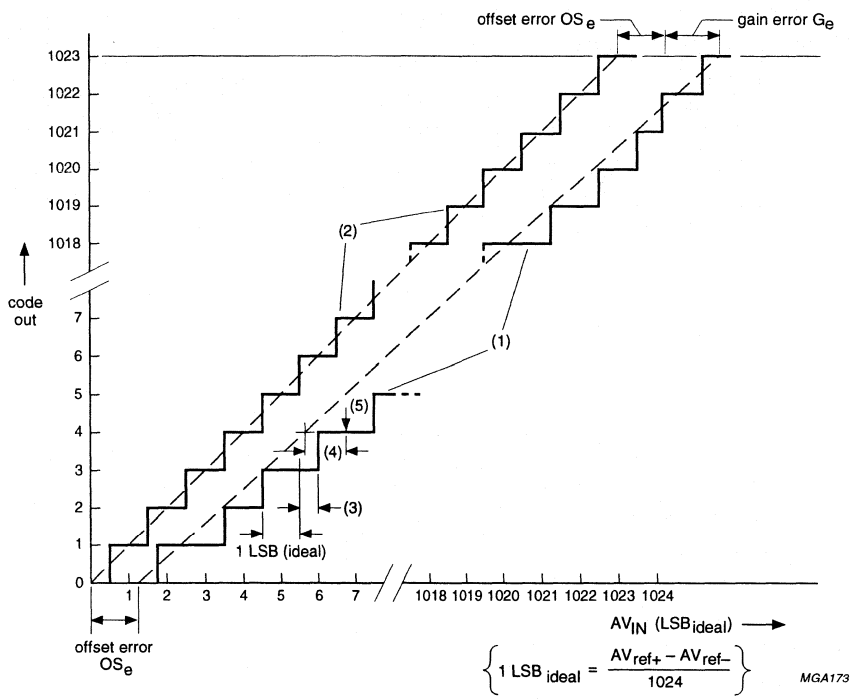
1. Conditions for:
   a) The **digital** operating current measurement: all output pins disconnected; XTAL1 is driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$ + 0.5 V; $V_{IH} = V_{DD}$ – 0.5 V; $\overline{EA}$ = RST = Port 0 = P1.6 = P1.7 = $\overline{EW}$ = V_{DD}; STADC = V_{SS}; CRX0 = 2.7 V; CRX1 = 2.3 V.
   b) The **analog** operating current measurement: Port 5 = AV_{DD}; CAN: register 6: = 00H; load current reference voltage source 100 µA.
2. Conditions for:
   a) The **digital** Idle mode supply current measurement: all output pins disconnected; XTAL1 is driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$ + 0.5 V; $V_{IH} = V_{DD}$ – 0.5 V; Port 0 = P1.6 = P1.7 = $\overline{EW}$ = V_{DD}; $\overline{EA}$ = RST = STADC = V_{SS}; CRX0 = 2.7 V; CRX1 = 2.3 V.
   b) The **analog** Idle mode current measurement: Port 5 = AV_{DD}; CAN: register 6: = 00H; load current reference voltage source 100 µA.
3. Conditions for:
   a) The **digital** Idle and Sleep mode supply current measurement: all output pins disconnected; XTAL1 is driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$ + 0.5 V; $V_{IH} = V_{DD}$ – 0.5 V; Port 0 = P1.6 = P1.7 = $\overline{EW}$ = CRX0 = V_{DD}; $\overline{EA}$ = RST = STADC = CRX1 = V_{SS}; CAN: register 6: = 00H, register 7: = 12H, register 8: = 02H, register 0: = 20H, wait 15t_{CY}, register 1: = 10H, wait for bit Sleep = 1.
   b) The **analog** Idle and Sleep mode current measurement: Port 5 = AV_{DD}; load current reference voltage source 100 µA.
4. Window devices have to be covered. Conditions for:
   a) The **digital** Power-down mode supply current measurement: all output pins and Port 5 disconnected; Port 0 = P1.6 = P1.7 = $\overline{EW}$ = CRX0 = V_{DD}; $\overline{EA}$ = RST = STADC = CRX1 = XTAL1 = AV_{REF+} = AV_{REF-} = CV_{SS} = V_{SS}; AV_{DD} = V_{DD}, but current into AVDD pin is not comprised in digital Power-down current.
   b) The **analog** Power-down mode supply current measurement: Port 5 = AV_{DD}.
5. Capacitive loads on Port 0 and Port 2 may degrade the LOW level output voltage of ALE, Port 1 and Port 3. During a HIGH-to-LOW transition on the Port 0 and Port 2 pins and a capacitive load > 100 pF, the ALE LOW level may exceed 0.8 V. In the case that it is necessary to connect ALE to a Schmitt trigger input respectively use an address latch with a Schmitt trigger STROBE input.

6. Capacitive loads on Port 0 and Port 2 may cause a HIGH level voltage degradation of ALE and $\overline{PSEN}$ below $0.9V_{DD}$ during the address bits are stabilizing.
7. $t_{CY} = 12\ t_{CLK}$ is the machine cycle time.
8. $AV_{REF+} = 5.12$ V; $AV_{REF-} = 0$ V; $AV_{DD} = 5.0$ V.
9. The differential non-linearity (DL_e) is the difference between the actual step width and the ideal step width.
10. The ADC is monotonic, there are no missing codes.
11. The integral non-linearity (IL_e) is the peak difference between the centre of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset error.
12. The offset error (OS_e) is the absolute difference between the straight line which fits the actual transfer curve after removing gain error, and a straight line which fits the ideal transfer curve. The offset error is constant at every point of the actual transfer curve.
13. The gain error (G_e) is relative difference in percent between the straight line fitting the actual transfer curve after removing offset error and the straight line which fits the ideal transfer curve. The gain error is constant at every point on the transfer curve.
14. The absolute voltage error (A_e) is the maximum difference between the centre of the steps of the actual transfer curve of the not calibrated ADC and the ideal transfer curve.
15. Not tested during production.
16. Source current for the CTX0, CTX1 outputs together.



(1) Maximum Operating mode (I_{DD}); $V_{DD} = 5.5$ V.
(2) Maximum Operating mode (I_{DD}); $V_{DD} = 4.5$ V.
(3) Maximum Idle and Sleep mode ($I_{DD(IS)}$); $V_{DD} = 5.5$ V.
(4) Maximum Idle and Sleep mode ($I_{DD(IS)}$); $V_{DD} = 4.5$ V.

Fig.27 Supply current (I_{DD}) as a function of frequency at XTAL1 (f_{CLK}).



(1) Example of an actual transfer curve.
(2) The ideal transfer curve.
(3) Differential non-linearity (DL_e).
(4) Integral non-linearity (IL_e).
(5) Centre of a step of the actual transfer curve.

Fig.28 ADC conversion characteristic.

21 AC CHARACTERISTICS

See notes 1 and 2; C_L = 100 pF for Port 0, ALE and $\overline{PSEN}$; C_L = 80 pF for all other outputs unless otherwise specified.

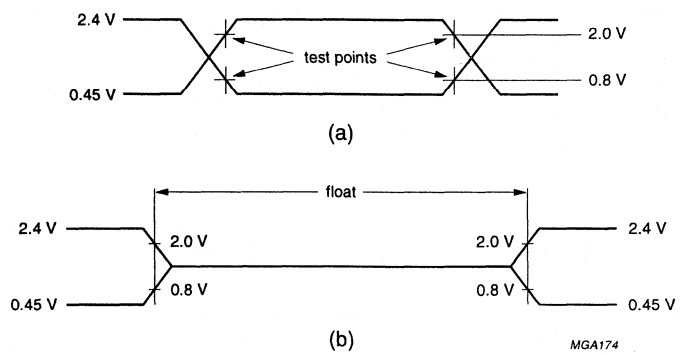
SYMBOL	PARAMETER	f_{CLK} = 16 MHz		f_{CLK} = 12 MHz		VARIABLE CLOCK 1.2 to 16 MHz		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
External Program Memory								
t_{LHLL}	ALE pulse width	85	–	127	–	$2t_{CLK} - 40$	–	ns
t_{AVLL}	address valid to ALE LOW	8	–	28	–	$t_{CLK} - 55$	–	ns
t_{LLAX}	address hold after ALE LOW	28	–	48	–	$t_{CLK} - 35$	–	ns
t_{LLIV}	ALE LOW to valid instruction in	–	150	–	233	–	$4t_{CLK} - 100$	ns
t_{LLPL}	ALE LOW to $\overline{PSEN}$ LOW	23	–	43	–	$t_{CLK} - 40$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	143	–	205	–	$3t_{CLK} - 45$	–	ns
t_{PLIV}	$\overline{PSEN}$ LOW to valid instruction in	–	83	–	145	–	$3t_{CLK} - 105$	ns
t_{PXIX}	input instruction hold after $\overline{PSEN}$	0	–	0	–	0	–	ns
t_{PXIZ}	input instruction float after $\overline{PSEN}$	–	38	–	59	–	$t_{CLK} - 25$	ns
t_{AVIV}	address to valid instruction in	–	208	–	312	–	$5t_{CLK} - 105$	ns
t_{PLAZ}	$\overline{PSEN}$ LOW to address float	–	10	–	10	–	10	ns
External data memory								
t_{RLRH}	$\overline{RD}$ pulse width	275	–	400	–	$6t_{CLK} - 100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	275	–	400	–	$6t_{CLK} - 100$	–	ns
t_{AVLL}	address valid to ALE LOW	8	–	28	–	$t_{CLK} - 55$	–	ns
t_{LLAX}	address hold after ALE LOW	33	–	53	–	$t_{CLK} - 30$	–	ns
t_{RLDV}	$\overline{RD}$ LOW to valid data in	–	148	–	252	–	$5t_{CLK} - 165$	ns
t_{RHDX}	data hold after $\overline{RD}$	0	–	0	–	0	–	ns
t_{RHDZ}	data float after $\overline{RD}$	–	55	–	97	–	$2t_{CLK} - 70$	ns
t_{LLDV}	ALE LOW to valid data in	–	350	–	517	–	$8t_{CLK} - 150$	ns
t_{AVDV}	address to valid data in	–	398	–	585	–	$9t_{CLK} - 165$	ns
t_{LLWL}	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW	138	238	200	300	$3t_{CLK} - 50$	$3t_{CLK} + 50$	ns
t_{AVWL}	address valid to $\overline{RD}$ or $\overline{WR}$ LOW	120	–	203	–	$4t_{CLK} - 130$	–	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	23	103	43	123	$t_{CLK} - 40$	$t_{CLK} + 40$	ns
t_{QVWX}	data valid to $\overline{WR}$ transition	3	–	23	–	$t_{CLK} - 60$	–	ns
t_{QVWH}	data valid time $\overline{WR}$ HIGH	288	–	433	–	$7t_{CLK} - 150$	–	ns
t_{WHQX}	data hold after $\overline{WR}$	13	–	33	–	$t_{CLK} - 50$	–	ns
t_{RLAZ}	$\overline{RD}$ LOW to address float	–	0	–	0	–	0	ns

Notes

1. For the AC Characteristics the following conditions are valid:
   a) **P8XCE598 FxB**: V_{DD} = 5 V ± 10%; T_{amb} = –40 to +85 °C (125 °C); f_{CLK} = 1.2 to 16 MHz.
   b) **P87CE598 EFx**: V_{DD} = 5 V ± 10%; T_{amb} = –40 to +85 °C; f_{CLK} = 3.5 to 16 MHz.
2. $t_{CLK} = \frac{1}{f_{CLK}}$ = one oscillator clock period; t_{CLK} = 62.5 ns at f_{CLK} = 16 MHz.

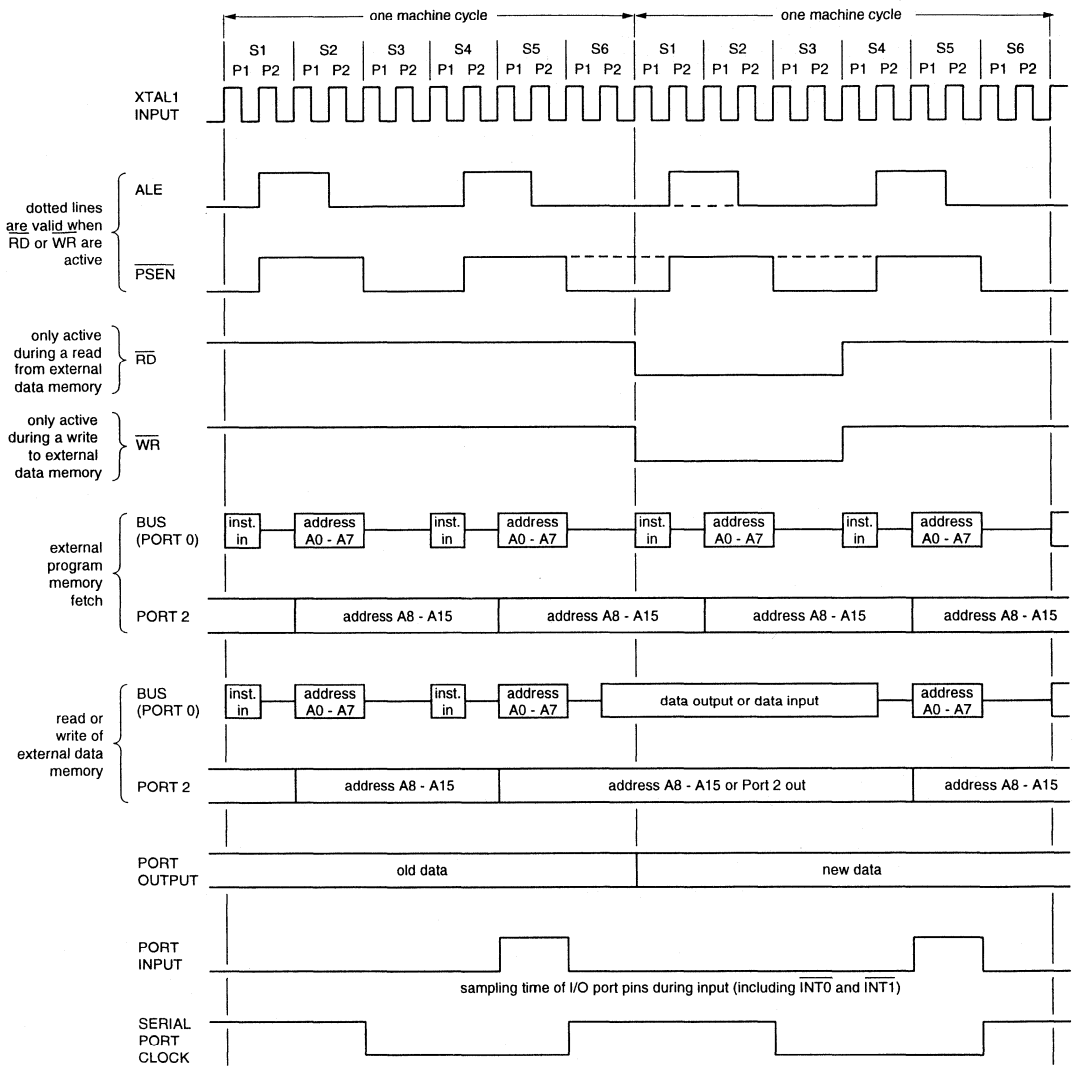
Table 90 CAN characteristics.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
CAN input comparator/output driver					
t_{sd}	sum of input and output delay	AV_{DD} = 5 V ± 5%; V_{DIF} = ± 32 mV; 1.4 V < V_I < AV_{DD} − 1.4 V			
	P8XCE598 xFx		–	60	ns
	P8XCE598 FHB		–	70	ns



AC testing inputs are driven at 2.4 V for a HIGH and 0.45 V for a LOW.
Timing measurements are taken at 2.0 V for a HIGH and 0.8 V for a LOW, see Fig.29 (a).
The float state is defined as the point at which a Port 0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels, see Fig.29 (b).

Fig.29 AC testing input, output waveform (a) and float waveform (b).



The Port 5 input buffers have a maximum propagation delay of 300 ns.
As a result Port 5 sample time begins 300 ns before state S5 and ends when S5 has finished.

Fig.30 Instruction cycle timing.

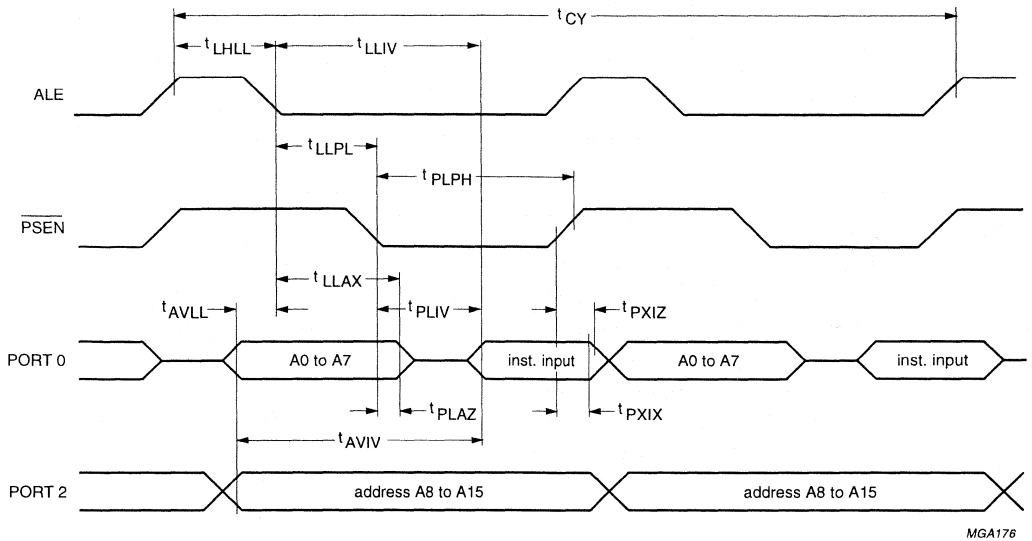


Fig.31 Read from external Program Memory.

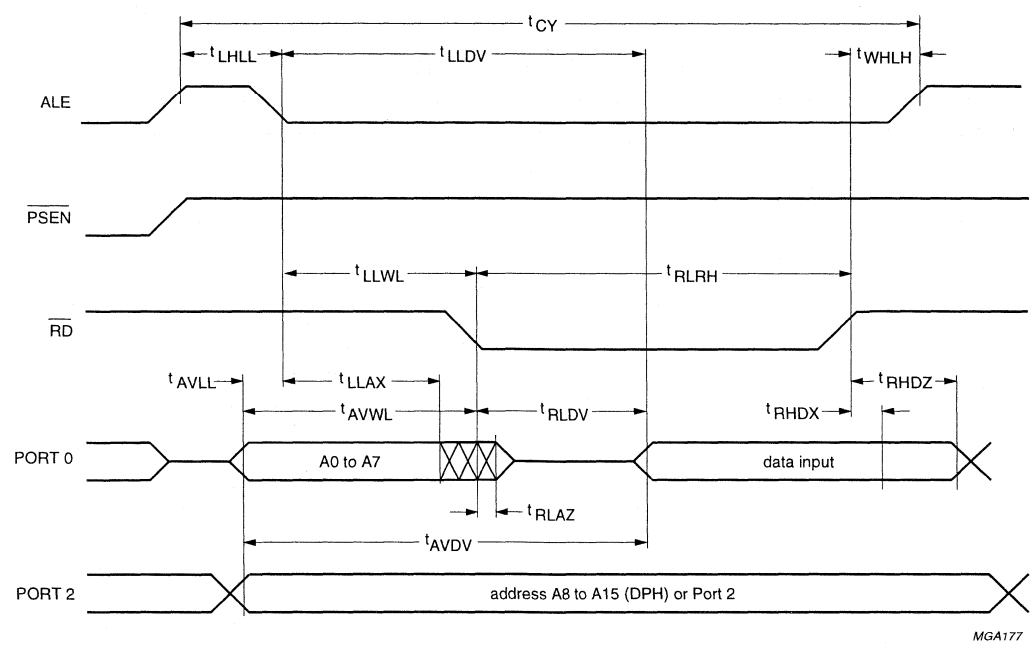


Fig.32 Read from external Data Memory.

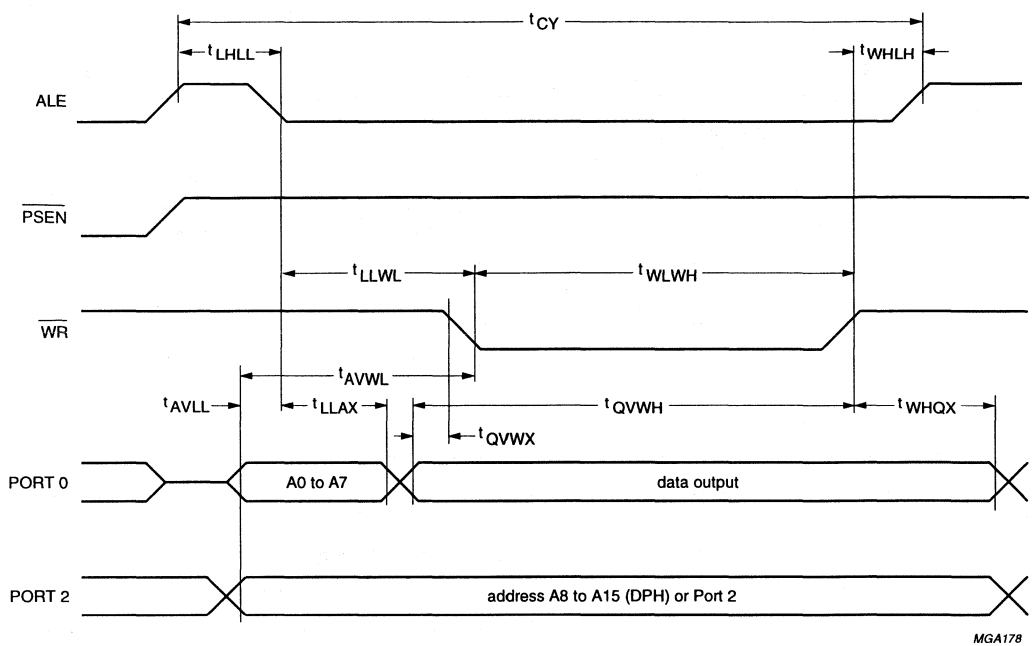


Fig.33 Write to external Data Memory.

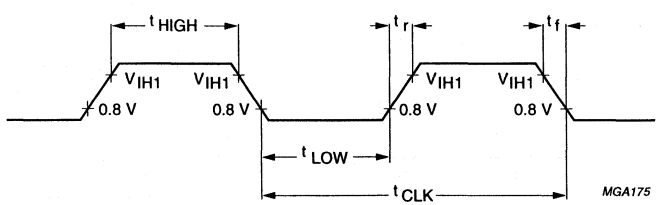


Fig.34 External clock drive XTAL1 (see Table 91).

Table 91 External clock drive XTAL1

SYMBOL	PARAMETER	VARIABLE CLOCK (f_{CLK} = 1.2/3.5 to 16 MHz)		UNIT
		MIN.	MAX.	
t_{CLK}	oscillator clock period			
	P83CE598	62.5	833.3	ns
	P87CE598	62.5	285.7	ns
t_{HIGH}	HIGH time	20	$t_{CLK} - t_{LOW}$	ns
t_{LOW}	LOW time	20	$t_{CLK} - t_{HIGH}$	ns
t_r	rise time	–	20	ns
t_f	fall time	–	20	ns
t_{CY}	cycle time ($12 \times t_{CLK}$)	0.75	10	µs

Table 92 UART Timing in Shift Register Mode

SYMBOL	PARAMETER	f_{CLK}						UNIT
		16 MHz		12 MHz		VARIABLE CLOCK		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{XLXL}	Serial Port clock cycle timing	0.75	–	1.0	–	12 t_{CLK}	–	ms
t_{QVXH}	output data setup to clock rising edge	492	–	700	–	10 t_{CLK} – 133	–	ns
t_{XHQX}	output data hold after clock rising edge	8.0	–	50	–	2 t_{CLK} – 117	–	ns
t_{XHDX}	input data hold after clock rising edge	0	–	0	–	0	–	ns
t_{XHDV}	clock rising edge to input data valid	–	492	–	700	–	10 t_{CLK} – 133	ns

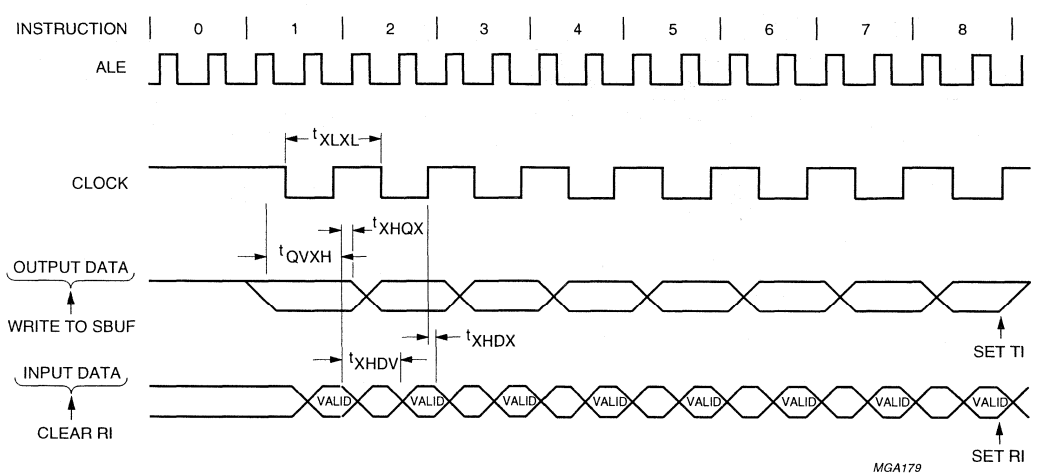


Fig.35 UART waveforms in Shift Register Mode.

22 EPROM CHARACTERISTICS

The P87CE598 has an on-chip 32 kbytes EPROM for fast and flexible controller software development.
Two versions are available:

- A ceramic QFP package with a window for UV-erasure, P87CE598 EFQ.
- A low-cost OTP-version in a plastic QFP package, which is not erasable, P87CE598 EFB.

22.1 Programming and Verification

The P87CE598 is programmed by using a modified Quick-Pulse Programming algorithm (Trademark algorithm of Intel Corporation).
In Table 95, the logic levels for reading the Signature bytes and for programming the Program Memory, the Encryption Table and the Lock bits are listed.

The circuit configuration and waveforms for programming are shown in the Figures 36 and 37. Fig.38 shows the circuit configuration for code data verification.
Note that programming and verification is done with an oscillator frequency of 4 to 6 MHz. The two Signature bytes identifying the device as an P87CE598 manufactured by Philips are located as shown in Table 93.

Table 93 Programming and Verification

ADDRESS	CONTENT	MEANING
30H	15H	Philips
31H	9EH	P87CE598

22.2 Security

For code protection the P87CE598 has an Encryption table and three Lock bits. After programming the Encryption table from addresses 00H to 3 FH, a verification sequence will present the data at Port 0 as a logical EXNOR of the program byte with one of the Encryption bytes. The Encryption table is not readable. The P87CE598 has 3 programmable lock bits which must be programmed according to Table to provide different levels of protection of the on-chip code and data. Erasing the EPROM also erases the encryption array and the program lock bits, returning the part to full functionality. The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.

Table 94 Protection Level Programming
P = programmed; U = unprogrammed.

PROTECTION LEVEL	PROGRAM LOCK BITS			PROTECTION DESCRIPTION
	LB1	LB2	LB3	
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external Program Memory are disabled from fetching code bytes from internal memory, EA is jumped and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as Protection Level 2 and also verify is disabled.
4	P	P	P	Same as Protection Level 3 and external execution is disabled. Internal data RAM is not accessible.

22.3 Erasure

A controlled erasure is done by exposing the EPROM window to an ultraviolet lamp of 12 $\mu W/cm^2$ for 20 to 39 minutes at a distance of about 2.5 cm. The integrated dose of the ultraviolet light (2537 Å) must be at least 15 Ws/cm^2. Erasure leaves the array in an all 'logic 1' state.

To avoid inadvertent erasure of the EPROM in sunlight or fluorescent lighting it is recommended to cover the window with an opaque label.

Table 95 EPROM programming modes

MODE	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.7	P2.6	P3.7	P3.6
Read Signature	HIGH	LOW	HIGH	HIGH	LOW	LOW	LOW	LOW
Program code data	HIGH	LOW	LOW (note 1)	V_{PP} (note 2)	HIGH	LOW	HIGH	HIGH
Verify code data	HIGH	LOW	HIGH	HIGH	LOW	LOW	HIGH	HIGH
Program Encryption table	HIGH	LOW	LOW (note 1)	V_{PP} (note 2)	HIGH	LOW	HIGH	LOW
Program Lock bit 1	HIGH	LOW	LOW (note 1)	V_{PP} (note 2)	HIGH	HIGH	HIGH	HIGH
Program Lock bit 2	HIGH	LOW	LOW (note 1)	V_{PP} (note 2)	HIGH	HIGH	LOW	LOW
Program Lock bit 3	HIGH	LOW	LOW (note 1)	V_{PP} (note 2)	LOW	HIGH	LOW	HIGH

Notes

1. Each programming pulse is:
   a) LOW for 100 ± 10 µs
   b) HIGH for at least 10 µs.
2. ALE/$\overline{PROG}$ receives 25 programming pulses while V_{PP} is held at 12.75 V ± 0.25 V.

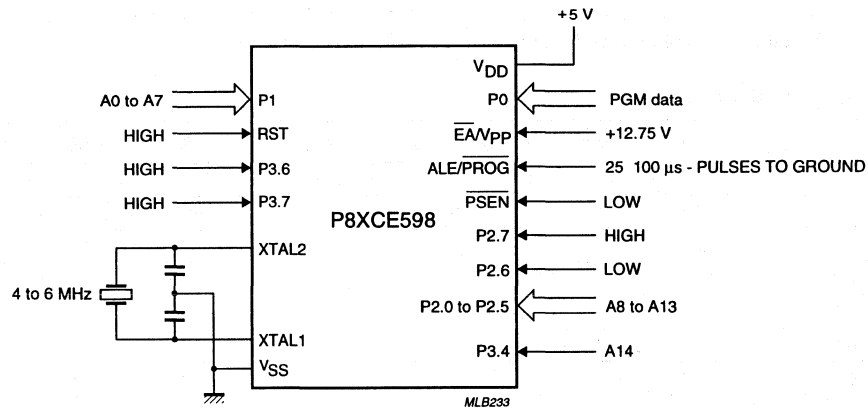


Fig.36 Programming configuration.

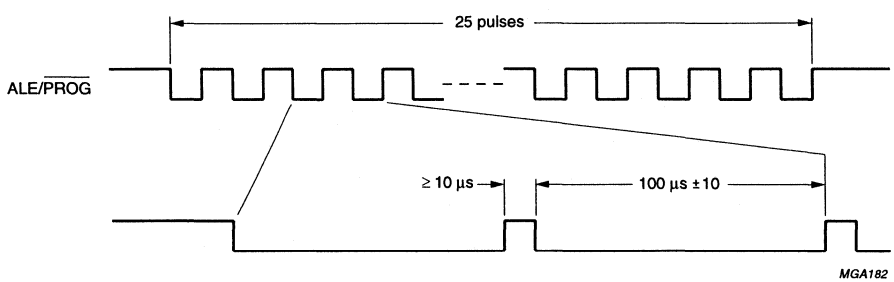


Fig.37 $\overline{\text{PROG}}$ waveform.

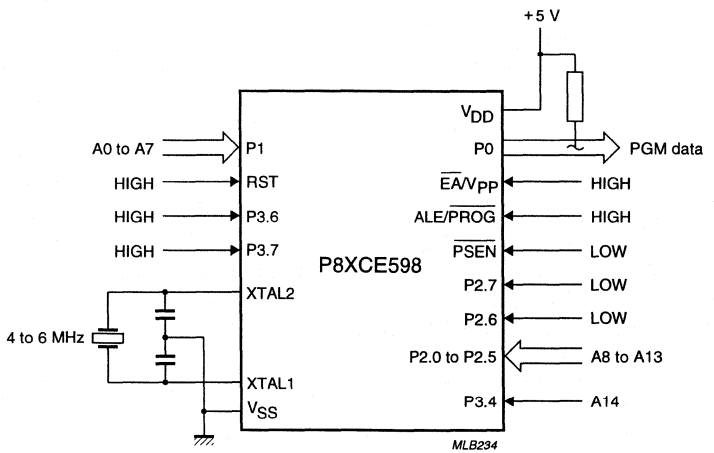
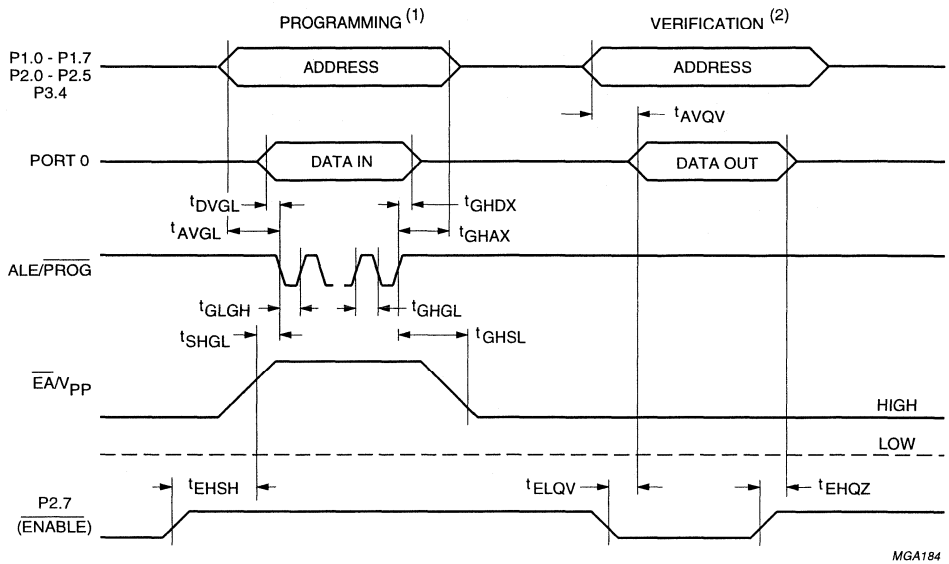


Fig.38 Program verification.

Table 96 EPROM programming and verification characteristics

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = 21 °C to 27 °C.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{PP}	programming supply voltage	12.5	13.0	V
I_{PP}	programming supply current	–	50	mA
f_{CLK}	oscillator frequency	4	6	MHz
t_{AVGL}	address set-up to $\overline{PROG}$ LOW	48 t_{CLK}	–	
t_{GHAX}	address hold after $\overline{PROG}$ HIGH	48 t_{CLK}	–	
t_{DVGL}	data set-up to $\overline{PROG}$ LOW	48 t_{CLK}	–	
t_{GHDX}	data hold after $\overline{PROG}$ HIGH	48 t_{CLK}	–	
t_{EHSH}	P2.7 ($\overline{ENABLE}$) HIGH to V_{pp}	48 t_{CLK}	–	
t_{SHGL}	V_{pp} set-up to $\overline{PROG}$ LOW	10	–	µs
t_{GHSL}	V_{pp} hold after $\overline{PROG}$ HIGH	10	–	µs
t_{GLGH}	$\overline{PROG}$ pulse width	90	110	µs
t_{AVQV}	address to data valid	–	48 t_{CLK}	
t_{ELQV}	P2.7 ($\overline{ENABLE}$) LOW to data valid	–	48 t_{CLK}	
t_{EHQZ}	data float after P2.7 ($\overline{ENABLE}$) HIGH	0	48 t_{CLK}	
t_{GHGL}	$\overline{PROG}$ HIGH to $\overline{PROG}$ LOW	10	–	µs



(1) For programming see Fig.36.
(2) For verification conditions see Fig.38.

Fig.39 EPROM Programming and Verification.

23 CAN APPLICATION INFORMATION

23.1 Latency time requirements

Real-time applications require the ability to process and transfer information in a limited and predetermined period of time. If knowing this total time and the time required to process the information, the (maximum allowed) transfer delay time is given.

It is measured from the initiation of the transfer up to the signalling of reception.
For instance, this is the period of time between programming the CAN Command Register bit 0 (Transmission Request) to HIGH and the time getting an interrupt at a receiving CAN-device (due to the reception of the respective message).

23.1.1 MAXIMUM ALLOWED BIT-TIME CALCULATION

The maximum allowed bit-time (t_{BIT}) due to latency time requirements can be calculated as:

$$t_{BIT} \leq \frac{t_{MAX\ TRANSFER\ TIME}}{(n_{BIT,\ MAX\ LATENCY} + n_{BIT,\ MESSAGE})} \quad (1)$$

Where:

- $t_{MAX\ TRANSFER\ TIME}$:
  the maximum allowed transfer delay time (application-specific).
- $n_{BIT,\ MAX\ LATENCY}$:
  the maximum latency time (in terms of number of bits), which depends on the actual state of the CAN network (e.g. another message already on the network).
- $n_{BIT,\ MESSAGE}$:
  the number of bits of a message; it varies with the number of transferred data bytes $n_{DATA\ BYTES}$ (0..8) and Stuffbits like:

$$44 + 8.n_{DATA\ BYTES} \leq n_{BIT,\ MESSAGE} \leq 52 + 10.n_{DATABYTES} \quad (2)$$

Example:

For the calculation of $n_{BIT,\ MAX\ LATENCY}$ the following is assumed (the term 'our message' refers to that one the latency time is calculated for):

- Since at maximum one-bit-time ago another CAN Controller is transmitting
- A single error occurs during the transmission of that message preceding ours, leading to the additional transfer of one Error Frame
- 'our message' has the highest priority,

giving:

$$n_{BIT,\ MAX\ LATENCY} \geq 44 + 8.n_{DATA\ BYTES,\ WORST\ CASE} + 18 \quad (3)$$

$$n_{BIT,\ MAX\ LATENCY} \leq 52 + 10.n_{DATA\ BYTES,\ WORST\ CASE} + 18 \quad (4)$$

Where:

- The additional 18 bits are due to the Error Frame and the Intermission Field preceding 'our message'.
- $n_{DATA\ BYTES,\ WORST\ CASE}$ denotes the number of data bytes contained by the longest message being used in a given CAN network.

23.1.2 CALCULATING THE MAXIMUM BIT-TIME

Table 97 Example for calculating the maximum bit-time

STATEMENT	COMMENTS
$t_{MAX\ TRANSFER\ TIME} = 10$ ms	assumption.
$n_{DATA\ BYTES,\ WORST\ CASE} = 6$	longest message in that network; assumption.
$n_{DATA\ BYTES} = 4$	'our message'; assumption.
$n_{BIT\ MAX\ LATENCY} \leq 130$	using Equations (3) and (4).
$n_{MESSAGE} \leq 92$	using Equation (2).
$t_{BIT} \leq \frac{10\ ms}{(130 + 92)} = 0.045\ ms = 45\ \mu s$	using Equation (1).

23.2 Connecting a P8XCE598 to a bus line (physical layer)

23.2.1 On-Chip Transceiver

The P8XCE598 features an on-chip differential transceiver including output driver and input comparator both being configurable (see Fig.41). Therefore it supports many types of common transmission media such as:

- Single wire bus line
- Two-wire bus line (differential)
- Optical cable bus line.

The P8XCE598 can directly drive a differential bus line. An example is given in Fig.42 for a bus line having a characteristic impedance of 120 Ω. Direct interfacing to the bus line is well suited for applications with limited requirements concerning electromagnetic susceptibility, wiring failure tolerance and protection against transients.

23.2.2 Transceiver for In-Vehicle Communication

Fig.43 shows a versatile transceiver implementation designed for automotive applications. It features a bit rate of up to 1 Mbit/s and dissipates low power during standby (1.4 mA). Thus it is suitable also for applications requiring a Sleep mode function with system activation via the bus line. The transceiver provides and extended common mode range for high electromagnetic susceptibility performance.

Two external driver transistors amplify the output current to 35 mA typically and provide protection against overvoltage conditions on the bus line (e.g. due to an accidental short-circuit between a bus wire and battery voltage). The serial diodes prevent in combination with the transistors the bus from being blocked in case of a bus not powered. More than 32 nodes may be connected to the bus line.

23.2.3 Detection and Handling of Bus Wiring Failures

Using the P8XCE598 a superior wiring failure tolerance and detection performance can be achieved. This requires both bus lines to be mutually decoupled as shown in Fig.44. Each bus wire is based separately to a reference voltage of $\frac{1}{2}AV_{DD}$.

The diodes suppress reverse current in case of a termination circuit being not properly powered or a bus line being short i.e. to a voltage higher than 5 V. Applying this bus termination circuit the following wiring failures on the bus are detectable and can be handled:

- Interruption of one bus wire at any location.
- Short-circuit of one bus wire to ground or battery voltage.
- Short-circuit between the bus wires.

A bus failure can be detected e.g. by a drop out of a status message, regularly being transmitted on the bus. If a bus wire is corrupted the following actions have to be taken:

- Switch the corresponding comparator input over to a reference voltage of $\frac{1}{2}AV_{DD}$.
- Disable the corresponding output driver stage.

As a consequence communication will continue on that bus wire not being corrupted. The required reference voltage and the switches for the comparator inputs are provided on-chip. An output driver stage can be disabled by reconfiguration of the on-chip output driver (reprogramming of the Output Control Register of the P8XCE598; see Section 13.5.11, Table 51). To find out which of the bus wires is corrupted a heuristic method is applied.

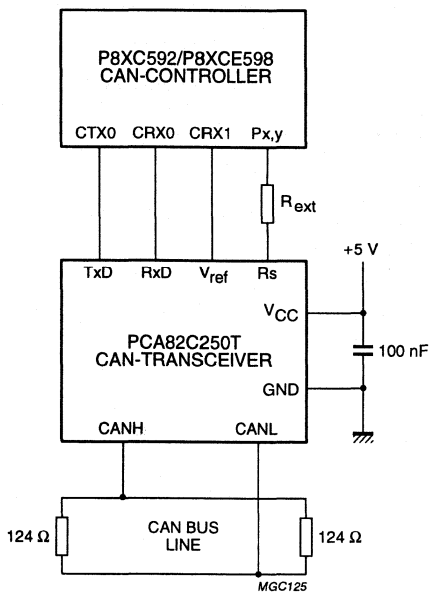


Fig.40 Application of a CAN-Transceiver (PCA82C250T).

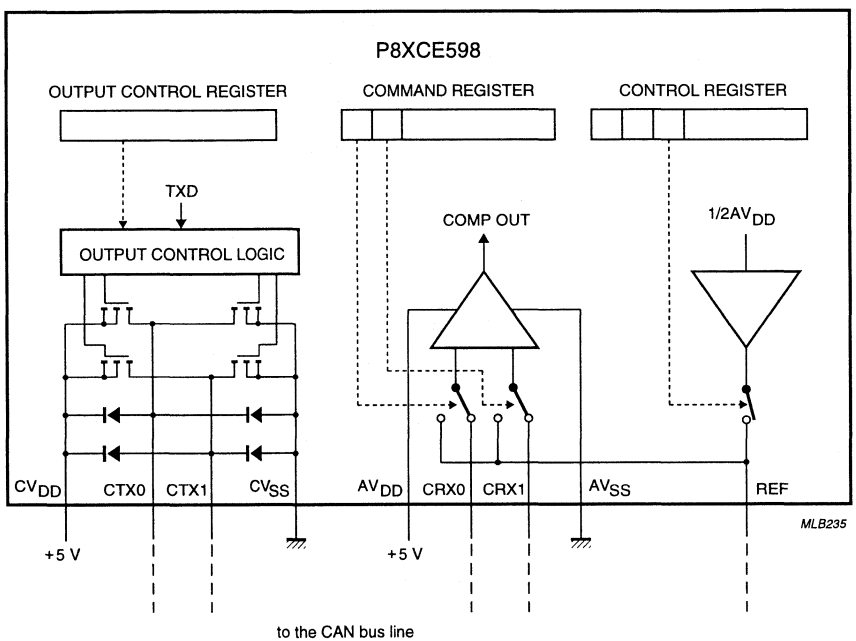


Fig.41 Structure of on-chip CAN-Transceiver.

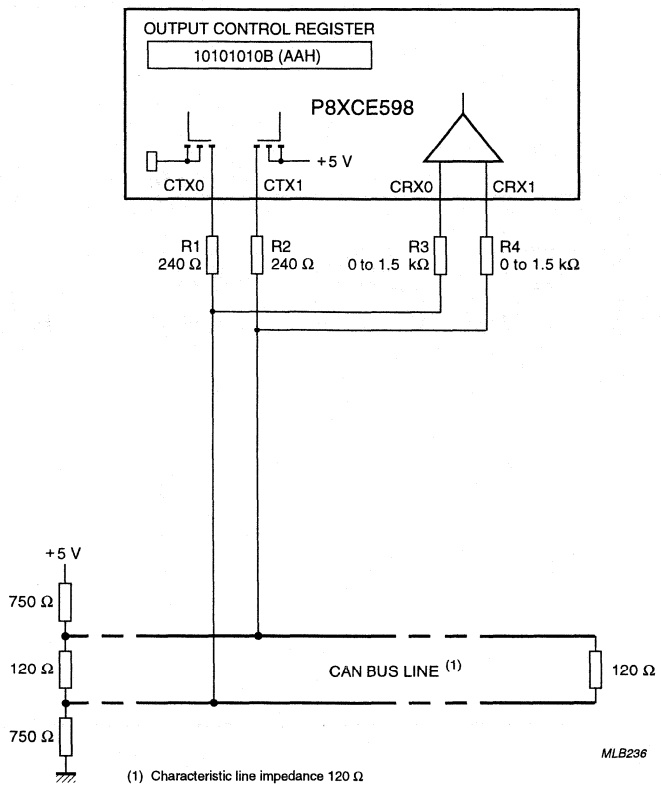


Fig.42 Direct interface to a two-wire differential bus.

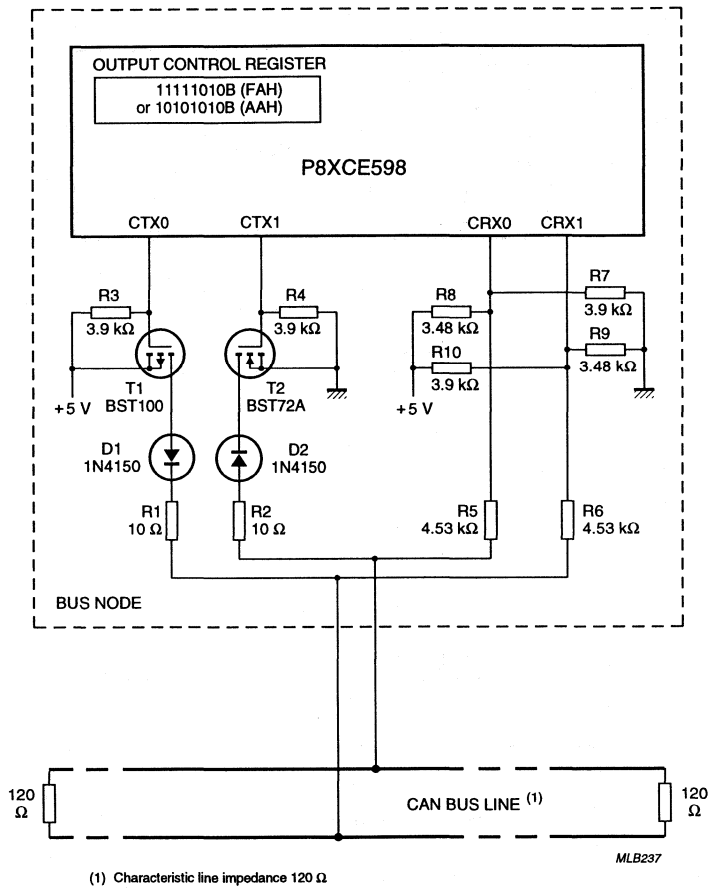


Fig.43 In-vehicle Transceiver.

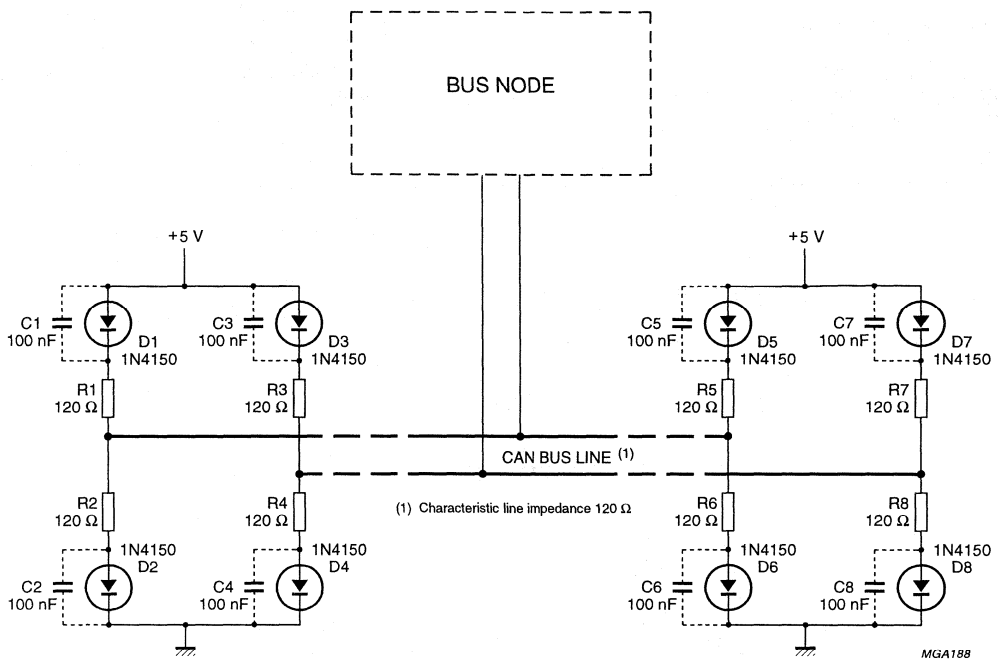


Fig.44 Bus termination with decoupled wires.

23.2.4 Connection to an Optical Bus Line

Using an optical medium provides the following advantages:

- Bus nodes are galvanically decoupled.
- Optical cable features very high noise immunity.
- No noise emission by the bus cable.

An example for an interface to an optical connector is given in Fig.45. In most cases a transistor is required to amplify the TX-output current.

Thus more optical power is provided to compensate for losses in the optical connectors and the optical star. The P8XCE598 features an on-chip $\frac{1}{2}AV_{DD}$ reference voltage output so only a capacitor is required for the receiver part. Two optical fibres are used to connect the bus nodes. The TX-fibre transfers the output signal of the CAN Controller to the optical star. The optical star transfers the TX-fibre input signal over to all the RX-fibres. The RX-fibres transfer the resulting optical signal over to the receivers of all the bus nodes.

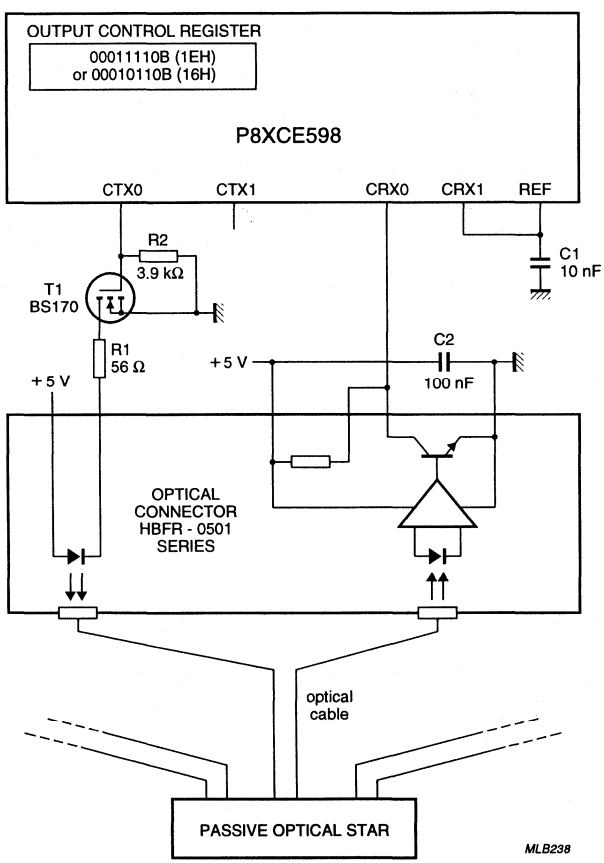


Fig.45 Optical Transceiver.

23.2.5 P8XCE598 CAN INTERRUPT HANDLER SOFTWARE EXAMPLE (INCLUDING FAST DMA TRANSFER)

MCS-51 MACRO ASSEMBLER CAN interrupt-handler

```
LOC  OBJ    LINE  SOURCE

             1    $TITLE 8XCE598 (CAN interrupt-handler)
00A0         2    $NOSYMBOLS NOPAGING
00A1         3
             4    ;*******************************************************************************************************
             5    ;
             6    ;Very fast receive-routine for the 8XCE598 CAN Interface. It:
             7    • is embedded in the interrupt-handler for the CAN Controller,
             8    • uses the DMA-logic and
             9    • handles up to eight different messages
00A2        10    ;(if these have the same leading 8 identifier-bits).
            11    ;
            12    ;To allow for faster receive-routine, it is assumed that all other routines
            13    ;accessing the CAN Controller, disable the interrupt of the CAN Controller
            14    ;(IEN0.5) during their execution.
00A5        15    ;
00A7        16    ;Version:    1.0
            17    ;Date:       12-April-90
            18    ;Author:     Bernhard Reckels
            19    ;at:         Philips Components Application Lab., Hamburg (PCALH)
00A9        20
00AB        21    ;*******************************************************************************************************
00AD        22
            23    ;*******************************************************************************************************
            24    ;initial stuff
            25    ;*******************************************************************************************************
            26
            27    ;equatas
            28
            29              ;addresses of Special Function Registers
00AE        30              CANADR      EQU     0DBH
00AF        31              CANDAT      EQU     0DAH
            32              CANCON      EQU     0D9H
00B0        33              CANSTA      EQU     0D8H
            34
```

```
LOC    OBJ      LINE  SOURCE
                   35          ;commands for the CAN Controller / DMA logic
                   36          CAN_REF_REL     EQU     00000100B       ;Release Receive Buffer
00A0               37          CAN_RX_DMA      EQU     80H + 22        ;Rx DMA-transfer
00A1               38
                   39          ; addresses of CAN Controller internal registers
                   40          CAN_REF         EQU     20              ;1st address of Rx-buffer
                   41
                   42          ; masks
                   43          INT_FLAG_MASK   EQU     00011111B       ;all CAN's interrupt-flags
                   44          ID2_0_MASK      EQU     11100000B       ;only ID.2 ... ID.0 bits
00A2               45      ; jump-address for a CAN Controller interrupt
                   46
                   47
                   48      CSEG at 2BH
         020080    49          LJMP            CAN_INT_HANDLER         ; CAN's interrupt-vector
00A5               50
00A7               51      ; data storage
                   52
                   53      DSEG at 20H
                   54          CAN_INT_IMAGE:  DS      1
00A9               55
00AB               56      BSEG at 00H
00AD               57          CAN_INT_RX:     DBIT    1               ; = CAN_INT_IMAGE.0
                   58          CAN_INT_TX:     DBIT    1               ; = CAN_INT_IMAGE.1
                   59          CAN_INT_KR:     DBIT    1               ; = CAN_INT_IMAGE.2
                   60          CAN_INT_OV:     DBIT    1               ; = CAN_INT_IMAGE.3
                   61          CAN_INT_WK:     DBIT    1               ; = CAN_INT_IMAGE.4
                   62
                   63      ;*******************************************************************************************************
                   64      ;CAN Controller interrupt-handler
00AE               65      ;
00AF               66      ;Only the receive-interrupt is coded.
                   67      ;
00B0               68      ;*******************************************************************************************************
                   69
                   70      CSEG at 080H
                   71
```

```
LOC  OBJ     LINE  SOURCE
00A0         72    CAN_INT_HANDLER:
00A1         73
             74            ; first save used registers
     C0D0    75            PUSH        PSW
     C0E0    76            PUSH        ACC
             77
             78            ; store the CAN Controller's Interrupt Register contents
             79            ; (here: at a bit-addressable location).
00A2         80            ; This is necessary because after reading the Interrupt Register
             81            ; its contents is cleared, but – on the other hand – several flags
             82            ; may be set in coincidence.
     E5D9    83            MOV         A, CANON
     541F    84            ANL         A, #INT_FLAG_MASK      ; only interrupt-flags
00A5 F520    85            MOV         CAN_INT_IMAGE, A
00A7         86
             87
             88    ;dispatcher----------------------------------------------------------------------------------------
             89    INT_TEST0:
00A9 100000  90            JBC     CAN_INT_RX,CAN_RX_SERV     ;receive-interrupt?
00AB         91
00AD         92    INT_TEST1:
             93            ; here the dispatcher has to be completed according
             94            ; to the application-specific requirements
             95            ; ...
             96            ; ...
             97    ; end of dispatcher--------------------------------------------------------------------------------
             98
             99    ;Rx-serve------------------------------------------------------------------------------------------
00AE         100   ; copy message (Data-Field only) from CAN- to CPU memory
00AF         101
             102   CAN_RX_SERVE
00B0         103           ; read 2nd Descriptor-Byte from the Rx-Buffer (address 21)
     75DB15  104           MOV         CANADR, #CAN_REF + 1
     E5DA    105           MOV         A, CANDAT
             106
```

```
LOC  OBJ     LINE  SOURCE
00A0         107   ; determine the destination address in data-memory for the
00A1         108   ; message's Data-Field
     54E0    109   ANL     A, #ID2_0_MASK      ; use ID.2 ... ID.0 only
     C4      110   SWAP    A
     03      111   RR      A                   ; A = 4*ID.2 + 2*ID.1 + ID.0
             112   ; this value is used as an index for an array of 8 bytes
             113   ; containing the destination-addresses for the 8 different
             114   ; messages. Note, that the #RX_ARRAY_OFFSET is due to the
00A2         115   ; program counter-relative access to the array.
     2415    116   ADD     A, #RX_ARRAY_START - RX_ARRAY_OFFSET
     83      117   MOVC    A, @A + PC
             118   RX_ARRAY_OFFSET:
             119
00A5         120   ; if a message passes the acceptance-filter of the CAN
00A7         121   ; Controller, but the CPU doesn't need it, the array
             122   ; entry's value may be set to zero indicating this.
             123   ; The following <jz> instruction cares for this.
     6007    124   JZ      CAN_RX_READY
00A9         125
00AB         126   ; now copy the Data-Field (only) from CAN- to CPU memory
00AD         127   ; with the aid of the DMA-logic. Note, that a TX-DMA is
             128   ; performed when writing 8AH (DMA + address 10) into CANADR
             129   ; and a RX-DMA is performed when writing 94H (DMA + address 20)
             130   ; ... 9DH (DMA + address 29) into CANADR. Here address 22 is
             131   ; used to copy just the Data-Field.
     F5D8    132   MOV     CANSTA, A           ; data-memory address
     75DB96  133   MOV     CANADR, #CAN_RX_DMA ; starts RX-DMA at address 22
             134
00AE         135   ; the DMA-transfer is done in at maximum 2 instruction cycles.
00AF         136   ; During the transfer, neither the data-memory (RAM) nor one
             137   ; of the SFRs CANADR, CANDAT, CANCON and
00B0         138   ; CANSTA may be accessed by the CPU.
             139   ; For simplicity, two NOPs are used here.
     00      140   NOP
     00      141   NOP
00A0         142
```

```
LOC   OBJ     LINE  SOURCE
00A1          143           ; after reading the Rx-Buffer it must be released back to
              144           ; the CAN Controller. In coincidence, the Clear Overrun bit
              145           ; (CANCON.3) may be set, regardless of an existing or
              146           ; non-existing data overrun.
              147   CAN_RX_READY:
      75D904  148           MOV         CANCON, #CAN_RBF_REL
              149
00A2          150           ; if no other interrupt-flag is set, the interrupt-handler
              151           ; for the CAN Controller can be left. Otherwise further
              152           ; services are required.
      E520    153           MOV         A, CAN_INT_IMAGE
      70E4    154           JNZ         INT_TEST1
00A5          155
00A7          156           ; no other service is required, so the interrupt-handler
              157           ; is left.
      D0E0    158           POP         ACC
      D0D0    159           POP         PSW
00A9  32      160           RETI
00AB          161   ; end of Rx-serve----------------------------------------------------------------------------------------
00AD          162
              163           ; here the array follows containing 8 destination-addresses
              164           ; for up to 8 different messages to be received. The values
              165           ; are fully application-specific (the values below show an
              166           ; example only).
              167   RX_ARRAY_START:
      E0      168           DB          0E0H    ; Rx-message #0
      00      169           DB          000H    ; this message is not used
00AE          170           ; ...
00AF  FA      171           DB          0FAH    ; RX-message #7, containing 6 data bytes
              172
00B0          173           END

REGISTER BANK(S) USED: 0

ASSEMBLY COMPLETE, NO ERRORS FOUND
```

24 EPROM/OTP DEVELOPMENT SUPPORT

For information on development tools:

- Contact your local Philips office for actual and detailed Development Support Tools offers from third-party vendors.
- See *"Data Handbook IC20", Development Support Tools"*.
- See Philips brochure *"Microcontrollers and Microprocessors for embedded control applications"* ordering code 9398 374 90011.

24.1 Evaluation

For evaluation and simulation (especially for the CAN interface) purposes the following tools are available.

24.1.1 Philips Semiconductors Evaluation Support Tools; P8XCE598 evaluation board

For evaluation of the P8XCE598 microcontrollers's CAN-bus interface, Philips Semiconductors offers the OM4240 board. It is a low-cost prototyping board providing powerful monitor functions for interactive development of programs for full access to the CAN-bus.

24.1.1.1 Targets

- Ready to use on-board demonstration application.
- Aid user in understanding CAN and P8XCE598.
- Support rapid proto-typing of specific applications.

24.1.1.2 Features

Major features of the OM4240 include:

- Evaluation of the P8XCE598 microcontroller's CAN interface.
- Full support of the CAN communication utilities:
  - Demonstration and monitor software for the CAN-bus system supports CAN communication of up to 1 Mbit/s
  - Interactive configuration of the CAN-controller
  - A plug-in CAN physical layer baby board with the 82C250 CAN transceiver IC for balanced bus wires
  - LED display.
- Interactive software development with up/down-loading of user-specific hex files, single/multi-step breakpoint setting and software trace functions.
- On-board monitor software (EPROM) and a PC DOS compatible cross-assembler on a diskette.
- On-board programming of a P87CE598.
- RS232C interface for connection to a PC.
- Wire-wrap area for prototyping, an application interface and two-wire CAN-bus connector.
- Supply voltage: 7.5 to 18 V.
- Dimensions: 200 × 160 mm.
- P87CE598 microcontroller:
  - 64 kbytes EPROM (32 kbytes on-chip, 32 kbytes external)
  - 2 × 256 bytes on-chip RAM; 32 kbytes external SRAM.
- Off-chip transceiver circuit designed to meet ISO/TC22/SC3/N608E (high-speed) with two selectable options:
  - Option 1: very low standby power consumption.
  - Option 2: support of single wire communication to recover from wiring failures.
- Power-down mode:
  - Small power consumption
  - Wake-Up via CAN-bus possible.

24.1.2 I+ME CAN Evaluation Design Tools

CAN Evaluation design tools offered by I+ME (Philips subcontractor):

- CAN/Net Sim
- CAN/Net Emu
- CAN/Net Ana.

Based on a PC System (Board + Monitor) a standard PC can be confirmed as a complete mode in CAN network.

For further information contact:

I+ME GmbH

Germany

Phone: +49-5331-72066

Fax: +49-5331-32455

CAN serial linked I/O device (SLIO) with digital and analog port functions

P82C150

CONTENTS

CAN serial linked I/O device (SLIO) with digital and analog port functions

P82C150

1 FEATURES

- Single-chip I/O device with CAN protocol controller
- Meets CAN protocol specification version 2.0 A and B (passive) with restricted bit timing
- Fully integrated clock oscillator (no crystal required)
- 16 configurable digital or analog I/O port pins
- Each of the port pins individually configurable via CAN-bus: port direction, port mode and event capture facilities for inputs (event driven or polling)
- Up to sixteen digital inputs; automatic transmission of a CAN message on a change on inputs individually selectable
- Up to sixteen 3-state outputs
- Up to two quasi-analog outputs with 10-bit accuracy
- 10-bit analog-to-digital converter with up to six multiplexed analog input channels
- Two general purpose comparators
- Bit rate from 20 kbit/s up to 125 kbit/s using internal oscillator
- Automatic bit rate detection and calibration
- Up to sixteen P82C150 nodes for one CAN-bus system
- Four identifier bits programmable
- SLIO functions controlled by a single intelligent node ('host')
- Sleep-mode with wake-up via CAN-bus
- Differential CAN-bus input comparator and CAN-bus output driver
- Supply voltage: 5 V ±4%
- Operating temperature: two ranges –40 to +85 °C and –40 to +125 °C.

2 GENERAL DESCRIPTION

The P82C150 is a single-chip 16-bit I/O device including a Controller Area Network (CAN) protocol controller with automatic bit rate detection and calibration. It features 16 configurable I/O port pins with programmable direction, digital and analog modes.

The P82C150 provides a configurable event capture facility supporting automatic transmission caused by a change on the port input pins.

The clock oscillator requires no external components, thus, the cost of the CAN link is reduced significantly.

The P82C150 is a very cost-effective way to increase the I/O capability of a microcontroller based CAN node as well as to reduce the amount and complexity of wiring. Advanced safety is provided by the CAN protocol.

Applications:

- Body electronics and instrumentation in automotive applications
- Sensor/actuator interface in automotive and general industrial applications
- Extension of I/O capabilities of microcontroller based CAN nodes.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE (°C)
	NAME	DESCRIPTION	VERSION	
P82C150 AFT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1	–40 to +85
P82C150 AHT				–40 to +125

4 BLOCK DIAGRAM

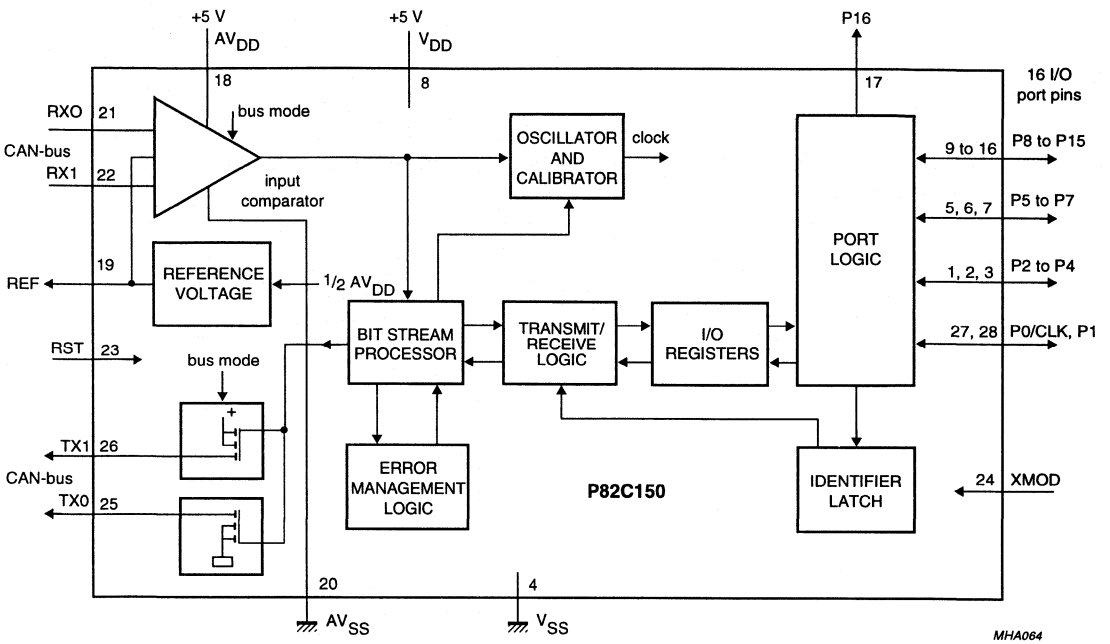


Fig.1 Block diagram.

5 FUNCTIONAL DIAGRAM

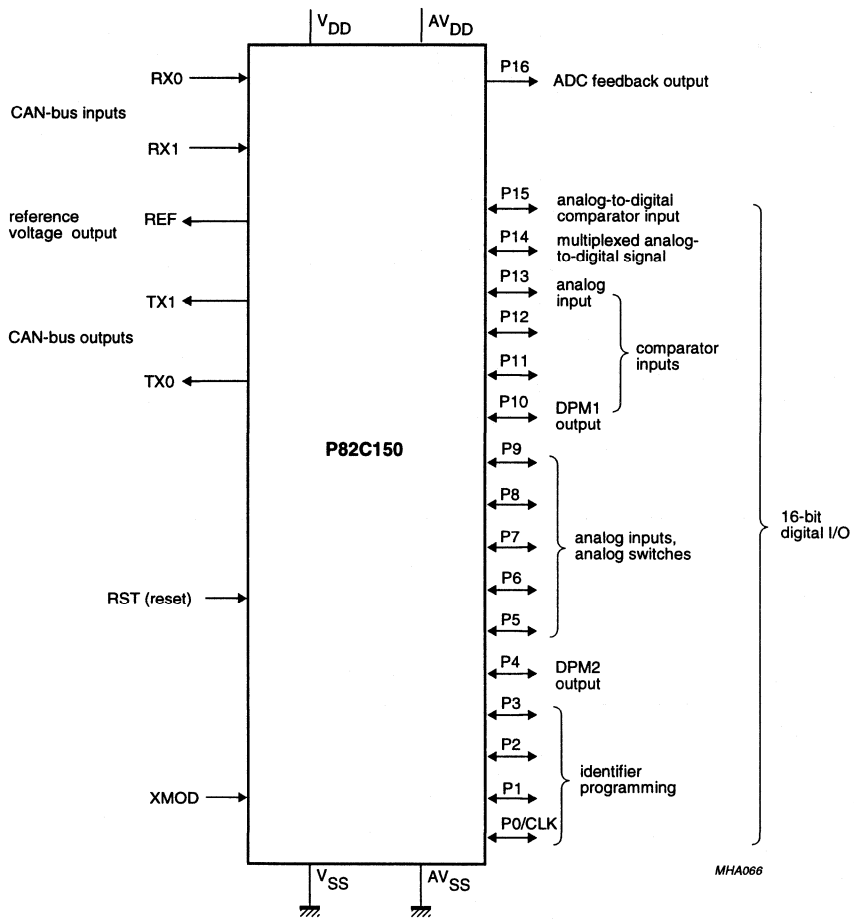


Fig.2 Functional diagram.

6 PINNING INFORMATION

6.1 Pinning

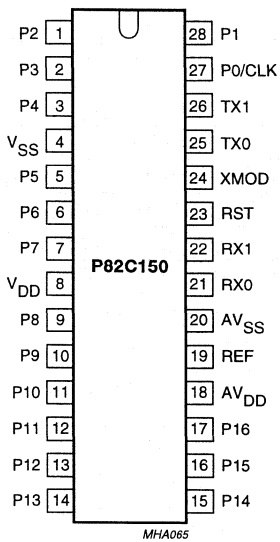


Fig.3 Pin configuration.

6.2 Pin description

Table 1 Pin description for P82C150; SO28; see note 1

SYMBOL	PIN	DESCRIPTION
P2	1	**I/O Ports P2 to P3;** Identifier programming input.
P3	2	
P4	3	**I/O Port 4;** DPM2 output.
V_{SS}	4	**Ground**, digital part (0V; logic circuits and CAN-bus driver).
P5	5	**I/O Ports P5 to P6;** analog input.
P6	6	
P7	7	**I/O Port 7;** analog input or analog-to-digital comparator 1 output.
V_{DD}	8	**Power supply,** digital part (+5 V; logic circuits and CAN-bus driver).
P8	9	**I/O Port 8;** analog input or comparator 3 output.
P9	10	**I/O Port 9;** analog input or comparator 2 output.
P10	11	**I/O Port 10;** comparator 3 inverting input or DPM1 output.
P11	12	**I/O Port 11;** comparator 3 non-inverting input.
P12	13	**I/O Port 12;** comparator 2 inverting input.
P13	14	**I/O Port 13;** comparator 2 non-inverting input.
P14	15	**I/O Port 14;** multiplexed analog signal.
P15	16	**I/O Port 15;** analog-to-digital comparator input.
P16	17	**Feedback output** of analog-to-digital converter.
AV_{DD}	18	**Power supply,** analog part (+5 V; CAN input, oscillator and reference).
REF	19	**Reference voltage output** ($\frac{1}{2} \times AV_{DD}$).
AV_{SS}	20	**Ground**, analog part (0 V; CAN input, oscillator, reference).
RX0	21	**CAN-bus input.**
RX1	22	
RST	23	**External reset input** (active-HIGH) for internal oscillator mode; pulled to +5 V for external oscillator mode (see Section 11.3).
XMOD	24	**Connected to GND for internal oscillator mode**; external reset input (active-LOW) for external oscillator mode (see Section 11.3).
TX0	25	**Open-drain CAN-bus output:** dominant = LOW; recessive = floating.
TX1	26	**Open-drain CAN-bus output:** dominant = HIGH; recessive or at bus mode 2 floating.
P0/CLK	27	**I/O Port P0**, Identifier programming input in internal oscillator mode; clock input in external oscillator mode (see Section 11.3).
P1	28	**I/O Port P1;** identifier programming input.

Note

1. In this documentation the port pins are referred to by their symbols, not by their pin number. For example P15 means I/O Port 15 at pin 16.

7 FUNCTIONAL DESCRIPTION

7.1 I/O functions

The P82C150 provides 16 port pins (P15 to P0) which are individually configurable via CAN-bus. Besides the digital I/O functions some of these port pins provide analog I/O functions.

7.1.1 DIGITAL INPUT FUNCTIONS

Input levels HIGH and LOW on the port pins (P15 to P0) can be read in two ways by the host node:

- **Polling:** a Remote Frame is sent to the P82C150 to be answered by a Data Frame containing the Data Input Register contents.
- **Event capture:** in case of edge-triggered mode, the P82C150 sends the same Data Frame caused by the event of a rising and/or falling edge on the corresponding port pins (see Table 3).

7.1.2 DIGITAL OUTPUT FUNCTIONS

The Data Output Register is set via a CAN message. Its content is only output when the corresponding bits of the Output Enable Register are set to logic 1s.

7.1.3 ANALOG INPUT/OUTPUT FUNCTIONS

- Up to six multiplexed analog input signals for analog-to-digital conversion or general purpose
- Up to two quasi-analog output channels (DPM; Distributed Pulse Modulation)
- Two input comparators, for example for window comparator applications
- A separate analog-to-digital input comparator with feedback output.

Analog-to-digital converted digital results are obtained by reading the Analog-to-Digital Conversion (ADC) Register. Analog functions of each port pin are individually controlled by the Analog Configuration Register.

Writing the I/O registers is done serially via CAN-bus by Data Frames. The first data byte contains the register address, and the second and third data bytes represent the register contents. If a read only register is addressed, the contents of the second and third data bytes are ignored.

It is recommended to set unused port pins to HIGH (100 kΩ resistor to V_{DD}).

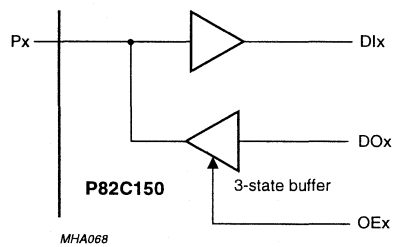


Fig.4 I/O port pins.

7.2 I/O registers

Table 2 I/O register map

15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
ADDRESS 0: DATA INPUT															
DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
ADDRESS 1: POSITIVE EDGE															
PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
ADDRESS 2: NEGATIVE EDGE															
NE15	NE14	NE13	NE12	NE11	NE10	NE9	NE8	NE7	NE6	NE5	NE4	NE3	NE2	NE1	NE0
ADDRESS 3: DATA OUTPUT															
DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
ADDRESS 4: OUTPUT ENABLE															
OE15	OE14	OE13	OE12	OE11	OE10	OE9	OE8	OE7	OE6	OE5	OE4	OE3	OE2	OE1	OE0
ADDRESS 5: ANALOG CONFIGURATION															
ADC	OC3	OC2	OC1	0	M3	M2	M1	SW3	SW2	SW1	0	0	0	0	0
ADDRESS 6: DPM1															
DP9	DP8	DP7	DP6	DP5	DP4	DP3	DP2	DP1	DP0	0	0	0	0	0	0
ADDRESS 7: DPM2															
DQ9	DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	0	0	0	0	0	0
ADDRESS 8: ANALOG-TO-DIGITAL CONVERSION (ADC)															
AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	0	0	0	0	0	0

7.2.1 Data Input Register (Address 0)

This read only register contains the states of port pins P15 to P0 which are transmitted on request, or automatically by change of one of the input levels, provided that the respective input is configured to event capture mode (see Table 3). When an edge is detected the port state is loaded into the transmit buffer after the Control Field of the triggered message is sent. Therefore a delay for input settling is provided. If between edge detection and transmission of the data input register another input signal change at the input port occurs, the corresponding data input register bit is overwritten by the current input port value. Additionally the register content is sent automatically after wake-up or bus mode change, once the bit time has been calibrated (part of the 'sign-on' message).

7.2.2 Positive Edge Register (Address 1)

This write only register contains configuration information per port pin for the event capture facility.
The corresponding PE-bit (see Table 3) has to be set to logic 1 to enable capturing of the rising edge.

7.2.3 Negative Edge Register (Address 2)

This write only register contains configuration information per port pin for the event capture facility.
The corresponding NE-bit (see Table 3) has to be set to logic 1 to enable capturing of the falling edge.

The combination of PE and NE functions is possible.

7.2.4 Data Output Register (Address 3)

This write only register contains the output data for the port pins. The output drivers are bitwise enabled by OE (see Section 7.2.5). New data for the output port register are processed and written to the output ports directly after the corresponding CAN message to the P82C150 is successfully checked and becomes valid.

7.2.5 Output Enable Register (Address 4)

This write only register controls the output drivers of the port pins. The corresponding Output Enable Register bit has to be set to logic 1 to enable an output driver. If set to logic 0, the corresponding output driver is disabled (floating; see Fig.7).

Table 3 Programming of the I/O registers to event capture on edge or to digital output
X = don' t care; n = 0 to 15.

FUNCTION	REGISTER CONTENTS OF PARTICULAR PORT PIN		
	POSITIVE EDGE (BITS PEn)	NEGATIVE EDGE (BITS NEn)	OUTPUT ENABLE (BITS OEn)
Digital output	X	X	1
Digital input			
Polling	X	X	X
Event capture on edge			
Rising	1	0	X
Falling	0	1	X
Rising and Falling	1	1	X

7.2.6 Analog Configuration Register (Address 5)

This read/write register contains the bits ADC, OC3 to OC1, M3 to M1 and SW3 to SW1 (see Fig.7).

- ADC bit (analog-to-digital conversion start bit; write only bit). The P82C150 starts an analog-to-digital conversion cycle at ADC = 1 ended with the transmission of a message containing the result. After that, the ADC bit is reset automatically.
- OC3 to OC1 bits (comparator output data; read only bits). The bits OC3 to OC1 represent the logical output level of the analog comparators at input port pins P10, P11, P12, P13 and P15. The P82C150 sends back the logical output value of these comparators after having received a Data Frame (see Section 7.3.3) addressing the Analog Configuration Register. The comparator outputs can be monitored at the output port pins P8, P9 and P7.
- M3 to M1 bits (multiplexer control bits; write only bits). The logical value of the comparators is monitored on port pins P8, P9 and P7 (see Fig.7) by setting M3 to M1 to logic 1, provided that these pins are configured as outputs (OE = 1). Additionally the register content is sent automatically when the corresponding port bits in the Positive Edge Register and/or Negative Edge Register and the corresponding bits in the Output Enable Register are set.
- SW3 to SW1 (analog switch control bits; write only bits). One of the analog switches S1 to S6 can be closed by setting the switch bits to the corresponding value (see Fig.7 and Table 4).

Table 4 Analog switch selection by SW3, SW2, SW1.

SW3	SW2	SW1	SWITCH STATE
0	0	0	no switch closed (S0); note 1
0	0	1	S1 closed
0	1	0	S2 closed
0	1	1	S3 closed
1	0	0	S4 closed
1	0	1	S5 closed
1	1	0	S6 closed
1	1	1	reserved

Note

1. Evidently if P14 is driven, it may not be connected to any other driven pin via the internal analog switches (avoid short-circuit!).

7.2.7 DPM1 Register (Address 6)

This write only register contains data for a quasi-analog output signal on port pin P10, which is generated by Distributed Pulse Modulation (DPM; see Fig.9). The Output Enable bit must be set for this functions (OE10 = 1). The DPM1 output signal is inverted by setting DO10 = 1. The number of output pulses during a DPM period is given by the DPM1 Register value. These pulses have $4 \times t_{CLK}$ length and are distributed over the DPM period. An analog voltage is provided after smoothing the output signal by an external RC combination.

7.2.8 DPM2 Register (Address 7)

This write only register contains data for a quasi-analog output signal on port pin P4. The function of the DPM2 corresponds to the definition of DPM1.

7.2.9 Analog-to-Digital Conversion (ADC) Register (Address 8)

This read only register contains the result of the analog-to-digital converted level of that I/O pin which was selected by the SW bits. The conversion is started by ADC-bit set to logic 1 (see Section 7.2.6), or by transmitting a Data Frame addressing the ADC Register.

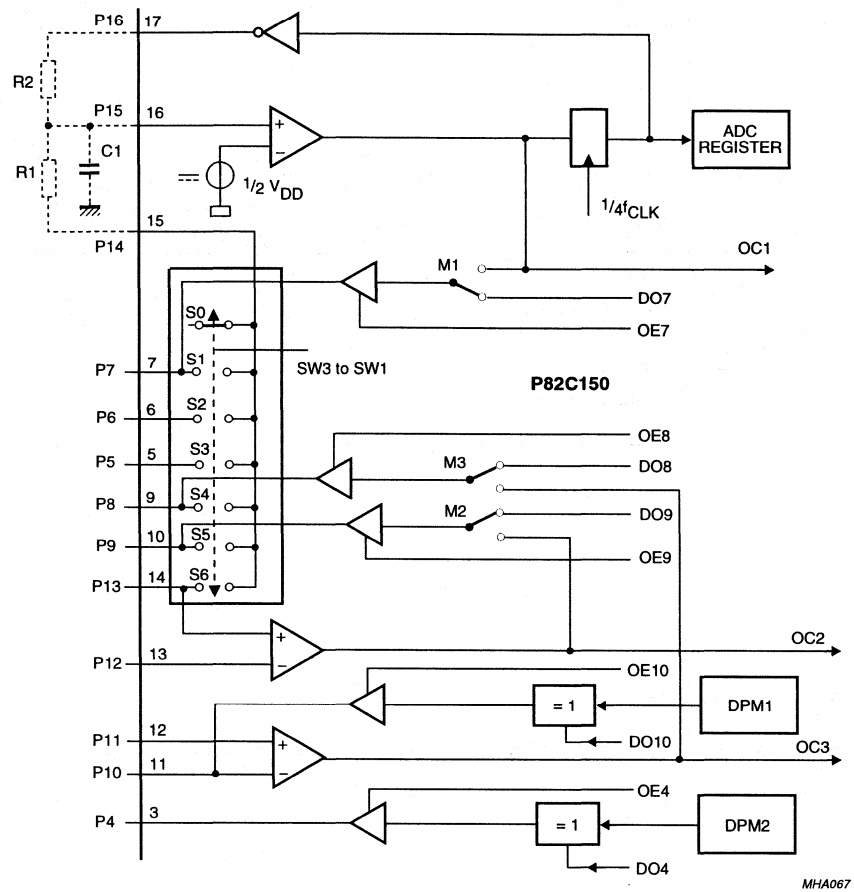
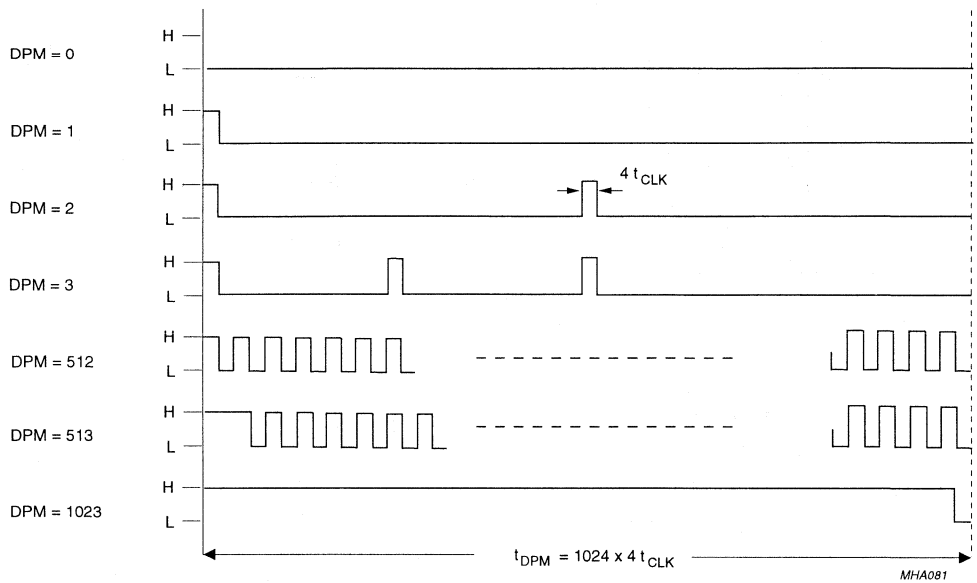


Fig.5 Analog configuration of I/O port pins; R1, R2 and C1 are used to implement the analog-to-digital converter.



Distributed Pulse Modulation (DPM) is a special pulse count modulation.

Fig.6 DPM output pulses at DO10(4) = 0; output pulses are inverted at DO10(4) = 1.

7.3 CAN functions

The P82C150 meets the CAN protocol specification version 2.0 A and B (passive) with restricted bit timing because of the on-chip RC-oscillator and the automatic bit rate detection.

In a system with P82C150 nodes there must be at least one conventional crystal-driven CAN controller (host node) which is compatible to the CAN specification V1.2 or later to control P82C150 nodes. Host nodes compatible to CAN specification V1.1 can also be used provided that the P82C150 nodes are powered by a high-accuracy power supply or they are in external oscillator mode (refer to Section 11.3).

Each time a P82C150 node receives a Data Frame, it initiates the transmission of a Data Frame containing four bits status information, the register address (previously received) and the current contents of the addressed register (exception: see Section 7.3.3.1). This enables the host node to verify that the addressed register has correctly been written in case of writeable registers, and to read the contents in case of readable registers.

7.3.1 CAN IDENTIFIER

Data and Remote Frames to be processed by the P82C150 are of Standard Format with 11 Identifier bits ID.10 to ID.0. Frames with extended Identifier (CAN specification version 2.0 B) are ignored.

The way of identifier programming is based on two facts:

- Each P82C150 operates with only two Identifiers distinguished by the LSB (see Tables 5, 6 and 7). The identifier with the higher priority is used for Data Frame reception. An extra Identifier is used for calibration purposes.
- There can be maximum sixteen P82C150 circuits in one network.

Table 5 Message types and format

FRAME	TRANSMISSION BY 82C150	RECEPTION AT 82C150
Data Frame	yes (DLC = 3; DIR = 1)	yes (DLC = 3; DIR = 0; calibration message with DLC = 2 to 8 allowed, see Section 7.3.10)
Remote Frame	no	yes (DLC = 3; DIR = 1)
Error Frame	yes	yes
Overload Frame	yes (only as a response)	yes

Note

1. DLC = Data Length Code; DIR = LSB of Identifier (see Section 7.3.1).

Table 6 Standard Format Identifier bits ID.10 to ID.0

1 = recessive; 0 = dominant

IDENTIFIER											
ID.10	ID.9	ID.8	ID.7	ID.6	ID.5	ID.4	ID.3	ID.2	ID.1	ID.0	
0	1	P3	1	0	P2	P1	P0	1	0	DIR	RTR

Table 7 Description of the Standard Format Identifier bits

BIT	SYMBOL	DESCRIPTION
ID.8	P3	Programmable identifier bits read from Port pins P3 to P0 during reset. The input levels on P3 to P0, for example set by resistors to V_{SS} or to V_{DD}, are latched in the Identifier latch with the falling edge of the RST input signal. They represent the variable part of the Identifier, while the remaining bits are fixed (mask-programmed), P3 to P0 can be used as I/O ports after reset.
ID.5 to ID.3	P2 to P0	
ID.0	DIR	DIR = 1 for transmission of Data Frames to the host. It must be set to a logic 1 in Remote Frames and to a logic 0 in Data Frames received from the host.
	RTR	Remote Transmission Request bit.

7.3.2 Transmission of Data Frames

Data Frames transmitted by the P82C150 contain three data bytes (see Fig.7). The first data byte contains the status information and the register address A3 to A0 (see Tables 8 and 9), the other two data bytes contain the content of the addressed I/O Register.

After each successful message transmission, the P82C150 delays the transmission of a possibly further pending message for three bit times. The reason is to give other CAN controllers - with a lower identifier priority - the possibility to transmit a message in case of faulty contact at one of the edge-triggered port pins.

7.3.3 Reception of Data Frames and Remote Frames

Received Data Frames have the same format as transmitted ones, only the DIR-bit (ID.0) in the Arbitration Field is different. The status bits RSTD, EW, BM1 and BM0 are ignored during reception.

The P82C150 confirms each reception of a Data Frame by transmitting a Data Frame containing the (new) contents of the addressed I/O Register.

7.3.3.1 Exceptions to the rule

1. Analog Configuration Register: If a P82C150 receives a Data Frame addressing the Analog Configuration Register and the ADC bit is set to logic 1, it will respond with two messages. The first message returns the contents of the Analog Configuration Register. The control instructions are executed (e.g. next analog input channel selected), and an analog-to-digital conversion cycle is started after a set-up time. After finishing the analog-to-digital conversion cycle, the second message is transmitted containing the result (ADC Register).
2. ADC Register: On receiving a Data Frame addressing the ADC Register, the P82C150 starts an analog-to-digital conversion cycle. It automatically returns the result of the conversion (ADC Register) by transmitting a respective Data Frame after finishing the analog-to-digital conversion cycle.
3. At normal operation, the calibration messages are confirmed by returning a dominant bit in the acknowledge slot. There is no particular confirmation message returned by the P82C150. Only after entering the calibrated state (start-up), a Data Frame ('sign-on' message) containing the Data Input Register contents is transmitted indicating to the host node, that the P82C150 is now ready for transmission.

7.3.3.2 Remote Frame

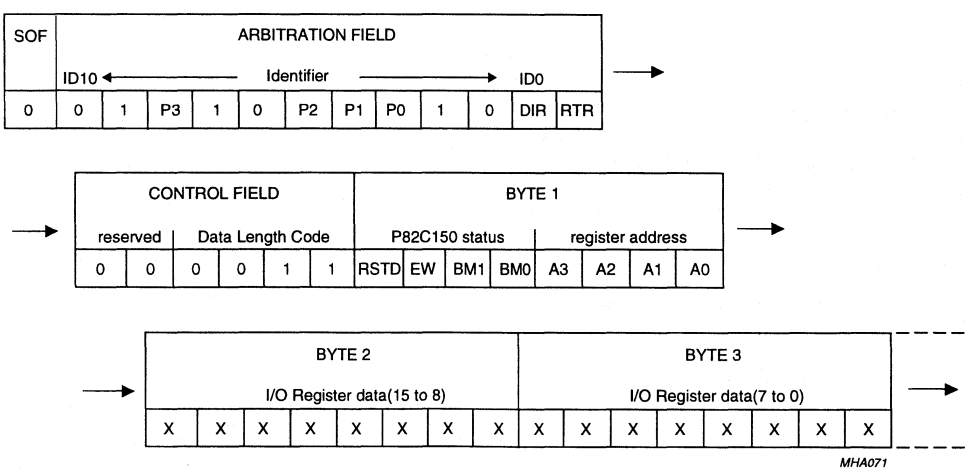
Received Remote Frames must have the Data Length Code DLC = 3 (Remote Frames with DLC $\neq$ 3 are ignored). It is answered by a Data Frame containing the contents of the Data Input Register.

Table 8 Data Frame Byte 1

STATUS				REGISTER ADDRESS			
RSTD	EW	BM1	BM0	A3	A2	A1	A0

Table 9 Description of Data Frame Byte 1 bits

SYMBOL	DESCRIPTION
Status	
RSTD	It is logic 1 in the first message ('sign-on' message) after the successful detection of the bit rate (bit time calibrated).
EW	Logic 1, if the error warning limit (32) is reached. In the "sign-on" message EW is always logic 1. The EW status bit is set when the Receive Error Counter or the Transmit Error Counter have exceeded the Error Warning Limit of 32, also temporarily, since the last successful transmission of a message.
BM1	Bus mode status bits.
BM0	
Register address	
A3 to A0	Register address bits.



SOF: Start Of Frame.
RTR: Remote Transmission Request.
P3 to P0: equals programmed identifier bits.

Fig.7 P82C150 Data Frame.

7.3.4 CAN-BUS MODES

The P82C150 can pass through four CAN-bus modes under certain conditions (see Fig.8). In the bus modes 0 to 2 (see Table 10) the P82C150 is operating with different input comparator configurations. Bus mode 3 is the power reduced Sleep Mode.

The bus modes support:

- Communication on two balanced wires (differential system)
- Communication on one wire in a two-wire differential system
- Sleep Mode with wake-up via either a dominant signal on RX0 or RX1 input
- Connection of a second transmission medium (redundancy)

There are two possibilities for condition 1 to switch to the next mode (see Fig.8):

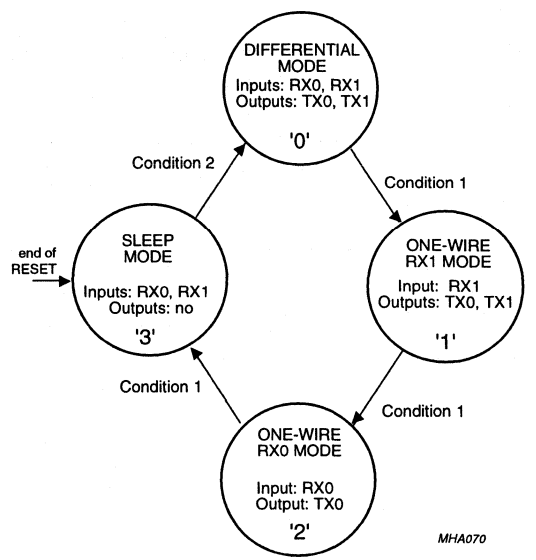
- Overflow of the bit counter when 8192 is reached since the last calibration message
- Overflow of the Transmit Error Counter (>255; bus-off limit reached).

When the bus mode changes, all I/O Registers are cleared and outputs become floating (OE bits cleared). That means the I/O ports return to a fail-safe state whenever the P82C150 looses connection to its host controller. This is a kind of network watchdog function. The status bits are set to the following values after a bus mode change:

- RSTD = 1
- EW = 0
- $BM_{new} = BM_{old} + 1$.

The programmed Identifier bits remain unchanged.

After reset the P82C150 changes directly into bus mode 3 (Sleep Mode). During Sleep Mode, the internal RC oscillator is stopped, and all the output drivers are disabled (I/O Register contents cleared). A P82C150 in Sleep Mode can be woken up via CAN-bus lines (dominant level on RX0 or RX1) or by a reset condition.



Condition 1:
bit counter overflow (>8191) or Transmit Error Counter overflow (>255).
Condition 2:
dominant bit detected on RX0 and RX1.

Fig.8 CAN-bus modes and switch-over conditions.

Table 10 Can-bus modes

BUS MODE	BITS		RECEPTION LEVEL		TRANSMISSION	
	BM1	BM0	RECESSIVE	DOMINANT	TX1	TX0
0 = Differential	0	0	RX0 > RX1	RX0 < RX1	enabled	enabled
1 = One-wire RX1	0	1	RX1 < REF	RX1 > REF	enabled	enabled
2 = One-wire RX0	1	0	RX0 > REF	RX0 < REF	disabled	enabled
3 = Sleep	1	1	RX0 > REF and RX1 < REF	RX0 < REF or RX1 > REF	disabled	disabled

Note

1. Output TX1 is disabled in bus mode 2 to tolerate short-circuit between the CAN-bus wires CAN_H and CAN_L.

7.3.5 Bit Timing

The Nominal Bit Time of the P82C150 is subdivided into 10 Time Quanta. The Synchronization Time Segment (SYNC_SEG) and the Propagation Time Segment (PROP_SEG) are each one Time Quantum long. The Phase Buffer Segment 1 (PHASE_SEG1) and the Phase Buffer Segment 2 (PHASE_SEG2) are each four Time Quanta long. The Resynchronization Jump Width (SJW) is four Time Quanta long.

The sample point is located at the end of the Phase Buffer Segment 1. The Nominal Bit Time is internally adjusted to that bit timing which is provided by the crystal driven host (calibration message).

The usable bus length at a given bit rate is reduced in comparison to other CAN controllers with programmable bit timing because the Propagation Time Segment is fixed to $1/10$ length of the Nominal Bit Time. The bit segmentation of the crystal driven host should be programmed like the fixed bit segmentation of the P82C150, e.g. one bit time segment is $1/10$ length of the Nominal Bit Time (refer also to Table 15 for bit time programming).

Table 11 Bit time subdivision

1 BIT TIME									
BT1	**BT2**	**BT3**	**BT4**	**BT5**	**BT6**	**BT7**	**BT8**	**BT9**	**BT10**
SYNC_SEG	PROP_SEG	PHASE_SEG1				PHASE_SEG2			

7.3.6 CAN-Bus Transceiver

The transceiver of the P82C150 consists of the configurable input comparator and of complementary open-drain driver outputs. The reference voltage REF is an additional output.

7.3.6.1 CAN-bus input comparator (RX0, RX1)

The input comparator monitors the transient voltage on RX1 and RX0.

The result of the input comparator is logic 1 if the voltage levels of the CAN-bus lines are regarded as recessive, and logic 0 if they are regarded as dominant.

The recessive state and the dominant state are not equivalent and may not be mixed-up.

The input comparator is configurable depending on the four CAN-bus modes (see Table 10), supporting battery-powered applications (Sleep Mode) and tolerance against bus wiring failures.

7.3.6.2 CAN-bus output drivers (TX0, TX1)

The output driver function is shown in Table 12. The output driver TX1 is disabled in bus mode 2 to tolerate a short-circuit between the CAN-bus lines in a two-wire differential CAN physical layer.

Table 12 CAN-bus driver output function

CAN OUTPUT	RECESSIVE	DOMINANT		RESET STATE, BUS-OFF AND SLEEP MODE (MODE 3)
		MODES 0 AND 1	MODE 2	
TX0	floating	LOW	LOW	floating
TX1	floating	HIGH	floating	floating

7.3.7 Transmit and receive logic

The transmit and receive logic stores the destuffed bit stream which was received or is about to be transmitted. The incoming Identifier is compared with that of the P82C150. The content of the message is transferred to the port logic in case of matching.

At transmission, the message about to be sent is put together: the Identifier, the status information, the register address and the content of the addressed register from the port logic.

7.3.8 Bit Stream Processor and Error Management Logic

The Bit Stream Processor (BSP) is a sequencer to control the data stream between the transmit/receive logic (parallel data) and the on-chip CAN transceiver (serial data). Reception/transmission, bit stuffing/destuffing, arbitration and error detection, according to CAN protocol specification version 2.0 A and B (passive), are performed. Further, automatic re-transmission of corrupted messages is handled by means of continuously comparing the output bit stream with the input bit stream. Moreover, the Bit Stream Processor provides control information to calibrate the internal bit time.

The Error Management Logic is responsible for the complete CAN-inherent error management.

7.3.9 Oscillator and calibration

The P82C150 contains an on-chip RC-oscillator. The bit time is automatically calibrated by messages being received via CAN-bus. During start-up (after wake-up or reset) any message is used to calibrate the bit time until the calibration is sufficient to receive messages correctly.

From this time on, the bit time is calibrated and fine-tuned by calibration messages with a special Identifier transmitted by the crystal-controlled host.

Only P82C150 nodes being calibrated by calibration messages can transmit messages. The first message is transmitted directly after entering the calibrated state ('sign-on' message). Since the P82C150 is not able to transmit as long as the bit time is not calibrated, it cannot wake-up other CAN nodes via the bus line. Hence to keep the network alive, the calibration message must be transmitted regularly by a crystal-controlled (host) node with a maximum repetition period of 8192 bit (bit length measured by the 82C150). It is recommended to select a repetition period between 3800 and maximum 8000 bit times.

7.3.10 Calibration message

The calibration message has to meet the following requirements

- Transmitted by a crystal-controlled node (host node)
- Identifier: 000 1010 1010 (1 = recessive; 0 = dominant)
- RTR bit: 0
- Allowed control field: DLC = 2 to 8
- The first recessive to dominant transition after the control field must be followed by another recessive to dominant transition in a distance of exactly 32 bit (stuff bits included).

Example of a suitable calibration message (there are others using different data bytes; see Table 13):

- Data length code: 0010
- 1st data byte: 1010 1010 (AAH)
- 2nd data byte: 0000 0100 (04H).

Table 13 Example of a suitable calibration message

The two important 1/0 transitions are marked by underlines; see note 1.

SOF	ARBITRATION FIELD	CONTROL FIELD	DATA BYTE 1	DATA BYTE 2	CRC FIELD
0	000 1010 1010 0	000I010	1010 1010	0000I 0100	000I0 1011 1000 00I0

Note

1. **I = stuff bit** (recessive); the total length is 67 bit from start-of-frame to end-of-intermission.

7.4 Initialization

7.4.1 IDENTIFIER PROGRAMMING

Most of the P82C150 identifier bits are fixed. Four bits are programmable via port pins P3 to P0. All output drivers are disabled at reset, also P3 to P0. Thus the outputs are floating unless the input level is defined by external components to define identifier bits. They are latched at the end of reset, and P3 to P0 can be used as port pins. It is not allowed, according to the CAN protocol specification, that multiple bus nodes transmit the same identifier bit combination. Therefore a P82C150 must have one of the 16 possible identifier bit combinations, one that is not yet occupied.

7.4.2 RESET FUNCTION

RST = HIGH disables all output drivers P16 to P0, TX0 and TX1. All I/O Registers are automatically cleared and set to logic 0. The bit time is set greater than 50 µs.

If a particular clock period is necessary, e.g. for a dedicated DPM output frequency, this can be achieved by feeding an external clock signal into P0. RST and TEST must be permanently HIGH for this special mode. A reset is then performed as usual (RST = HIGH; TEST = LOW).

Table 14 Situation after RESET

STATUS BITS	IDENTIFIER BITS
RSTD = 1	ID.8 equals P3
EW = 1	ID.5 equals P2
BM1 = 0	ID.4 equals P1
BM0 = 0	ID.3 equals P0

7.4.3 BIT TIME CALIBRATION

The P82C150 must receive at least three messages to calibrate its bit time after reset or change of bus mode. The first message is used to detect the bit time length (rough calibration) between two consecutive falling edges at the output of the CAN input comparator. Therefore the bit stream should contain a sequence of '1010'.

After rough calibration the P82C150 can receive any valid CAN message correctly and executes respective commands without giving an acknowledge. With another valid CAN message and additionally with one valid calibration message the P82C150 is fully calibrated and sends its 'sign-on' message. As long as the P82C150 is fully calibrated the P82C150 acts as an active CAN node.

The P82C150 treats any CAN message (including the calibration message) as a valid message, when these messages are terminated by an error passive frame because of a missing acknowledge. This situation may occur whenever a host node works together with P82C150's and the host node doesn't receive an acknowledge as long as the P82C150's are not fully calibrated.

7.4.3.1 Sign-on message

This special Data Frame is transmitted once by the P82C150 after entering the calibrated state. It indicates to the host node that the P82C150 is ready for transmission.

The sign-on message returns the contents of the Data Input Register, and can be recognized by the host mode by checking the RSTD status bit:

- Sign-on message RSTD = 1
- Other Data Frames RSTD = 0

Note that in the sign-on message the EW bit is logic 1. Nevertheless the P82C150 status with the error counters are set to logic 0.

7.5 P82C150 operation after RESET or change of bus mode

Figure 9 illustrates the calibration procedure of the P82C150 after Power-on-reset or after a bus mode change.

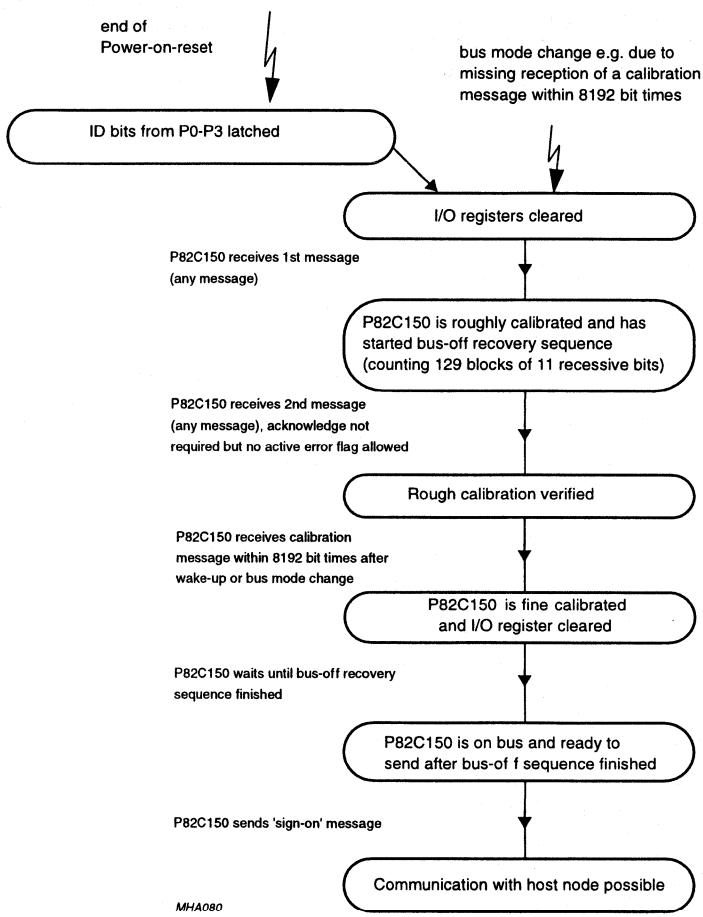


Fig.9 SLIO operation flow after reset and bus mode change.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage on V_{DD} pin	−0.5	+6.5	V
V_I	DC input voltage on any pin (RX0, RX1, TX0, TX1 excluded)	−0.5	V_{DD} + 0.5	V
I_I	RX1 and RX0 input current	–	±2	mA
I_{REF}	reference output current	–	±2	mA
I_O	port output current at port enabled (pins P0 to P15)	–	±5	mA
	port output current at analog switch enabled (OE-bits = 0; pins P5 to P9, P13, P14)	–	7.5	mA
	TX0 and TX1 output current	–	30	mA
P_{Otot}	total power dissipation (port outputs together)	–	200	mW
T_{amb}	operating ambient temperature range:	−40	+125	°C
T_{stg}	storage temperature range	−65	+150	°C
P_{tot}	total power dissipation	–	1	W

9 DC CHARACTERISTICS

V_{DD} = 5 V ± 4%; V_{SS} = 0 V; T_{amb} = −40 to +85 °C and T_{amb} = −40 to +125 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DD}	supply voltage	note 1	4.8	5.2	V
I_{DD}	operating supply current	$V_{RST} = V_{DD}$; all port inputs connected via 1 MΩ to GND	–	22	mA
$I_{DD(SM)}$	supply current Sleep mode	Ports P15, P13 and P11 connected to V_{DD}; Ports P12 and P10 connected to V_{SS}; all other port inputs connected via 1 MΩ to GND		1	mA
CAN Input comparators RX0 and RX1					
V_{DIF}	differential input voltage	$0.3AV_{DD} < V_I < 0.7AV_{DD}$; note 2	±100	–	mV
V_{HYST}	input voltage hysteresis		8	60	mV
I_I	input current	$0.45\ V < V_I < V_{DD} - 0.45\ V$	–	±400	nA
CAN output driver TX0 and TX1; port pins P0 to P16 unloaded					
V_{OLT}	TX0 output voltage LOW; note 3	I_{OLT} = 1.5 mA	–	0.1	V
		I_{OLT} = 10 mA		1.0	V
V_{OHT}	TX1 output voltage HIGH; note 4	I_{OHT} = −1.5 mA	$V_{DD} - 0.1$	–	V
		I_{OHT} = −10 mA	$V_{DD} - 1.0$		V
Reference voltage REF					
V_{REF}	reference output voltage	I_O < ±75 µA	$0.5AV_{DD} - 0.25$	$0.5AV_{DD} + 0.25$	V
Control inputs RST, XMOD and digital port inputs P0/CLK, P1 to P15					
V_{IL}	input voltage LOW		–	$0.2V_{DD}$	V
V_{IH}	input voltage HIGH		$0.7V_{DD}$	–	V
V_{HYST}	input voltage hysteresis	note 2	0.5	–	V
I_{IL1}	input leakage current	$0.45\ V < V_I < V_{DD} - 0.45\ V$		±10	µA
Digital port outputs P0/CLK, P1 to P16; OE bits set					
V_{OL}	output voltage LOW	I_{OL} = 4mA (sink)	–	1.0	V
V_{OH}	output voltage HIGH	I_{OH} = −4mA (source)	$V_{DD} - 1.0$	–	V
OC2 comparator P12, P13 and OC3 comparator P10, P11					
V_{DIF1}	differential input voltage	$1.5\ V < V_I < (AV_{DD} - 1.5\ V)$; note 2	±20	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
OC1 comparator input P15					
$V_{i\ sw}$	input switch-over voltage	1.5 V < V_I < (AV_{DD} – 1.5 V); note 2			
	lower threshold		$0.5V_{DD}$ – 0.02		V
	upper threshold		–	$0.5V_{DD}$ + 0.02	V
I_{LI2}	input leakage current	0.45 V < V_I < V_{DD} – 0.45 V	–	±400	nA
C_{IA}	analog input capacitance	note 2	–	20	pF
Analog switches; ION = ±4 mA					
R_{ON}	On resistance	between P5 to P9, P13 and P14; note 2	20	200	Ω

Notes to the DC characteristics:

1. Alteration of V_{DD} between two calibration messages should not exceed 0.2 V to avoid failures during CAN message transfer. If CAN devices according to CAN specification V1.0 or V1.1 (like the 82C200 V0 or V1) are in the same network with the 82C150, then this alteration of V_{DD} should be limited to 0.1V for the 82C150.
2. These values are characterized but not 100% production tested.
3. The TX0 output pin is an open drain pull-down driver (no pull-up driver included).
4. The TX1 output pin is an open drain pull-up driver (no pull-down driver included).

10 AC CHARACTERISTICS

V_{DD} = 5 V ± 4%; V_{SS} = 0 V; C_L = 100 pF (output pins); T_{amb} = –40 to +85 °C and T_{amb} = –40 to +125 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{CLK_INT}	system clock frequency on-chip	internal oscillator	4	10	MHz
t_{bit}	bit time on CAN-bus	note 1	8	50	µs
t_{RST1}	min. RST pulse width after power on	note 2	150	–	ms
t_{RST2}	min. RST pulse width during operation	note 2	1	–	µs
t_{hold}	ID hold time after end of reset	note 2	–	100	ns
t_d	total signal delay of CAN input comparator and CAN output driver	$0.3AV_{DD}$ < V_I < $0.7AV_{DD}$; note 2	–	100	ns
t_{rep}	max. time without recalibration message		–	8000	bit
Analog-to-digital comparator input P15					
t_{cyc}	analog-to-digital conversion cycle time		0.4	1.1	ms
t_{init}	initialization time of analog-to-digital conversion		0.4	2.1	ms
OC2 comparator P12, P13 and OC3 comparator P10, P11					
t_{resp}	response time	V_{DIF1} = ±100 mV; note 2		1	µs
DPM1 and DPM2 outputs					
t_{DPM}	repetition time of DPM cycle		0.4	1.1	ms

Notes

1. Other bit time values are possible with the external oscillator mode (refer to Chapter 11.3).
2. These values are characterized but not 100% production tested.

11 APPLICATION INFORMATION

11.1 Maximum bus length

The bit timing parameters refer to using a P8XCE598 or P8XC592 microcontroller with on-chip CAN interface as a host node (see Fig.20).

11.1.1 ASSUMPTIONS

- The total in/out delay of external transceiver circuit is less than 180 ns (e.g. PCA82C250 CAN transceiver; see Fig.20).
- The propagation delay on the transmission medium is 5.0 ns/m.

Table 15 Maximum bus length for CAN-bus systems with P82C150 nodes.

BIT RATE (kbit/s)	t_{prop}(1) (µs)	INDICATION FOR MAXIMUM BUS LENGTH (m)	BIT TIMING (P8XCE598/P8XC592)		
			f_{CLK} (MHz)	BTR0(2)	BTR1(2)
125	0.8	25	15	C5H	34H
100	1	45	16	C7H	34H
50	2	145	16	CEH	34H
20	5	445	16	E7H	34H

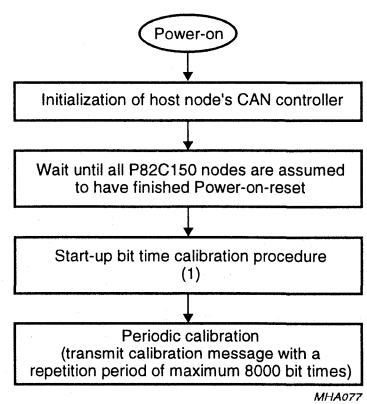
Notes

1. t_{prop} is the maximum propagation delay between two CAN-bus nodes (delays of on- and off-chip transceiver circuits included).
2. BTR0 and BTR1 (hex values) are particular configuration registers referring to bit timing.

11.2 Start up sequence

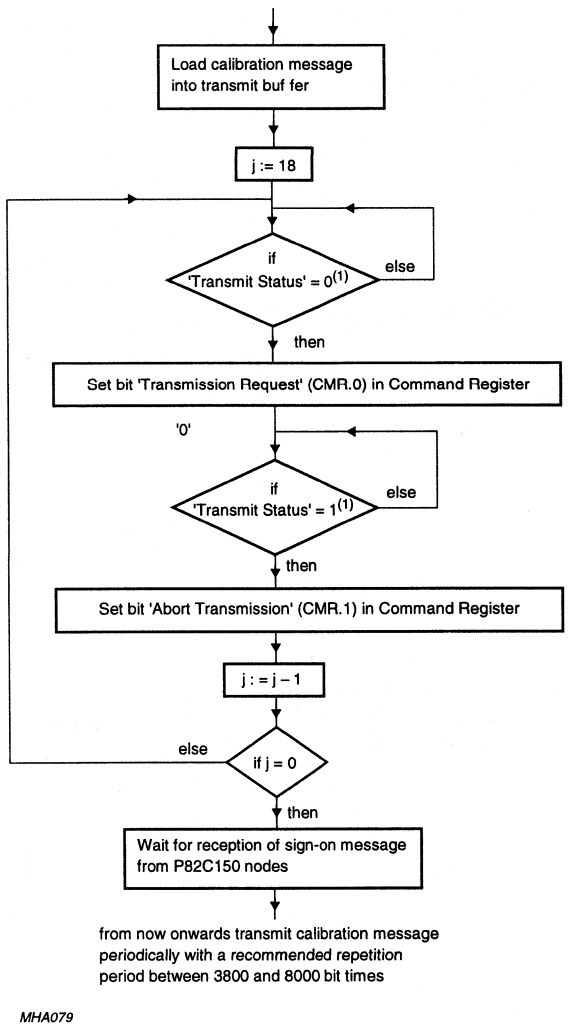
The following start-up sequence, illustrated by Figures 10 and 11, shows a simple example how P82C150 nodes can be controlled from a host node. This application example works with different system configurations:

- One conventional crystal-controlled CAN node and one or more P82C150 nodes.
- More than one conventional crystal-controlled CAN node and one or more P82C150 nodes.



(1) See Fig.11.

Fig.10 General start-up procedure for CAN-bus systems with P82C150 nodes.



(1) Bit SR.5 in Status Register.

Fig.11 P82C150 start-up bit time calibration procedure for host node **(P8XC592, P8XCE598 or P82C200)**.

11.3 External oscillator mode

In this mode the P82C150 operates with an external clock instead with the on-chip RC-oscillator. Figure 14 shows the application with an external clock.

In this mode the P82C150 can achieve bit rates below 20 kbit/s and above 125 kbit/s. The DPM pulse width is $4 \times t_{CLK}$ of the external clock. The corresponding CAN identifier bit at Port P0 is set to a logic 0. Therefore only eight P82C150 based CAN nodes operate within the same network in external oscillator mode.

11.3.1 NOTE

The external oscillator mode is not the normal operation mode.

11.4 Using digital I/O port functions

Figures 12 and 13, show the principle application for digital input and output.

11.5 Using DPM

The simplest way to generate an analog voltage using the P82C150 is to apply an external low pass filter at one of the DPM (Distributed Pulse Modulation) outputs. The simplest implementation concept is a RC-filter of the first order (refer to Fig.15). Regarding the selection of the time constant (edge frequency) of this filter, a trade-off between minimizing of the ripple voltage for maximum accuracy and minimum of the settling time has to be considered.

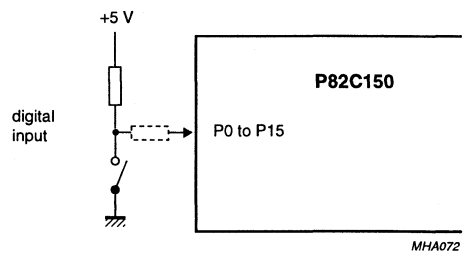


Fig.12 Example for digital input application.

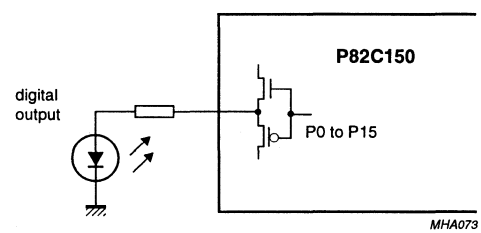


Fig.13 Example for digital output application.

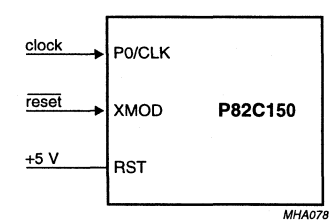
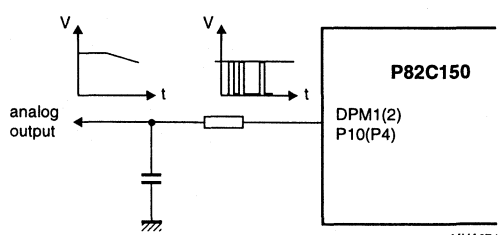


Fig.14 P82C150 in external oscillator mode.



If the output is loaded by a resistive load, this will decrease the accuracy due to the voltage drop across the series resistor. In these cases a low value for the series resistor should be chosen.

The repetition time of one DPM cycle can be derived from:

$$t_{CYC} = \frac{4096}{f_{OSC}}$$

Fig.15 Example for DPM application.

11.6 Using ADC

The application in Fig.16 can be used for analog-to-digital conversion for only one analog input signal. The evaluation of ADC were done with the values R1 = R2 = 100 kΩ and C = 3.3 nF; under these conditions the ADC may reach an accuracy of 7 to 8 bit (depends on application). The external components should be connected close to the port pins P15 and P16 with short wiring to avoid disturbances at the analog input port pin P15.

Using the on-chip multiplex function the P82C150 provides up to six input port pins to convert analog input signals to digital values (see Fig.17).

The period for one ADC cycle is identical to the length of one DPM cycle.

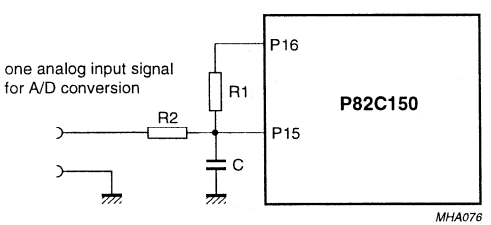


Fig.16 ADC implementation.

11.7 Using analog input port functions

Figure 18 shows the wide range of analog input applications:

- Comparison of two analog input signals.
- Comparison of one analog input signal against a fixed threshold.
- Window comparator including monitoring the comparator outputs at the port pins P8 and P9; additional automatically generated messages, when the corresponding port bits in the Negative Edge and/or Positive Edge register are set.
- Local control two-step system.

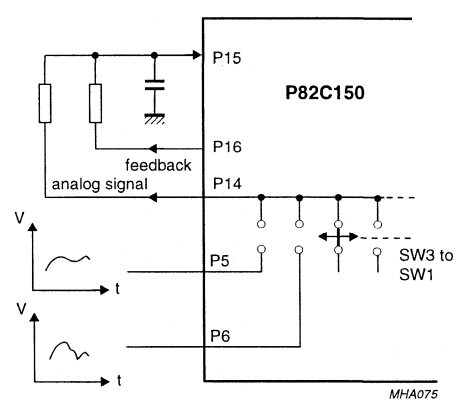


Fig.17 Two multiplexed analog input signals switched for analog-to-digital conversion (maximum 6 signals; see Fig.5).

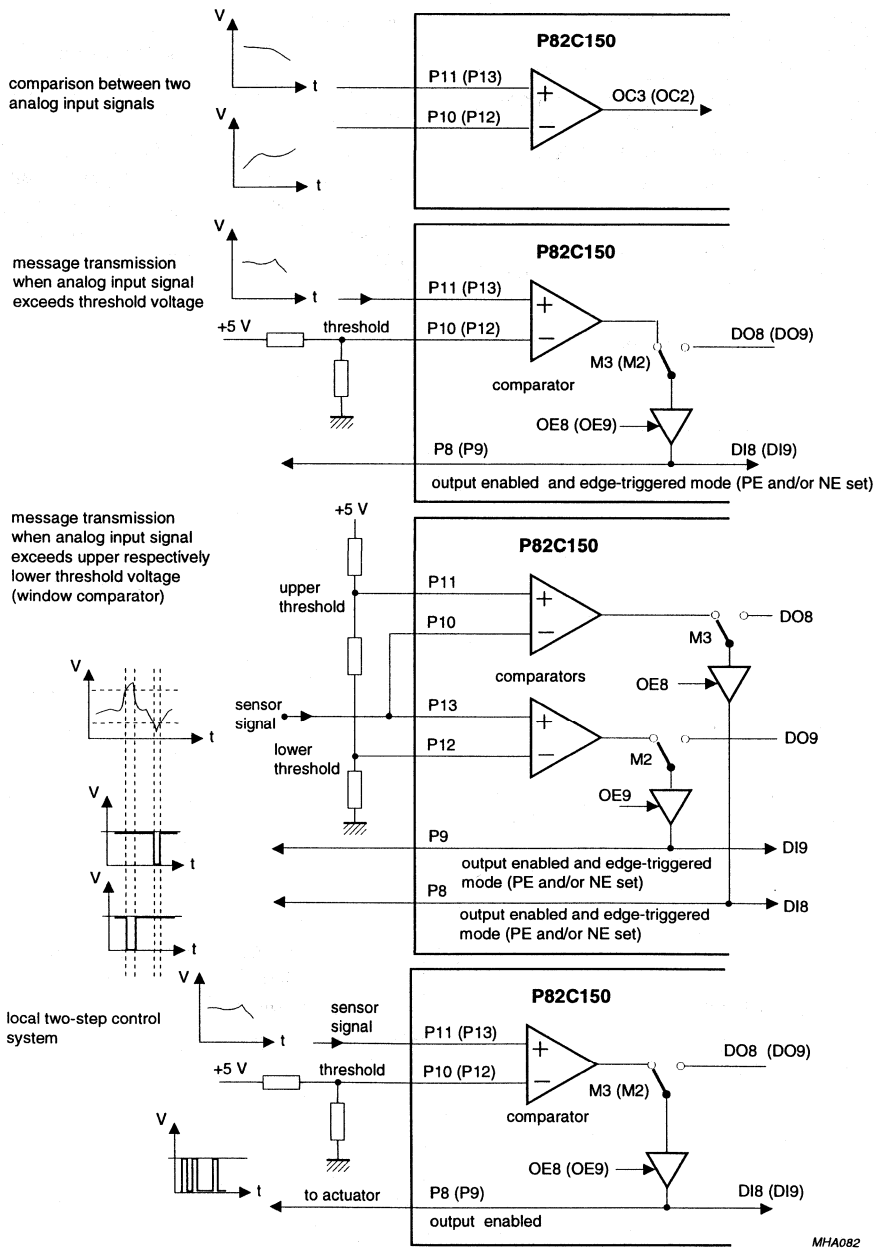


Fig.18 Examples of comparator applications.

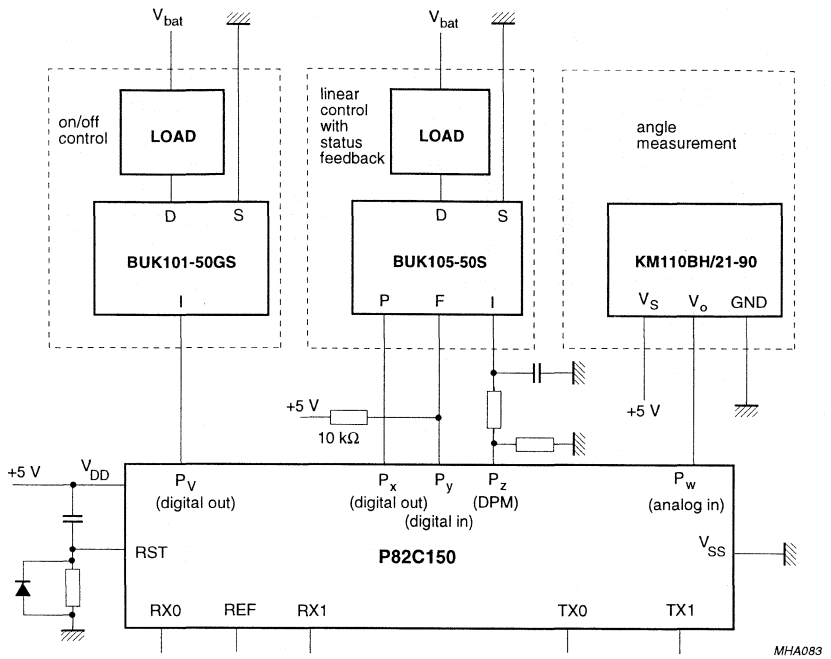
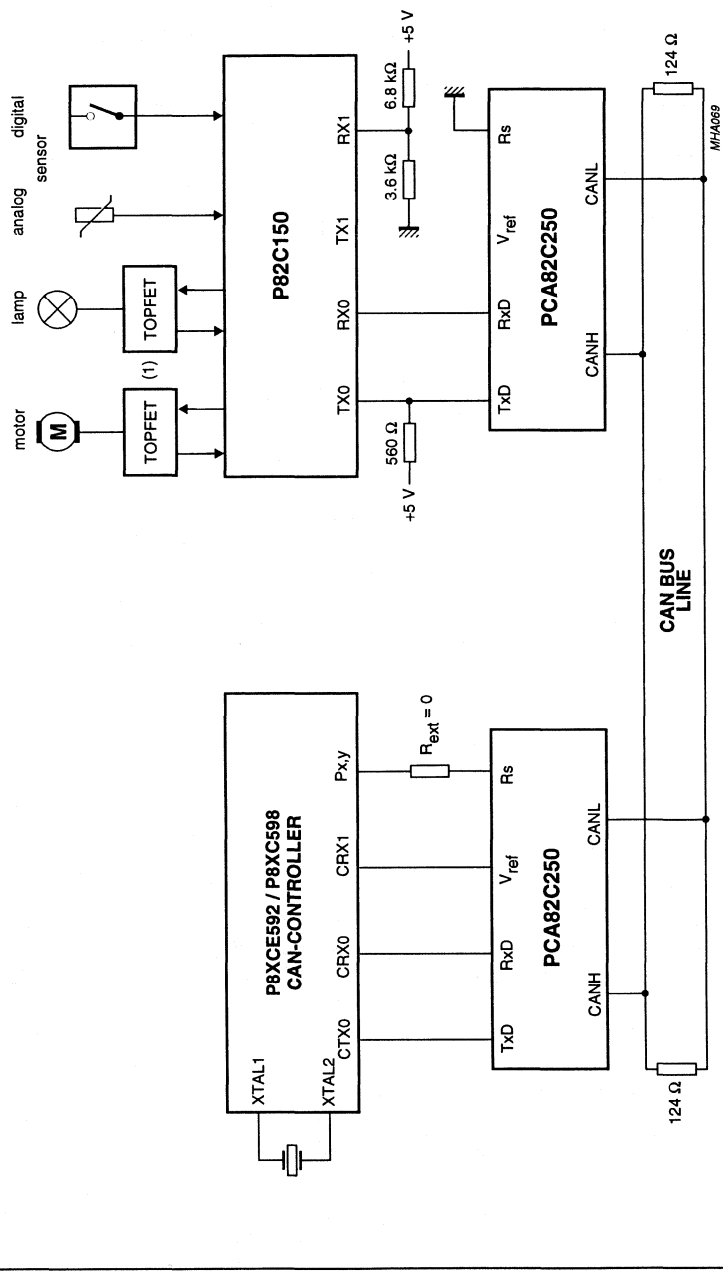


Fig.19 Examples of TOPFET applications with P82C150.

11.8 CAN-bus system applications



(1) TOPFET = temperature and Overload-Protected Field-Effect-Transistor

Fig.20 P82C150 system application using CAN transceiver PCA82C250 (ISO/DIS 11898 standard).

P82C150 Serial linked I/O (SLIO) device

Application report AN94088

Abstract

A Serial Linked I/O device (SLIO) like the P82C150 is a port device directly interfacing to the CAN-bus. It can be used as an extension of digital and analog port functions for a remote microcontroller. The CAN-bus is used as the serial link between the microcontroller and the port extension. The 82C150 provides several digital I/O-ports, two comparators, two D/A-converters using the 'Distributed Pulse Modulation' and one A/D-converter. The port functions are programmable by the host via the serial link.

This application note gives information on the implementation of a SLIO in a CAN network and discusses different topics of interest for ease of use of the device.

APPLICATION NOTE

P82C150 Serial Linked I/O (SLIO) Device

AN94088

Author(s):

Egon Jöhnk, Heinrich Waterholter
Product Concept & Application Laboratory Hamburg, Germany

Keywords

Automotive, Industrial
Serial Linked I/O, SLIO
CAN
P82C150
ADC
DPM
calibration

Date: 20th December, 1994

P82C150 Serial linked I/O (SLIO) device

Application report AN94088

Summary

This report is intended to provide application support for designing SLIO nodes based on the P82C150 in a CAN network.

The report describes a typical application of the P82C150 with respect to interfacing to the CAN-bus. It informs about resetting and initializing the P82C150, giving some examples of reset circuits and the programming of the variable bits of the identifier. The aspect of calibration and communication in a CAN network with SLIOs are discussed. Information on the bit timing and the possible bus length are given.The structure of the I/O ports are shown and typical applications are given for the digital and analogue functions available in the P82C150.

P82C150 Serial linked I/O (SLIO) device

Application report AN94088

CONTENTS

P82C150 Serial linked I/O (SLIO) device

Application report AN94088

1. INTRODUCTION

A *S*erial *L*inked *I/O* device (SLIO), like the P82C150 from Philips Semiconductors, allows the design of low-cost I/O nodes in a CAN-bus system. The P82C150 includes a controller area network (CAN) protocol controller on-chip.

Fig. 1 shows the principal configuration of CAN nodes (Module 1) and different configurations with microcontrollers as "module controller", CAN-bus controllers (integrated on the microcontroller or as separate IC) and CAN-bus transceivers for the physical interface. A SLIO node contains a CAN bus controller with I/O facilities and a transceiver.

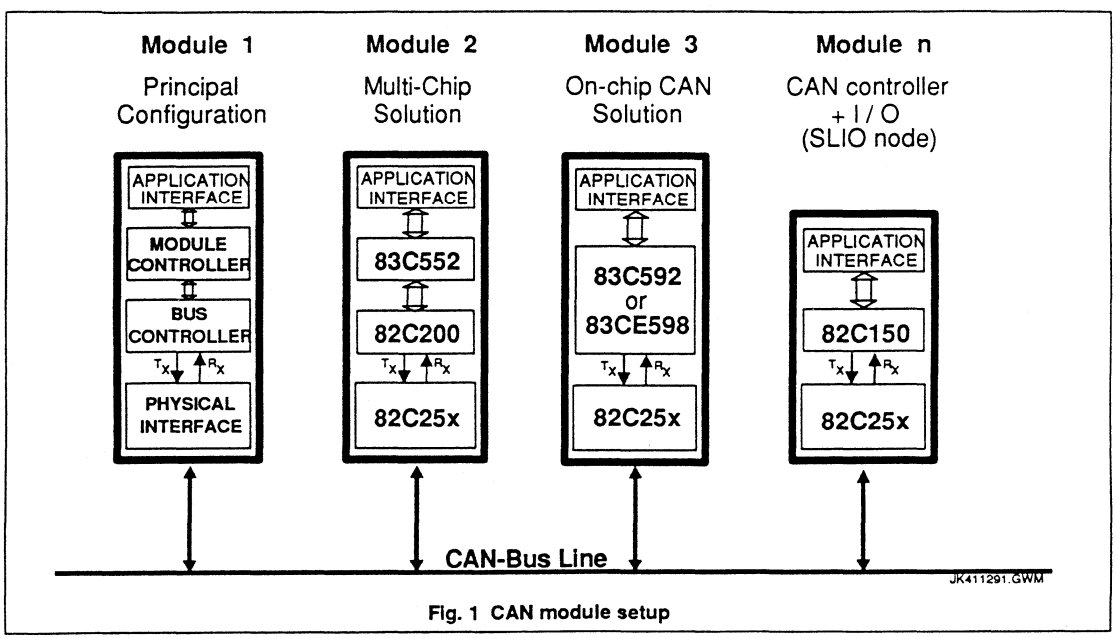


Fig. 1 CAN module setup

The principal configuration of a node is composed of

- the physical interface to the CAN-bus line
- a CAN-bus controller (takes care of the CAN protocol, Data Link Layer and Physical Layer Signalling [4], [5])
- a microcontroller, which prepares the data to be transmitted over the CAN-bus and processes data which was received from the CAN-bus,
- and an interface to the application.

The P82C150 (SLIO) takes over the tasks of the CAN-bus controller and the microcontroller. It needs a host micro controller in the CAN network in order to be able to operate (see chapters 4., 5. and 6.).

The reader of this application note is supposed to be familiar with the CAN specification ([2], [4] and [5]) and the principle functions of the P82C150. He should have the data sheet of the device (refer to [1]) available. This application note gives further information on parts of the device and hints on how to build up a network, where the SLIO is used in one or more nodes.

2. FUNCTIONS AND FEATURES OF P82C150

Fig. 2 gives an overview of all functions of the P82C150. The 'CAN Controller' does all interfacing to the CAN-bus line and is responsible for the correct handling of the CAN protocol. The 'Oscillator + Calibrator' unit contains the on-chip RC-oscillator and does all synchronisation and calibration for receiving messages correctly. The data received from the host CAN-controller is stored internally in a series of registers. The P82C150 organizes the functioning of all 16 I/O-pins according to the content of these registers (more information on these items may be found in the data sheet [1]).

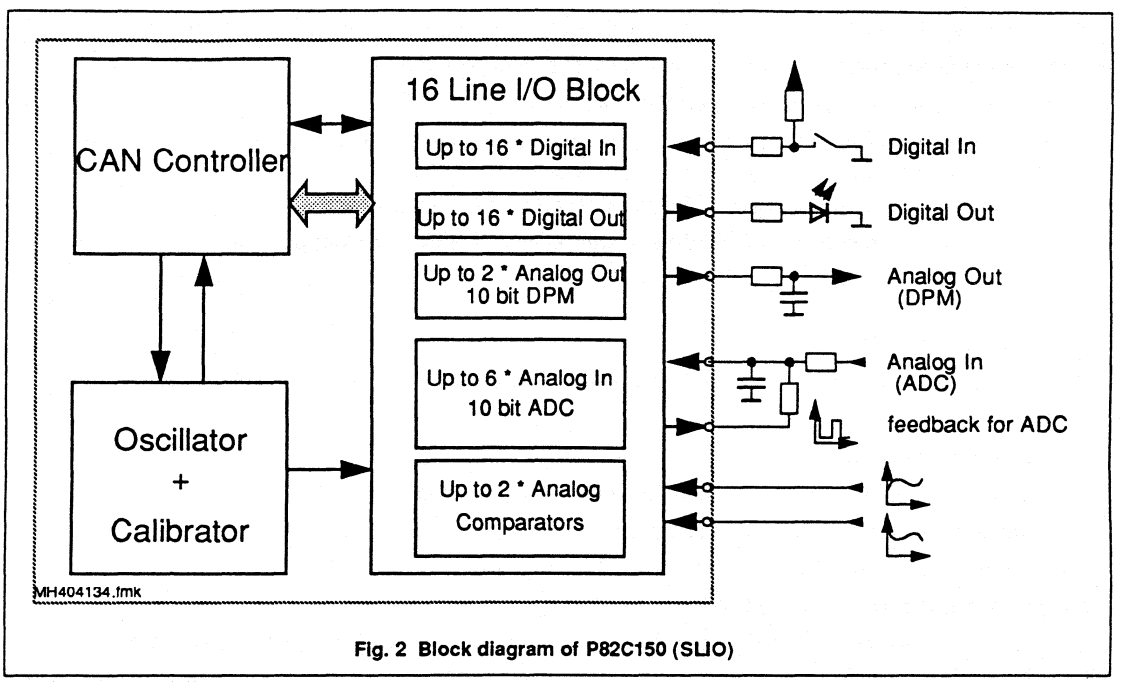


Fig. 2 Block diagram of P82C150 (SLIO)

2.1 General Features

- The P82C150
  - is a stand-alone I/O device with a CAN controller on-chip.
  - is fully compatible to the CAN specification V2.0 A and B.
  - has 16 I/O pins for various digital or analogue configurations.
  - has an on-chip oscillator (no external components).
  - supports a sleep mode with wake-up via the bus.
  - comes in a 28-pin package.
- There may be up to 16 P82C150-devices in one network.

2.2 I/O Port Features

- Each port pin's mode is individually configurable via the CAN-bus:
  - up to 16 pins for digital output.
  - up to 16 pins for digital input.
- The input values at the port pins are transmitted to the host
  - on request by the remote CPU via the CAN-bus (polling of input data).
  - if a signal edge is detected at the port pin (event capture mode, programmable for each pin).
- Up to 2 pins may be used for a quasi analogue output (2 DPM generators).
- 1 pin can be used for the input to a 10-bit A/D-converter.
- Up to 6 pins may be used as an analog 6:1-multiplexer. It may be used for general purpose or connected to the A/D-converter input.
- Up to 4 pins may be used for comparator functions (2 comparators are available):
  - 2 analogue signals can be compared with a reference voltage applied to other port pins.
  - the comparator outputs may be routed to digital I/Os e.g. for using the event capture possibility.

2.3 CAN Communication

- All functions are controlled by one 'intelligent' communication partner ('host' e.g. P8xC592, P8xCE598).
- A P82C150
  - adapts its local bit clock to the bit timing of the bus.
  - broadcasts messages to 'intelligent' communication partners (not to other P82C150s).
  - supports bit rates between 20 kbit/s and 125 kbit/s.
- The communication with a host uses 2 identifiers (Standard Frame):
  - 6 identifier bits are fixed for all P82C150s.
  - 4 identifier bits are programmable by external pull-up/down resistors applied to port pins (=> max. 16 devices in one network).
  - 1 identifier bit determines the transfer direction of a message (from or to the P82C150).
- The host has to send periodically calibration messages.
  - recommended interval: 3800 bit times
  - examples of periodic calibration time intervals for different bit rates:

bit rate	time interval
20 kbit/s	190 ms
50 kbit/s	76 ms
125 kbit /s	30 ms

3. A TYPICAL APPLICATION OF P82C150

Fig. 3 shows a typical application of the P82C150. A reset circuit sets the P82C150 into a proper state after power on. Some suitable circuits are discussed in chapter 3.1. Four bits of the identifiers (used by the P82C150 for the acceptance filter and the transmission identifier) are programmed via pins (hardwired). This item is discussed in more detail in chapter 3.2 where also an example is given (Fig. 8). The connection to the bus is done via the transceiver circuit PCA82C250 (compatible with the ISO 11898 standard). See chapter 3.3 for further information. Information about configurations of the ports and how to use them are discussed under the respective functional descriptions in chapter 8 and chapter 9.

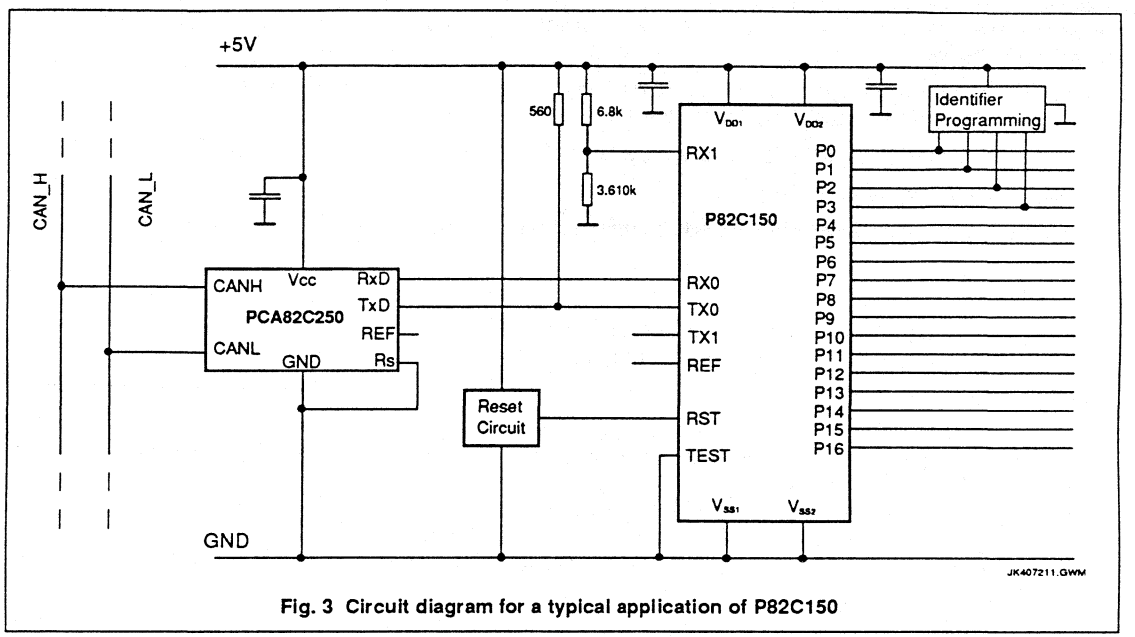


Fig. 3 Circuit diagram for a typical application of P82C150

3.1 Reset Circuit for the P82C150

The device P82C150 needs a reset signal at the input RST during ramp up of the power supply. Fig. 4 shows a possible simple reset circuit with an RC-network and the example of Fig. 8 gives a solution with a supervisory circuit.

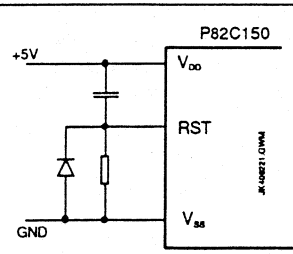


Fig. 4 Reset circuit with an RC-network

3.1.1 Reset Circuit with an RC-Network

This simple reset circuit uses an appropriate RC-network. If the power supply is rising to its nominal value the voltage at the input RST follows the supply voltage as long as the capacitor is nearly unloaded. When the supply voltage has reached its nominal voltage, the capacitor will be loaded via the resistor and the voltage at the reset input ramps down to GND.

If the supply voltage is switched off the input voltage at RST would be shifted to a value below GND as long as the capacitor still is loaded. Thus the limiting values for the DC voltage on any pin (see the data sheet [1]) would be exceeded. In order to avoid this a diode is used for discharging the capacitor quickly clamping the voltage at pin RST. Furthermore the quick discharging of the capacitor helps to generate a new reset pulse, if the supply voltage should be switched on again after a short time.

The values of the components have to be selected in such a way, that the pulse at the reset input RST meets the requirements given in the data sheet [1], as there are:

- input voltage level HIGH at RST for generating a reset of the SLIO
- min. reset pulse width after power on
- the max. allowed negative voltage at pin RST must not be exceeded

Example:

Possible values for the components of the reset circuit are: C = 10 µF, R = 27 kΩ.
The clamping can be made by a fast switching diode, like 1N4148 or BAS32L.

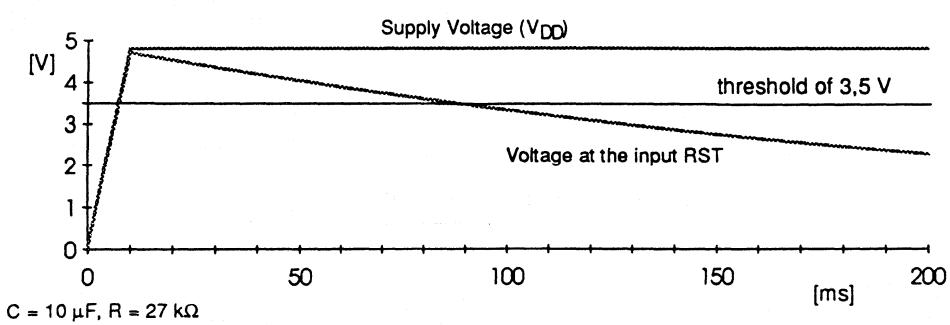


Fig. 5 Switching on the supply voltage

Fig. 5 and Fig. 6 show the supply voltage and the voltage at the RST-input during ramp-up and ramp-down (simulated results). With the selected components the voltage at the input RST stays above a threshold of 3,5 V for about 75 ms, giving enough scope for using components with greater tolerances.
These values are achieved only if the supply voltage ramps up in less than 10 ms.

This simple reset circuit has one general disadvantage: Short dips of the supply voltage (brownout condition) are not detected and don't result in a proper reset pulse for the P82C150. Furthermore the rise time of the supply voltage has to be shorter than a given maximum value (as indicated in the above example).

3.1.2 Reset with a Supervisory Circuit

The drawbacks of the simple reset circuit are removed by employing an integrated power supervisory circuit, either a stand-alone device or combined with a voltage regulator. The supervisory circuit has to generate a positive going reset pulse for being able to reset the P82C150. This pulse has to be held stable during a given time

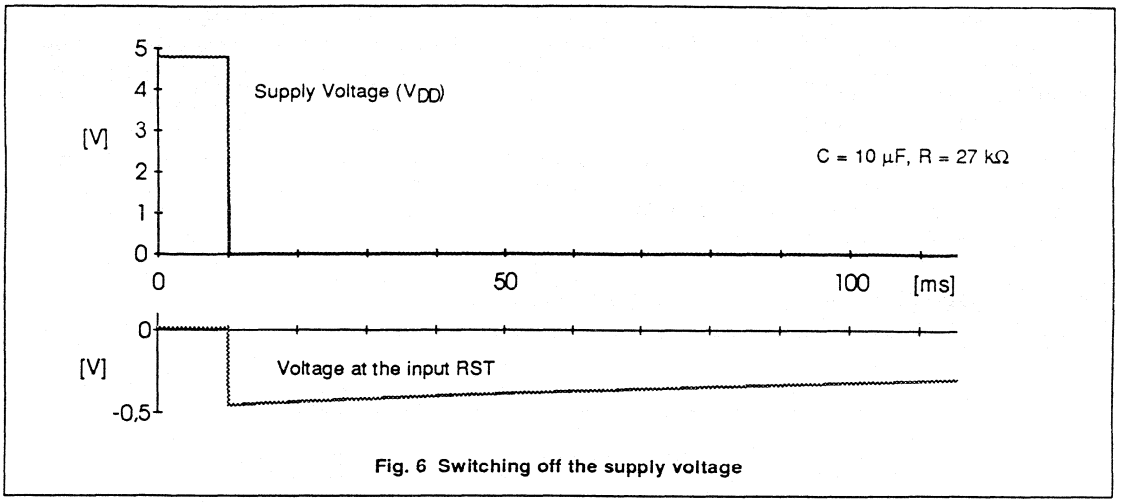


Fig. 6 Switching off the supply voltage

after power on according to [1]. Normally these supervisory circuits are designed to detect dips of the supply voltage below a certain value properly (brownout condition). The min. supply voltage for a proper operation of the P82C150 is given in the data sheet [1].

An example using the supervisory circuit PCF1252 from PHILIPS is given in chapter 3.2 (see Fig. 8).

3.2 Identifier Programming

Four bits of the identifiers used by the P82C150 are programmable via pins while 6 bits are fixed and one bit defines the direction of the message flow - to or from the SLIO (see also chapter 6 on this item). Thus the CAN-identifier distinguishes between the different SLIOs (max. 16 in a system) and their messages in a system. Each SLIO has its own identifier, which is set by applying voltage levels (V_{DD} or V_{SS}) at the pins of the I/O ports P0...P3 during the reset phase. The input levels are read into the identifier latch with the falling edge of the RST input signal. The voltage levels must be held stable for a given time (see [1]) after the falling edge of the reset (see Fig. 7).

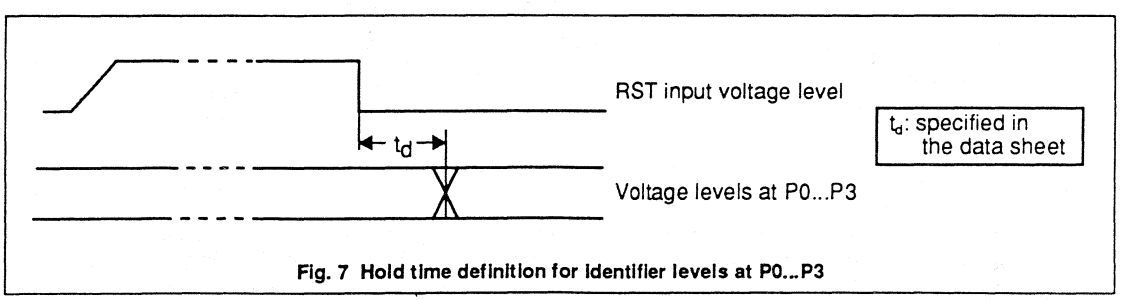


Fig. 7 Hold time definition for identifier levels at P0...P3

These four pins may be used as I/O-ports after the end of the reset. If the voltage levels for the identifier information are determined by resistors, their presence have to be taken into account when designing the circuitry attached to P0...P3.

If a pin is used as an output port, the identifier resistor (pull-up or pull-down) puts an extra load on the output. The resistor should therefore be high-ohmic (suggested range of about 100 kΩ). Care has to be taken of the reaction

of the connected circuit during reset, when the port output is set to HIGH-impedance state and is used as an input reading the programmed identifier information provided by the resistor connected to the pin. The logic level at this pin must not create hazardous conditions of the connected circuit during reset. And the other way round, the connected circuit must not falsify the input port level during reset, in order to reading the programmed identifier into the internal latch correctly.

If a pin is used as an input port, the driving circuit has to override the input voltage produced by the connected resistor during normal operation. During the reset phase the connected output of the application has to be switched into a HIGH-impedance state to allow for proper voltage level generation as defined by the identifier resistor at this pin. An example is given in Fig. 8.

Example: Usage of Identifier Pins as I/O Ports after Reset

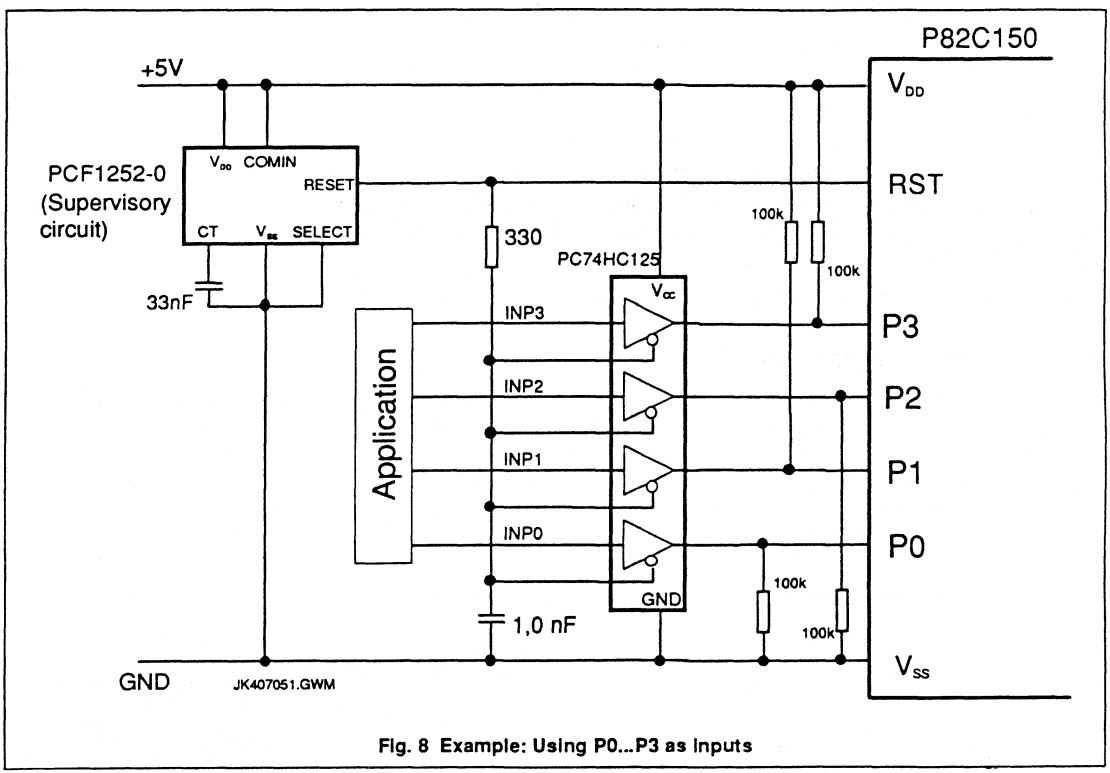


Fig. 8 Example: Using P0...P3 as Inputs

The ports used for the programming of the identifier bits during reset may be used as inputs or outputs after the end of the reset pulse (see the latest data sheet [1] for the specification of the hold time). In cases, where the levels at the ports could be falsified (ports used as inputs) or the connected application would not allow certain input levels (ports used as outputs) during reset, it is necessary to implement buffers between the ports and the attached circuit. Fig. 8 shows an example where the ports are used as inputs.

The power supply supervisory circuit, PCF1250-0, is used for generating the HIGH-level active reset signal during ramp up and short dips below 4,75 V (typ.) of the power supply. With the capacitor of 33 nF at the input CT of the circuit a duration of 33 ms (typ., slew rate of the supply voltage <25 V/ms) for the reset pulse may be

achieved. For the mentioned values and for further information about the possibilities of this circuit e.g a different voltage etc., please have a look into the data sheet of the PCF1252-x [9].

The buffer circuit 74HC125 is used for disconnecting the outputs of the application from the ports during reset. The levels at the ports P3 ... P0 (determined by 100 kΩ resistors) are latched with the H-to-L edge of the reset pulse. In order to prevent the application circuit from falsifying the levels at the port inputs, the outputs of the buffer 74HC125 are switched into TRISTATE during reset. An RC-combination at the $\overline{OE}$-inputs of the buffers (330 Ω / 1,0 nF) is used to delay the reactivation of the buffer outputs to achieve a hold time >200 ns (H->L-transition of the reset pulse <100 ns).

3.3 Physical Layer Interfacing

A CAN node consists not only of the protocol controller like the P82C150 but also needs an interface to the CAN-bus. For a balanced wire implementation of the bus the basic requirements of this interface are to provide

- a differential line driver for transmitting data,
- a receiver comparator for reading the data on the bus.

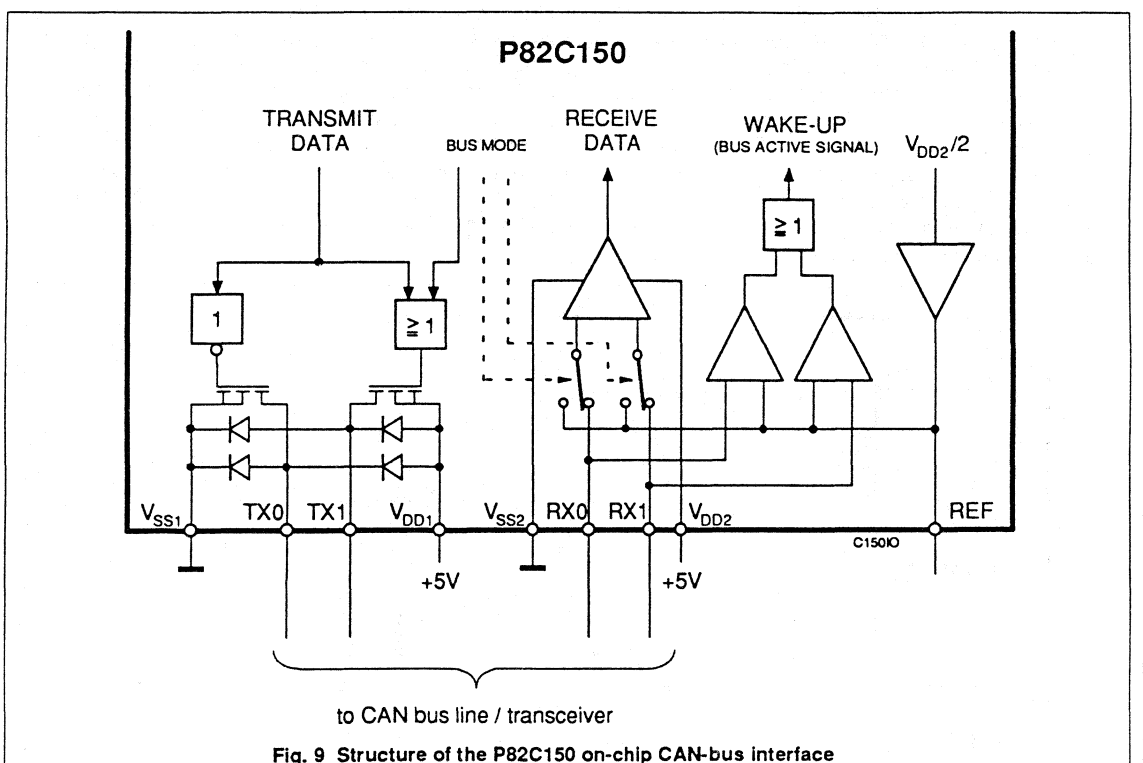


Fig. 9 Structure of the P82C150 on-chip CAN-bus interface

To some extent the controller itself comprises the main functions for such an interface which can be implemented either by external discrete components[1] or by an IC like the Philips transceiver PCA82C250 [3]. This transceiver is connected between the protocol controller and the CAN bus and represents the physical layer interface.

1. For details on the implementation of discrete physical layer interfaces see [8]

Normally data transfer takes place on balanced bus wires in differential mode. In cases where communication in this mode fails the controller can enter one of two single wire modes in order to try to establish message transfer in this way.[2]

Table 1 CAN bus modes

Bus mode	Status Bits BM1, BM0	Reception Level		Transmission	
		Recessive	Dominant	TX1	TX0
0 Differential	00	RX0 > RX1	RX0 < RX1	enabled	enabled
1 One-wire RX1	01	RX1 < REF	RX1 > REF	enabled	enabled
2 One-wire RX0	10	RX0 > REF	RX0 < REF	disabled	enabled
3 Sleep	11	RX0 > REF and RX1 < REF	RX0 < REF or RX1 > REF	disabled	disabled

The structure of the interface that is built into the P82C150 is depicted in Fig. 9. There are two transmit outputs and two receive inputs. If the chip is connected to the bus by discrete components, TX1 and RX1 are connected to the bus wire CAN_H while TX0 and RX0 are connected to CAN_L. Of the two drivers for transmitting data one can be turned off. This is required in bus mode 2 where communication is maintained on one wire only and a short-circuit between the two wires has to be tolerated. Receiving data is done by a comparator. In bus mode 0 (normal mode) the differential signal voltage between RX0 and RX1 is evaluated. Bus modes 1 and 2 are one-wire modes. In mode 1 the input RX0 is disabled and the comparator input is connected to a reference voltage. In mode 2 input RX1 is disabled and RX0 is compared with the reference voltage. Bus mode 3 is sleep mode. Wake-up from this mode is done by two separate comparators which detect a dominant level on either wire. An overview of the bus modes is given in Table 1 (see also Fig. 12 on page 18). For more details see the data sheet of the P82C150 [1].

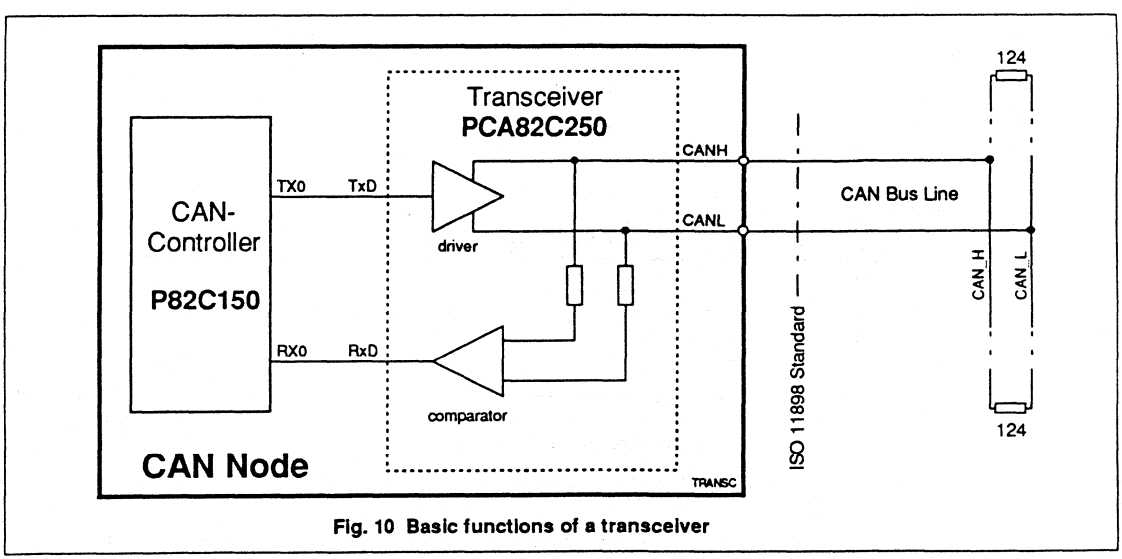


Fig. 10 Basic functions of a transceiver

Using a separate transceiver IC like the PCA82C250 not only simplifies the design and layout of a CAN node significantly but offers even more advantages. Due to its wide common mode range in receiving the differential bus signal it improves immunity against electromagnetic interference and thus provides increased reliability of the bus

2. For details on bus failure management see ISO 11519-2 [5] and [10]

communication. Electromagnetic emission can be reduced by the 'slope control' feature. This function decreases the slew rate of the signal transitions on the bus. In many cases this permits the extended use of twisted pair wires where otherwise a shielded cable would have to be chosen.

The basic functions of the transceiver PCA82C250 are depicted in Fig. 10. The CAN controller sends the serial data to be transmitted to the TxD input of the transceiver. Depending on the logical level the output drivers of the transceiver are activated. Due to the wired-AND characteristic of the bus only dominant levels (LOW) can be transmitted. During recessive states (HIGH) the drivers stay inactive and the bias network determines the bus voltage - unless another node is transmitting a dominant level. The receiver comparator converts the differential bus signal to a logical signal which is output at pin RxD and sent to the controller to be decoded. This receiver comparator is always active and thus monitors the bus while the node is transmitting. In this way the CAN controller can compare the received bits with the transmitted ones.

As shown in Fig. 3 on page 10 the SLIO pins Tx0 and Rx0 are used to transfer data to and from the transceiver. Tx1 is not used and Rx1 is put on a bias voltage of 1.7...1.8 V. The reason for this is to present a recessive bus level to the internal comparator, which is necessary for enabling the sleep mode (see Table 1). Furthermore a recessive bus level is seen, when the P82C150 is in bus mode 1 (a mode not used in this configuration) during the calibration procedure (see chapter 4, Fig. 12 and Fig. 13) and tries to receive data at pin Rx1 only. The transmit outputs Tx0 and Tx1 are designed to be connected directly to the bus and are therefore of open-drain type. If a transceiver is used these pins need an additional external pull-up resistor of about 560 Ω to speed up the otherwise slow LOW-to-HIGH signal transitions, because the TxD pin of the PCA82C250 is equipped with a weak internal pull-up resistor only.

The pin R_S of the transceiver is the slope control input. If it is connected to GND (V_{RS} = 0 V, Fig. 3 on page 10), the transistors driving the bus operate at maximum speed. This gives short rise and fall times of the signals on the bus. Slope control is adjusted by connecting a resistor from pin R_S to ground. For more information about the slope control function please see the data sheet of the PCA82C250 [3].

Reducing the slew rate increases the total delay of the transceiver. This has to be taken into account when calculating the maximum achievable bus length.

The example of a bus interface as depicted in Fig. 3 on page 10 uses the same power supply ground for both the transceiver and the CAN controller. This means that the controller and its application circuitry are galvanically connected to the transceiver and the CAN bus. In cases where this is not desired, optocouplers can be placed between the transceiver and the controller. Fig. 11 shows an example with the controller and its application being isolated from the transceiver and the bus.

Using optocouplers increases the delay of a node. The signal has to pass these devices twice per node (in the transmitting and receiving path). This has to be taken into account when calculating the maximum achievable bus length (see chapter 7.4).

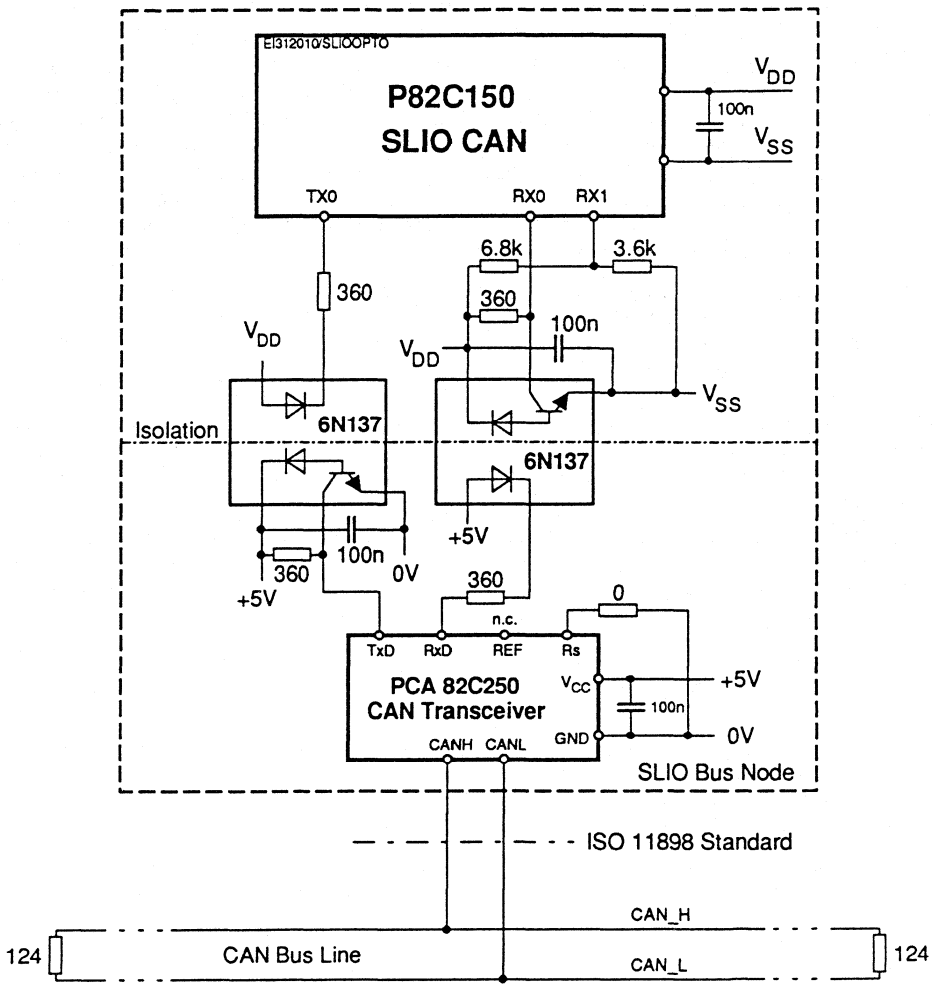
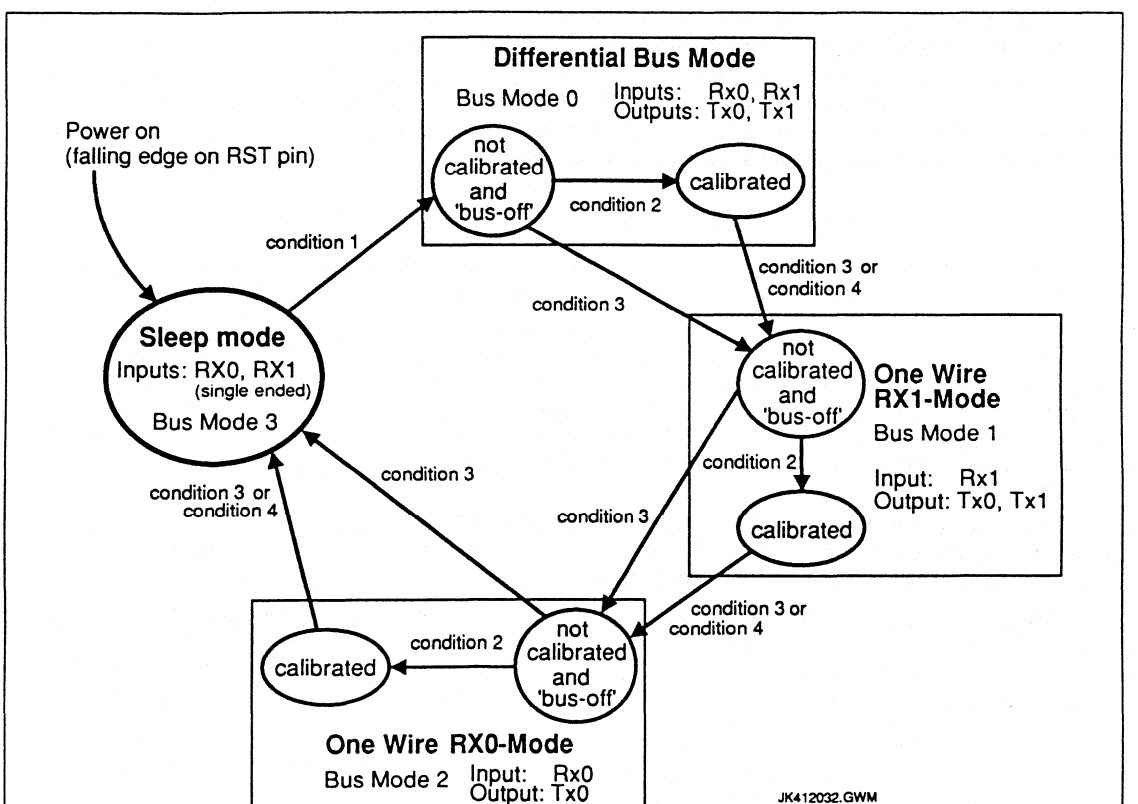


Fig. 11 Example of a CAN bus interface with galvanic isolation using optocouplers

4. INITIALIZATION OF THE P82C150

The P82C150 has been designed for the implementation of low cost nodes in a CAN network in order to reduce the overall system cost. The reduction is achieved by avoiding as many external components as possible. Therefore an on-chip oscillator without external circuitry has been designed into the P82C150 and an automatic bit rate detection has been implemented. The P82C150 calibrates its internal bit clock to the bit timing of the bus by means of a specific calibration message (see chapter 4.2).

A P82C150 in a SLIO node may be regarded as a port and function extension of a remote host microcontroller. It is programmable with respect to its I/O-ports. This implies that it has to be initialized after power-on before it may be used in a system.



Condition 1: dominant bit detected on Rx0 or on Rx1
Condition 2: successful performance of the calibration procedure according to Fig. 13
Condition 3: bit counter overflow (>8191), causes also 'bus-off' state
Condition 4: Transmit Error Counter overflow (>255), causes also 'bus-off' state

Fig. 12 CAN-bus modes, calibration status and switch over conditions

4.1 Reset and Bus Mode Change

After a power-on reset the P82C150 enters the sleep mode — one of 4 different bus modes, which are supported by the P82C150 (see Fig. 12 and Table 1 on page 15, further information on bus modes is found in the data sheet [1]). With the HIGH-to-LOW transition of the reset pulse the information at the port pins P3 ... P0 is latched into the identifier latch for being used as part of the acceptance filter and the transmission identifier. All internal I/O registers are cleared. In this mode the P82C150 is uncalibrated and in the 'bus-off' state ([4]) only scanning the bus line inputs (Rx0 and Rx1) for a dominant level. If a dominant level is detected, the P82C150 wakes up and starts a calibration procedure in bus mode 0 (differential mode) according to Fig. 13 and chapter 4.2. If the P82C150 has not successfully calibrated its bit clock within 8192 local bit times, it will change to bus mode 1. The bit counter is reset and a new calibration procedure is started. If the P82C150 neither can calibrate its internal bit clock in bus mode 1 nor in bus mode 2, it changes to sleep mode, again scanning the bus line inputs for a dominant level. Any dominant level will restart such a 'trying-to-calibrate' cycle until it is met with success.

If the bus transceiver PCA82C250 is connected to the P82C150 as given in the typical application of Fig. 3 on page 10, the P82C150 can never calibrate its internal bit clock in bus mode 1 as Rx1 is connected to a fixed recessive level. When changing to bus mode 1 after having been unsuccessful in bus mode 0 it will always get a bit counter overflow and change to bus mode 2 (condition 3 in Fig. 12).

4.2 Initial Calibration Procedure after Reset or Bus Mode Change

The initial calibration procedure as given in Fig. 13 is discussed in this chapter. Special aspects of the calibration of SLIO nodes in different system configurations and during normal operation are discussed in chapter 5.

After a power-on reset or a bus mode change the P82C150 is uncalibrated and 'bus-off'. The local bit time derived from the internal oscillator is set greater than 50 µs (see the data sheet [1] for the proper value after reset). It is calibrated using messages sent over the CAN-bus. A message on the bus causes the P82C150 to measure any distance between two transitions from recessive to dominant at the output of the CAN-bus input comparator. Only if one half of this time distance is shorter than the current local bit time, it is taken as a better approximation and will be used as local bit time for receiving further messages (stepwise adaptation of the internal bit clock).

In parallel to the calibration process of the local bit time length the P82C150 has started the 'bus-off' recovery sequence using the current local bit time. According to the ISO Standard [4] it has to monitor at least 128 blocks of 11 consecutive recessive bits in the bit stream before being able to leave the 'bus-off' state.

Any message on the bus may roughly calibrate the local bit time of the P82C150, but only after having received the bit sequence '1010', the P82C150 can receive messages correctly. The early occurrence of this bit sequence after reset or bus mode change shortens the time for a rough calibration of the internal bit clock. Any second message, which is received correctly according to the CAN-protocol (an acknowledge is not required but no active error flag is allowed), verifies that the local bit time is in line with the bit time on the bus. During this state of rough calibration the P82C150 may receive messages and set ports into defined states. As long as the P82C150 neither is fine calibrated nor has finished the 'bus-off' recovery sequence, the P82C150 does neither give an acknowledge nor transmit any messages on the bus.

After having verified the rough calibration of the internal bit clock, the P82C150 must receive a calibration message[3] correctly within 8192 local bit times after wake up or bus mode change. Then it has fine calibrated its internal bit clock and the local bit time corresponds to the bit time on the bus. All internal I/O registers are cleared once more, as they may contain garbled information. Before the P82C150 may take part in the communication on the CAN-bus as a member with all rights (receiving **and** transmitting), it has to finish the 'bus-off' recovery sequence. Then it is 'on-bus' as an 'error active' node and sends the sign-on message[4], which signals the controlling host, that the P82C150 now is able to transmit messages and its internal data registers are ready for a configuration (see chapter 4.3).

3. A special message used only for calibrating the internal bit clock of the SLIOs in the CAN network. For more information see the data sheet [1] on 'Oscillator and Calibration', 'Calibration Message' and 'Bit time Calibration'.

After this initial calibration procedure the P82C150 expects to receive calibration messages at a regular basis, at least one message within 8192 local bit times (see chapter 5.3).

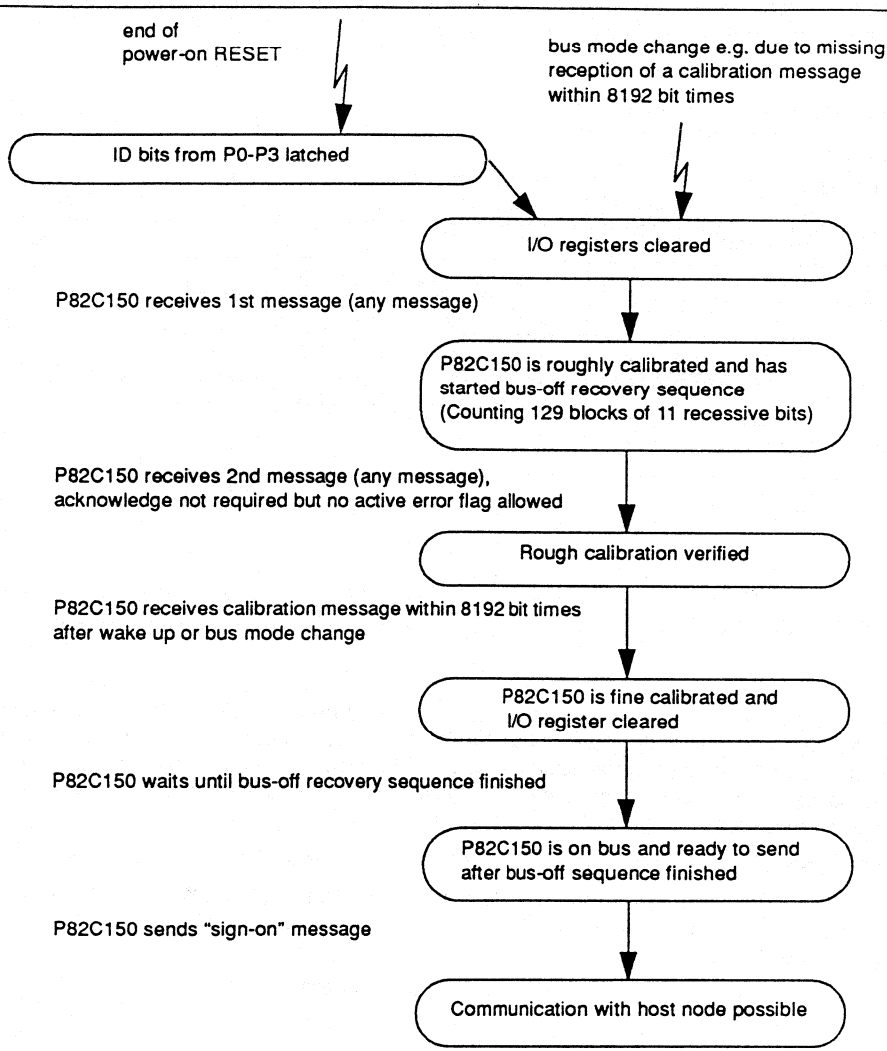


Fig. 13 P82C150: Calibration procedure after reset and bus mode change

4. See the data sheet [1] for more information about the sign-on message.
ATTENTION: In a sign-on message the error warning bit (EW) is set, but nevertheless internally the status of the error counters are cleared. The error warning bit in a sign-on message must be ignored.

4.3 Configuration of internal Control Registers

After a successful calibration of a SLIO node, the P82C150 needs a configuration of its internal data registers. The host node has to send configuration messages, which prepare the ports for the specific needs of the connected application at the SLIO node. Table 2 gives an overview of the different port functions which may be selected.

Table 2 Alternative port functions

Port Function			Port Number															
			16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
identifier programming																X	X	X	X
digital I/O				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
comparator input						X	X	X	X										
comparator output										X	X								
DPM output									X						X				
ADC	1 signal only	input line		X															
		AD feedback out	X																
	2 to 6 signals	input lines				X				X	X	X	X	X					
		multiplexer out			X														
		AD converter in		X															
		AD feedback out	X																
ADC comparator output												X							

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During the reset phase the output drivers of all ports have been disabled (switched into tristate) and all registers are cleared (set to '0'). The host should transmit all configuration and output data to the P82C150 before switching the output drivers on. Automatic transmission of data due to edge triggering should be activated not before having finished setting switches and output data and activated the drivers of the output ports in order to be undisturbed of triggered messages during the setup of the P82C150.

The recommended sequence of configuration messages for the initialization of the P82C150 is:

1. transmit the value for the configuration of the A/D-converter inputs (SW3 .. SW1) and the ports used for monitoring the outputs of the comparators (M3 .. M1) (register address 5) without starting an A/D-conversion (ADC='0')
2. transmit the values for the DPM outputs (if used) (register addresses 6 and 7)
3. transmit the data for the digital port outputs (register address 3)
4. enable the output drivers (output enable bits in register address 4)
5. define the edge trigger mode (register address 1 and 2):
   'polling' i.e. no edge trigger enabled, trigger on a positive or negative edge, trigger on both edges.
6. An A/D conversion may now be started by setting ADC='1' in the analog configuration register (address 5) or by addressing the A/D data register (address 8).

5. CALIBRATION STRATEGY FOR THE P82C150

A network containing one or more SLIO nodes, which need calibration messages from other nodes, must have at least one node operating autonomously. Such nodes (in the following discussion they are called ***'normal node's*** in contrast with SLIO nodes) may serve as **host nodes** for the communication with SLIO nodes. If normal nodes are **crystal-operated** (clock stability must be within 0,1%), they may send calibration messages to SLIO nodes. In general the host function and the calibration function are combined in one normal node, but it is allowed to distribute these functions to different normal nodes (see chapter 6.2). For the discussion in this chapter it is assumed that the host node also takes care of the calibration function.

After wake-up or bus mode change the P82C150 needs to be calibrated by an operating CAN-node sending specific calibration messages. As long as the P82C150 is uncalibrated and bus-off it is unable to acknowledge any message. Once it is calibrated and operating, it needs recalibration messages on a regular basis. Calibration messages must be sent by a crystal-operated normal node.

For the further discussion it is necessary to distinct between different sequences of calibration messages dependent on the number and the status of the normal nodes in the CAN-network:

- CAN-bus systems with only **one** normal node (host node and crystal-operated for the communication with and the calibration of SLIO nodes) and one or more **uncalibrated** SLIO nodes (see Fig. 14).
  - Sequence if the host node is error active after start-up of the SLIO nodes (see chapter 5.1.1).
  - Sequence if the host node is error passive after start-up of the SLIO nodes (see chapter 5.1.2).
- CAN-bus systems with **more** than one normal node (e.g. one crystal-operated host node for the communication with and the calibration of SLIO nodes and other normal nodes) and one or more **uncalibrated** SLIO nodes (see Fig. 17).
  - Sequence after start-up of the SLIO nodes (see chapter 5.2).
- Sequence of messages for the **re**calibration of **operating** SLIO nodes (see chapter 5.3).

For the mentioned situations different optimal sequences of calibration messages are suggested. From the discussion in the following chapters a recommended strategy for calibrating SLIO nodes may be derived (see chapter 5.4).

5.1 A Network with only One Normal Node (Host Node)

5.1.1 The Host Node is Error Active

After a wake-up or bus mode change the P82C150 is uncalibrated and bus-off. It is not allowed to acknowledge any message. Thus an error active host node, if it is the only normal node with a fixed bit rate in a CAN network (Fig. 14), will detect acknowledge errors after having sent a calibration message. It then sends an error frame destroying the 'End of Frame' field as the transmitted active error flag consists of dominant bits. Therefore the P82C150 does not receive a correct message, which is necessary for the verification of the rough calibration (see Fig. 13). After having transmitted 16 calibration messages without receiving an acknowledge, the host becomes error passive, which means that it transmits an error frame with a passive error flag (recessive bits) after having detected the acknowledge error. This will not destroy the 'End of Frame' field and the SLIO node receives the 17th calibration message correctly and can verify the rough calibration. The reception of one further calibration message (the 18th) enables the P82C150 to fine calibrate its internal bit clock. After having finished the 'bus-off' recovery sequence the P82C150 is 'on-bus' and sends its sign-on message.

Fig. 15 gives an example of a calibration procedure of an error active host node, achieving a fast calibration of all P82C150 devices in a network e.g. after power on. After having received a burst of at least 18 calibration messages the P82C150s are fine calibrated. For achieving a short 'bus-off' recovery time the host should now stop sending any further messages. This will result in a long 'bus idle' period, which may be used by the P82C150s for counting the remaining blocks of 11 recessive bits (129 blocks requested in total). If further (re)transmissions of

messages are not stopped in time before the sign-on messages are sent by the SLIOs, the host node would fail to receive the first sign-on message due to its start during the passive error flag of the host.

A possible flow chart for programming a CAN controller (e.g. P8xC592 or P8xCE598) for such a bit time calibration procedure is given in the data sheet [1].

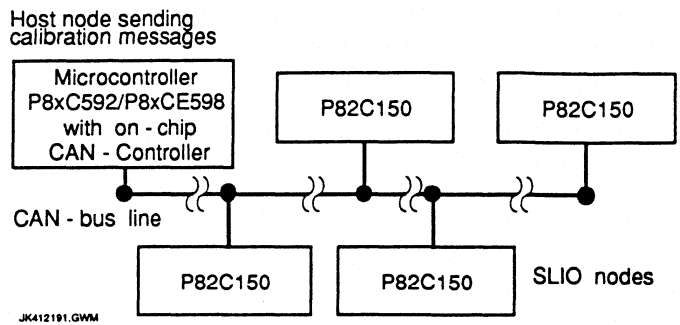


Fig. 14 CAN network with one normal node (host node)

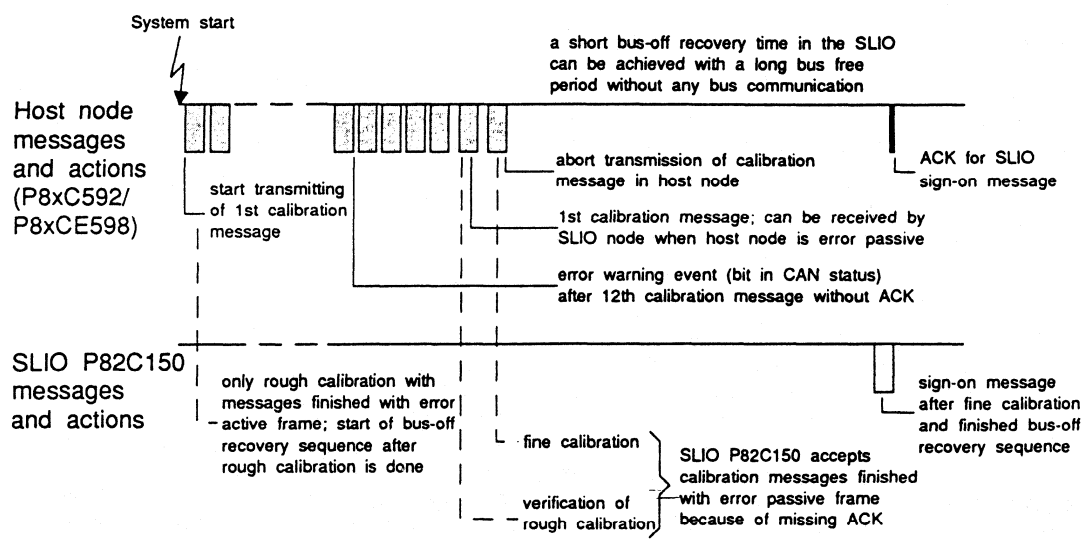


Fig. 15 Example of a calibration sequence if the host node is error active (e.g. after power-on)

5.1.2 The Host Node is Error Passive

In case the normal node (host node), which is sending calibration messages, is error passive already not destroying the 'End of Frame' field (compare with the discussion on an error active host in chapter 5.1.1), a fast calibration sequence may be achieved with the example given in Fig. 16. The first calibration message is used for the rough calibration and starts the 'bus-off' recovery sequence. The second message will be received correctly and is used for the verification of the rough calibration. Thus the third message is used by the P82C150 for the fine calibration of its internal bit clock. If the host generates a long 'bus idle' period, the SLIO node can count the requested 129 blocks of 11 recessive bits for 'bus-off' recovery in the shortest possible time.

The necessary three calibration messages may also be distributed equally as shown in the example given in Fig. 18.

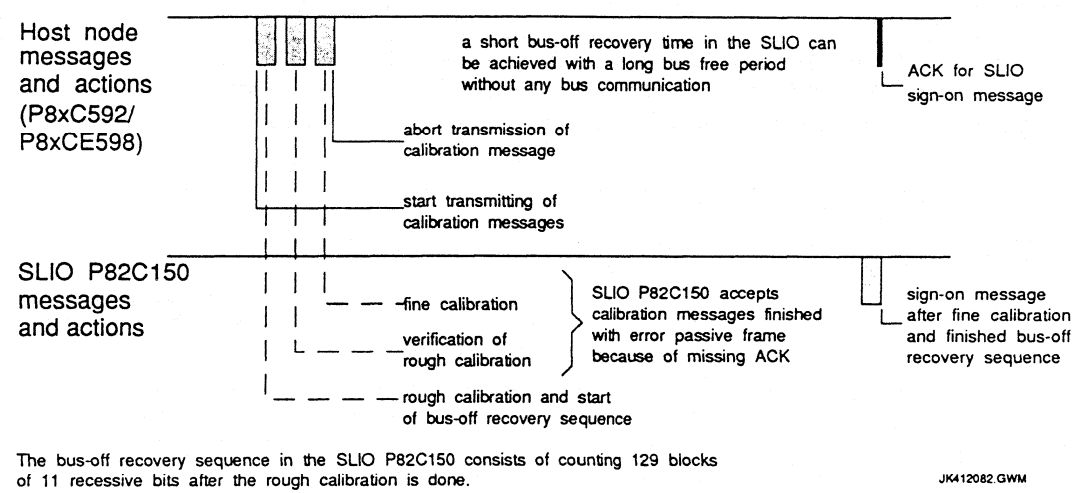


Fig. 16 Example of a calibration sequence if the host node is error passive

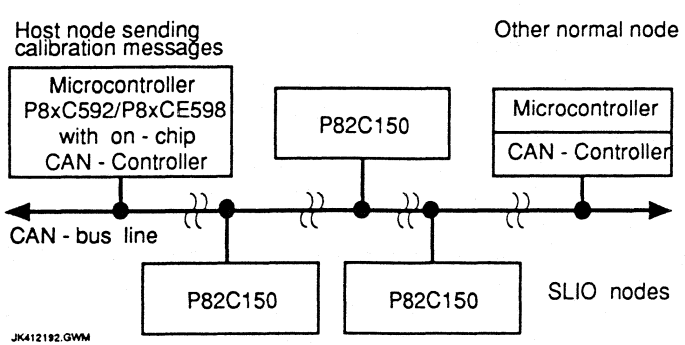


Fig. 17 CAN network with more than one normal node

5.2 A Network with More than One Normal Node

If there are more than one normal node in a CAN system (see Fig. 17), each message always gets an acknowledge from the other normal node(s), i.e. the messages are not destroyed by error frames, which corresponds to the case discussed in chapter 5.1.2 for an error passive host. Each calibration message may be used by the SLIO node for the calibration of its internal bit clock achieving a fast fine calibration after having received three messages correctly. Both examples given in Fig. 16 and Fig. 18 apply for this situation.

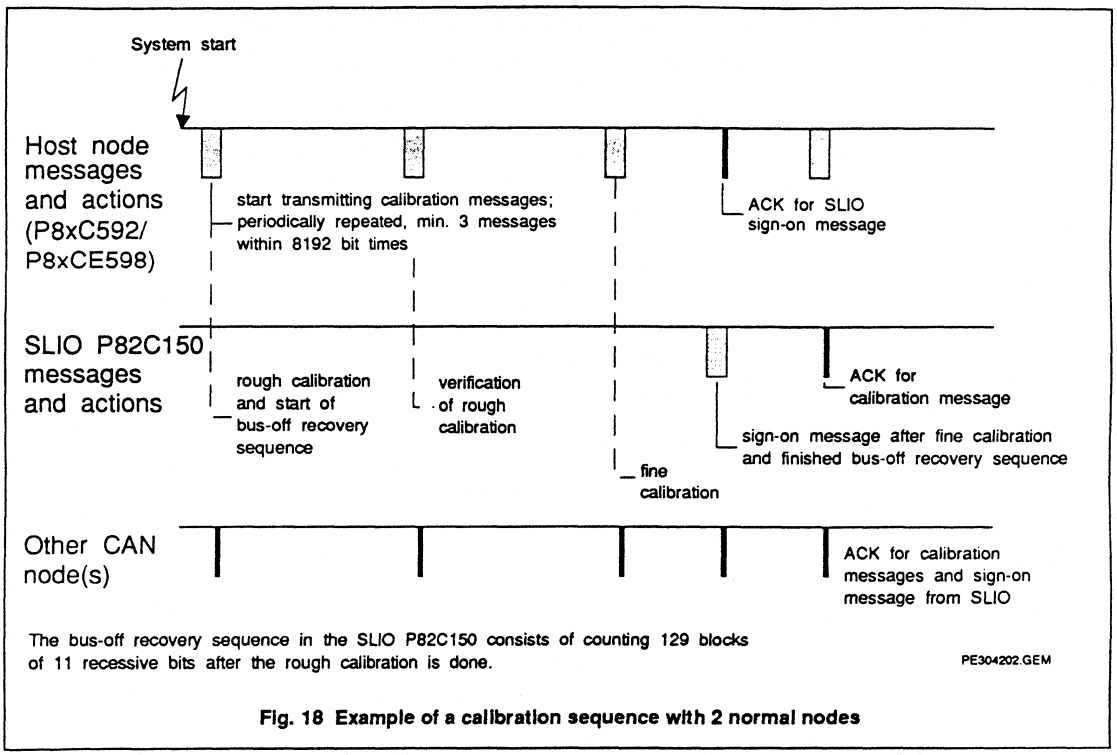


Fig. 18 Example of a calibration sequence with 2 normal nodes

5.3 Recalibration of an Operating P82C150

Following the initial calibration the P82C150 needs a regular recalibration, as the frequency of the internal oscillator varies with temperature and supply voltage changes. It is expected that the temperature of the environment and the supply voltage does not change significantly between the reception of two calibration messages (short time stability of temperature and supply voltage). If the P82C150 does not receive a calibration message within 8192 local bit times, it switches into the 'bus-off' state and tries to calibrate its local bit time in a different bus mode (see data sheet [1], Fig. 12 and Fig. 13).

Fig. 12 on page 18 gives an overview of the different conditions under which the P82C150 switches between the 'calibrated' and 'not calibrated' state. After power-on the P82C150 is not calibrated (sleep mode). It enters the calibrated state after having received calibration messages as discussed in chapter 4.2, chapter 5.1 and chapter 5.2. After a successful execution of the 'bus-off' recovery sequence it is fully operating on the CAN-bus. Two conditions may bring the P82C150 back into the 'not calibrated' state at any time:

- The bit counter overflows, because a calibration message has not been received within 8192 bit times.
- The Transmit Error Counter overflows (>255) and the node is switched into the 'bus-off' state ([2], [4] or [5]).

In order to keep a network with SLIO nodes alive at least one calibration message within 8192 local bit times is requested for a recalibration of the P82C150s. Due to the inaccuracy of the calibration process and the allowed oscillator tolerance in a CAN-bus system a repetition period lower than 8000 bit times (at the host node) is recommended [1].

5.4 Recommended Calibration Strategy for the P82C150

In the previous chapters four possible sequences of calibration messages were discussed, which adapts to different situations of the network:

1. One burst of 18 calibration messages (see Fig. 15).
2. Blocks of three calibration messages every 8000 bit times (host node) (see Fig. 16).
3. Equally distributed calibration messages every 3800 bit times (host node) (see Fig. 18).
4. One calibration message every 8000 bit times (host node).

In Table 3 characteristics of the discussed sequences are given.

Table 3 Characteristics of Calibration Sequences

Number	start-up (after power-on) or restart (after bus mode change) of SLIOs	recalibration	bus load (recalibration)*
1.	fast	not applicable	not applicable
2.	slow	yes	high (*~2,5%*)
3.	slow	yes	medium (*~1,75%*)
4.	not applicable	yes	very low (*~0,8%*)

* Calculated with a calibration message of 67 bits and an error free transmission.

The sequences 2. and 3. may be used in all situations but are not very fast for being used during start-up or restart of P82C150 devices. Therefore it is recommended to use one of the following combinations of sequences.

Table 4 Recommended Sequences of Calibration Messages

	Description	Properties
1 + 2 or 1 + 3	Sequence 1 (a burst of 18 calibration messages) is used after the power-on of the host node only (host is always error active). Afterwards sequence 2 or 3 is used continuously (applies for restart due to bus mode change and for recalibration).	fast start-up after power-on slow restart after bus mode change easy to implement, as no complex decisions have to be taken

In the demonstration software of the SLIO Evaluation Board (OM4272) the sequences 1., 2. and 3. are used for the calibration process. This solution may be used as an example for a more complex calibration, where each situation of the system is met with an optimized sequence of calibration messages[5].

Sequence 4. is optimized for the recalibration process with a very low bus load but is not applicable during the start-up or restart of an uncalibrated P82C150 (e.g. after power-on of a SLIO node). It should only be used in case a very low bus load is required, as it lacks the possibility to calibrate P82C150 devices which have been disconnected (e.g. hot-plugging of SLIOs, see chapter 6.2.2).

5. for further information refer to the software flow given in the User Manual [6]

6. GENERAL COMMUNICATION ASPECTS OF SYSTEMS WITH SLIO NODES

The aspects of power-on reset, calibration after power-on, initialization and recalibration of a SLIO node equipped with the P82C150 have already been discussed in the previous paragraphs (see chapter 3, chapter 4 and chapter 5). This chapter discusses some other general aspects of CAN networks where one or more nodes are SLIO nodes.

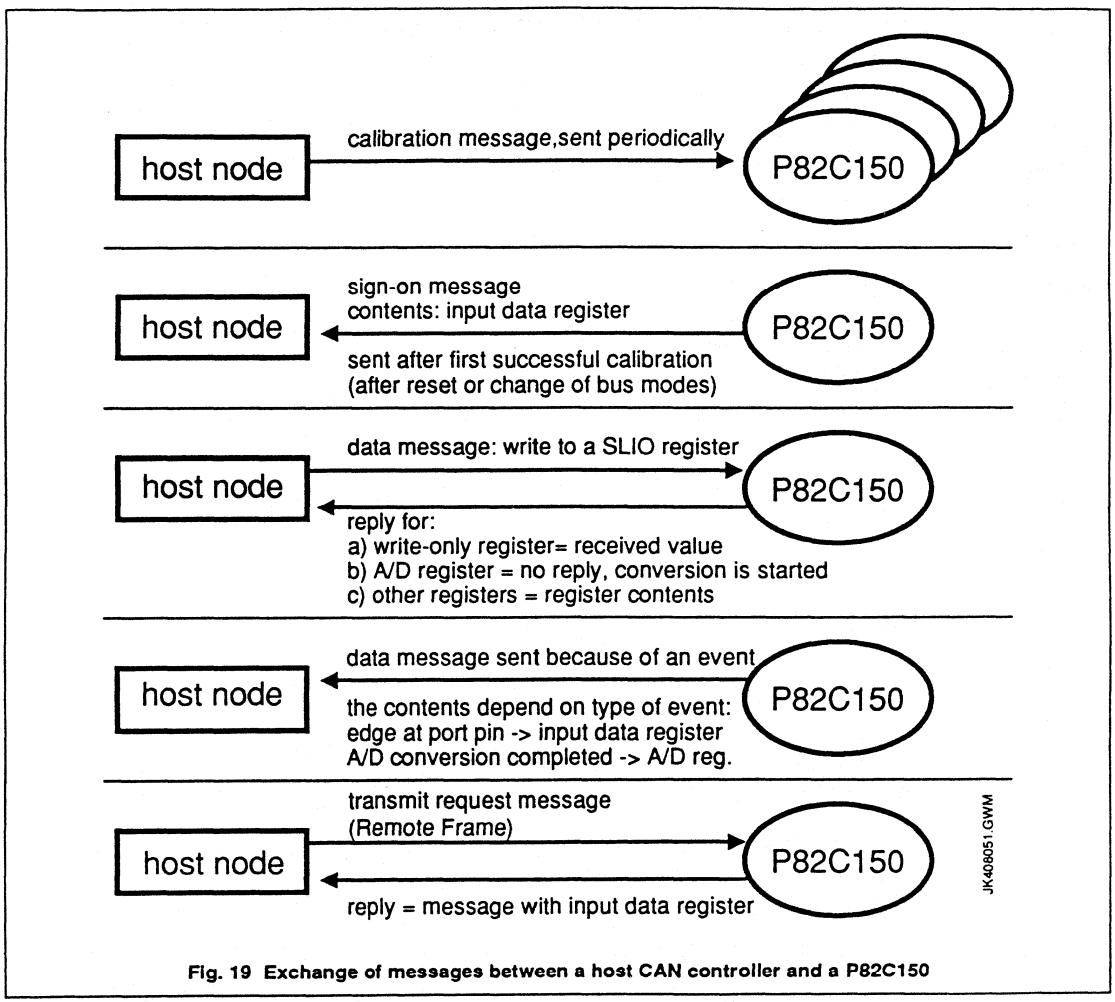


Fig. 19 Exchange of messages between a host CAN controller and a P82C150

6.1 Message Structure

A CAN network cannot be built up only of SLIO nodes because they need at least one normal node (crystal-operated, host node), which takes care of the calibration and initialization of the SLIO nodes (see Fig. 14 on page 23). The messages, which are exchanged between a host and the SLIOs it is controlling, are in general calibration messages, the sign-on message, data messages and remote frames [1]. Fig. 19 gives an overview of

all mentioned messages indicating the direction of the transmission and the reaction of the P82C150 on received messages.

The acceptance filter of the P82C150 has a fixed value for receiving calibration messages (identifier: "000 1010 1010") and a partly fixed value for receiving data and remote frames. The variable part is defined by the voltage levels at P3 ... P0 during reset (see chapter 3.2, chapter 4.2 and [1]) and by the type of frame (identifier bit 'DIR' [1]). The composition of the different messages are shown in Fig. 20 (general message format as defined by the CAN standard) and Table 5 (defining bits and bytes for the different messages of the P82C150).

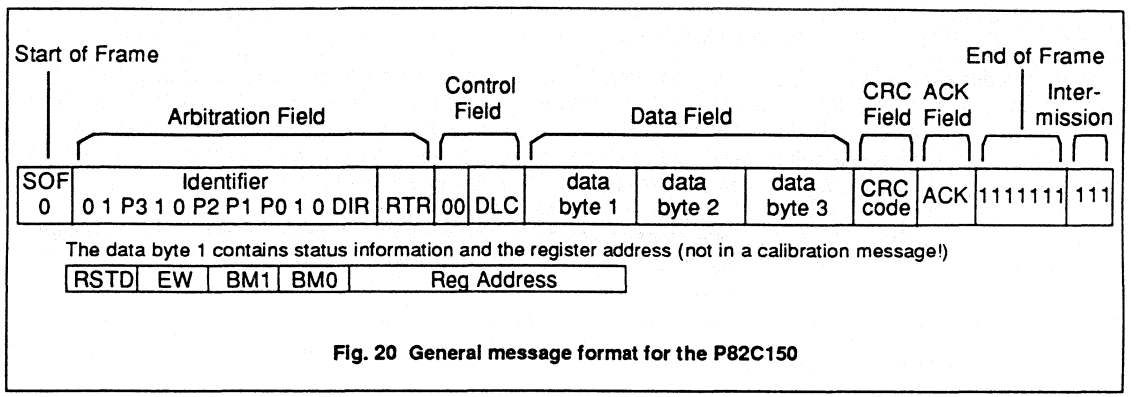


Fig. 20 General message format for the P82C150

Table 5 Specification of Bits and Data Bytes in the SLIO messages

message type	DIR	RTR	DLC	Data Byte 1				
				RSTD	EW	BM1	BM0	Reg.Address
data message (host to SLIO)	0	0	0011	X	X	X	X	current
data message (SLIO to host)	1	0	0011	0	EW	BM1	BM0	current
sign-on message	1	0	0011	1	1*	BM1	BM0	0000
Remote Frame	1	1	0011					

* In the sign-on message the error warning bit (EW) is set to "1". Nevertheless the error counters are cleared. The error warning bit of the sign-on message must be ignored.

Because the priority of a SLIO message can not be changed (fixed identifier), the P82C150 delays the transmission of a further pending message for three bit times after each successful transmission (special 'Suspend Transmission'). This enables other CAN nodes with lower priority to transmit before a SLIO node starts a new transmission.

The fixed acceptance filter for each P82C150 in the system defines a bundle of messages (sign-on message, data message to SLIO, data message from SLIO and remote frames) for that specific SLIO. Not more than 16 such 'bundle messages' (corresponds to the number of SLIO nodes) can exist in a CAN network and each bundle represents all messages for one SLIO node. It is not possible to define messages for functions e.g. with separate identifiers for 'digital port functions' and 'analog functions', which are sent to more than one SLIO node.

Only one host may send messages to that SLIO node it is controlling (except calibration messages). Messages from different hosts, if they are transmitted simultaneously, could be superimposed as they differ first after the arbitration field - in the data fields - and cause errors. Calibration messages have one special identifier, which is accepted by all P82C150s in a network. It does not matter, if the calibration messages are sent by one host to all SLIOs or if each host sends the calibration messages to its own SLIOs only. As long as the calibration messages contain the same data, a superimposition does not lead to errors.

6.2 Network Management

6.2.1 Calibration Server

The initial calibration of all P82C150s and holding them alive with a regular recalibration is one of the important tasks in a network. If the same bit stream for the calibration is used throughout the network for all nodes equipped with a P82C150, each host may calibrate its own SLIO nodes (Fig. 21 case 3), as errors are not produced, even in case the hosts would transmit simultaneously. If one host has been set into the 'bus-off' state or is not more available for one reason or other, the second host, sending calibration messages to its own SLIO nodes, holds also the SLIO nodes of the first one alive.

In order to reduce the bus load it is recommended to assign the calibration task to one normal node (host node, crystal-operated) in the network. This node is then acting as a **calibration server** (Fig. 21 case 1). This solution has the disadvantage, that if the calibration server runs into severe problems and perhaps is switched into the 'bus-off' state, all SLIO nodes will be taken out of the communication process due to the missing calibration messages. As every CAN node may listen to any message on the bus and use the information for its own purpose, another normal node (crystal-operated) may listen to the calibration messages and take over the task, if the calibration messages fail to be transmitted after a certain time (Fig. 21, case 2). With such a feature implemented in the network management the redundancy for keeping the SLIO nodes alive has been recovered and the bus load is reduced.

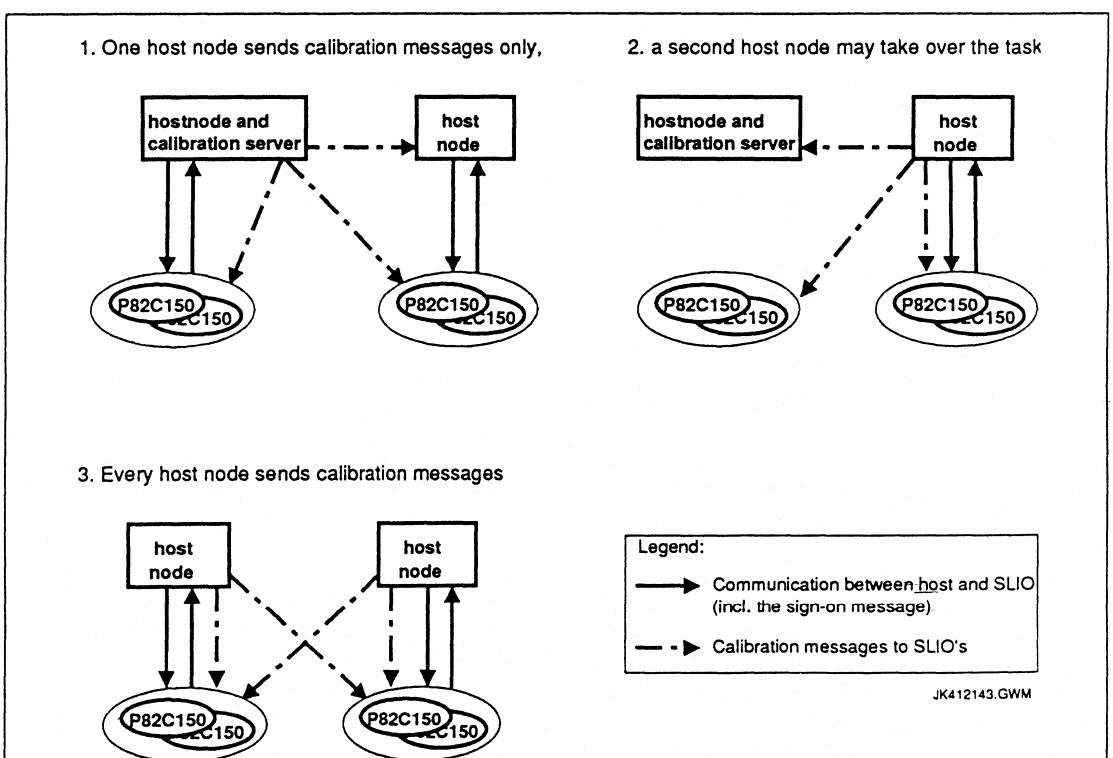


Fig. 21 SLIO communication; a calibration server in the network

6.2.2 Hot-Plugging of SLIO Nodes

In some applications it is necessary to allow for 'hot-plugging' of CAN nodes, which means that nodes can be switched on and off or taken physically out of the network without disturbing the communication in the network. The calibration procedure, which ends with the transmission of the sign-on message, is an instrument which may be used in a network management for this purpose.

If a calibration message does not reach a certain SLIO node, the host must not necessarily be informed (as long as the messages are acknowledged by other nodes). Thus SLIO nodes may be physically taken out, switched off or disconnected from the communication on the bus (e.g. due to a malfunctioning of bus lines). In the latter case the host is even sure that the P82C150 does not disturb the communication, as it will have entered the sleep mode after having tried - without success - to calibrate its bit time in the other bus modes. All its output drivers will be switched off.

The host will learn at the reception of a sign-on message from a SLIO node, that this node has been disconnected and can react in an appropriate way again. The sign-on message, which is sent by the P82C150 only after a successful calibration of its local bit timing after reset or bus mode change, is set up as a normal data message to the host transmitting the content of the input data register, but with the status bit RSTD set to '1' (see Fig. 20 and Table 5). Thus it is easily distinguished from all other data messages from the P82C150. The sign-on message indicates to the host, that a SLIO node had lost calibration due to some reason or other or had been 'bus-off' since the last message, which had been sent to that node. This 'lost&found' node needs an initialization of its internal data registers for further proper operation.

In order to be able to calibrate 'lost&found' nodes again the strategy recommended in chapter 5.4 should be implemented in the network management.

6.3 Summary of Communication Conditions

- Who may communicate with whom in a network containing SLIO nodes?
  - A P82C150 should receive data messages (data frames) from one single host only.
  - A host node may transmit data messages and remote frames to several P82C150s.
  - A crystal-operated node may transmit calibration messages to all P82C150s in the network.
  - It is allowed, that several crystal-operated nodes transmit (the same) calibration messages.
  - Every normal node may transmit remote frames to each P82C150 in the network.
  - Every normal node may receive data messages and sign-on messages sent by all P82C150s in the network and use the received information for its own purpose.
  - Every normal node may receive the calibration message and use it for its own purpose.
  - A direct message exchange between P82C150s is **not** possible.
- Calibration of the local bit timing of the P82C150
  - An initial calibration of the bit timing is necessary.
  - A regular recalibration of the bit timing is necessary (e.g. one calibration message every 3800 bit times).
- The bit rate in a network with P82C150 nodes is restricted, as described in the data sheet [1].
- The location of the sample point and the size of the resynchronization jump width of the other CAN nodes have to match that of the P82C150, as described in the data sheet [1]. See also chapter 7.3.
- The maximum distance between the outermost bus nodes is reduced, compared to networks with 'conventional' CAN controllers (see chapter 7.4).
- If CAN controllers according to the CAN specification V1.1 (e.g. 82C200 V0) are used together with SLIOs, a more stable power supply voltage for the SLIOs is required (refer to the data sheet [1]).

7. BIT TIMING AND BUS LENGTH

The SLIO P82C150 represents an easy and cost-effective way to implement a CAN node. The main reason for this is that the CAN controller does not need any on-chip or on-board software. It also does not need an own crystal oscillator, as it has a built-in clock generator and its local bit clock is automatically calibrated by the received bit stream. Any bit rate between 20 kbit/s and 125 kbit/s can be used. The calibration procedure is described in chapter 4.2 on page 19 of this application note.

7.1 Influences on the Clock Accuracy

This automatic bit clock calibration gives great flexibility considering the bit rate being used. A SLIO node can be hooked onto the bus without having its bit timing registers set - the only adjustments possible apply to the identifier bits.

However this calibration mechanism gives only limited accuracy. The main reasons for this are the following:

- The clock stability of the node sending the calibration messages must be within 0.1%. In calculating the SLIO node's absolute clock accuracy this must always be included.
- The calibration mechanism does not continually monitor the bit stream for adjusting the clock frequency, but relies on particular messages which are required to be sent by crystal-operated host nodes only. During a calibration message the P82C150 determines the time between two recessive-to-dominant transitions which have to be 32 bit periods apart. The tolerance of this calibration process also affects the overall accuracy.
- Between two calibrations the stability of the SLIO's clock frequency can basically be influenced by temperature and supply voltage changes. The effect of temperature changes however usually can be neglected because of the short time between two calibrations: even at the lowest bit rate of 20 kbit/s and a calibration occurring every 8000 bits the interval is as short as 400 ms.
- The main source for clock frequency changes therefore are supply voltage variations. In order to keep the overall clock accuracy within the required limits of 1.58%[6] the voltage must be kept constant[7]. This refers to short-term changes (from one calibration to the next one), the nominal voltage is not that critical in this case.

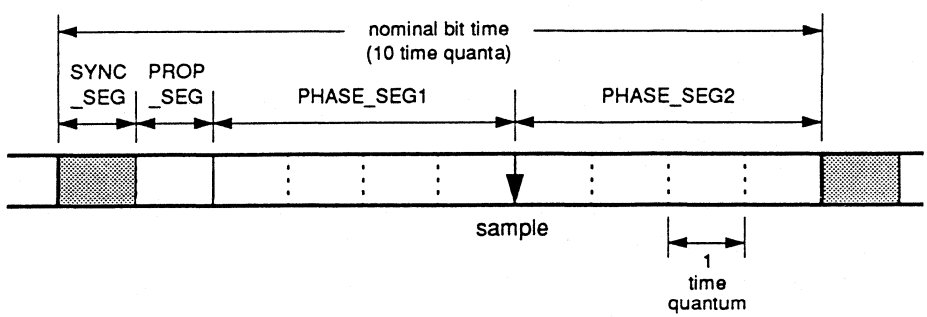


Fig. 22 Bit timing optimized for oscillator tolerance for P82C150

7.2 Bit Time Optimized for Tolerance

Since each node runs on its own clock, certain clock frequency differences are inevitable (even between crystal-operated nodes). Apart from the P82C150 and its calibration mechanism, a node generally is unable to detect a frequency offset, but can only notice the integral over time of this offset: a phase difference between its

6. More on oscillator tolerance including a derivation of this value can be found in the CAN specification [2].
7. For exact data on the required stability of the supply voltage refer to the data sheet of the P82C150 [1].

own internal bit clock and the bit rate on the bus. In order to realign its clock phase to the bus the CAN specification offers the process of resynchronization. A node can shorten or lengthen a bit time by up to four time quanta to get its synchronization segment (the first segment of a bit) back in phase with the transition on the bus. With a bit stuffing length of 5 a recessive-to-dominant transition on the bus can be expected at least every 10 bits during normal data transmission. Between crystal-operated nodes the amount of phase difference that can accumulate during these 10 bits is so small that a resynchronization jump width (SJW) setting of 1 is sufficient for these nodes.

If a SLIO is used in the network, the accumulated phase difference between two transitions can be much larger. A SLIO has set its SJW to 4. Moreover the bit time is divided into 10 time quanta only, so SJW amounts to 40% of the bit time. This results in a bit timing with the highest possible oscillator tolerance for CAN. Fig. 22 shows the bit timing as it is implemented in the P82C150.

7.3 Bit Timing of different Nodes in a Network

According to the CAN specification [2] nodes in a CAN network may run on clocks having up to 1.58% of frequency deviation. This permits devices like the P82C150 which run a non-crystal-operated clock to take part in the communication in the network.

If the SLIO P82C150 is used all other nodes in the network should have the same bit timing as the P82C150 in order to maintain a safe link. When programming a node the difference between the protocol definition used so far and the implementation definition of the bit timing should be noticed (see Fig. 23). The length of a bit (NBT, Nominal Bit Time) is determined by programming TSEG1 and TSEG2 (see Fig. 23 for definitions):

$$NBT = TSEG1 + TSEG2 + 1$$

The time when a node samples the bus is at the beginning of TSEG2. Therefore the length of TSEG2 determines the position of the sample point.

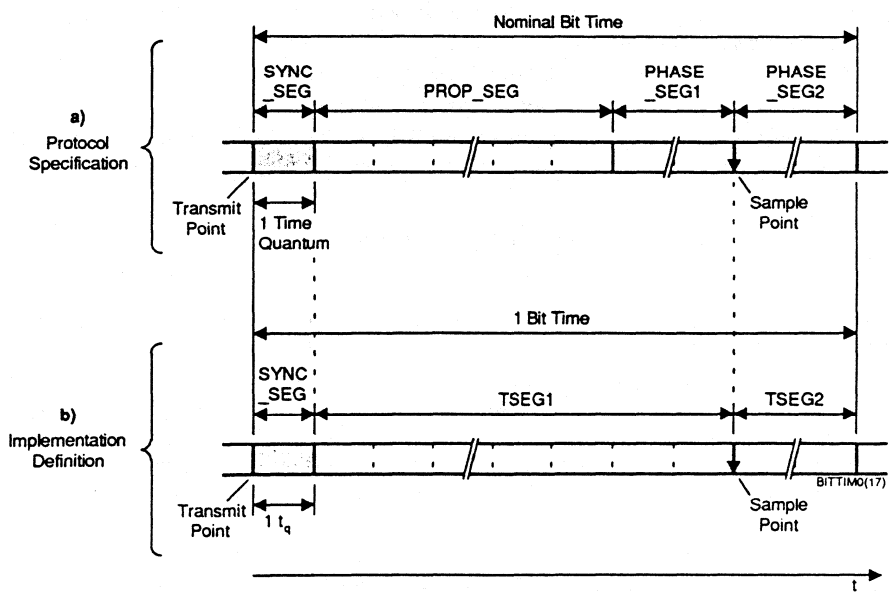


Fig. 23 Structure of a CAN bit time

In programming a node for the communication with a SLIO the bit time parameters should be set according to Table 6:

Table 6 Bit time parameters for communication with SLIOs P82C150

Parameter	value
bit rate	between 20 kbit/s and 125 kbit/s, set baud rate prescaler BRP appropriately
synchronization jump width (SJW)	4 time quanta
sampling	0, the bus is sampled once
time segment 1 (TSEG1)	5 time quanta
time segment 2 (TSEG2)	4 time quanta

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bus Timing Register 0	SJW.1	SJW.0	BRP.5	BRP.4	BRP.3	BRP.2	BRP.1	BRP.0
for SLIO communication:	*1*	*1*	*	*	*	*	*	*
Bus Timing Register 1	SAM	TSEG2.2	TSEG2.1	TSEG2.0	TSEG1.3	TSEG1.2	TSEG1.1	TSEG1.0
for SLIO communication:	*0*	*0*	*1*	*1*	*0*	*1*	*0*	*0*

* *... value depends on oscillator frequency and desired bit rate*

BRP	Baud Rate Prescaler	$t_q = 2\,t_{CLK}(32\,BRP.5 + 16\,BRP.4 + 8\,BRP.3 + 4\,BRP.2 + 2\,BRP.1 + BRP.0 + 1)$ (t_{CLK} = time period of the oscillator of the CAN controller)
SJW	Synchronization Jump Width	$t_{SJW} = t_q(2\,SJW.1 + SJW.0 + 1)$
SAM	Sampling	SAM = 1: 3 samples are taken SAM = 0: the bus is sampled once
TSEG1	Time Segment 1	$t_{TSEG1} = t_q(8\,TSEG1.3 + 4\,TSEG1.2 + 2\,TSEG1.1 + TSEG1.0 + 1)$
TSEG2	Time Segment 2	$t_{TSEG2} = t_q(4\,TSEG2.2 + 2\,TSEG2.1 + TSEG2.0 + 1)$

Fig. 24 Bus timing register layout of Philips CAN controllers

Fig. 24 shows the layout of the bus timing registers 0 and 1 of the Philips CAN controllers and gives the rules of how to program the individual bits.

Generally, nodes can have different bit timings. If all nodes are crystal-operated the only requirement for establishing a communication is, that the bit rate is the same throughout the network. Differences in TSEG2 and thus the position of the sample point only influence the maximum achievable bus length. If however a P82C150 is present in the network the synchronization jump width must be set to 40% of the bit time (4 out of 10 time quanta). Since the maximum value for SJW is 4 this requirement can only be met if the total number of time quanta in a bit is 10 (see Fig. 25).

Fig. 25 also shows that the requirement for compensating a maximum of oscillator tolerance is contrary to the requirement of achieving a maximum of bus length. Moreover the relative time left for propagation delay (bus length) increases with the number of time quanta per bit and with the sample point being positioned closer to the end of the bit time.

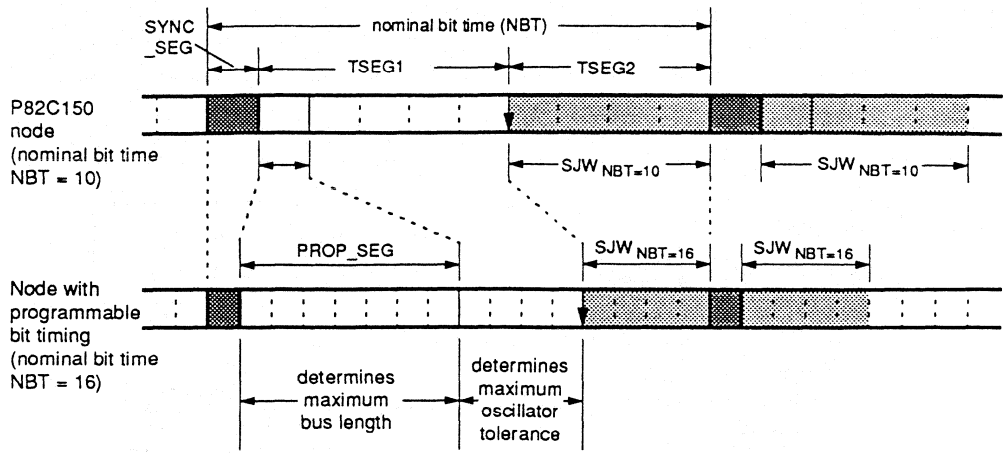


Fig. 25 SJW comparison

7.4 Bus Length with P82C150 Nodes

Due to the fact that the bit timing of P82C150 nodes is optimized for compensating oscillator tolerances only one time quantum is left for propagation delay compensation (PROP_SEG), see Fig. 25. The first time quantum (SYNC_SEG) of the bit time is reserved, because the accuracy of the resynchronization is always limited to one time quantum. The last eight time quanta (PHASE_SEG1 and PHASE_SEG2) are needed to cover the phase error that can have accumulated after a number of bits without resynchronization.

Although the bit timing is fixed and only one time quantum is intended for propagation delay compensation, the maximum achievable bus length can be increased if measures are taken to reduce the possible oscillator tolerance. This means that the resynchronization jump width SJW of 4 is not utilized fully which leaves more room for delay compensation. As was pointed out at the beginning of this chapter, clock frequency variations of the P82C150 are mainly due to changes in supply voltage. Therefore implementing a more stable power supply can increase the usable bus length.

The propagation delay t_{PROP} is the sum of all delays that a signal encounters when travelling from one node to another *and back* (see Fig. 26):

$$t_{PROP} = t_{CON,A} + t_{TRANS,A} + t_{TRANS,B} + t_{CON,B} + 2\,t_{BUS}$$

The abbreviations have the following meaning:

$t_{CON,A}$, $t_{CON,B}$	sum of input and output delay of CAN controller A, B
$t_{TRANS,A}$, $t_{TRANS,B}$	sum of transmit and receive delay of transceiver A, B
t_{BUS}	delay of bus cable (one way)

The allowed bus delay thus is

$$t_{BUS} = (t_{PROP} - t_{CON,A} - t_{CON,B} - t_{TRANS,A} - t_{TRANS,B}) / 2$$

or, if the same transceivers are used,

$$t_{BUS} = (t_{PROP} - t_{CON,A} - t_{CON,B}) / 2 - t_{TRANS}$$

With t_p [ns/m] being the specific line delay of the cable,
the maximum achievable bus length L is found by the formula

$$L = \frac{t_{BUS}}{t_p}$$

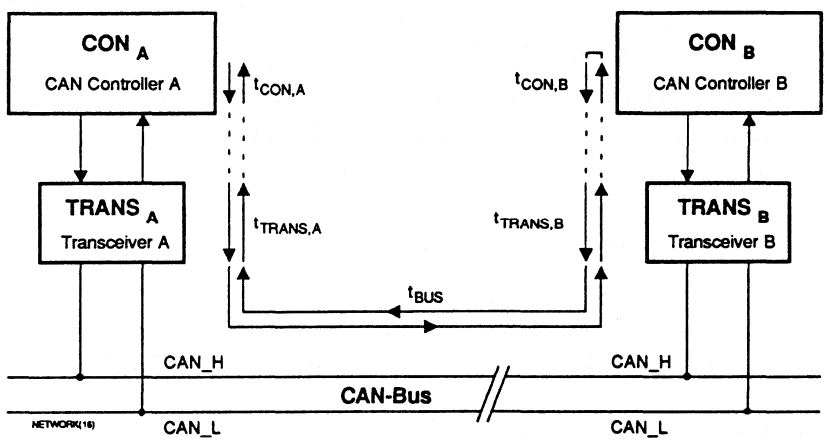


Fig. 26 Propagation delay in a CAN network

Sample bus length calculation

In the succeeding example the maximum bus length for a CAN network containing SLIOs is calculated. The calculation assumes the following maximum delay figures:

$t_{CON,A} = t_{HOST} = 60$ ns

$t_{CON,B} = t_{SLIO} = 60$ ns[8]

$t_{TRANS} = 170$ ns

$t_p = 5$ ns/m

At a bit rate of 100 kbit/s the length of the propagation segment is

$t_{PROP} = 1000$ ns

This gives a maximum bus length of

$$L = \frac{(1000 - 60 - 60)\ \text{ns}/2 - 170\ \text{ns}}{5\ \text{ns/m}}$$

$L = 54$ m

8. Refer to the data sheet of the P82C150 for exact delay data [1]

Optocouplers

Optocouplers can be used with SLIO nodes. For example they can be placed between the protocol controller and the transceiver (see Fig. 11 on page 17). They are used in pairs: the transmitted and the received signal both have to pass an optocoupler. Due to their extra delay these devices directly reduce the maximum achievable bus length.

If the delay of a *single* optocoupler is t_{OPTO}, using *one pair* of them in a node reduces the bus length by

$$L_R = \frac{t_{OPTO}}{t_p}$$

With a specific cable delay of t_p = 5 ns/m the achievable bus length is reduced by 1 m for every 5 ns of optocoupler delay, for example.

Instead of placing optocouplers between the transceiver and the controller, a galvanic isolation may also be done by placing isolating elements between the power supply of the application or the application inputs and the CAN controller. This has the advantage, that the achievable bus length is not reduced.

8. DIGITAL PORT FUNCTIONS

The P82C150 provides 16 digital I/O port pins. By means of several 16-bit-registers each pin can be individually configured, see Table 7.

Table 7 I/O Register map (digital outputs)

Register	Address	MSB	...	LSB
Data input register	0	DI15	...	DI0
Positive edge register	1	PE15	...	PE0
Negative edge register	2	NE15	...	NE0
Data output register	3	DO15	...	DO0
Output enable register	4	OE15	...	OE0

The data input register contains the logic levels of the port pins. Reading it by CAN bus is done by sending a remote frame or a data message addressing the data input register to the P82C150 which is answered by a data frame containing the contents of the data input register (see also Fig. 19 on page 27). If any bit of the positive or negative edge register is set, a change on any one of these selected pins will automatically send a data frame with the contents of the data input register. Data intended to be output is loaded into the data output register. However, it is output only on those pins whose corresponding bits are set to '1' in the output enable register.

Several port pins have additional functions: they can also be used as analog I/O pins or they monitor the output of the built-in comparators, see Fig. 27. If these ports are used as digital I/O the additional functions must be disabled: the bits M3 ... M1 and SW3 ... SW1 of register 5 (analog configuration) and all bits of registers 6 and 7 (DPM1 and DPM2) must be set to zero, see Table 8.

Table 8 I/O Register map (analog outputs)

		MSB															LSB
Register	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Analog config.	5	ADC	OC3	OC2	OC1	0	M3	M2	M1	SW3	SW2	SW1	0	0	0	0	0
DPM1	6	DP9	DP8	DP7	DP6	DP5	DP4	DP3	DP2	DP1	DP0	0	0	0	0	0	0
DPM2	7	DQ9	DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	0	0	0	0	0	0
A/D	8	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	0	0	0	0	0	0

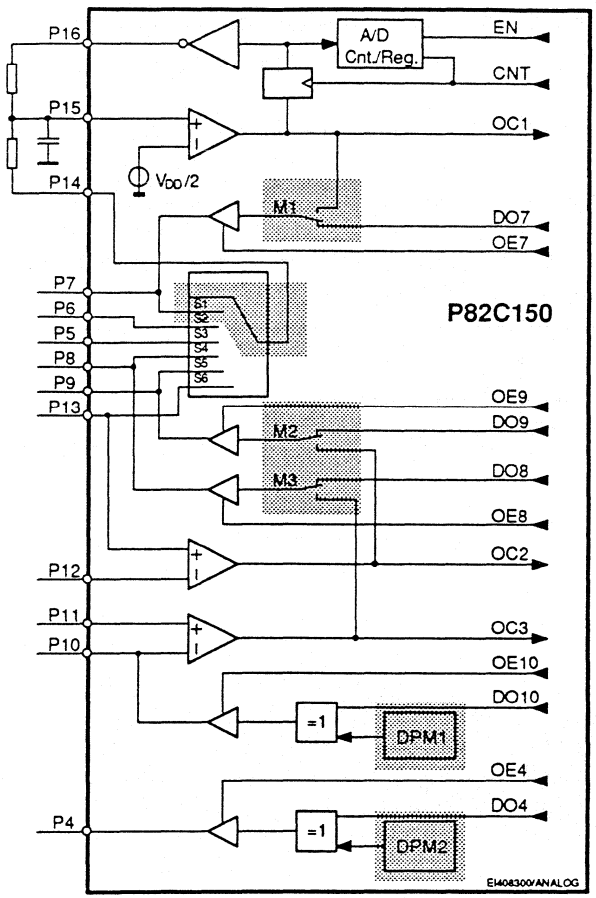


Fig. 27 Additional functions to be disabled for digital I/O

9. ANALOG PORT FUNCTIONS

Besides functioning as digital I/O ports (chapter 8) the port pins may be used for several analog functions.

- Input comparators for analog signals (differential or single ended).
  Application examples:
  - Minimum or maximum supervision of analog signals [1].
  - Window comparator for an analog signal [1].
- Digital-to-Analog converters using the algorithm of the distributed pulse modulation (DPM).
- Analog-to-Digital converter.
  One separate input comparator is available for the A/D conversion task. An implemented multiplexer allows for the extension to a maximum of 6 multiplexed A/D-input channels.

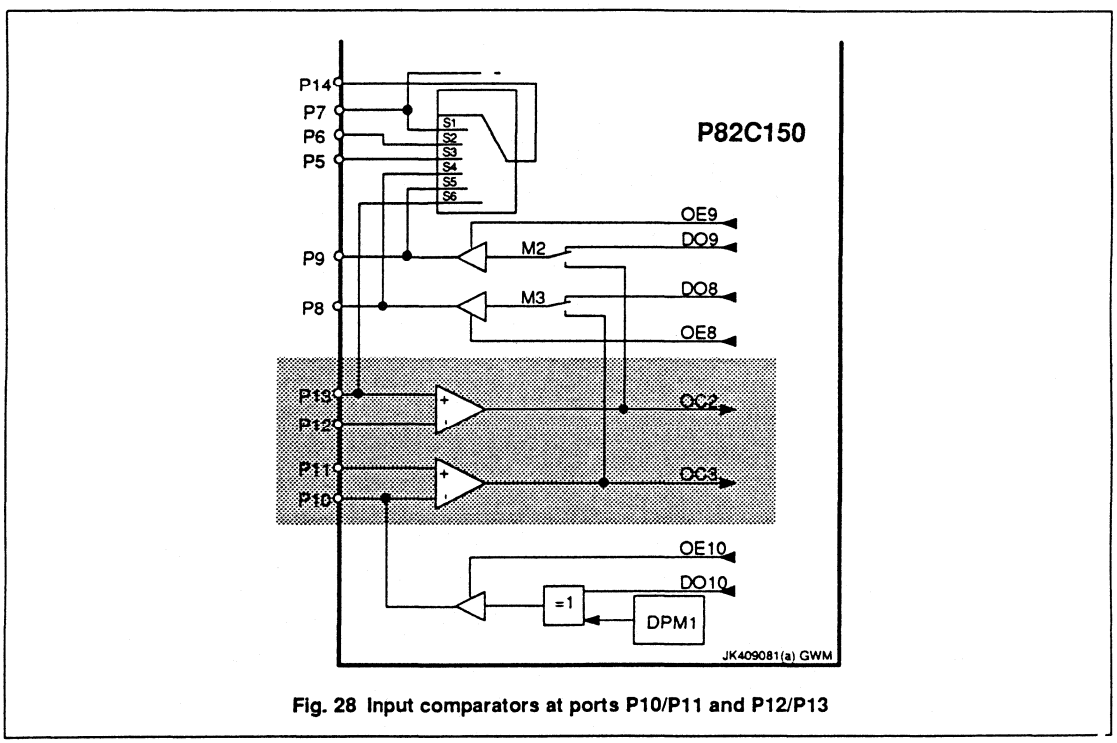


Fig. 28 Input comparators at ports P10/P11 and P12/P13

Table 9 I/O register content if both input comparators are used

I/O Register	Addr.	I/O Register Content															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Output enable	4	OE(n)															
		X	X	0	0	0	0	X	X	X	X	X	X	X	X	X	X

(X = not relevant for this configuration)

9.1 Comparators

The P82C150 provides two general purpose comparators (see Fig. 28). The inputs are provided at the ports P10/P11 and P12/P13. Table 9 shows the setting of the I/O register control bits, if the comparators are used in an application. The outputs of the ports P10 through P13 must be disabled, which means that P10 can not serve as DPM1 output at the same time either.

For the electrical characteristics of the input comparators see the data sheet [1].

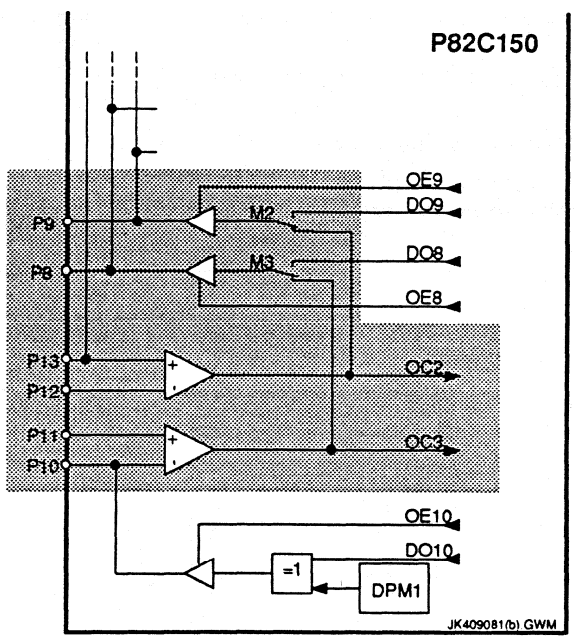


Fig. 29 Comparator outputs connected to ports P8 and P9

Table 10 I/O register content for connecting the comparator outputs to ports P8 and P9

I/O Register	Addr.	I/O Register Content 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Output enable	4	OE(n) X	X	0	0	0	0	1	1	X	X	X	X	X	X	X	X
Analog configuration	5	ADC X	OC3 X	OC2 X	OC1 X	0	M3 1	M2 1	M1 0	SW3 X	SW2 X	SW1 X	0	0	0	0	0
Positive edge	1	PE(n) X	X	X	X	X	X	0/1	0/1	X	X	X	X	X	X	X	X
Negative edge	2	NE(n) X	X	X	X	X	X	0/1	0/1	X	X	X	X	X	X	X	X

(X = not relevant for this configuration, 0/1 = depends on application)

The comparator output is switched to HIGH, if input 'plus' > input 'minus'. In sleep mode the output is forced HIGH regardless of the input levels. The logical result of the comparison is placed into the analog configuration register (bits OC3 and OC2) and may be read by addressing this register in a data frame on the CAN-bus.

The logical result of the comparison may be switched to an output port (P8 for OC3 and P9 for OC2) for being used in the connected application (Fig. 29). Table 10 shows the setting of the I/O register control bits for this case (M2 and M3 in the analog configuration register is set to '1'). Furthermore this opens the possibility of reading the comparator output values via the digital input port (data input register) and being able to use the event capture facility of the ports for an automatic transmission of the input data via the CAN-bus, if the PE8/NE8 and PE9/NE9 are set properly in the I/O registers 1 (positive edge trigger) and 2 (negative edge trigger).

9.2 Distributed Pulse Modulation (DPM) Outputs

9.2.1 General Description of the DPM

The P82C150 provides two output channels (DPM1 at port P10 and DPM2 at port P4, Fig. 32) for converting a 10 bit digital value into a quasi-analog output signal - 'Distributed Pulse Modulation'. The function of the modulator may be explained with the help of Fig. 30, which shows a simplified functional block diagram of a DPM-circuit

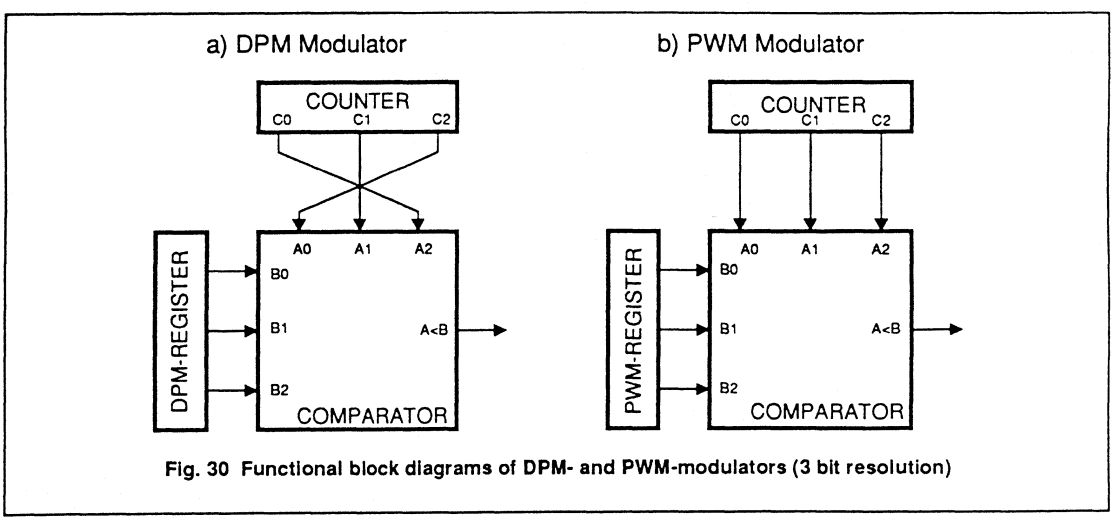


Fig. 30 Functional block diagrams of DPM- and PWM-modulators (3 bit resolution)

and a PWM-circuit with a resolution of 3 bit. The value to be converted (value 'B') is compared with the output (PWM) or modified output (DPM) (value 'A') of a continuous running counter. If the value 'A' is smaller than the value 'B', the pulse output is switched HIGH else it stays LOW. The resulting output pulses are given in Fig. 31. If the value to be converted ('B') is increased continuously, the PWM generates a pulse with a growing mark to space ratio, whereas the DPM generates more equally spaced pulses. Further information may be found in [7].

The repetition time of the pulse stream (one DPM cycle) is defined by the resolution of the modulator and the width of a single pulse, which again is related to the clock frequency of the counter. The DPM of the P82C150 has a resolution of 10 bit and the width of a single pulse is equal to four cycles of the internal oscillator clock. Thus the repetition time may be calculated from the formula:

$$T_{DPM} = 1024 \times 4\, T_{CLK}$$

Refer to [1] for more information about the electrical characteristics.

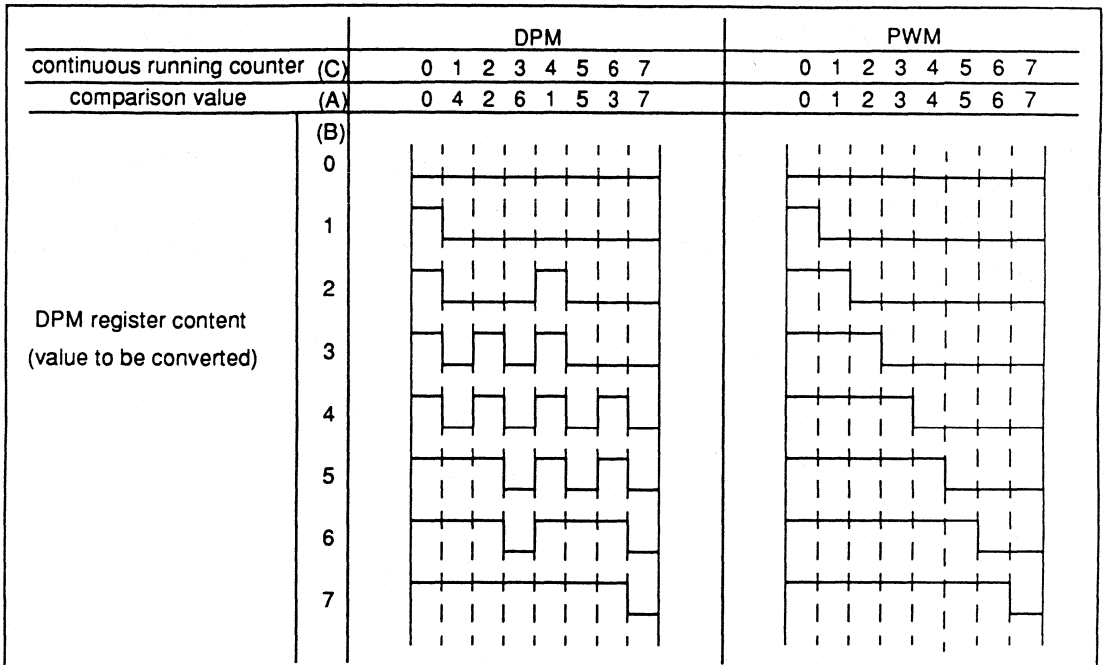


Fig. 31 DPM- and PWM- output signals (3 bit resolution)

In order to use the quasi-analog output signal of the DPM in an application the I/O control registers have to be set according to the information given in Table 11. The output enable bits have to be set for port P4 and P10.

The pulse trains at the outputs P4 and P10, which are generated from the latched DPM value, are inverted, if the corresponding bits in the data output register (DO4 and DO10) are set to '1', as may be seen from the logic diagram given in Fig. 32.

If the DPM1 output is used, the general comparator (OC3), which has its input 'minus' connected to P10, can not be used.

9.2.2 Digital to Analog Conversion using the DPM

The simplest way to generate an analog voltage from the quasi-analog signal is to apply an external low pass filter at the DPM output. One possible implementation would be a RC-filter of first order as indicated in Fig. 32.

Regarding the selection of the time constant (edge frequency) of this filter, a trade-off between minimizing the ripple voltage for maximum accuracy and minimizing the settling time has to be considered. The following examples are a guideline how to select the components.

Example 1:

- 10 bit accuracy; settling time <30 ms; a ripple voltage <5 mV_{pp} (<0,1%, which means less than the resolution) may be achieved by $\tau > 2 \times$ period of the pulse stream [7]:
- $\tau = R \times C \geq 4$ ms (recommended)
  - R = 1 kΩ; C = 4,7 µF or R = 10 kΩ, C = 470 nF

Example 2:

- 8 bit accuracy; settling time = 6 ms; a ripple voltage <20 mV_{pp} (<0,4%, which means less than the resolution):
- $\tau = R \times C \geq 1$ ms (recommended)
  - R = 1 kΩ; C = 1 µF or R = 10 kΩ, C = 100 nF

NOTE 1: If the output is loaded by a resistive load, the accuracy will be decreased due to the voltage drop across the series resistor. In these cases a low value for the series resistor should be chosen. However, it is recommended to provide a minimum series resistor of 1 kΩ for protection.

NOTE 2: The external RC-filter should be placed close to the corresponding DPM output pin in order to minimize the radiated emission of this output.

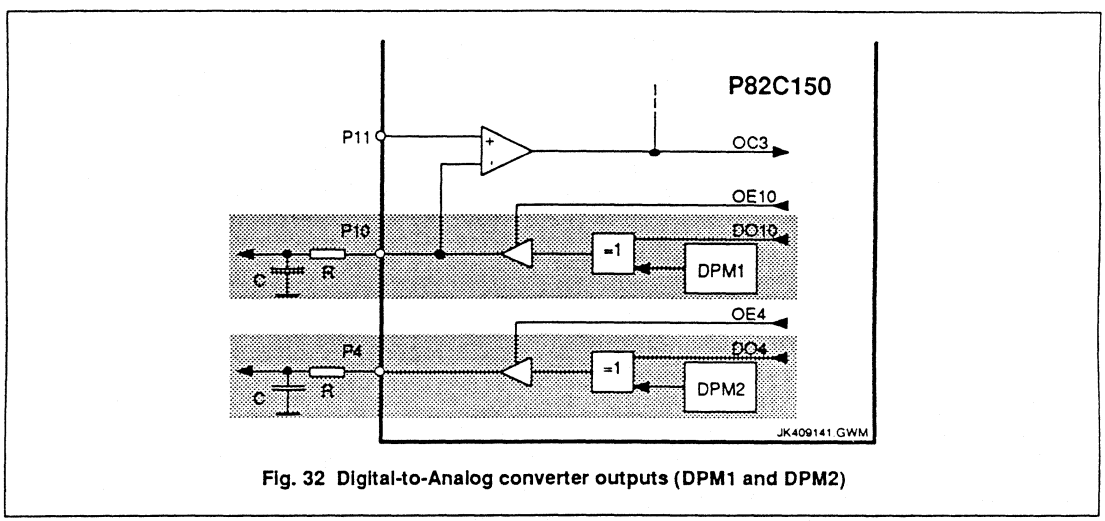


Fig. 32 Digital-to-Analog converter outputs (DPM1 and DPM2)

Table 11 I/O register content if using the D/A-converter outputs at ports P4 and P10

I/O Register	Addr.	I/O Register Content															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Output enable	4	OE(n)															
		X	X	X	X	X	1	X	X	X	X	X	1	X	X	X	X
Analog configuration	5	ADC	OC3	OC2	OC1		M3	M2	M1	SW3	SW2	SW1					
		X	X	X	X	0	X	X	X	X	X	X	0	0	0	0	0
DPM1 or DPM2	6 or 7	DP.. or DQ.. (= current digital value)															
		Dx9	Dx8	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	0	0	0	0	0	0
Data output	3	DO(n)															
		X	X	X	X	X	0/1	X	X	X	X	X	0/1	X	X	X	X

(X = not relevant for this configuration

DO(n) = 0: DPM output is not inverted, DO(n) = 1: DPM output is inverted)

9.2.3 Generation of Clock Pulses using the DPM-Outputs

The DPM-outputs may also be used as clock outputs in systems, where the connected application needs an external clock e.g. for driving a display. Not all digital values of the DPM-register content are qualified for such an application as not all generated pulse streams do have equally spaced pulses. Table 12 gives suitable values together with the generated frequencies. The values in the right part of the table may also be achieved by inverting the DPM-output by setting the corresponding data output bits in the control register (address 3).

Table 12 Generated clock frequencies for different DPM values

	Clock			Clock	
DPM-value	**Frequency**	**mark-to-space ratio**	**DPM-value**	**Frequency**	**mark-to-space ratio**
0000 0000 01	f_{CLK}/ 4096	1 : 1023	1111 1111 11	f_{CLK}/ 4096	1023 : 1
0000 0000 10	f_{CLK}/ 2048	1 : 511	1111 1111 10	f_{CLK}/ 2048	511 : 1
0000 0001 00	f_{CLK}/ 1024	1 : 255	1111 1111 00	f_{CLK}/ 1024	255 : 1
0000 0010 00	f_{CLK}/ 512	1 : 127	1111 1110 00	f_{CLK}/ 512	127 : 1
0000 0100 00	f_{CLK}/ 256	1 : 63	1111 1100 00	f_{CLK}/ 256	63 : 1
0000 1000 00	f_{CLK}/ 128	1 : 31	1111 1000 00	f_{CLK}/ 128	31 : 1
0001 0000 00	f_{CLK}/ 64	1 : 15	1111 0000 00	f_{CLK}/ 64	15 : 1
0010 0000 00	f_{CLK}/ 32	1 : 7	1110 0000 00	f_{CLK}/ 32	7 : 1
0100 0000 00	f_{CLK}/ 16	1 : 3	1100 0000 00	f_{CLK}/ 16	3 : 1
1000 0000 00	f_{CLK}/ 8	1 :1			

f_{CLK} = system clock frequency [1]

9.3 Analog-to-Digital Converter

9.3.1 General Description of the ADC

The P82C150 provides one Analog-to-Digital converter on-chip ('bit-stream' or 'sigma-delta' conversion).

A 'bit-stream' converter (Fig. 33) includes a feedback loop consisting of

- an adder, which subtracts the output signal from the input signal to determine the approximation error
- a loop filter (e.g of 1st order, integrator), which extracts the low frequency content of the approximation error
- a 1-bit quantizer (comparator) and a sampling flipflop, which stores the comparator output for one period of the sampling clock
- a 1-bit Digital-to-Analog converter (e.g. an inverter), which converts the 1-bit data stream into a quasi analog signal to be compared with the analog input signal.

This type of converter produces a 1-bit code, which is converted to a n-bit code by the digital decimation filter.

As indicated in Fig. 33, the comparator and the 1-bit DAC of the ADC of the P82C150 are on-chip and the adder and the integrator are to be connected externally (see also Fig. 34). The analog input signal is fed via the adder and integrator (external RC-combination) to the input of the comparator at port 15. The output of the comparator is clocked into a flipflop (CNT = f_{CLK}/4 with f_{CLK} = frequency of the internal oscillator) and fed back via an inverter (1-bit DAC and inversion for the subtraction) to the output port P16, which is connected to the adder.

The behaviour of the feedback loop may be explained with an example:

The start-up situation may be: A small analog input signal is applied (near to 0 V).

Assuming that a voltage above the upper switch-over voltage of the comparator is present at port P15, then the output at P16 is set to a voltage near to 0 V (Fig. 35). Now both the input and the feedback signal are discharging

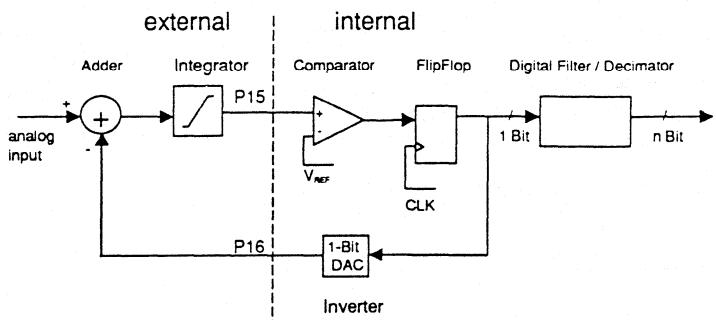


Fig. 33 Principle of 'bit-stream' conversion

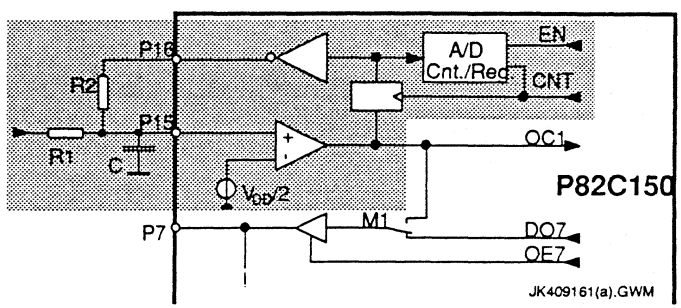


Fig. 34 Analog-to-Digital converter of P82C150

the capacitor. As long as the voltage at P15 stays above the lower switch-over voltage of the comparator, a '1' is clocked into the flipflop, holding P16 'LOW'. If the lower switch-over voltage is reached, the comparator output switches to 'LOW'. With the next active edge of the sampling clock the flipflop will store a '0' and the output P16 will be switched to 'HIGH' (a voltage near to V_{DD}). Now the capacitor will be loaded and the voltage at P15 increases again. A '0' will be stored as long as the voltage stays below the upper switch-over voltage of the comparator. When the upper switch-over voltage is reached, the comparator output is set to 'HIGH' and the port output P16 is switched to 0 V again. Here the cycle starts again.

This example clarifies that the voltage at the output P16 has to compensate fully the low voltage introduced by the input signal in order to being able to increase the voltage at port P15. The same applies for a high input voltage, but here the voltage at the output of P16 has to be low enough for the compensation.

The generated bit stream is fed to a counter, which counts the 'HIGH' states of the flipflop during a period of 1024 clocks, which corresponds to a duration of 1024×4 t_{CLK} (t_{CLK} = repetition time of the internal oscillator). The content of the counter/register corresponds to the achieved digital value.

A conversion is started either by setting the bit 'ADC' in the 'analog configuration register' to '1' or by reading the 'A/D register'. Upon receiving a conversion request, the P82C150 is waiting for the current cycle of 1024 clocks to be finished. Before enabling the counter another cycle of 1024 clocks is waited for to allow for settling of the analog input voltage. This is important, if the analog voltage has been switched through to the input of the ADC via the multiplexer by setting the switches SW1...SW3 together with the conversion request bit (ADC).

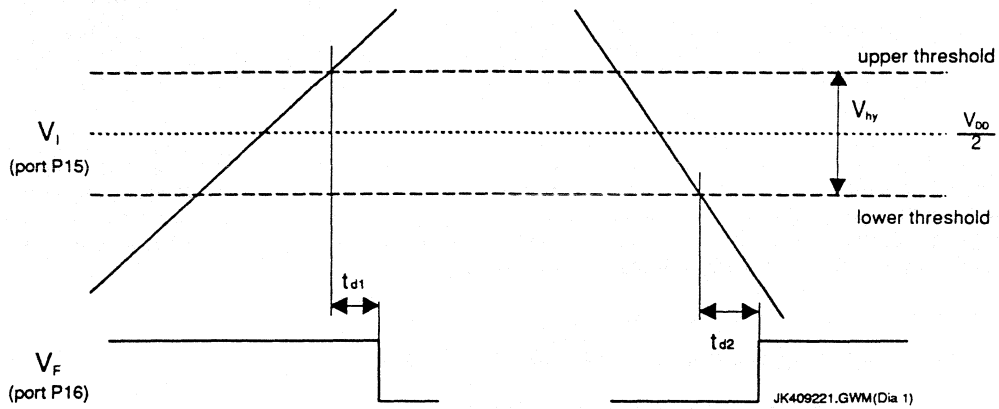
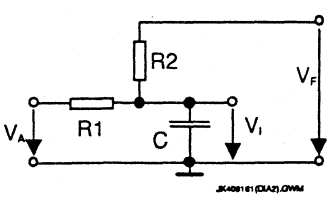


Fig. 35 ADC: switch-over points of the input comparator

9.3.2 The external Circuit of the ADC

The external circuit is shown in Fig. 34 together with the internal circuit closing the loop for the A-to-D conversion process. Whereas Fig. 36 shows the external circuit only, together with charging and discharging equations for the capacitor if the loop is opened.



Charging the capacitor (V_F switches from V_{FOL} to V_{FOH}):

$$v_I(t) = \frac{R1 \times R2}{R1 + R2}\left(\frac{V_{FOH}}{R2} + \frac{V_A}{R1} - \frac{1}{R2}(V_{FOH} - V_{FOL})\, e^{-t/\tau}\right)$$

Discharging the capacitor (V_F switches from V_{FOH} to V_{FOL}):

$$v_I(t) = \frac{R1 \times R2}{R1 + R2}\left(\frac{V_{FOL}}{R2} + \frac{V_A}{R1} + \frac{1}{R2}(V_{FOH} - V_{FOL})\, e^{-t/\tau}\right)$$

V_A: analog input voltage

$V_I, v_I(t)$: input voltage at port P15

V_F, V_{FOL}, V_{FOH}: output voltage at port P16 (LOW, HIGH)

$$\tau = \frac{R1 \times R2}{R1 + R2} \times C$$

Fig. 36 Open loop equations for the ADC input voltage

From the equations given in Fig. 36 V_{Imin} and V_{Imax} are calculated for $t \rightarrow \infty$:

$$V_{Imin} = \frac{R1 \times R2}{R1 + R2}\left(\frac{V_{FOL}}{R2} + \frac{V_{Amin}}{R1}\right) \quad \text{and} \quad V_{Imax} = \frac{R1 \times R2}{R1 + R2}\left(\frac{V_{FOH}}{R2} + \frac{V_{Amax}}{R1}\right) \qquad (1)$$

V_{Imin} is achieved with V_{Amin} and V_{Imax} is achieved with V_{Amax}.

The range of the input voltage V_A (analog voltage to be converted) is restricted due to two conditions:

1. The voltage level at the input of the ADC (port P15) must not exceed the 'DC input voltage on any pin' of the 'limiting values' given in the data sheet [1]. This leads to the following two relations:

   $V_{Imin} \geq 0V$ and $V_{Imax} \leq V_{DD}$

   During operation the voltage at the input of port P15 is controlled by the feedback loop to approximately $V_{DD}/2$ i.e. it will not exceed the limiting values. But if the loop is opened — as it happens during sleep mode, where the internal oscillator is stopped — the worst case value for V_I has to be considered. The output voltage at port P16 (the feedback voltage V_F) is either ~0 V (V_{FOL}) or ~V_{DD} (V_{FOH}) dependent on the last cycle of the ADC-operation before the oscillator did stop.

   With the above range for V_I, V_{FOL} and V_{FOH}
   the input range for V_A is calculated from equation (1): $0V < V_A < V_{DD}$ (2)

   The input range for the voltage V_A is independent of the value of the resistors.

2. For a proper operation of the ADC, the voltage V_I at port P15 must at least reach the upper and lower threshold voltage (see Fig. 35) during the charging and discharging cycles. This condition leads to the following relations:

   Under the worst case condition for **charging** the capacitor ($V_F = V_{FOH}$ and $V_A = V_{Amin}$) the relation

   $V_{lend}(t \rightarrow \infty) > \frac{V_{DD} + V_{hy}}{2}$ must be fulfilled (the output port P16 is set to 'LOW' again: $V_F = V_{FOL}$).

   Under the worst case condition for **discharging** the capacitor ($V_F = V_{FOL}$ and $V_A = V_{Amax}$) the relation

   $V_{lend}(t \rightarrow \infty) < \frac{V_{DD} - V_{hy}}{2}$ must be fulfilled (the output port P16 is set to 'HIGH' again: $V_F = V_{FOH}$).

   (V_{hy} = hysteresis of the switch-over point of the input comparator, see Fig. 35).

   With the above relations for V_I and the mentioned worst case conditions the following relation for V_A is received from the equations given in Fig. 36 on page 46:

$$\left(\frac{R1 + R2}{2 \times R2}(V_{DD} + V_{hy}) - \frac{R1}{R2}V_{FOH}\right) < V_A < \left(\frac{R1 + R2}{2 \times R2}(V_{DD} - V_{hy}) - \frac{R1}{R2}V_{FOL}\right) \quad (3)$$

With the ratio R1/R2 = 1 a conversion is achieved, which best transforms the voltage range of V_A into the whole range of achievable digital values, where 1 digital step corresponds to ΔV_A ~5 mV.

With $\frac{R1}{R2} = 1$ and $V_{FOH} = V_{DD} - \Delta V_{FOH}$ and $V_{FOL} = \Delta V_{FOL}$

the relation (3) is reduced to: $(V_{hy} + \Delta V_{FOH}) < V_A < (V_{DD} - (V_{hy} + \Delta V_{FOL}))$

which is even more restrictive than the relation (2). More information on the characteristics of the input port P15 if used for the ADC and of the output port P16 is given in the data sheet [1].

Ratios >1 (R1 > R2) would allow for a wider range of the analog input voltage V_A, but according to the previous mentioned restriction (2) only the range between ~0 V and ~V_{DD} can be converted. So the analog voltage has to be transformed into the allowed range of V_A before it may be applied to the external circuit of the ADC.

Ratios <1 (R1 < R2) result in a reduced voltage range of V_A according to the relation (3).

Example 1

If a ratio of R1/R2 = 1/2 is chosen the achievable range for V_A is calculated from (3) to

$$\frac{V_{DD} - V_{hy} - 2\Delta V_{FOH}}{4} + V_{hy} + \Delta V_{FOH} < V_A < (V_{DD} - (V_{hy} + \Delta V_{FOL})) - \frac{V_{DD} - V_{hy} - 2\Delta V_{FOL}}{4}$$

Compared with the result for R1/R2 = 1 the voltage range for V_A is reduced with ~V_{DD}/4 at both ends.

The resulting range for V_I, which determines the digital representation of the analog signal is calculated from (1) to:

$$V_{Imin} = \frac{V_{DD} + 3V_{hy} + 2\Delta V_{FOH} + 2\Delta V_{FOL}}{6} \quad \text{and} \quad V_{Imax} = V_{DD} - \frac{V_{DD} + 3V_{hy} + 2\Delta V_{FOH} + 2\Delta V_{FOL}}{6}$$

As it is seen from this example, there exists a possibility of transforming a small range of V_A (<V_{DD}) into a wider range of V_I, but it is still smaller than V_{DD}.

Example 2

Given is a range for the input voltage of $1{,}5\ V < V_A < 3{,}5\ V$ which corresponds to

$$\frac{3}{10}V_{DD} < V_A < V_{DD} - \frac{3}{10}V_{DD}, \text{ if } V_{DD} = 5V.$$

Which ratio (R1/R2) have to be selected transforming the range into the widest possible range for V_I?

The ratio is calculated using the relations for V_{Amin} or V_{Amax} given in equation (3).

The result is $\frac{R1}{R2} = \frac{2V_{DD} + 5V_{hy}}{5(V_{DD} + V_{hy} + 2\Delta V_{FOH})} \approx \frac{2}{5}$ or $\frac{R1}{R2} = \frac{2V_{DD} + 5V_{hy}}{5(V_{DD} - V_{hy} - 2\Delta V_{FOL})} \approx \frac{2}{5}$

The resulting range for V_I, which determines the digital representation of the analog signal is calculated from (1) to:

$$V_{Imin} = \frac{3V_{DD} + 4\Delta V_{FOL}}{14} \approx 1{,}07V \quad \text{and} \quad V_{Imax} = V_{DD} - \frac{3V_{DD} + 4\Delta V_{FOH}}{14} \approx V_{DD} - 1{,}07V$$

Due to the equation (3) the small range of V_A cannot be transformed into the maximum range for V_I, which would make use of the whole range of possible digital values.

The value to be chosen for the resistors R1 and R2 depends on

- the leakage current of the input at port P15 (ADC comparator input) [1] and
- the ability of the analog source (V_A) to sink or source current.

It is up to the designer to decide upon this value for the resistors, as the trade-off between a low value for reducing the influence of the leakage current and a high value for reducing the load of the output of the analog source must be considered. The values given in the data sheet [1] are recommended as a first approach. If the analog multiplexer is used, the on-resistance of the analog switches has to be taken into account for the calculation of the external components.

NOTE: The components of the external circuit should be placed close to the corresponding pins they are connected to in order to avoid the introduction of noise.

9.3.3 Controlling the Operation of the ADC

If the ADC is used the digital output at port P15 must not be enabled. The settings of the I/O registers are shown in Table 13.

Table 13 I/O register content if the Analog-to-Digital converter is used

I/O Register	Addr.	I/O Register Content 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Output enable	4	OE(n) 0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Analog configuration	5	ADC X	OC3 X	OC2 X	OC1 X	0	M3 X	M2 X	M1 0	SW3 X	SW2 X	SW1 X	0	0	0	0	0

(X = not relevant for this configuration)

In case a node application needs to convert more than one analog signal a 6:1-analog multiplexer is added on chip (Fig. 37). The analog inputs are provided at the ports P5 through P9 and P13, the output at P14. For the use together with the ADC port P14 has to be connected to R1 of the external circuit of the ADC. The input for an analog voltage is selected by setting the analog switch bits 'SW1'...'SW3' of the 'analog configuration' register appropriately. For the coding see the data sheet [1]. For each port used for an analog input signal the digital output driver must not be enabled. The setting of the I/O control registers is shown in Table 14.

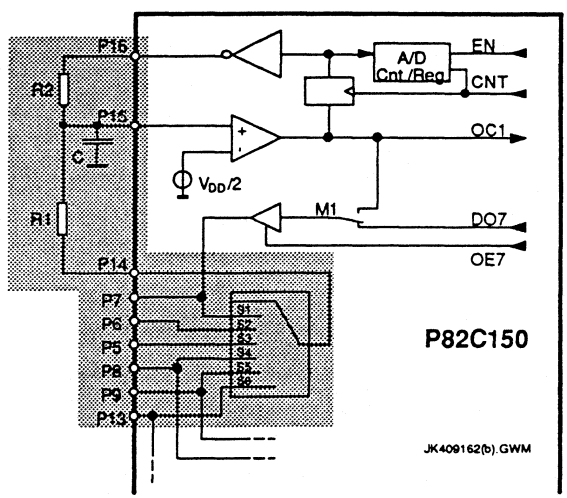


Fig. 37 ADC: Internal multiplexer is used

The output of the ADC comparator may be switched to the output of port P7 by setting the bit 'M1' in the 'analog configuration' register (see Fig. 37 and Table 15). The digital output of port P7 has to be enabled for this case and can thus not be used as analog input. Furthermore it is possible to automatically generate transmissions via the CAN-bus if the input of port P7 changes either from 'LOW' to 'HIGH' or from 'HIGH' to 'LOW' due to the comparator output level. In this case the bits for positive or negative edge triggering for this port have to be set in the respective registers.

Table 14 I/O register content if the Analog-to-Digital converter is used together with the multiplexer*

I/O Register	Addr.	I/O Register Content															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Output enable	4	OE(n)															
		0	0	0	X	X	X	0	0	0	0	0	X	X	X	X	X
Analog configuration	5	ADC	OC3	OC2	OC1		M3	M2	M1	SW3	SW2	SW1					
		X	X	X	X	0	X	X	X	0/1	0/1	0/1	0	0	0	0	0

(X = not relevant for this configuration, 0/1 = depends on application)

* This multiplexer may also be used independent of the ADC.

Table 15 I/O register content for connecting the comparator output of the ADC to port P7

I/O Register	Addr.	I/O Register Content															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Output enable	4	OE(n)															
		0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X
Analog configuration	5	ADC	OC3	OC2	OC1		M3	M2	M1	SW3	SW2	SW1					
		X	X	X	X	0	X	X	1	X	X	X	0	0	0	0	0
Positive edge	1	PE(n)															
		X	X	X	X	X	X	X	X	0/1	X	X	X	X	X	X	X
Negative edge	2	NE(n)															
		X	X	X	X	X	X	X	X	0/1	X	X	X	X	X	X	X

(X = not relevant for this configuration, 0/1 = depends on application)

10. CONCLUSION

The P82C150 (SLIO, Serial Linked I/O device) may be used in a CAN-network as a low cost I/O controlling various functions of an application.

It may be prepared to take over several different tasks as

- switching digital signals,
- monitoring digital signals incl. edge trigger function,
- comparing analog signals with each other or with a reference,
- generating quasi-analog signals (DPM, distributed pulse modulated output signal) usable in Digital-to-Analog converters,
- converting an analog signal to a digital value (ADC).

With its ability to adapt its timing to the bitrate on the bus the P82C150 may be implemented easily in systems. The device gets all configuration information (except the message identifier) via the bus line. Nodes equipped with the P82C150 may be plugged or unplugged in a running system, if a proper network management is provided.

11. LIST OF REFERENCES

[1] P82C150 Data Sheet - Can serial linked I/O device (SLIO) with digital and analog port functions, Philips Semiconductors (latest version)

[2] CAN Bus Specification, Philips Semiconductors, 1994, 12NC: 9398 706 64011

[3] Data Sheet / Specification of the P82C250, Philips Semiconductors (latest version)

[4] Road vehicles - Interchange of digital information - Controller area network (CAN) for highspeed communication.
Document ISO 11898, International Standardization Organization 1993

[5] Road vehicles - Low-speed serial datacommunication.
Document ISO 11519-2, International Standardization Organization 1994

[6] OM4272 -SLIO Evaluation Board with the 82C150 and 82C250 CAN ICs, Philips Semiconductors
User Manual: SLIO P82C150 Demonstration Software.

[7] Michael Heiss, Wolfgang Dittrich: 'Pulsanzahlmodulator als D/A-Umsetzer', Elektronik, H.19, 15.9.89

[8] Harald Eisele: 'CAN Physical Layer Concepts for the P8x592 Microcontroller', Application Note, Philips Semiconductors PCALH, Report No.: HKI/AN 91 027, Date: 92-07-03

[9] PCF 1252-Family Data Sheet, Power Failure Detector and Reset Generator, Philips Semiconductors, March 1990

[10] Jens-Ulf Pehrs: 'CAN Bus Failure Management Using the P8xC592 Microcontroller', Application Note, Philips Semiconductors PCALH, Report No.: HKI/AN 91 020, Date: 91-10-16

Stand-alone CAN-controller 82C200

1 FEATURES

- Multi-master architecture
- Interfaces with a large variety of microcontrollers
- Bus access priority (determined by the message identifier)
- 2032 message identifiers
- Guaranteed latency time for high priority messages
- Powerful error handling capability
- Data length from 0 to 8 bytes
- Configurable bus interface
- Programmable clock output
- Multicast and Broadcast message facility
- Non destructive bit-wise arbitration
- Non-return-to-zero (NRZ) coding/decoding with bit-stuffing
- Programmable transfer rate (up to 1 Mbit/s)
- Programmable output driver configuration
- Suitable for use in a wide range of networks including the SAE networks Class A, B and C
- 16 MHz clock frequency
- –40 to +85/125 °C operating temperature.

2 GENERAL DESCRIPTION

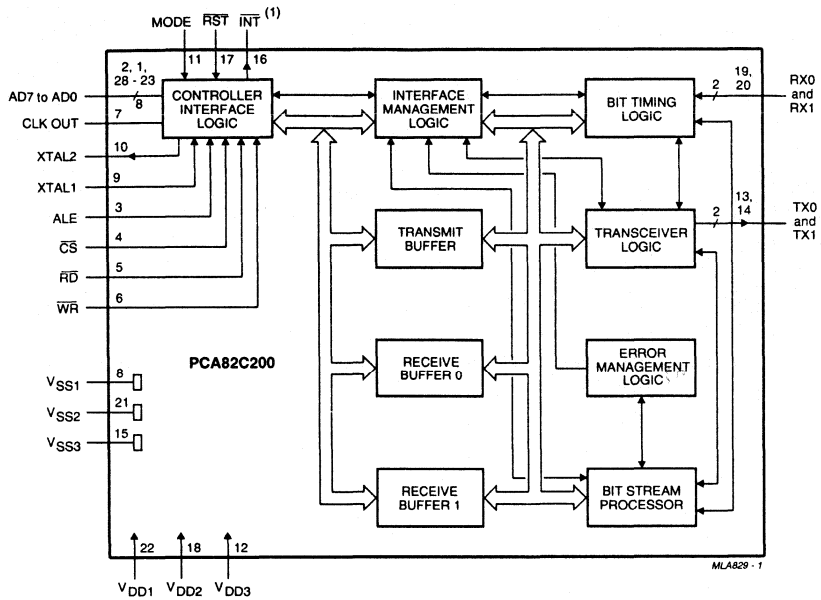
The PCA82C200; PCF82C200 (hereafter generically referred to as PCX82C200) is a highly integrated stand-alone controller for the controller area network (CAN) used within automotive and general industrial environments. The temperature range includes an automotive temperature range version (PCA82C200) of –40 to +125 °C and a –40 to +85 °C version (PCF82C200) for general applications.

The PCX82C200 contains all necessary features required to implement a high performance communication protocol. The PCX82C200 with a simple bus line connection performs all the functions of the physical and data-link layers. The application layer of an Electronic Control Unit (ECU) is provided by a microcontroller, to which the PCX82C200 provides a versatile interface. The use of the PCX82C200 in an automotive or general industrial environment, results in a reduced wiring harness and an enhanced diagnostic and supervisory capability.

3 ORDERING AND PACKAGE INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING	PHILIPS NORTH AMERICA PART ORDER NUMBER[1]	PACKAGE				TEMPERATURE RANGE (°C)
		PINS	PIN POSITION	MATERIAL	CODE	
PCA82C200P	PCA82C200PN	28	DIL	plastic	SOT117	–40 to +125
PCA82C200T	PCA82C200TD	28	SO28	plastic	SOT136A	–40 to +125
PCF82C200P	PCF82C200PN	28	DIL	plastic	SOT117	–40 to +85
PCF82C200T	PCF82C200TD	28	SO28	plastic	SOT136A	–40 to +85

NOTE:
1. Parts ordered by the Philips North America part number will be marked with the Philips part marking.



(1) During 'sleep mode' this pin functions as an input.

Fig.1 Block diagram.

4 PINNING

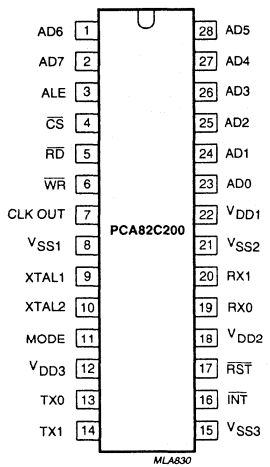


Fig.2 Pin configuration.

Pinning description

SYMBOL	PIN	DESCRIPTION
AD7–AD0	2, 1, 28–23	Multiplexed address/data bus.
ALE	3	ALE signal (Intel mode) or AS input signal (Motorola mode).
$\overline{CS}$	4	Chip select input, LOW level allows access to the PCX82C200.
$\overline{RD}$	5	$\overline{RD}$ signal (Intel mode) or E enable signal (Motorola mode) from the microcontroller.
$\overline{WR}$	6	$\overline{WR}$ signal (Intel mode) or RD/$\overline{WR}$ signal (Motorola mode) from the microcontroller.
CLK OUT	7	Clock output signal produced by the PCX82C200 for the microcontroller. The clock signal is derived from the built-in oscillator, via the programmable divider (see section 6.5). This output is capable of driving one CMOS or NMOS load.
V_{SS1}	8	Ground potential for the logic circuits.
XTAL1 (note 1)	9	Input to the oscillator's amplifier. External oscillator signal is input via this pin.
XTAL2 (note 1)	10	Output from the oscillator's amplifier. Output must be left open when an external oscillator signal is used.
MODE	11	Mode select input: connected to V_{DD} selects Intel mode; connected to V_{SS} selects Motorola mode.
V_{DD3}	12	5 V power supply for the output driver.
TX0	13	Output from the output-driver 0 to the physical bus-line.
TX1	14	Output from the output-driver 1 to the physical bus-line.
V_{SS3}	15	Ground potential for the output driver.
$\overline{INT}$	16	Interrupt output, used to interrupt the microcontroller (see section 6.2.4). $\overline{INT}$ is active if the Interrupt Register contains a logic HIGH bit (present). $\overline{INT}$ is an open drain output and is designed to be a wired-OR with other $\overline{INT}$ outputs within the system. A LOW level on this pin will reactivate the IC from the sleep mode (see section 6.2.2).
$\overline{RST}$	17	Reset input, used to reset the CAN interface (LOW level). Automatic power-ON reset can be obtained by connecting $\overline{RST}$ via a capacitor to V_{SS} and via a resistor to V_{DD} (e.g. C = 1 µF; R = 50 kΩ).
V_{DD2}	18	5 V power supply for the input comparator.
RX0–RX1	19, 20	Input from the physical bus-line to the input comparator of the PCX82C200. A dominant level will wake-up the PCX82C200. A recessive level is read if RX0 is higher than RX1 and vice versa for the dominant level.
V_{SS2}	21	Ground potential for the input comparator.
V_{DD1}	22	5 V power supply for the logic circuits.

Note

1. XTAL1 and XTAL2 pins should be connected to V_{SS} via 15 pF capacitors.

5 FUNCTIONAL DESCRIPTION

The PCX82C200 contains all necessary hardware for a high performance serial network communication (see Fig.1). The PCX82C200 controls the communication flow through the area network using the CAN-protocol. The PCX82C200 meets the following automotive requirements:

- short message length
- guaranteed latency time for urgent messages
- bus access priority, determined by the message identifier
- powerful error handling capability
- configuration flexibility to allow area network expansion.

The latency time defines the period between the initiation (Transmission Request) and the start of the transmission on the bus. Latency time is dependent on a variety of bus related conditions. In the case of a message being transmitted on the bus and one distortion the latency time can be up to 149 bit times (worst case). For more information see section 7.

5.1 Interface Management Logic (IML)

The IML interprets commands from the microcontroller, allocates the message buffers (TBF, RBF0 and RBF1) and provides interrupts and status information to the microcontroller.

5.2 Transmit Buffer (TBF)

The TBF is a 10 byte memory into which the microcontroller writes messages which are to be transmitted over the CAN network.

5.3 Receive Buffers (RBF0 AND RBF1)

The RBF0 and RBF1 are each 10 byte memories which are alternatively used to store messages received from the CAN network. The CPU can process one message while another is being received.

5.4 Bit Stream Processor (BSP)

The BSP is a sequencer, controlling the data stream between the Transmit Buffer, the Receive Buffer (parallel data) and the CAN-bus (serial data).

5.5 Bit Timing Logic (BTL)

The BTL synchronizes the PCX82C200 to the bitstream on the CAN-bus.

5.6 Transceiver Control Logic (TCL)

The TCL controls the output driver.

5.7 Error Management Logic (EML)

The EML performs the error confinement according to the CAN-protocol.

5.8 Controller Interface Logic (CIL)

The CIL is the interface to the external microcontroller. The PCX82C200 can directly interface with a variety of microcontrollers.

6 CONTROL SEGMENT AND MESSAGE BUFFER DESCRIPTION

The PCX82C200 appears to a microcontroller as a memory-mapped I/O device due to the on-chip RAM, guaranteeing the independent operation of both devices.

6.1 Address allocation

The address area of the PCX82C200 consists of the Control Segment and the message buffers. The Control Segment is programmed during an initialization download in order to configure communication parameters (e.g. bit timing). Communication over the CAN-bus is also controlled via this segment by the CPU. During initialization the CLOCK OUT signal may be programmed to a value determined by the microcontroller (see Fig.1). A message which is to be transmitted, must be written to the Transmit Buffer. After a successful reception the microcontroller may read the message from the Receive Buffer and then release it for further use.

6.2 Control Segment layout

The exchange of status, control and command signals between the microcontroller and the PCX82C200 is performed in the control segment. The layout of this segment is shown in Fig.3. After an initial down-load, the contents of the registers Acceptance Code, Acceptance Mask, Bus Timing Registers 0 and 1, and Output Control should not be changed. These registers may only be accessed when the Reset Request bit in the Control Register, is set HIGH (see section 6.2.1).

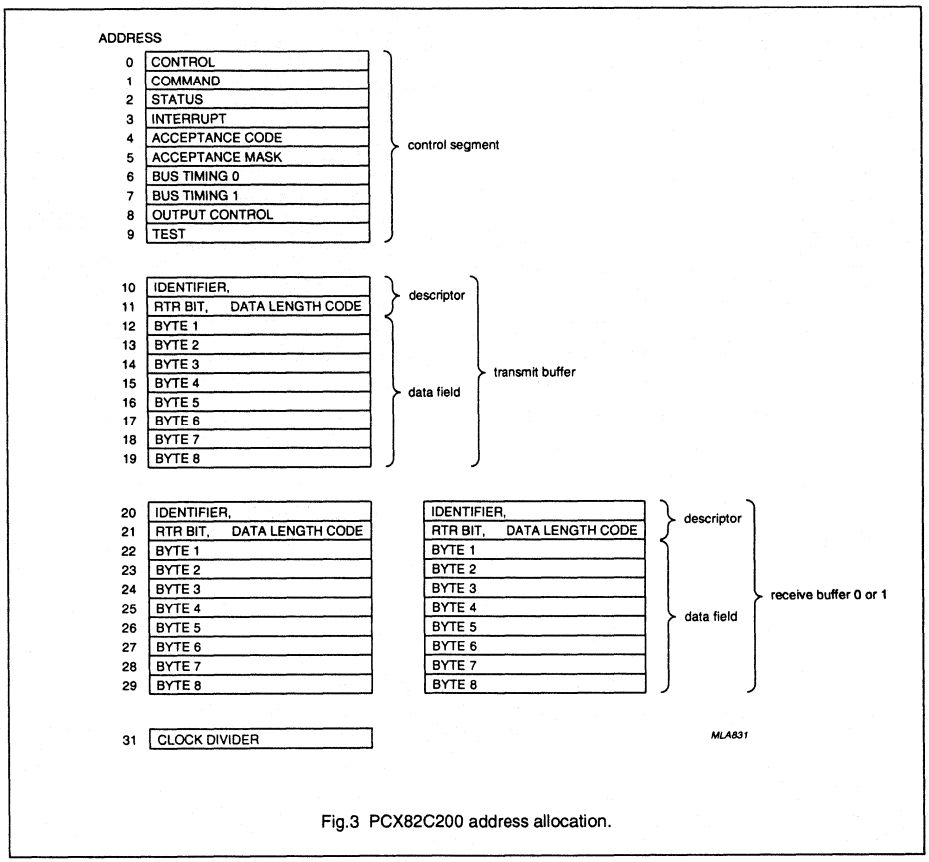


Fig.3 PCX82C200 address allocation.

Table 1 Register map

TITLE	ADDR	7	6	5	4	3	2	1	0
Control Segment									
Control Register	0	Test Mode	Sync	reserved	Overrun Interrupt Enable	Error Interrupt Enable	Transmit Interrupt Enable	Receive Interrupt Enable	Reset Request
Command Register	1	reserved	reserved	reserved	Goto Sleep	Clear Overrun Status	Release Receive Buffer	Abort Trans-mission	Trans-mission Request
Status Register	2	Bus Status	Error Status	Transmit Status	Receive Status	Trans-mission Complete Status	Transmit Buffer Access	Data Overrun	Receive Buffer Stat
Interrupt Register	3	reserved	reserved	reserved	Wake-Up Interrupt	Overrun Interrupt	Error Interrupt	Transmit Interrupt	Receive Interrupt
Acceptance Code Register	4	AC.7	AC.6	AC.5	AC.4	AC.3	AC.2	AC.1	AC.0
Acceptance Mask Register	5	AM.7	AM.6	AM.5	AM.4	AM.3	AM.2	AM.1	AM.0
Bus Timing Register 0	6	SJW.1	SJW.0	BRP.5	BRP.4	BRP.3	BRP.2	BRP.1	BRP.0
Bus Timing Register 1	7	SAM	TSEG2.2	TSEG2.1	TSEG2.0	TSEG1.3	TSEG1.2	TSEG1.1	TSEG1.0
Output Control Register	8	OCTP1	OCTN1	OCPOL1	OCTP0	OCTN0	OCPOL0	OCMODE1	OCMODE0
Test Register (note 1)	9	reserved	reserved	Map Internal Register	Connect RX Buffer 0 CPU	Connect TX Buffer CPU	Access Internal Bus	Normal RAM Connect	Float Output Driver
Transmit Buffer									
Identifier	10	ID.10	ID.9	ID.8	ID.7	ID.6	ID.5	ID.4	ID.3
RTR, Data Length Code	11	ID.2	ID.1	ID.0	RTR	DLC.3	DLC.2	DLC.1	DLC.0
bytes 1–8	12–19	Data	Data	Data	Data	Data	Data	Data	Data
Receive Buffer 0/1									
identifier	20	ID.10	ID.9	ID.8	ID.7	ID.6	ID.5	ID.4	ID.3
RTR, Data Length Code	21	ID.2	ID.1	ID.0	RTR	DLC.3	DLC.2	DLC.1	DLC.0
bytes 1–8	22–29	Data	Data	Data	Data	Data	Data	Data	Data
Clock Divider	31	reserved	reserved	reserved	reserved	reserved	CD.2	CD.1	CD.0

Notes

1. The Test Register is used for production testing only.
2. Register 30 is not implemented.

6.2.1 Control Register (CR)

The contents of the Control Register are used to change the behaviour of the PCX82C200. Control bits may be set or reset by the attached microcontroller which uses the Control Register as a read/write memory.

Table 2 Description of the Control Register bits

CR	ADDRESS 0			
BIT	**SYMBOL**	**NAME**	**VALUE**	**FUNCTION**
CR.7	TM	Test Mode (note 1)	HIGH (enabled)	PCX82C200 enters Test Mode (normal operation impossible).
			LOW (disabled)	Normal operating mode.
CR.6	S	Sync (note 2)	HIGH (2 edges)	Bus-line transitions from recessive-to-dominant and vice versa are used for resynchronization (see sections 7.2 and 8).
			LOW (1 edge)	Only transitions from recessive-to-dominant are used for resynchronization.
CR.5	–	–	–	Reserved.
CR.4	OIE	Overrun Interrupt Enable	HIGH (enabled)	If the Data Overrun bit is set (see section 6.2.3), the microcontroller receives an Overrun Interrupt signal.
			LOW (disabled)	Microcontroller receives no Overrun Interrupt signal from the PCX82C200.
CR.3	EIE	Error Interrupt Enable	HIGH (enabled)	If the Error or Bus Status change (see section 6.2.3), the microcontroller receives an Error Interrupt signal.
			LOW (disabled)	Microcontroller receives no Error Interrupt signal.
CR.2	TIE	Transmit Interrupt Enable	HIGH (enabled)	When a message has been successfully transmitted or the transmit buffer is accessible again, (e.g. after an Abort Transmission command) the PCX82C200 transmits a Transmit Interrupt signal to the microcontroller.
			LOW (disabled)	No transmission of the Transmit Interrupt signal by the PCX82C200 to the microcontroller.
CR.1	RIE	Receive Interrupt Enable	HIGH (enabled)	When a message has been received without errors, the PCX82C200 transmits a Receive Interrupt signal to the microcontroller.
			LOW (disabled)	No transmission of the Receive Interrupt signal by the PCX82C200 to the microcontroller.
CR.0	RR	Reset Request (note 3)	HIGH (present)	Detection of a Reset Request results in the PCX82C200 aborting the current transmission or reception of a message and entering the reset state.
			LOW (absent)	On the HIGH-to-LOW transition of the Reset Request bit, the PCX82C200 returns to its normal operating state.

Notes

1. The Test Mode is intended for factory testing and not for customer use.
2. The Sync bit should only be modified if the Reset Request bit is set HIGH (present), otherwise it is ignored. It is possible to set the Sync bit while the Reset Request bit is changed from HIGH to LOW.
3. During an external reset ($\overline{RST}$ = LOW) or when the Bus Status bit is set HIGH (Bus-Off), the IML forces the Reset Request HIGH (present). During an external reset the microcontroller cannot set the Reset Request bit LOW (absent). Therefore, after having set the Reset Request bit LOW (absent), the microcontroller must check this bit to ensure that the external reset pin is not being held HIGH (present). After the Reset Request bit is set LOW (absent) the PCX82C200 will wait for:
   - one occurrence of the Bus-Free signal (11 recessive bits, see section 8.9.6), if the preceding reset (Reset Request = HIGH) was due to an external reset or a microcontroller initiated reset
   - 128 occurrences of Bus-Free, if the preceding reset (Reset Request = HIGH) was due to a PCX82C200 initiated Bus-Off, before re-entering the Bus-On mode (see section 8.9).

   When Reset Request is set HIGH (present), for whatever reason, the control, command, status and interrupt bits are affected, see Table 3. When Reset Request is set HIGH (present) the registers at addresses 4 to 8 are accessible but the TBF is not.

Table 3 Effects of setting the Reset Request bit HIGH (present)

TYPE	BIT	FUNCTION	EFFECT
Control	CR.7	Test Mode	LOW (disabled)
Command	CMR.4	Goto Sleep	LOW (wake-up)
	CMR.3	Clear Overrun Status	HIGH (clear)
	CMR.2	Release Receive Buffer	HIGH (released)
	CMR.1	Abort Transmission	LOW (absent)
	CMR.0	Transmission Request	LOW (absent)
Status	SR.7	Bus Status	LOW (Bus-On) (note 1)
	SR.6	Error Status	LOW (no error) (note 1)
	SR.5	Transmit Status	LOW (idle)
	SR.4	Receive Status	LOW (idle)
	SR.3	Transmission Complete Status	HIGH (complete)
	SR.2	Transmit Buffer Access	HIGH (released)
	SR.1	Data Overrun	LOW (absent)
	SR.0	Receive Buffer Status	LOW (empty)
Interrupt	IR.3	Overrun Interrupt	LOW (reset)
	IR.1	Transmit Interrupt	LOW (reset)
	IR.0	Receive Interrupt	LOW (reset)

Note

1. Only after an external reset; see note 1 to Table 5 "Description of the Status Register bits".

6.2.2 Command Register (CMR)

A command bit initiates an action within the transfer layer of the PCX82C200. The Command Register appears to the microcontroller as a write only memory. If a read access is performed to this address the byte 11111111 (binary) is returned.

Table 4 Description of the Command Register bits

CMR	ADDRESS 1			
BIT	**SYMBOL**	**NAME**	**VALUE**	**FUNCTION**
CMR.7	–	–	–	Reserved.
CMR.6	–	–	–	Reserved.
CMR.5	–	–	–	Reserved.
CMR.4	GTS	GoTo Sleep (note 1)	HIGH (sleep)	The PCX82C200 enters sleep mode, if the $\overline{INT}$ = HIGH (no interrupt signal from the PCX82C200 to the microcontroller pending or external source pending) and there is no bus activity.
			LOW (wake up)	The PCX82C200 functions normally.
CMR.3	COS	Clear Overrun Status (note 2)	HIGH (clear)	The Data Overrun status bit is set to LOW (see section 6.2.3).
			LOW (no action)	No action.
CMR.2	RRB	Release Receive Buffer (note 3)	HIGH (released)	The receive buffer attached to the microcontroller is released.
			LOW (no action)	No action.
CMR.1	AT	Abort Transmission (note 4)	HIGH (present)	If not already in progress, a pending Transmission Request is cancelled.
			LOW (absent)	No action.
CMR.0	TR	transmission Request (note 5)	HIGH (present)	A message shall be transmitted.
			LOW (absent)	No action.

Notes

1. The PCX82C200 will enter sleep mode, if Goto Sleep is set HIGH (sleep), there is no bus activity and $\overline{INT}$ = HIGH (inactive). After sleep mode is set, the CLK OUT signal continues until at least 15 bit times have passed. The PCX82C200 will wake up when one of the three previously mentioned conditions is negated: after Goto Sleep is set LOW (wake up), there is bus activity or $\overline{INT}$ is driven LOW (active). On wake up, the oscillator is started and a Wake-Up Interrupt (see section 6.2.4) is generated. A PCX82C200 which is sleeping and then awakened by bus activity will not be able to receive this message until it detects a Bus-Free signal (see section 8.9.6).
2. This command bit is used to acknowledge the Data Overrun condition signalled by the Data Overrun status bit. It may be given or set at the same time as a Release Receive Buffer command bit.
3. After reading the contents of the Receive Buffer (RBF0 or RBF1) the microcontroller must release this buffer by setting the Release Receive Buffer bit HIGH (released). This may result in another message becoming immediately available.
4. The Abort Transmission bit is used when the microcontroller requires the suspension of the previously requested transmission, for example to transmit an urgent message. A transmission already in progress is not stopped. In order to determine if the original message had been transmitted successfully, or aborted, the Transmission Complete status bit should be checked after the Transmit Buffer Access bit has been set HIGH (released) or a Transmit Interrupt has been generated (see section 6.2.4).
5. If the Transmission Request bit was set HIGH in a previous command, it cannot be cancelled by setting the Transmission Request bit LOW (absent). Cancellation of the requested transmission may be performed by setting the Abort Transmission bit HIGH (present).

6.2.3 Status Register (SR)

The contents of the Status Register reflect the status of the PCX82C200 bus controller. The Status Register appears to the microcontroller as a read only memory.

Table 5 Description of the Status Register bits

SR	ADDRESS 2			
BIT	**SYMBOL**	**NAME**	**VALUE**	**FUNCTION**
SR.7	BS	Bus Status (note 1)	HIGH (Bus-Off)	The PCX82C200 is not involved in bus activities.
			LOW (Bus-On)	The PCX82C200 is involved in bus activities.
SR.6	ES	Error Status	HIGH (error)	At least one of the Error Counters (see section 8.10.3) has reached the microcontroller Warning Limit.
			LOW (ok)	Both Error Counters have not reached the Warning Limit.
SR.5	TS	Transmit Status (note 2)	HIGH (transmit)	The PCX82C200 is transmitting a message.
			LOW (idle)	No message is transmitted.
SR.4	RS	Receive Status (note 2)	HIGH (receive)	The PCX82C200 is receiving a message.
			LOW (idle)	No message is received.
SR.3	TCS	Transmission Complete Status (note 3)	HIGH (complete)	Last requested transmission has been successfully completed.
			LOW (incomplete)	Previously requested transmission is not yet completed.
SR.2	TBS	Transmit Buffer Access (note 3)	HIGH (released)	The microcontroller may write a message into the TBF.
			LOW (locked)	The microcontroller cannot access the Transmit Buffer. A message is either waiting for transmission or is in the process of being transmitted.
SR.1	DO	Data Overrun (note 4)	HIGH (overrun)	This bit is set HIGH (Overrun), when both Receive Buffers are full and the first byte of another message should be stored.
			LOW (absent)	No data overrun has occurred since the Clear Overrun command was given.
SR.0	RBS	Receive Buffer Status (note 5)	HIGH (full)	This bit is set when a new message is available.
			LOW (empty)	No message has become available since the last Release Receive Buffer command bit was set.

Notes

1. When the Bus Status bit is set HIGH (Bus-Off), the PCX82C200 will set the Reset Request bit HIGH (present). It will stay in this state until the microcontroller sets the Reset Request bit LOW (absent). Once this is completed the PCX82C200 will wait the minimum protocol-defined time (128 occurrences of the Bus-Free signal) before setting the Bus Status bit LOW (Bus-On), the Error Status bit LOW (ok) and resetting the Error Counters.
2. If both the Receive Status and Transmit Status bits are LOW (idle) the CAN-bus is idle.
3. If the microcontroller tries to write to the Transmit Buffer when the Transmit Buffer Access bit is LOW (locked), the written bytes will not be accepted and will be lost without this being signalled. The Transmission Complete Status bit is set LOW (incomplete) whenever the Transmission Request bit is set HIGH (present). If an Abort Transmission command is issued, the Transmit Buffer will be released. If the message, which was requested and then aborted, was not transmitted, the Transmission Complete Status bit will remain LOW.
4. If Data Overrun = HIGH (Overrun) is detected, the currently received message is dropped. A transmitted message, granted acceptance, is also stored in a Receive Buffer. This occurs because it is not known if the PCX82C200 will lose arbitration and so become a receiver of the message. If no Receive Buffer is available, Data Overrun is signalled.
5. If the command bit Release Receive Buffer is set HIGH (released) by the microcontroller, the Receive Buffer Status bit is set LOW (empty) by IML. When a new message is stored in any of the receive buffers, the Receive Buffer Status bit is set HIGH (full) again.

6.2.4 Interrupt Register (IR)

The Interrupt Register allows the identification of an interrupt source. When one or more bits of this register are set, the $\overline{INT}$ pin is activated. All bits are reset by the PCX82C200 after this register is read by the microcontroller. This register appears to the microcontroller as a read only memory.

Table 6 Description of the Interrupt Register bits

IR	ADDRESS 3			
BIT	**SYMBOL**	**NAME**	**VALUE**	**FUNCTION**
IR.7	–	–	–	Reserved.
IR.6	–	–	–	Reserved.
IR.5	–	–	–	Reserved.
IR.4	WUI	Wake-Up Interrupt	HIGH (set)	The Wake-Up Interrupt bit is set HIGH, when the sleep mode is left (see section 6.2.2).
			LOW (reset)	Wake-Up Interrupt bit is reset by a read access of Interrupt Register by the microcontroller.
IR.3	OI	Overrun Interrupt (note 1)	HIGH (set)	This bit is set HIGH, if both Receive Buffers contain a message and the first byte of another message should be stored (passed acceptance), and the Overrun Interrupt Enable is HIGH (enabled).
			LOW (reset)	Overrun Interrupt bit is reset by a read access of Interrupt Register by the microcontroller.
IR.2	EI	Error Interrupt	HIGH (set)	This bit is set on a change of either the Error Status or Bus Status bits (see section 6.2.3) if the Error Interrupt Enable is HIGH (enabled).
			LOW (reset)	The Error Interrupt bit is reset by a read access of the Interrupt Register by the microcontroller.
IR.1	TI	Transmit Interrupt	HIGH (set)	This bit is set on a change of the Transmit Buffer Access bit from LOW to HIGH (released) and Transmit Interrupt Enable is HIGH (enabled).
			LOW (reset)	Transmit Interrupt bit will be reset after a read access of the Interrupt Register by the microcontroller.
IR.0	RI	Receive Interrupt (note 2)	HIGH (set)	This bit is set when a new message is available in the Receive Buffer and the Receive Interrupt Enable bit is HIGH (enabled).
			LOW (reset)	Receive Interrupt bit is automatically reset by a read access of Interrupt Register by the microcontroller.

Notes

1. Overrun Interrupt bit (if enabled) and Data Overrun bit (see section 6.2.3) are set at the same time.
2. Receive Interrupt bit (if enabled) and Receive Buffer Status bit (see section 6.2.3) are set at the same time.

6.2.5 Acceptance Code Register (ACR)

The Acceptance Code Register is part of the acceptance filter of the PCX82C200. This register can be accessed (read/write), if the Reset Request bit is set HIGH (present). When a message is received which passes the acceptance test and if there is an empty Receive Buffer, then the respective Descriptor and Data Field (see Fig.4) are sequentially stored in this empty buffer. In the case that there is no empty Receive Buffer, the Data Overrun bit is set HIGH (overrun), see sections 6.2.3 and 6.2.4. When the complete message has been correctly received the following occurs:

- the Receive Buffer Status bit is set HIGH (full)
- if the Receive Interrupt Enable bit is set HIGH (enabled), the Receive Interrupt is set HIGH (set).

The Acceptance Code bits (AC.7-AC.0) and the eight most significant bits of the message's Identifier (ID.10-ID.3) must be equal to those bit positions which are marked relevant by the Acceptance Mask bits (AM.7-AM.0). If the following equation is satisfied, acceptance is given:

$$[\,(\,ID.10\,..\,ID.3\,) = (\,AC.7\,..\,AC.0\,)\,]\ \textit{or}\ (\,AM.7\,..\,AM.0\,) = 1111\ 1111\ \textit{binary}$$

During transmission of a message which passes the acceptance test, the message is also written to its own Receive Buffer. If no Receiver Buffer is available, Data Overrun is signalled because it is not known at the start of a message whether the PCX82C200 will lose arbitration and so become a receiver of the message.

Table 7 Acceptance Code Register bits

ACR	ADDRESS 4						
7	6	5	4	3	2	1	0
AC.7	AC.6	AC.5	AC.4	AC.3	AC.2	AC.1	AC.0

6.2.6 Acceptance Mask Register (AMR)

The Acceptance Mask Register is part of the acceptance filter of the PCX82C200. This register can be accessed (read/write) if the Reset Request bit is set HIGH (present). The Acceptance Mask Register qualifies which of the corresponding bits of the acceptance code are "relevant" or "don't care" for acceptance filtering.

Table 8 Acceptance Mask Register bits

AMR	ADDRESS 5						
7	6	5	4	3	2	1	0
AM.7	AM.6	AM.5	AM.4	AM.3	AM.2	AM.1	AM.0

Table 9 Description of the Acceptance Mask Register bits

ACCEPTANCE MASK BIT	VALUE	COMMENTS
AM.7 to AM.0	HIGH (don't care)	This bit position is "don't care" for the acceptance of a message.
	LOW (relevant)	This bit position is "relevant" for acceptance filtering.

6.2.7 Bus Timing Register 0 (BTR0)

The contents of Bus Timing Register 0 defines the values of Baud Rate Prescaler (BRP) and the Synchronization Jump Width (SJW). This register can be accessed (read/write) if the Reset Request bit is set HIGH (present).

Table 10 Bus Timing Register 0 bits

BTR0	ADDRESS 6						
7	6	5	4	3	2	1	0
SJW.1	SJW.0	BRP.5	BRP.4	BRP.3	BRP.2	BRP.1	BRP.0

Baud Rate Prescaler (BRP)

The period of the system clock t_{SCL} is programmable and determines the individual bit timing. The system clock is calculated using the following equation:

$t_{SCL} = 2t_{CLK}$ (32BRP.5 + 16BRP.4 + 8BRP.3 + 4BRP.2 + 2BRP.1 + BRP.0 + 1)

t_{CLK} = time period of the PCX82C200 oscillator.

Synchronization Jump Width (SJW)

To compensate for phase shifts between clock oscillators of different bus controllers, any bus controller must resynchronize on any relevant signal edge of the current transmission. The synchronization jump width defines the maximum number of clock cycles a bit period may be shortened or lengthened by one resynchronization:

$t_{SJW} = t_{SCL}$ (2SJW.1 + SJW.0 + 1)

For further information on bus timing see sections 6.2.8 and 7.

6.2.8 Bus Timing Register 1 (BTR1)

The contents of Bus Timing Register 1 defines the length of the bit period, the location of the sample point and the number of samples to be taken at each sample point. This register may be accessed (read/write) if the Reset Request bit is set HIGH (present).

Table 11 Bus Timing Register 1 bits

BTR1	ADDRESS 7						
7	6	5	4	3	2	1	0
SAM	TSEG2.2	TSEG2.1	TSEG2.0	TSEG1.3	TSEG1.2	TSEG1.1	TSEG1.0

Sampling (SAM)

Table 12 Selection of sampling

BIT	VALUE	COMMENTS
SAM	HIGH (3 samples)	Three samples are taken.
	LOW (1 sample)	The bus is sampled once.

SAM = LOW (logic 0) is recommended for high speed buses (SAE class C), while SAM = HIGH (logic 1) is recommended for slow/medium speed buses (class A and B) where filtering of spikes on the bus-line is beneficial (see section 7.1.6).

Time Segment 1 (TSEG1) and Time Segment 2 (TSEG2)

TSEG1 and TSEG2 determine the number of clock cycles per bit period and the location of the sample point:

$t_{TSEG1} = t_{SCL}$ (8TSEG1.3 + 4TSEG1.2 + 2TSEG1.1 + TSEG1.0 + 1)

$t_{TSEG2} = t_{SCL}$ (4TSEG2.2 + 2TSEG2.1 + TSEG2.0 + 1)

For further information on bus timing see sections 6.2.7 and 7.

6.2.9 OUTPUT CONTROL REGISTER (OCR)

The Output Control Register allows, under software control, the set-up of different output driver configurations. This register may be accessed (read/write) if the Reset Request bit is set HIGH (present).

Table 13 Output Control Register bits

OCR	ADDRESS 8						
7	6	5	4	3	2	1	0
OCTP1	OCTN1	OCPOL1	OCTP0	OCTN0	OCPOL0	OCMODE1	OCMODE0

If the PCX82C200 is in the sleep mode (Goto Sleep = HIGH) a recessive level is output on the TX0 and TX1 pins. If the PCX82C200 is in the reset state (Reset Request = HIGH) the output drivers are floating.

Normal Output Mode

In Normal Output Mode the bit sequence (TXD) is sent via TX0 and TX1. The voltage levels on the output driver pins TX1 and TX0 depend on both the driver characteristic programmed by OCTPx, OCTNx (float, pull-up, pull-down, push-pull) and the output polarity programmed by OCPOLx (see Fig.4).

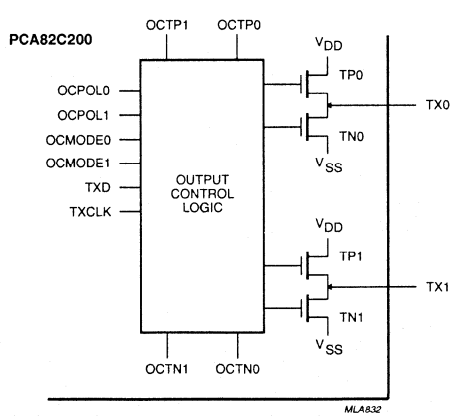


Fig.4 Configurable CAN transmitter.

Clock Output Mode

For the TX0 pin this is the same as in Normal Output Mode. However, the data stream to TX1 is replaced by the transmit clock (TXCLK). The rising edge of the transmit clock (non inverted) marks the beginning of a bit period. The clock pulse width is t_{SCL}.

Bi-phase Output Mode

In contrast to Normal Output Mode the bit representation is time variant and toggled. If the bus controllers are galvanically decoupled from the bus-line by a transformer, the bit stream is not allowed to contain a DC component. This is achieved by the following scheme. During recessive bits all outputs are deactivated (3-state). Dominant bits are sent alternatingly on TX0 and TX1, i.e. the first dominant bit is sent on TX0, the second is sent on TX1, and the third one is sent on TX0 again, etc.

Test Output Mode

For the TX0 pin this is the same as in Normal Output Mode. To measure the delay time of the transmitter and receiver this mode connects the output of the input comparator (COMP OUT) with the input of the output driver TX1. This mode is used for production testing only.

The following two tables, Table 14 and Table 15, show the relationship between the bits of the Output Control Register and the two serial output pins TX0 and TX1 of the PCX82C200, connected to the serial bus (see Fig.1).

Table 14 Description of the Output Mode bits

OCMODE1	OCMODE0	DESCRIPTION
1	0	Normal Output Mode; TX0, TX1: bit sequence (TXD; note 1).
1	1	Clock Output Mode; TX0: bit sequence, TX1: bus clock (TXCLK).
0	0	Bi-phase Output Mode.
0	1	Test Output Mode; TX0: bit sequence, TX1: COMP OUT.

Note

1. TXD is the data bit to be transmitted.

Table 15 Output pin set-up

DRIVE	OCTPx	OCTNx	OCPOLx	TXD	TPx (note 1)	TNx (note 2)	TXx (note 3)
Float	0	0	0	0	OFF	OFF	float
	0	0	0	1	OFF	OFF	float
	0	0	1	0	OFF	OFF	float
	0	0	1	1	OFF	OFF	float
Pull-down	0	1	0	0	OFF	ON	LOW
	0	1	0	1	OFF	OFF	float
	0	1	1	0	OFF	OFF	float
	0	1	1	1	OFF	ON	LOW
Pull-up	1	0	0	0	OFF	OFF	float
	1	0	0	1	ON	OFF	HIGH
	1	0	1	0	ON	OFF	HIGH
	1	0	1	1	OFF	OFF	float
Push/Pull	1	1	0	0	OFF	ON	LOW
	1	1	0	1	ON	OFF	HIGH
	1	1	1	0	ON	OFF	HIGH
	1	1	1	1	OFF	ON	LOW

Notes

1. TPx is the on-chip output transistor x, connected to V_{DD}; x = 0 or 1.
2. TNx is the on-chip output transistor x, connected to V_{SS}; x = 0 or 1.
3. TXx is the serial output level on pin TX0 or TX1. It is required that the output level on the CAN-bus is dominant with TXD = 0 and recessive with TXD = 1 (see section 8.1.1).

6.2.10 Test Register (TR)

The Test Register is used for production testing only.

6.3 Transmit Buffer layout

The global layout of the Transmit Buffer is shown in Fig.3. This buffer serves to store a message from the microcontroller to be transmitted by the PCX82C200. It is subdivided into Descriptor and Data Field. The Transmit Buffer can be written to and read from by the microcontroller (see note 3 to Table 2).

6.3.1 DESCRIPTOR

Table 16 Descriptor Byte 1 (DSCR1)

DSCR1	ADDRESS 10						
7	6	5	4	3	2	1	0
ID.10	ID.9	ID.8	ID.7	ID.6	ID.5	ID.4	ID.3

Table 17 Descriptor Byte 2 (DSCR2)

DSCR2	ADDRESS 11						
7	6	5	4	3	2	1	0
ID.2	ID.1	ID.0	RTR	DLC.3	DLC.2	DLC.1	DLC.0

Identifier (ID)

The Identifier consists of 11 bits (ID.10 to ID.0). ID.10 is the most significant bit, which is transmitted first on the bus during the arbitration process. The Identifier acts as the message's name, used in a receiver for acceptance filtering and also determines the bus access priority during the arbitration process. The lower the binary value of the Identifier the higher the priority. This is due to the larger number of leading dominant bits during arbitration (see section 8.7 "Bus organization").

Remote Transmission Request bit (RTR)

Table 18 Description of the RTR bit

BIT	VALUE	COMMENTS
RTR	HIGH (remote)	Remote Frame will be transmitted by the PCX82C200.
	LOW (data)	Data Frame will be transmitted by the PCX82C200.

Data Length Code (DLC)

The number of bytes (Data Byte Count) in the Data Field of a message is coded by the Data Length Code. At the start of a Remote Frame transmission the Data Length Code is not considered due to the RTR bit being HIGH (remote). This forces the number of transmitted/received data bytes to be 0. Nevertheless, the Data Length Code must be specified correctly to avoid bus errors, if two CAN-controllers start a Remote Frame transmission simultaneously.

The range of the Data Byte Count is 0 to 8 bytes and coded as follows:

Data Byte Count = 8DLC.3 + 4DLC.2 + 2DLC.1 + DLC.0

For reasons of compatibility no Data Byte Counts other than 0 to 8 should be used.

6.3.2 DATA FIELD

The number of transferred data bytes is determined by the Data Length Code. The first bit transmitted is the most significant bit of data byte 1 at address 12.

6.4 Receive Buffer layout

The layout of the Receive Buffer and the individual bytes correspond to the definitions given for the Transmit Buffer layout, except that the addresses start at 20 instead of 10 (see Fig.3).

6.5 Clock Divider Register (CDR)

The Clock Divider Register controls the CLK OUT frequency for the microcontroller (see Fig.1). It can be written to or read by the microcontroller. The default state of the register is divide by 12 for Motorola mode and divide by 2 for Intel mode. Values from 0 to 7 may be written into this register and will result in the CLK OUT frequencies shown in Table 20.

Table 19 Clock Divider Register bits

CDR	ADDRESS 31						
7	6	5	4	3	2	1	0
–	–	–	–	–	CD.2	CD.1	CD.0

Note

Bits CDR.7 to CDR.3 are reserved.

Table 20 CLK OUT frequency selection

CD.2	CD.1	CD.0	CLK OUT FREQUENCY
0	0	0	$f_{CLK}/2$
0	0	1	$f_{CLK}/4$
1	1	0	$f_{CLK}/6$
0	1	1	$f_{CLK}/8$
1	0	0	$f_{CLK}/10$
1	0	1	$f_{CLK}/12$
1	1	0	$f_{CLK}/14$
1	1	1	f_{CLK}

Note

1. f_{CLK} is the frequency of the oscillator.

7 BUS TIMING/SYNCHRONIZATION

The Bus Timing Logic (BTL) monitors the serial bus-line via the on-chip input comparator and performs the following functions (see section 5):

- monitors the serial bus-line level
- adjusts the sample point, within a bit period (programmable)
- samples the bus-line level using majority logic (programmable, 1 or 3 samples)
- synchronization to the bit stream:
  - hard synchronization at the start of a message
  - resynchronization during transfer of a message.

The configuration of the BTL is performed during the initialization of the PCX82C200. The BTL uses the following three registers:

- Control register (Sync)
- Bus Timing Register 0
- Bus Timing Register 1.

7.1 Bit timing

A bit period is built up from a number of system clock cycles (t_{SCL}), see section 6.2.7. One bit period is the result of the addition of the programmable segments TSEG1 and TSEG2 and the general segment SYNCSEG (see sections 6.2.7 to 6.2.8).

7.1.1 Synchronization Segment (SYNCSEG)

The incoming edge of a bit is expected during this state; this state corresponds to one system clock cycle (1 x t_{SCL}).

7.1.2 Time Segment 1 (TSEG1)

This segment determines the location of the sampling point within a bit period, which is at the end of TSEG1. TSEG1 is programmable from 1 to 16 system clock cycles (see section 6.2.8).

The correct location of the sample point is essential for the correct functioning of a transmission. The following points must be taken into consideration:

- a Start-Of-Frame (see section 8.2.1) causes all PCX82C200's to perform a 'hard synchronization' (see section 7.2.1) on the first recessive-to-dominant edge. During arbitration, however, several PCX82C200's may simultaneously transmit. Therefore it may require twice the sum of bus-line, input comparator and the output driver delay times until the bus is stable. This is the propagation delay time.
- to avoid sampling at an incorrect position, it is necessary to include an additional synchronization buffer on both sides of the sample point. The main reasons for incorrect sampling are:
  - incorrect synchronization due to spikes on the bus-line
  - slight variations in the oscillator frequency of each PCX82C200 in the network, which results in a phase error.

Time Segment 1 consists of the segment for compensation of propagation delays and the synchronization buffer directly before the sample point (see Fig.5).

7.1.3 Time Segment 2 (TSEG2)

This time segment provides:

- additional time at the sample point for calculation of the subsequent bit levels (e.g. arbitration)
- synchronization buffer segment directly after the sample point (see section 7.1.2).

TSEG2 is programmable from 1 to 8 system clock cycles (see section 6.2.8).

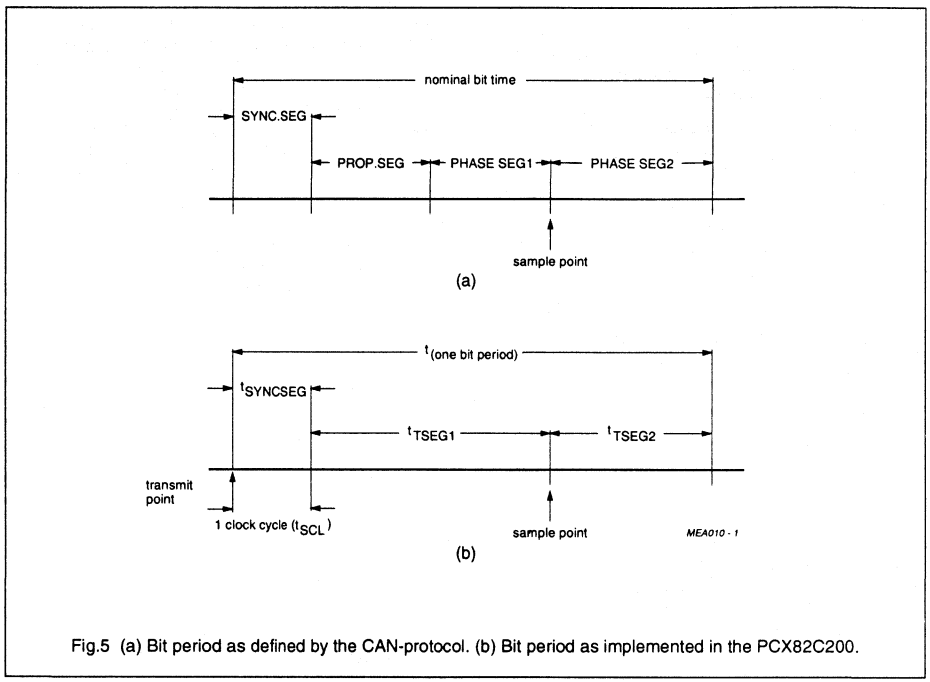


Fig.5 (a) Bit period as defined by the CAN-protocol. (b) Bit period as implemented in the PCX82C200.

7.1.4 Synchronization Jump Width (SJW)

SJW defines the maximum number of clock cycles (t_{SCL}) a bit period may be reduced or increased by one resynchronization. SJW is programmable from 1 to 4 system clock cycles (see section 6.2.7).

7.1.5 Propagation delay time

The propagation delay time (t_{prop}) is calculated by summing the maximum propagation delay times of the physical bus, the input comparator and the output driver. The resulting sum is multiplied by 2 and then rounded up to the nearest multiple of t_{SCL}.

t_{prop} = 2 x (physical bus delay + input comparator delay + output driver delay)

7.1.6 Bit timing restrictions

Restrictions on the configuration of the bit timing are based on internal processing. The restrictions are:

- $t_{TSEG2} \geq 2t_{SCL}$
- $t_{TSEG2} \geq t_{SJW}$
- $t_{TSEG1} \geq t_{TSEG2}$
- $t_{TSEG1} \geq t_{SJW} + t_{prop}$

The three sample mode (SAM = 1) has the effect of introducing a delay of one system clock cycle on the bus-line. This must be taken into account for the correct calculation of TSEG1 and TSEG2:

- $t_{TSEG1} \geq t_{SJW} + t_{prop} + 2t_{SCL}$
- $t_{TSEG2} \geq 3t_{SCL}$

7.2 Synchronization

Synchronization is performed by a state machine which compares the incoming edge with its actual bit timing and adapts the bit timing by hard synchronization or resynchronization.

7.2.1 Hard synchronization

This type of synchronization occurs only at the beginning of a message. The PCX82C200 synchronizes on the first incoming recessive-to-dominant edge of a message (being the leading edge of a message's Start-Of-Frame bit; see section 7.1).

7.2.2 Resynchronization

Resynchronization occurs during the transmission of a message's bit stream to compensate for:

- variations in individual PCX82C200 oscillator frequencies
- changes introduced by switching from one transmitter to another (e.g. during arbitration).

As a result of resynchronization either t_{TSEG1} may be increased by up to a maximum of t_{SJW} or t_{TSEG2} may be decreased by up to a maximum of t_{SJW}:

- $t_{TSEG1} \leq t_{SCL}$ ((TSEG1 + 1) + (SJW + 1))
- $t_{TSEG2} \geq t_{SCL}$ ((TSEG2 + 1) − (SJW + 1))

Note: TSEG1, TSEG2 and SJW are the programmed numerical values.

The phase error (e) of an edge is given by the position of the edge relative to SYNCSEG, measured in system clock cycles (t_{SCL}). The value of the phase error is defined as:

- e = 0, if the edge occurs within SYNCSEG
- e > 0, if the edge occurs within TSEG1
- e < 0, if the edge occurs within TSEG2.

The effect of resynchronization is:

- the same as that of a hard synchronization, if the magnitude of the phase error (e) is less or equal to the programmed value of t_{SJW} (see section 6.2.7)
- to increase a bit period by the amount of t_{SJW}, if the phase error is positive and the magnitude of the phase error is larger than t_{SJW}
- to decrease a bit period by the amount of t_{SJW}, if the phase error is negative and the magnitude of the phase error is larger than t_{SJW}.

7.2.3 Synchronization Rules

The synchronization rules are as follows:

- only one synchronization within one bit time is used
- an edge is used for synchronization only if the value detected at the previous sample point differs from the bus value immediately after the edge
- hard synchronization is performed whenever there is a recessive-to-dominant edge during Bus-Idle (see section 7)

- all other edges (recessive-to-dominant and optionally dominant-to-recessive edges if the Sync bit is set HIGH; see section 6.2.1) which are candidates for resynchronization will be used with the following exception:
  - a transmitting PCX82C200 will not perform a resynchronization as a result of a recessive-to-dominant edge with positive phase error, if only these edges are used for resynchronization. This ensures that the delay times of the output driver and input comparator do not cause a permanent increase in the bit time.

8 COMMUNICATION PROTOCOL

8.1 Frame types

The PCX82C200 bus controller supports the four different CAN-protocol frame types for communication:

- Data Frame, to transfer data
- Remote Frame, request for data
- Error Frame, globally signal a (locally) detected error condition
- Overload Frame, to extend delay time of subsequent frames (an Overload Frame is not initiated by the PCX82C200).

8.1.1 Bit representation

There are two logical bit representations used in the CAN-protocol:

- a recessive bit on the bus-line appears only if all connected PCX82C200's send a recessive bit at that moment
- dominant bits always overwrite recessive bits i.e. the resulting bit level on the bus-line is dominant.

8.2 Data Frame

A Data Frame carries data from a transmitting PCX82C200 to one or more receiving PCX82C200's. A Data Frame is composed of seven different bit-fields:

- Start-Of-Frame
- Arbitration Field
- Control Field
- Data Field (may have a length of zero)
- CRC Field
- Acknowledge Field
- End-Of-Frame.

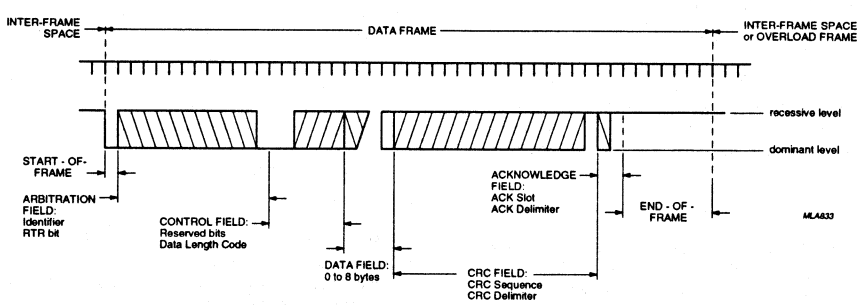


Fig.6 Data Frame.

8.2.1 Start-Of-Frame bit

Signals the start of a Data Frame or Remote Frame. It consists of a single dominant bit used for hard synchronization of a PCX82C200 in receive mode.

8.2.2 Arbitration Field

Consists of the message Identifier and the RTR bit (see section 6.3.1). In the event of simultaneous message transmissions by two or more PCX82C200's the bus access conflict is solved by bit-wise arbitration, which is active during the transmission of the Arbitration Field.

Identifier

This 11-bit field is used to provide information about the message, as well as the bus access priority. It is transmitted in the order ID.10 to ID.0 (LSB). The situation that the seven most significant bits (ID.10 to ID.4) are all recessive must not occur.

An Identifier does not define which particular PCX82C200 will receive the frame, because a CAN based communication network does not discriminate between a point-to-point, multicast or broadcast communication.

Remote Transmission Request bit (RTR)

A PCX82C200, acting as a receiver for certain information may initiate the transmission of the respective data by transmitting a Remote Frame to the network, addressing the data source via the Identifier and setting the RTR bit HIGH (remote; recessive bus level). If the data source simultaneously transmits a Data Frame containing the requested data, it uses the same Identifier. No bus access conflict occurs due to the RTR bit being set LOW (data; dominant bus level) in the Data Frame.

8.2.3 Control Field

This field consists of six bits. It includes two reserved bits (for future expansions of the CAN-protocol), transmitted with a dominant bus level, and is followed by the Data Length Code (4 bits). The number of bytes in the (destuffed; number of data bytes to be transmitted/received) Data Field is indicated by the Data Length Code. Admissible values of the Data Length Code and hence the number of bytes in the (destuffed) Data Field, are 0 to 8. A logic 0 (logic 1) in the Data Length Code is transmitted as a dominant (recessive) bus level, respectively.

8.2.4 Data Field

The data, stored within the Data Field of the Transmit Buffer, are transmitted according to the Data Length Code. Conversely, data of a received Data Frame will be stored in the Data Field of a Receive Buffer. Data is stored byte-wise both for transmission by the microcontroller and on reception by the PCX82C200. The most significant bit of the first data byte (lowest address) is transmitted/received first.

8.2.5 Cyclic Redundancy Code Field (CRC)

The CRC Field consists of the CRC Sequence (15 bits) and the CRC Delimiter (1 recessive bit). The Cyclic Redundancy Code (CRC) encloses the destuffed bit stream of the Start-Of-Frame, Arbitration Field, Control Field, Data Field and CRC Sequence. The most significant bit of the CRC Sequence is transmitted/received first. This frame check sequence, implemented in the PCX82C200, is derived from a cyclic redundancy code best suited for frames with a total bit count of less than 127 bits, see section 8.8.3 With Start-Of-Frame (dominant bit) included in the code word, any rotation of the code word can be detected by the absence of the CRC Delimiter (recessive bit).

8.2.6 Acknowledge Field (ACK)

The Acknowledge Field consists of two bits, the Acknowledge Slot and the Acknowledge Delimiter, which are transmitted with a recessive level by the transmitter of the Data Frame. All PCX82C200's having received the matching CRC Sequence, report this by overwriting the transmitter's recessive bit in the Acknowledge Slot with a dominant bit (see section 8.9.2). Thereby a transmitter, still monitoring the bus level recognizes that at least one receiver within the network has received a complete and correct message (i.e. no error was found). The Acknowledge Delimiter (recessive bit) is the second bit of the Acknowledge Field. As a result, the Acknowledge Slot is surrounded by two recessive bits: the CRC Delimiter and the Acknowledge Delimiter.

All nodes within a CAN network may use all the information coming to the network by the PCX82C200's (shared memory concept). Therefore, acknowledgement and error handling are defined to provide all information in a consistent way throughout this shared memory. Hence, there is no reason to discriminate different receivers of a message in the acknowledge field. If a

node is disconnected from the network due to bus failure, this particular node is no longer part of the shared memory. To identify a 'lost node' additional and application specific precautions are required.

8.2.7 End-Of-Frame

Each Data Frame or Remote Frame is delimited by the End-Of-Frame bit sequence which consists of seven recessive bits (exceeds the bit stuff width by two bits). Using this method a receiver detects the end of a frame independent of a previous transmission error because the receiver expects all bits up to the end of the CRC sequence to be coded by the method of bit-stuffing (see section 8.7.3). The bit-stuffing logic is deactivated during the End-Of-Frame sequence.

8.3 Remote Frame

A PCX82C200, acting as a receiver for certain information may initiate the transmission of the respective data by transmitting a Remote Frame to the network, addressing the data source via the Identifier and setting the RTR bit HIGH (remote; recessive bus level). The Remote Frame is similar to the Data Frame with the following exceptions:

- RTR bit is set HIGH
- Data Length Code is ignored
- no Data Field contained.

Note that the Data Length Code value should be the same as for the corresponding Data Frame (although this is ignored for a Remote Frame).

A Remote Frame is composed of six different bit fields:

- Start-Of-Frame
- Arbitration Field
- Control Field
- CRC-Field
- Acknowledge Field
- End-Of-Frame.

See section 8.2 for a more detailed explanation of the Remote Frame bit fields.

8.4 Error Frame

The Error Frame consists of two different fields. The first field is accomplished by the superimposing of Error Flags contributed from different PCX82C200s. The second field is the Error Delimiter (see Fig.7).

8.4.1 Error Flag

There are two forms of an Error Flag:

- Active Error Flag, consists of six consecutive dominant bits
- Passive Error Flag, consists of six consecutive recessive bits unless it is overwritten by dominant bits from other PCX82C200's.

An error-active PCX82C200 (see section 8.9) detecting an error condition signals this by transmission of an Active Error Flag. This Error Flag's form violates the bit-stuffing law (see section 8.7.3) applied to all fields, from Start-Of-Frame to CRC Delimiter, or destroys the fixed form of the fields Acknowledge Field or End-Of-Frame (see Fig.6). Consequently, all other PCX82C200's detect an error condition and start transmission of an Error Flag. Therefore the sequence of dominant bits, which can be monitored on the bus, results from a superposition of different Error Flags transmitted by individual PCX82C200's. The total length of this sequence varies between six (minimum) and twelve (maximum) bits.

An error-passive PCX82C200 (see section 8.9) detecting an error condition tries to signal this by transmission of a Passive Error Flag. The error-passive PCX82C200 waits for six consecutive bits with identical polarity, beginning at the start of the Passive Error Flag. The Passive Error Flag is complete when these six identical bits have been detected.

8.4.2 Error Delimiter

The Error Delimiter consists of eight recessive bits and has the same format as the Overload Delimiter. After transmission of an Error Flag, each PCX82C200 monitors the bus-line until it detects a transition from a dominant-to-recessive bit level. At this point in time, every PCX82C200 has finished sending its Error Flag and all PCX82C200's start transmission of seven recessive bits (plus the recessive bit at dominant-to-recessive transition, results in a total of eight recessive bits). After this event and an Intermission Field all error-active PCX82C200's within the network can start a transmission simultaneously.

If a detected error is signalled during transmission of a Data Frame or Remote Frame, the current message is spoiled and a retransmission of the message is initiated.

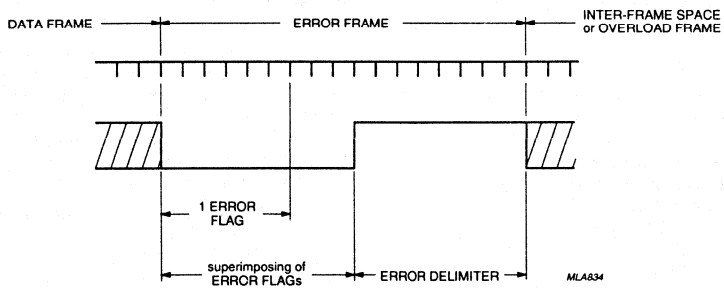


Fig.7 Error Frame.

If a PCX82C200 monitors any deviation of the Error Frame, a new Error Frame will be transmitted. Several consecutive Error Frame's may result in the PCX82C200 becoming error-passive and leaving the network unblocked.

In order to terminate an Error Flag correctly, an error-passive CAN-bus controller requires the bus to be Bus-Idle (see section 8.6.2) for at least three bit periods (if there is a local error at an error-passive receiver). Therefore a CAN-bus should not be 100% permanently loaded.

8.5 Overload Frame

The Overload Frame consists of two fields, the Overload Flag and the Overload Delimiter. There are two conditions in the CAN-protocol which lead to the transmission of an Overload Flag:

- condition 1; receiver circuitry requires more time to process the current data before receiving the next frame (receiver not ready)
- condition 2; detection of a dominant bit during Intermission Field (see section 8.6.1).

The transmission of an Overload Frame may only start:

- condition 1; during the first bit period of an expected Intermission Field
- condition 2; one bit period after detecting the dominant bit during Intermission Field.

The PCX82C200 will never initiate transmission of a condition 1 Overload Frame and will only react on a transmitted condition 2 Overload Frame, according to the CAN-protocol. No more than two Overload Frames are generated to delay a Data Frame or a Remote Frame. Although the overall form of the Overload Frame corresponds to that of the Error Frame, an Overload Frame does not initiate or require the retransmission of the preceding frame.

8.5.1 Overload Flag

The Overload Flag consists of six dominant bits and has a similar format to the Error Flag.

The Overload Flag's form corrupts the fixed form of the Intermission Field. All other PCX82C200's detecting the overload condition also transmit an Overload Flag (condition 2).

8.5.2 Overload Delimiter

The Overload Delimiter consists of eight recessive bits and takes the same form as the Error Delimiter. After transmission of an Overload Flag, each PCX82C200 monitors the bus-line until it detects a transition from a

dominant-to-recessive bit level. At this point in time, every PCX82C200 has finished sending its Overload Flag and all PCX82C200's start simultaneously transmitting seven more recessive bits.

8.6 Inter-Frame Space

Data Frames and Remote Frames are separated from preceding frames (all types) by an Inter-Frame Space, consisting of an Intermission Field and a Bus-Idle. Error-passive PCX82C200's also send a Suspend Transmission (see section 8.9.5) after transmission of a message. Overload Frames and Error Frames are not preceded by an Inter-Frame Space.

8.6.1 Intermission Field

The Intermission Field consists of three recessive bits. During an Intermission period, no frame transmissions will be started by any PCX82C200. An Intermission is required to have a fixed time period to allow a CAN-controller to execute internal processes prior to the next receive or transmit task.

8.6.2 Bus-Idle

The Bus-Idle time may be of arbitrary length (minimum 0 bit). The bus is recognized to be free and a CAN-controller having information to transmit may access the bus. The detection of a dominant bit level during Bus-Idle on the bus is interpreted as the Start-Of-Frame.

8.7 Bus organization

Bus organization is based on five basic rules described in the following paragraphs.

8.7.1 Bus access

PCX82C200's only start transmission during the Bus-Idle state. All PCX82C200's synchronize on the leading edge of the Start-Of-Frame (hard synchronization).

8.7.2 Arbitration

If two or more PCX82C200's simultaneously start transmitting, the bus access conflict is solved by a bit-wise arbitration process during transmission of the Arbitration Field.

During arbitration every transmitting PCX82C200 compares its transmitted bit level with the monitored bus level. Any PCX82C200 which transmits a recessive bit and monitors a dominant bus level immediately becomes the receiver of the higher priority message on the bus without corrupting any information on the bus. Each message contains an unique Identifier and a RTR bit describing the type of data within the message.

The Identifier together with the RTR bit implicitly define the message's bus access priority. During arbitration the most significant bit of the Identifier is transmitted first and the RTR bit last. The message with the lowest binary value of the Identifier and RTR bit has the highest priority. A Data Frame has higher priority than a Remote Frame due to its RTR bit having a dominant level.

For every Data Frame there is an unique transmitter. For reasons of compatibility with other CAN-bus controllers, use of the Identifier binary bit pattern ID = 1111111XXXX (X being bits of arbitrary level) is forbidden. The number of available different Identifiers is 2032 ($2^{11} - 2^4$).

8.7.3 Coding/decoding

The following bit fields are coded using the bit-stuffing technique:

- Start-Of-Frame
- Arbitration Field
- Control Field
- Data Field
- CRC Sequence.

When a transmitting PCX82C200 detects five consecutive bits of identical polarity to be transmitted, a complementary (stuff) bit is inserted into the transmitted bit-stream.

When a receiving PCX82C200 has monitored five consecutive bits with identical polarity in the received bit streams of the above described bit fields, it automatically deletes the next received (stuff) bit. The level of the deleted stuff bit has to be the complement of the previous bits; otherwise a Stuff Error will be detected and signalled (see section 8.8.2).

The remaining bit fields or frames are of fixed form and are not coded or decoded by the method of bit-stuffing.

The bit-stream in a message is coded according to the Non-Return-to-Zero (NRZ) method, i.e. during a bit period, the bit level is held constant, either recessive or dominant.

8.7.4 Error signalling

A PCX82C200 which detects an error condition, transmits an Error Flag. Whenever a Bit Error, Stuff Error, Form Error or an Acknowledgement Error is detected, transmission of an Error Flag is started at the next bit. Whenever a CRC Error is detected, transmission of an Error Flag starts at the bit following the Acknowledge Delimiter, unless an Error Flag for another error condition has already started. An Error Flag violates the bit-stuffing law or corrupts the fixed form bit fields. A violation of the bit-stuffing law affects any PCX82C200 which detects the error condition. These devices will also transmit an Error Flag.

An error-passive PCX82C200 (see section 8.9) which detects an error condition, transmits a Passive Error Flag. A Passive Error Flag is not able to interrupt a current message at different PCX82C200's, but this type of Error Flag may be cancelled by other PCX82C200's. After having detected an error condition, an error-passive PCX82C200 will wait for six consecutive bits with identical polarity and when monitoring them, interpret them as an Error Flag.

After transmission of an Error Flag, each PCX82C200 monitors the bus-line until it detects a transition from a dominant-to-recessive bit level. At this point in time, every PCX82C200 has finished transmitting its Error Flag and all PCX82C200's start transmitting seven additional recessive bits (Error Delimiter, see section 8.4.2).

The message format of a Data Frame or Remote Frame is defined in such a way, that all detectable errors can be signalled within the message transmission time and therefore, it is very simple for a PCX82C200 to associate an Error Frame to the corresponding message and to initiate retransmission of the corrupted message.

If a PCX82C200 monitors any deviation of the fixed form of an Error Frame, it transmits a new Error Frame.

8.7.5 Overload signalling

Some CAN-controllers (but not the PCX82C200) require to delay the transmission of the next Data Frame or Remote Frame by transmitting one or more Overload Frames. The transmission of an Overload Frame must start during the first bit of an expected Intermission. Transmission of Overload Frames which are reactions on a dominant bit during an expected Intermission Field, start one bit after this event.

Though the format of Overload Frame and Error Frame are identical, they are treated differently. Transmission of an Overload Frame during Intermission Field does not initiate the retransmission of any previous Data Frame or Remote Frame.

If a CAN-controller which transmitted an Overload Frame monitors any deviation of its fixed form, it transmits an Error Frame.

8.8 Error detection

The processes described in the following paragraphs are implemented in the PCX82C200 for error detection.

8.8.1 Bit Error

A transmitting PCX82C200 monitors the bus on a bit-by-bit basis. If the bit level monitored is different from the transmitted one, a Bit Error is signalled. The exceptions being:

- during the Arbitration Field, a recessive bit can be overwritten by a dominant bit. In this case, the PCX82C200 interprets this as a loss of arbitration
- during the Acknowledge Slot, only the receiving PCX82C200's are able to recognize a Bit Error.

8.8.2 Stuff Error

The following bit fields are coded using the bit-stuffing technique:

- Start-Of-Frame
- Arbitration Field
- Control Field
- Data Field
- CRC Sequence.

There are two possible ways of generating a Stuff Error:

- the disturbance generates more than the allowed five consecutive bits with identical polarity. These errors are detected by all PCX82C200's
- a disturbance falsifies one or more of the five bits preceding the stuff bit. This error situation is not recognized as a Stuff Error by the receivers. Therefore, other error detection processes may detect this error condition such as: CRC check, format violation at the receiving PCX82C200's or Bit Error detection by the transmitting PCX82C200.

8.8.3 CRC Error

To ensure the validity of a transmitted message all receivers perform a CRC check. Therefore, in addition to the (destuffed) information digits (Start-Of-Frame up to Data Field), every message includes some control digits (CRC Sequence; generated by the transmitting PCX82C200 of the respective message) used for error detection.

The code used for the PCX82C200 bus controller is a (shortened) BCH code, extended by a parity check and has the following attributes:

- 127 bits as maximum length of the code
- 112 bits as maximum number of information digits (maximum 83 bits are used by PCX82C200)
- length of the CRC Sequence amounts to 15 bits
- Hamming distance d = 6.

As a result, (d-1) random errors are detectable (some exceptions exist).

The CRC Sequence is calculated by the following procedure:

1. the destuffed bit stream consisting of Start-Of-Frame up to the Data Field (if present) is interpreted as a polynomial with coefficients of 0 or 1
2. this polynomial is divided (modulo-2) by the following generator polynomial:

$f(X) = (X^{14} + X^9 + X^8 + X^6 + X^5 + X^4 + X^2 + X + 1)(X + 1)$ = 1100010110011001 binary.

The remainder of this polynomial division is the CRC Sequence which includes a parity check. Burst errors are detected up to a length of 15 [degree of f(X)]. Multiple errors (number of disturbed bits at least d = 6) are not detected with a residual error probability of 2^{-15} ($\approx 3 \times 10^{-5}$) by CRC check only.

8.8.4 Form Error

Form Errors result from violation of the fixed form of the following bit fields:

- End-Of-Frame
- Intermission
- Acknowledge Delimiter
- CRC Delimiter.

During the transmission of these bit fields an error condition is recognized if a dominant bit level instead of a recessive one is detected.

8.8.5 Acknowledgement Error

This is detected by a transmitter whenever it does not monitor a dominant bit during the Acknowledge Slot.

8.8.6 Error detection by an Error Flag of another PCX82C200

The detection of an error is signalled by transmitting an Error Flag. An Active Error Flag causes a Stuff Error, a Bit Error or a Form Error at all other PCX82C200's.

8.8.7 Error detection capabilities

Errors which occur at all PCX82C200's (global errors) are 100% detected. For local errors, i.e. for errors occurring at some PCX82C200's only, the shortened BCH code, extended by a parity check, has the following error detection capabilities:

- up to five single bit errors are 100% detected, even if they are distributed randomly within the code
- all single bit errors are detected if their total number (within the code) is odd
- the residual error probability of the CRC check amounts to 3×10^{-5}. As an error may be detected not only by CRC check but also by other detection processes described in sections 8.8.1 to 8.8.5, the residual error probability is several magnitudes less than 3×10^{-5} for undetected errors.

8.9 Error confinement (definitions)

8.9.1 Bus-Off

A PCX82C200 which has too many unsuccessful transmissions, relative to the number of successful transmissions, will enter the Bus-Off state. It remains in this state, neither receiving nor transmitting messages until the Reset Request bit is set LOW (absent) and both Error Counters are set to '0' (see note 1 to Table 5 and section 8.10.3).

8.9.2 Acknowledge (ACK)

A PCX82C200 which has received a valid message correctly, indicates this to the transmitter by transmitting a dominant bit level on the bus during the Acknowledge Slot, independent of accepting or rejecting the message.

8.9.3 Error-Active

An error-active PCX82C200 is in its normal operating state able to receive and to transmit normally and also to transmit an active Error Flag (see section 8.10.3).

8.9.4 Error-Passive

An error-passive PCX82C200 may transmit or receive messages normally. In the case of a detected error condition it transmits a Passive Error Flag, instead of an Active Error Flag. Hence the influence on bus activities by an error-passive PCX82C200 (e.g. due to a malfunction) is reduced.

8.9.5 Suspend Transmission

After an error-passive PCX82C200 has transmitted a message, it sends eight recessive bits after the Intermission Field and then checks for Bus-Idle. If during Suspend Transmission another PCX82C200 starts transmitting a message the suspended PCX82C200 will become the receiver of this message; otherwise being in Bus-Idle it may start to transmit a further message.

8.9.6 Start-up

A PCX82C200 which was either switched off or is in the Bus-Off state, must run a start-up routine in order to:

- synchronize with other available PCX82C200's, before starting to transmit. Synchronizing is achieved, when 11 recessive bits, equivalent to Acknowledge Delimiter, End-Of-Frame and Intermission Field, have been detected (Bus-Free)
- wait for other PCX82C200s without passing into the Bus-Off state (due to a missing acknowledge), if there is no other PCX82C200 currently available.

8.10 Aims of error confinement

8.10.1 Distinction of short and long-lasting disturbances

The microcontroller must be informed when there are long-lasting disturbances and when bus activities have returned to normal operation. During long-lasting disturbances, a PCX82C200 enters the Bus-Off state and the microcontroller may use default values.

Minor disturbances of bus activities will not affect a PCX82C200. In particular, a PCX82C200 does not enter the Bus-Off state or inform the microcontroller of a short-lasting bus disturbance.

8.10.2 Detection and localization of hardware disturbances and defects

The rules for error confinement are defined by the CAN-protocol specification (and implemented in the PCX82C200), in that the PCX82C200, being nearest to the error-locus, reacts with a high probability, the quickest (i.e. becomes error-passive or Bus-Off). hence errors can be localized and their influence on normal bus activities is minimized.

8.10.3 Error Confinement

All PCX82C200's contain a Transmit Error Counter and a Receive Error Counter, which registers errors during the transmission and the reception of messages, respectively.

If a message is transmitted or received correctly, the count is decreased. In the event of an error, the count is increased. The Error Counters have an non-proportional method of counting: an error causes a larger counter increase than a correctly transmitted/received message causes the count to decrease. Over a period of time this may result in an increase in error counts, even if there are fewer corrupted messages than uncorrupted ones. The level of the Error Counters reflect the relative frequency of disturbances. The ratio of increase/decrease depends on the acceptable ratio of invalid/valid messages on the bus and is hardware implemented to eight.

If one of the Error Counters exceeds the Warning Limit of 96 error points, indicating a significant accumulation of error conditions, this is signalled by the PCX82C200 (Error Status, Error Interrupt).

A PCX82C200 operates in the error-active mode until it exceeds 127 error points on one of its Error Counters. At this point it will enter the error-passive state.

A transmit error which exceeds 255 error points results in the PCX82C200 entering the Bus-Off state.

9 LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range	4.5	5.5	V
I_I	input/output current on any pin except from TX0 and TX1	–	±10	mA
I_{OT}	sink current of TX0 and TX1 together (note 1)	–	28	mA
I_{OT}	source current of TX0 and TX1 together (note 1)	–	–20	mA
T_{amb}	operating ambient temperature range:			
	PCA82C200	–40	+125	°C
	PCF82C200	–40	+85	°C
T_{stg}	storage temperature range	–65	+150	°C
P_{tot}	total power dissipation (note 2)	–	1	W

Notes

1. I_{OT} is allowed in case of a bus failure condition because then the TX-outputs are switched off automatically after a short time (Bus-Off state). During normal operation I_{OT} is a peak current, permitted for t < 100 ms. The average output current must not exceed 10 mA for each TX-output.
2. The value is based on the maximum allowable die temperature and the thermal resistance of the package, not on device power consumption.

10 DC CHARACTERISTICS

$V_{DD} \leq 5$ V ±10%; $V_{SS} = 0$ V; $T_{amb} = -40$ to +125 °C for the PCA82C200 and $T_{amb} = -40$ to +85 °C for the PCF82C200. All voltages measured with respect to V_{ss} unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DD}	supply voltage range		4.5	5.5	V
I_{DD}	supply current: operating	$\overline{RST} = V_{SS}$; f_{CLK} = 16 MHz (note 1)	–	15	mA
I_{sm}	sleep mode	oscillator inactive (note 2)	–	40	µA
Inputs					
V_{IL1}	LOW level input voltage (except XTAL1, RX0 and RX1)		–0.5	0.8	V
V_{IL2}	XTAL1 LOW level input voltage		–	$0.2V_{DD}$	V
V_{IH1}	HIGH level input voltage (except XTAL1, $\overline{RST}$, RX0 and RX1)		3.2	V_{DD} + 0.5	V
V_{IH2}	XTAL1 HIGH level input voltage		$0.7V_{DD}$	–	V
V_{IH3}	$\overline{RST}$ HIGH level input voltage		3.3	V_{DD} + 0.5	V
I_{LI}	input leakage current (except XTAL1, RX0 and RX1)	0.45 V < V_I < V_{DD}	–	±10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Outputs					
V_{OL}	LOW level output voltage (except XTAL2, TX0 and TX1)	I_{OL} = 1.6 mA	–	0.45	V
V_{OH1}	HIGH level output voltage (except TX0, TX1, $\overline{INT}$ and CLK OUT)	I_{OH} = –80 µA	2.4	–	V
V_{OH2}	CLK OUT HIGH level output voltage	I_{OH} = –80 µA	$0.8V_{DD}$	–	V
CAN input comparator					
		V_{DD} = 5 V ±5%; 1.4 V < V_I < V_{DD} – 1.4 V			
V_{DIF}	differential input voltage	note 3	±42	–	mV
V_{HYST}	hysteresis voltage	note 3	12	45	mV
I_I	input current		–	±400	nA
CAN output driver					
		V_{DD} = 5 V ±5%			
V_{OLT}	TX0 and TX1 output voltage LOW	I_O = 1.2 mA (note 3)	–	0.1	V
		I_O = 10 mA	–	1.0	V
V_{OHT}	TX0 and TX1 output voltage HIGH	I_O = 1.2 mA (note 3)	V_{DD} – 0.1	–	V
		I_O = 10 mA	V_{DD} – 1.0	–	V

Notes

1. (AD0 – AD7) = ALE = $\overline{RD}$ = $\overline{WR}$ = $\overline{CS}$ = V_{DD}; MODE = V_{SS}; RX0 = 2.7 V; RX1 = 2.3 V; XTAL1 = 0.5V/V_{DD} – 0.5 V; all outputs unloaded.
2. (AD0 – AD7) = ALE = $\overline{RD}$ = $\overline{WR}$ = $\overline{INT}$ = $\overline{RST}$ = $\overline{CS}$ = MODE = RX0 = V_{DD}; RX1 = XTAL1 = V_{SS}; all outputs unloaded.
3. Not tested during production.

11 AC CHARACTERISTICS

V_{DD} = 5 V ±10%; V_{SS} = 0 V; C_L = 50 pF (output pins); T_{amb} = −40 to +85/125 °C; unless otherwise specified (note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{CLK}	oscillator frequency		3	16	MHz
t_{SU1}	address set-up to ALE/AS LOW		10	–	ns
t_{HD1}	address hold time		22	–	ns
t_{PW1}	ALE/AS pulse width		35	–	ns
t_{VD1}	$\overline{RD}$ LOW to valid data output	Intel mode	–	60	ns
t_{VD2}	E HIGH to valid data output	Motorola mode	–	60	ns
t_{DF1}	data float after $\overline{RD}$ HIGH	Intel mode	10	55	ns
t_{DF2}	data float after E LOW	Motorola mode	10	55	ns
t_{SU2}	input data set-up to $\overline{WR}$ HIGH	Intel mode	30	–	ns
t_{HD2}	input data hold after $\overline{WR}$ HIGH	Intel mode	13	–	ns
t_{HH1}	$\overline{WR}$ HIGH to next ALE HIGH		23	–	ns
t_{LH3}	E LOW to next AS HIGH	Motorola mode	23	–	ns
t_{SU3}	input data set-up to E LOW	Motorola mode	30	–	ns
t_{HD3}	input data hold after E LOW	Motorola mode	25	–	ns
t_{LL1}	ALE LOW to $\overline{WR}$ LOW	Intel mode	10	–	ns
t_{LL2}	ALE LOW to $\overline{RD}$ LOW	Intel mode	10	–	ns
t_{LH1}	AS LOW to E HIGH	Motorola mode	10	–	ns
t_{SU4}	set-up time of RD/$\overline{WR}$ to E HIGH	Motorola mode	20	–	ns
t_{PW2}	$\overline{WR}$ pulse width	Intel mode	170	–	ns
t_{PW3}	$\overline{RD}$ pulse width	Intel mode	170	–	ns
t_{PW4}	E pulse width	Motorola mode	170	–	ns
t_{LL3}	$\overline{CS}$ LOW to $\overline{WR}$ LOW	Intel mode	0	–	ns
t_{LL4}	$\overline{CS}$ LOW to $\overline{RD}$ LOW	Intel mode	0	–	ns
t_{LH2}	$\overline{CS}$ LOW to E HIGH	Motorola mode	0	–	ns
Input comparator/output driver					
t_{sd}	sum of the input and output delays	V_{DD} = 5 V ±5%; V_{DIF} = ±42 mV; 1.4 V < V_I < V_{DD} − 1.4 mV	–	62	ns

Note

1. AC characteristics are not tested.

11.1 AC timing diagrams

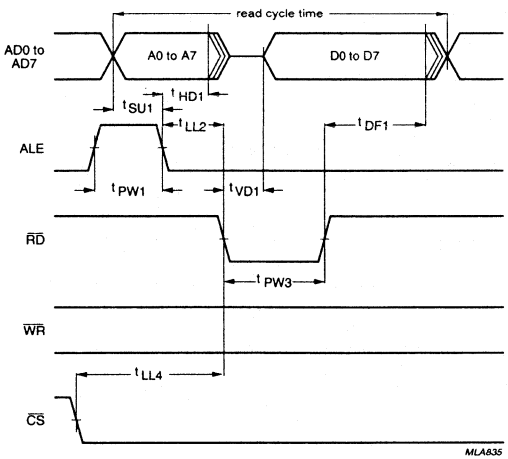


Fig.8 Read cycle timing diagram; Intel mode.

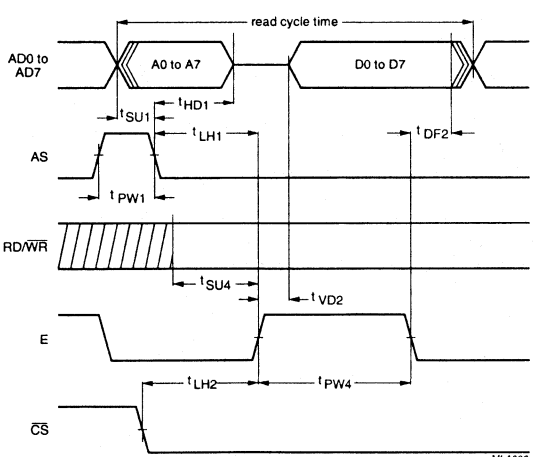


Fig.9 Read cycle timing diagram; Motorola mode.

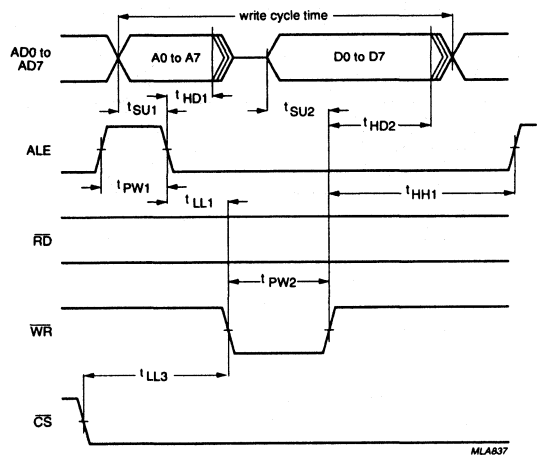


Fig.10 Write cycle timing diagram; Intel mode.

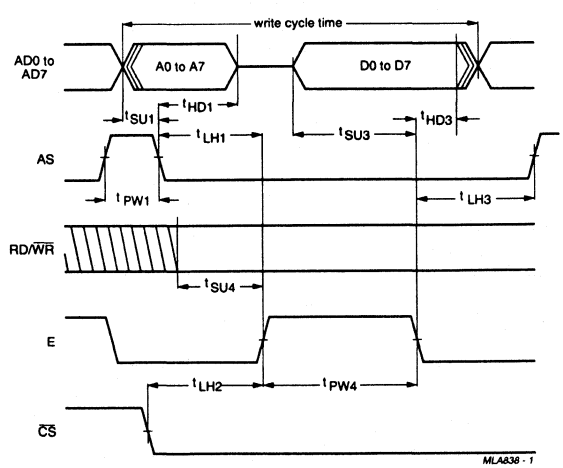


Fig.11 Write cycle timing diagram; Motorola mode.

11.2 Additional AC information

To provide optimum noise immunity under worse case conditions, the chip is powered by three separate pins and grounded by three separate pins, see Fig.12.

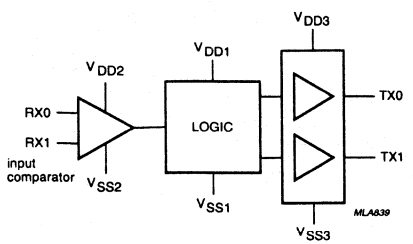


Fig.12 Optimized noise immunity block diagram.

12 DEVELOPMENT SUPPORT AND TOOLS

12.1 The PCX82C200 Evaluation Board

Philips offers powerful support during the design and test stages of CAN networks, working closely with customers to develop their systems. The 'Philips Stand-alone CAN-Controller (PSCC) Evaluation Board' is a versatile tool being a ready-to-use hardware and software module, very similar to a real CAN module. Since a 5 V power supply is provided, the board can be used in any vehicle without modification. An RS232 interface allows a terminal or a PC with terminal-emulation software to be connected to the board. The board comprises:

- a PCX82C200 CAN-bus controller
- a PCA80C552 microcontroller with up to 32K x 8 bits external RAM and EPROM
- a 5 V power supply with protection against car battery disturbances
- two different physical CAN-bus interfaces (selectable)
- an RS232 interface
- demonstration hardware
- a wrap field for customer-specific circuitry.

The software provided with the board supports "learning about CAN" and assists in prototype (e.g. in-vehicle) networks. It provides:

- demonstration software (automatically-initiated)
- the menu-driven software comprises:
  - a facility to alter the contents of the PCX82C200 registers
  - a bus monitor to receive messages from the CAN-bus and to display them on a terminal
  - a download facility for the user's application software.

With these facilities the board is a basis for prototype modules; when using entirely your own software, the board can be used as a custom, debugged and proven hardware module.

12.2 Advanced support

For further development support, Philips subcontractor I+ME offers a complete set of development tools including:

- a CAN simulator; CAN/Net Sim
- an emulator; CAN/Net Emu
- a network analyzer; CAN/Net Anal.

I+ME can be contacted through the following address:

I+ME GmbH
Ferdinandstrasse 15 A
D-3340 Wolfenbuettel
West Germany.

Phone: ++49-5331-72066
Fax: ++49-5331-32455

PCA82C200 CAN controller — Application report

1. Introduction

The integrated circuit PCA82C200 (from now on, abbreviated to 82C200) is a versatile CAN (Controller Area Network) protocol controller designed for automotive and industrial applications. This device is also known as "Philips Stand-Alone CAN Controller" (PSCC).

The 82C200 fulfills the complete CAN specification, to provide the following important features:

- multi-master operation in a serial communication network with an unlimited number of active network nodes,
- programmable data transmission rate, up to 1 Mbit/s,
- very low probability of undetected errors, due to powerful error handling,
- at least 40 m maximum distance between two bus nodes at a data transmission rate of 1 Mbit/s, lower transmission rates allow even longer distances,
- guaranteed latency time supporting real-time applications.

The main applications for CAN-based networks are:

- in an automotive environment (SAE classes A, B and C):
  - low data transmission rate (e.g. 20 kbit/s) for multiplex-wiring systems,
  - medium data transmission rate (e.g. 100 kbit/s) for vehicle parametric data and diagnostics,
  - high data transmission rate (up to 1 Mbit/s) for engine management control or drive train control applications.
- in an industrial environment:
  - as a field bus in industrial plants,
  - as an "in-machine" local bus in large tooling equipment, etc.

The purpose of this technical note is to describe simple and proven circuit examples for a module in a CAN network based on several 82C200s. The 82C200 may be interfaced to various types of microcontrollers/microprocessors such as the 80C51 family and some members of the 68XX family.

Contents

Since the 82C200 needs an interface with the physical layer (i.e. the bus wires), three examples of discrete interface circuits are also described. To apply and understand the application examples given in this document, the reader should be familiar with the Philips PCA82C200 data sheet.

2. Hardware

This section covers hardware considerations of a CAN-based module in a network. The first part describes the interface between the 82C200 and two commonly-used microcontroller/processor families. The second part deals with the interface between the 82C200 and the transmission medium.

2.1. CPU interfacing

The 82C200 is designed to interface efficiently with two commonly-used microcontroller and microprocessor families: the 80C51-type and some members of the 68XX family. The wiring of the MODE pin (pin 11) determines the operating mode of the 82C200's CPU interface (see table 1).

Table 1. Modes of the 82C200 CPU interface

82C200		80C51 mode	68XX mode
pin 11 (MODE)	connected to:	V_{DD} (+5 V)	V_{SS} (0 V)
pin 3		ALE	AS
pin 5		$\overline{RD}$	E
pin 6		$\overline{WR}$	R/$\overline{W}$
default CLOCKOUT frequency		OSCIN/2	OSCIN/12

The 80C51-type interface is characterized by the strobe signals:

- $\overline{RD}$,
- $\overline{WR}$,
- ALE (Address Latch Enable).

Figure 1 is a schematic of a typical core of a bus node in a CAN bus system. The 82C200 (U1) is connected to the 8-bit data/address bus of the microcontroller. The 82C200 latches the address internally. Only the 5 lower address bits are used to access the registers in the 82C200, the upper 3 bits are ignored.

The external circuits of the microcontroller U2 (type 80C31) are, as usual, a latch U3 to separate address and data, and an EPROM (U4) to store the object code.

The 82C200 is connected directly to the address/data bus of the microcontroller without an address decoder. As a result, both the EPROM (opcode) and the 82C200 (bus controller) use the same address space, beginning with 0_H. This is not a problem since the strobe signals differentiate between program code access for the EPROM (via $\overline{PSEN}$) and access to the 82C200 (via $\overline{RD}$, $\overline{WR}$). (Note: the MODE pin must be tied to +5 V to enable the 80C51 family interface.)

The reset logic circuit resets the 82C200 and 80C31 after power-on. If it is required to control the hardware reset of the 82C200 by the CPU (e.g. for test purposes or to reset the error counters instantly), the NOT-gate may be replaced by a NOR-gate whose second input is driven by an 80C31 port output pin. During the reset phase of the CPU, all port output pins are set to a logic high until programmed otherwise. Therefore, the reset signal for the 82C200 is active until the 80C31 is programmed to set the relevant port output pin to a logic low.

The TRANSCEIVER circuit performs the following functions:

- it converts signals Tx0, Tx1 into the voltage levels for the bus wires,
- it converts the voltage levels on the bus wires to be compatible with the Rx0, Rx1 inputs of the 82C200.

In addition, the 82C200 is designed to accept interface signals from another microcontroller/processor family: the 68XX family.

The 68XX-type interface is characterized by the strobe signals:

- AS,
- R/$\overline{W}$,
- E.

The AS signal must be connected to the ALE pin of the 82C200, R/$\overline{W}$ to the $\overline{WR}$ pin, and E to the $\overline{RD}$ pin.

When this processor/controller is used, the MODE pin of the 82C200 must be tied to V_{ss} (ground) so that the 82C200 provides the above-mentioned strobe signals. This affects the interface timing of the 82C200 as well as the default frequency on the CLOCKOUT output:

MODE = low → 68XX-type interface → default CLOCKOUT frequency = OSCIN/12,

MODE = high → 80C51-type interface → default CLOCKOUT frequency = OSCIN/2.

OSCIN is the frequency of the crystal connected to the 82C200.

2.2. Single/dual crystal operation

The 82C200 can operate with a crystal oscillator with a maximum frequency of 16 MHz. At this frequency the maximum data transmission rate is 1 Mbit/s. If the CLOCKOUT pin of the 82C200 provides the clock frequency of the CPU, then the CPU requires no additional crystal oscillator.

After power-up, the default CLOCKOUT frequency with a 16 MHz crystal oscillator is:

- 80C51 mode (MODE pin high): 8 MHz,
- 68XX mode (MODE pin low): 1,33 MHz.

The CLOCK DIVIDER register can be programmed with frequency-division register factors of 1, 2, 4, 6, 8, 10, 12, or 14. The frequency of the CLOCKOUT output is calculated as follows:

$$f_{CLOCKOUT} = \frac{\text{82C200 crystal oscillator frequency}}{\text{CLOCK DIVIDER factor}}$$

If another CPU clock frequency value is required (e.g. 12 MHz with an 80C51 controller), there are two options:

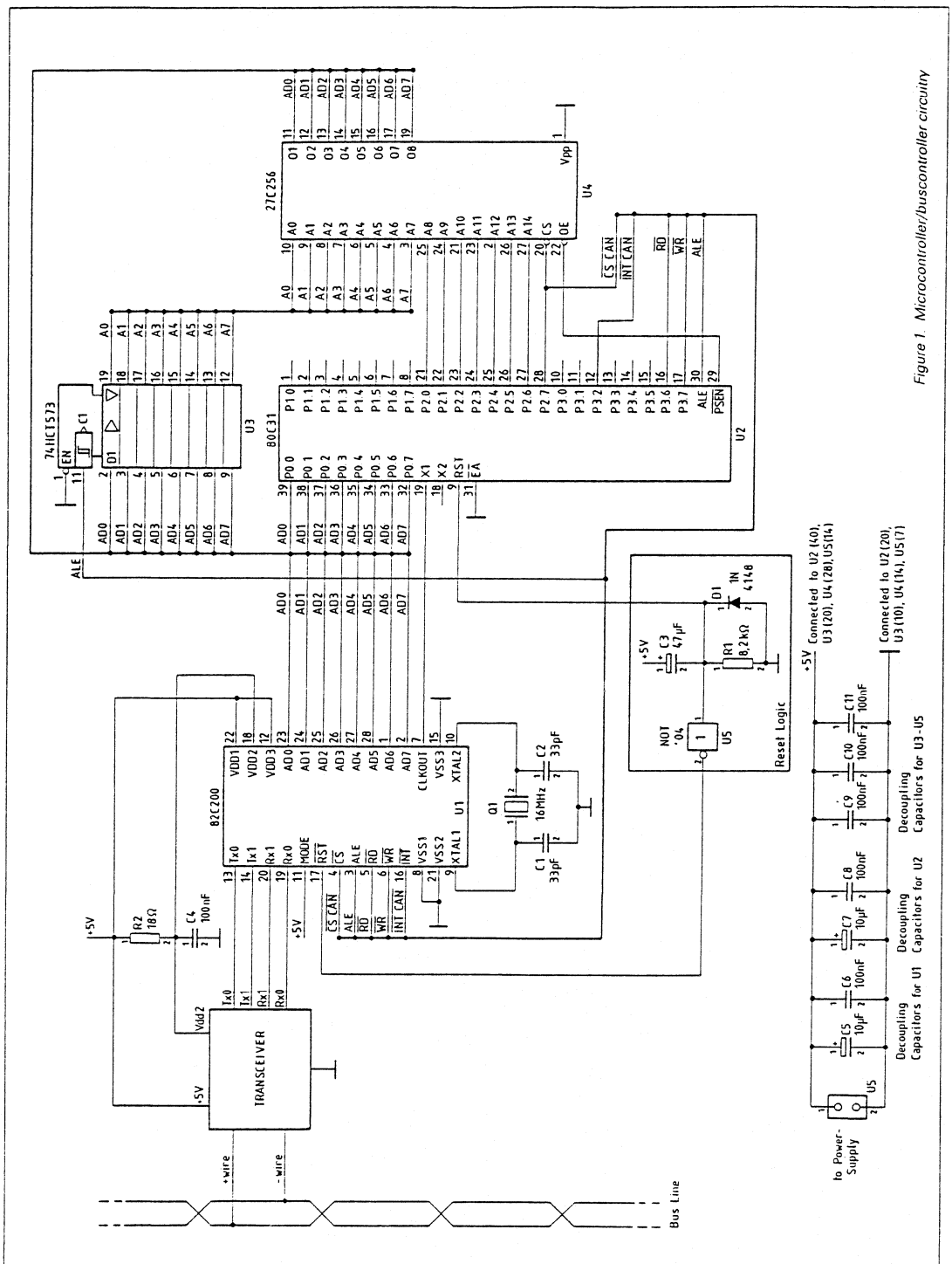


Figure 1. Microcontroller/buscontroller circuitry

1) if the application does not need a data transmission rate of 1 Mbit/s, a lower crystal frequency can be used (e.g. 12 MHz, the maximum CAN bus data transmission rate is then 750 kbit/s);
2) two crystal oscillators can be used, one for the 82C200 and one for the microcontroller/processor.

2.3. Transceiver/Interface to the transmission medium

The transceiver/interface to the transmission medium (from now on, abbreviated to transceiver) converts logic-level data into physical bus data and vice versa.

The 82C200 can be used with different types of transceivers, e.g.:

- wire-type transceivers,
  - one-wire bus with a return (e.g. coaxial cable),
  - two-wire bus, with a common return (e.g. differential voltage, twisted pair);
- optical transceivers (fibre optic links).

There is one common requirement of the transceiver in that it has to support bit-by-bit arbitration over the transmission medium, i.e. one well-defined bit value (referred to as "dominant") must be able to override the other bit value (referred to as "recessive").

Several aspects have to be considered when a physical layer is to be defined:

- the required immunity against noise/overvoltage,
- the necessary immunity against wiring failures (e.g. failure of one wire of a two-wire bus),
- the level of radiation which can be tolerated,
- the allowed power consumption of the network,
- the required data transmission rate,
- the type of connectors to be used.

Three proven examples are provided below, they are:

1) a simple transceiver; this demonstrates the principle of the operation of a simple, two-wire, differential-signal bus,
2) a high-speed, two-wire, differential bus transceiver with external drive transistors (e.g. automotive engine management applications),
3) a low-speed, two-wire, differential bus transceiver with external drive transistors (e.g. automotive multiplex-system applications).

All three examples support the "sleep mode" of the 82C200 where low power is consumed in the recessive state. When the 82C200 is in the "sleep mode" it can be "woken up" via the transceiver.

Note: When designing the Printed Circuit Board (PCB) of a module it is highly recommended to separate the digital circuitry from the analog transceiver circuits.

2.3.1. Simple transceiver

The 82C200 already includes the following transceiver elements:

- the transmitter output stages,
- the receiver input comparator.

This allows the design of a relatively simple interface between the 82C200 and the bus wires. For a simple transceiver, the transmitter output stages may drive the bus wires directly via protection resistors R4 and R5, as shown in figure 2. R8, R9, R10 and R11 determine the voltage at the receiver input comparator of the 82C200 in the recessive state. R6 and R7, together with R8 . . . R11, determine the voltage at the receiver input comparator in the dominant state and the common mode voltage range on the differential signal bus. R3 is a terminating impedance, used on the two outermost network nodes only.

As shown in figure 2, the complete interface between the bus and the 82C200 consists of only 8 or 9 resistors. Actual, typical levels of the two-wire bus signals are shown in figure 3.

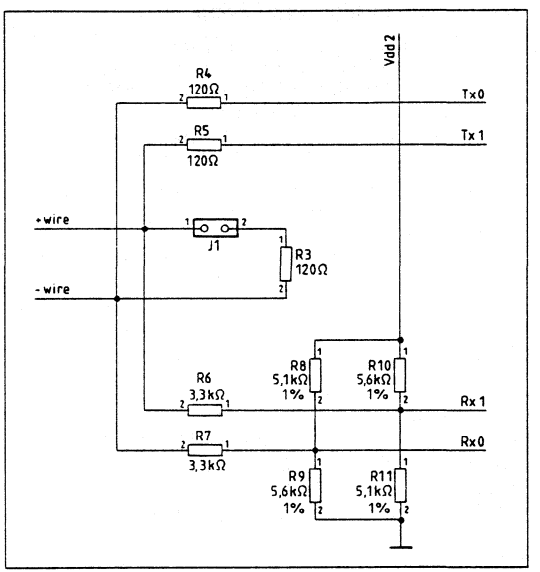


Figure 2. Bus interface for a simple transceiver

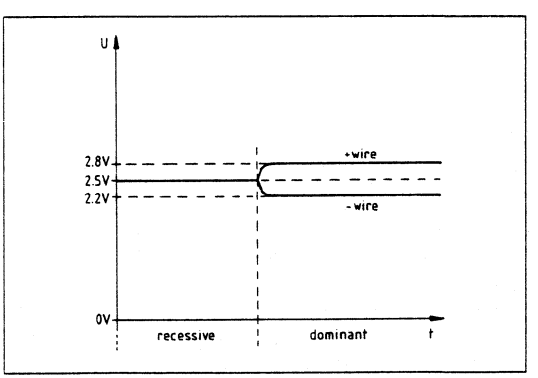


Figure 3. Level diagram for the simple transceiver (bus wire potentials, normal operation)

The operating characteristics of this circuit are:

data transmission rate	0 . . . 1 Mbit/s
number of nodes	2 . . . 16
output current	10 mA
standby current	<1 mA (one node)
value of OUTPUT CONTROL REGISTER	$0AA_H$
general features and remarks	– limited electromagnetic susceptibility performance, – the bus may be blocked when a node is not (or incorrectly) powered.

2.3.2. Transceiver for high-speed application

The circuit, shown in figure 4, is designed for high data transmission rates up to 1 Mbit/s, with a high noise immunity. The transmitter outputs are amplified by the external drive transistors T1 and T2 to increase immunity to noise on the bus signals. Diodes D2 and D3 prevent the bus being blocked when a module is not (or incorrectly) powered.

Capacitors C12 and C13 in combination with resistors R8, R9 provide a low pass filter at the receiver inputs and therefore decrease electromagnetic susceptibility. Resistors R4 and R5 have lower values compared to the simple transceiver to provide more output current (e.g. to drive more nodes). R6 and R7 switch off the driver transistors when the outputs Tx0, Tx1 are floating.

Actual, typical levels of the bus signals are shown in figure 5.

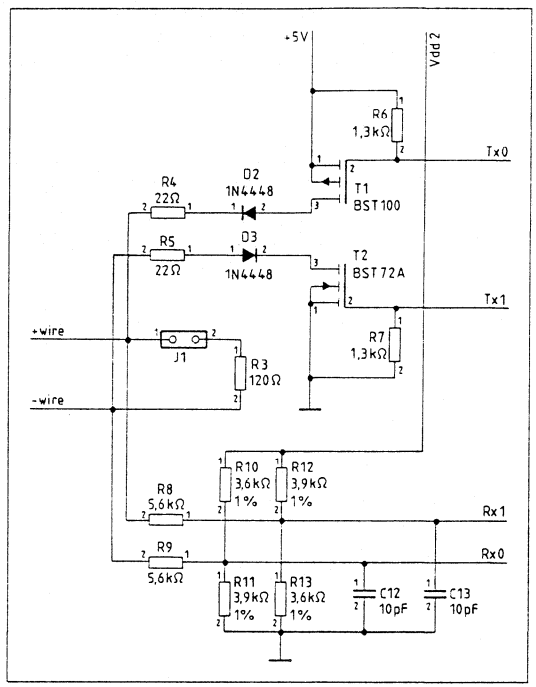


Figure 4. Bus interface for a high-speed application transceiver

The operating characteristics of this circuit are:

data transmission rate	0 . . . 1 Mbit/s
number of nodes	2 . . . 32
output current	30 mA
standby current	<1.4 mA (one node)
value of OUTPUT CONTROL REGISTER	$0FA_H$
general features and remarks	– low susceptibility to electromagnetic noise compared to the simple transceiver, – the bus is not blocked when a node is not (or incorrectly) powered.

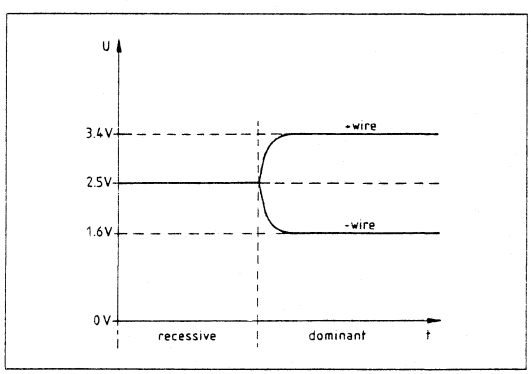


Figure 5. Level diagram for the high-speed application transceiver (bus wire potentials, normal operation)

2.3.3. Transceiver for low-speed application

The interface shown in figure 6 is optimized against wiring failures. It also achieves good immunity to transient noise, and power consumption in the "sleep mode" is very low. These characteristics are intended to satisfy the requirements of "multiplex wiring" in the automotive industry.

The transmitter outputs are amplified by R9, R10, T1 and T2, with protection resistors R7 and R8.

The receiver circuit is basically the same as described in section 2.3.1 but, in this case, the bus signals are coupled into the receiver input comparator of the 82C200 by capacitors C12 and C13 to allow for DC-offset failures (short circuit the electromagnetic susceptibility. D2 and D3 limit the voltage swing at the receiver input comparator.

In case of a cut bus wire, R5 or R6 pulls the respective wire to a definite level so that the differential input voltage at the receiver input stays in the operational range. Consequently, communication is possible via the other undamaged wire.

In comparison to the simple transceiver of chapter 2.3.1, two (instead of one) terminating resistors R3 and R4 are

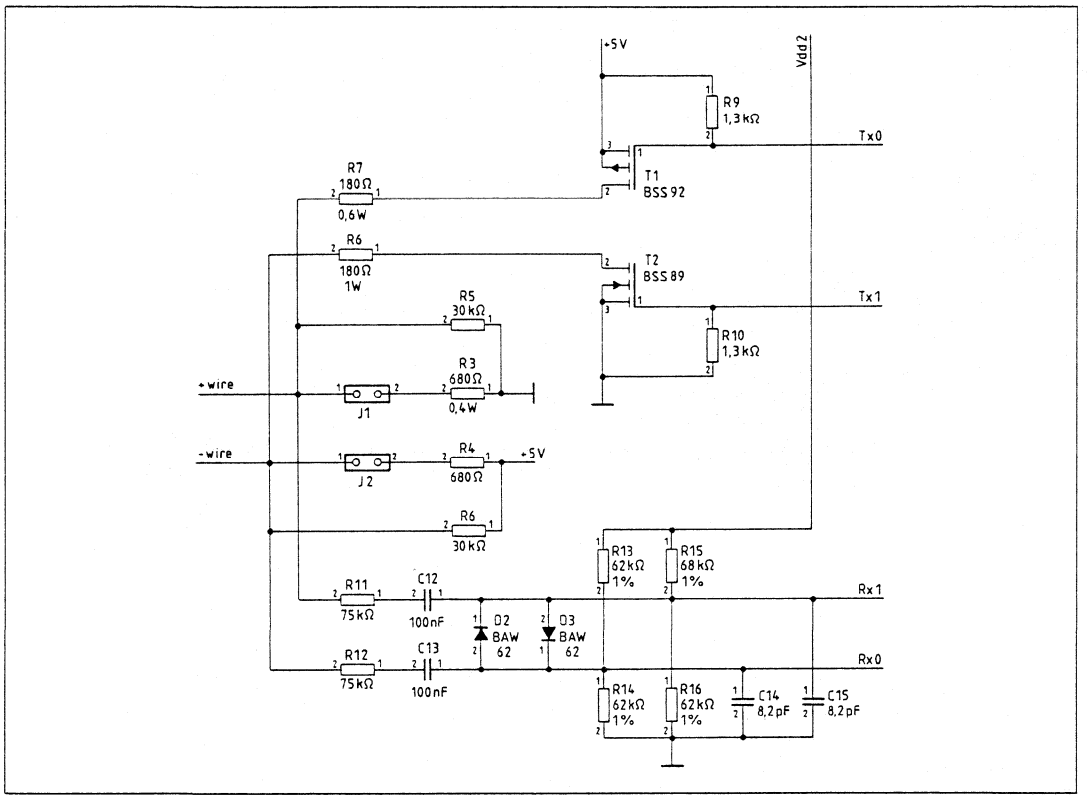


Figure 6. Bus interface for a low-speed application transceiver

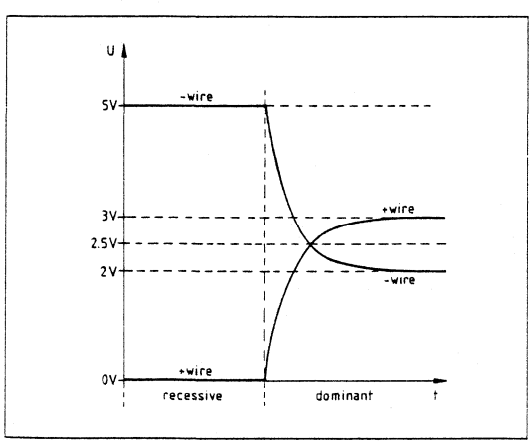


Figure 7. Level diagram for the low-speed application transceiver (bus wire potentials, normal operation)

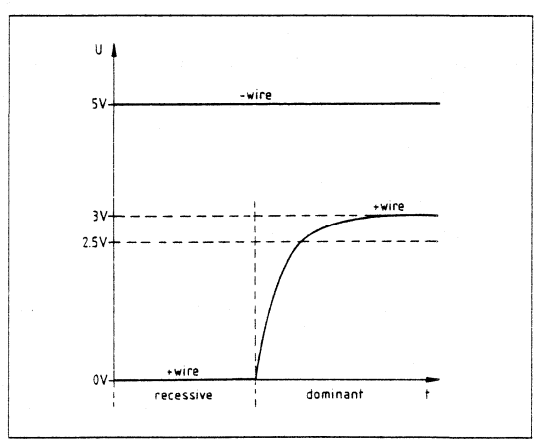


Figure 8. Level diagram (bus wire potentials) for the low-speed application transceiver, special example: interruption of -wire

two bus wires are mutually decoupled to allow for single-wire operation.

Actual, typical levels of the bus signals are shown in figure 7. Figure 8 shows the voltage levels on the two wires when a wiring failure occurs. In this example, the −wire is open-circuit and, as a result, is set to 5 V via R6. The recessive and dominant voltage levels on the +wire are sufficient to maintain communication over the bus.

The operating characteristics of this circuit are:

data transmission rate	5 . . . 100 kbit/s
number of nodes	2 . . . 20
output current	10 mA
standby current	80 µA (one node)
value of OUTPUT CURRENT REGISTER	$0FA_H$
general features and remarks	– low susceptibility to electromagnetic noise compared to the simple transceiver, – the bus is not blocked when a node is not (or incorrectly) powered, – single-wire operation is possible, – low power consumption in the "sleep mode", – high immunity to over-voltage on the bus.

If one of the bus wires is shorted to a voltage higher than 5 V, current flows into the module power supply via R4 and R7. There are two means of protecting the module against an increased supply voltage:

- The current is absorbed by the circuit loads of the module.
- Additional circuit loads are provided, e.g. a sink path for the module power supply. (This increases in importance when the normal sink capability is reduced, as in the "sleep mode".)

3. Programming the PCA82C200

This section surveys the registers of the 82C200 in use in an application and basic flow charts for programming the 82C200 via these registers.

3.1. Register survey

A survey of all 82C200 registers is given in figure 9.

3.2. Basic functions of the PCA82C200

In this section basic flow charts to program the 82C200 are described:

- initialization of the 82C200,
- transmission,
- reception,
- other events:
  - interrupts
  - polling
  - sleep mode
  - clock divider.

Note: The 82C200 must be initialized after a power-up; this is not necessary when it leaves the "sleep mode"

Table 2. Flow chart of the initialization procedure

(* start initialization; write CONTROL REGISTER *)
- set RESET_REQUEST := "present"
- set TEST_MODE := "disabled"

(* write acceptance filter *)
- write ACCEPTANCE CODE REGISTER
- write ACCEPTANCE MASK REGISTER

(* example:
contents of ACCEPTANCE CODE REGISTER = 01110010_B
contents of ACCEPTANCE MASK REGISTER = 00111000_B
allows for messages with following IDs: $01XXX010XXX_B$
*)

(* define bus timing (baud rate on the CAN bus) *)
- write BUS TIMING 0 REGISTER
- write BUS TIMING 1 REGISTER

(* example:
contents of BUS TIMING 0 REGISTER = 10001001_B
contents of BUS TIMING 1 REGISTER = 11101011_B
results in:

t_{SCL}	$= (9+1) \cdot 2 \cdot t_{OSC}$ (with $f_{OSC} = 16$ MHz:	1.25 µs)
t_{SJW}	$= (2+1) \cdot t_{SCL}$	(3.75 µs)
SAMPLING	= 1 (three samples/bit taken)	
$t_{SYNCSEG}$	$= 1 \cdot t_{SCL}$	(1.25 µs)
t_{TSEG2}	$= (6+1) \cdot t_{SCL}$	(8.75 µs)
t_{TSEG1}	$= (11+1) \cdot t_{SCL}$	(15.00 µs)
t_{BIT}	$= t_{SYNCSEG} + t_{TSEG1} + t_{TSEG2} = 20 \cdot t_{SCL}$	(25.00 µs)

variation of bit time due to resynchronization

t_{BITmin}	$= t_{BIT} - t_{SJW} = 17\ t_{SCL}$	(21.25 µs)
t_{BITmax}	$= t_{BIT} + t_{SJW} = 23\ t_{SCL}$	(28.75 µs)

*)

(* define bus driver characteristics *)
- write OUTPUT CONTROL REGISTER

(* example:
contents of OUTPUT CONTROL REGISTER = 10101010_B
results in:
output mode: normal 1 (bit sequence on TX0 and TX1 pins)
TX0 configuration: bit state 0 (1) → output state low (float)
TX1 configuration: bit state 0 (1) → output state high (float)
*)

(* end initialization; write to CONTROL REGISTER *)
- enable interrupt sources (* bits 4 . . 1 *)
- define the resynchronization mode (* SYNCH: bit 6 *)
- set RESET REQUEST := absent

(* note:
after reseting RESET REQUEST, check for an external hardware reset, which may hold RESET REQUEST to "present". If so, repeat reseting until RESET REQUEST bit is really set to "absent" *)

3.2.1. Initialization

During initialization the 82C200 is programmed according to the required mode of operation. Initialization can be performed only if the RESET REQUEST bit in the CONTROL REGISTER is set to "present" (high). To allow for any receive or transmit operation the RESET REQUEST bit must be reset to "absent" (low) after initialization.

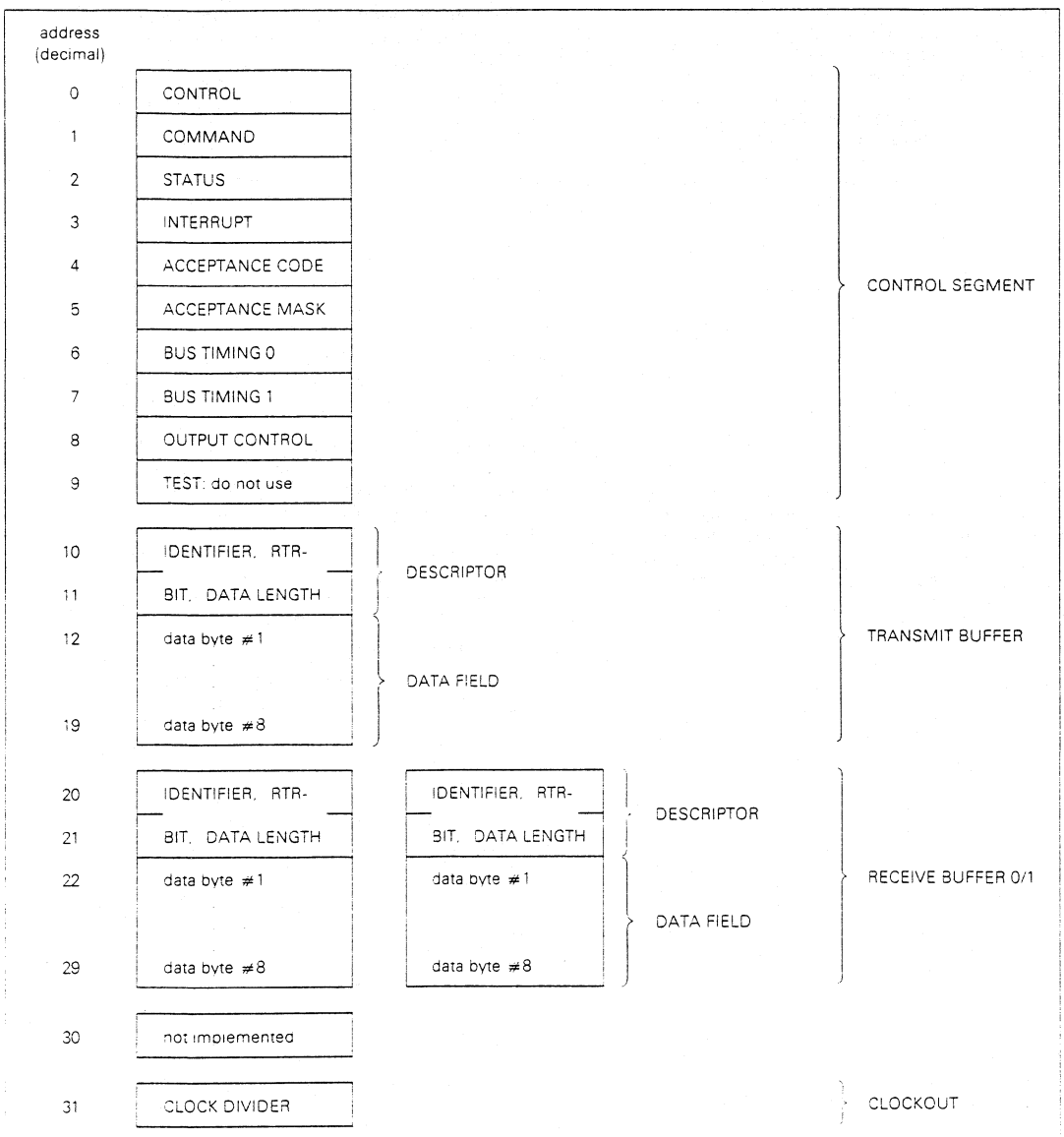
A flow chart of the initialization procedure is given in table 2.

3.2.2. Transmission

The flow chart in table 3 describes how to transmit a message.

3.2.3. Reception

The flow chart in table 4 describes how to receive a message. Normally, reception is initiated by an interrupt (see



"Interrupt" and "Polling" flow charts). However, whenever the STATUS REGISTER shows RECEIVE BUFFER STATUS = "full", a message is present and can be read.

Table 3. Flow chart of a transmission procedure

if (status bit TRANSMIT BUFFER ACCESS = "released")	
then	else
write message from CPU into 82C200's TRANSMIT BUFFER	if (<high priority message to be transmitted>)
	then / else
	set command bit ABORT TRANSMISSION := "present"
set command bit TRANSMISSION REQUEST := "present"	(* the next transmission is delayed until TRANSMIT BUFFER ACCESS = "released" is signalled by a TRANSMIT INTERRUPT or by polling the STATUS REGISTER *)

Table 4. Flow chart of a reception procedure

read message from 82C200 RECEIVE BUFFER into CPU
set command bit RELEASE RECEIVE BUFFER := "released"

3.2.4. Other events

In order to detect some types of events (e.g. reception of a message), an interrupt can be generated by the 82C200; most of these events can also be detected by polling bits of the STATUS REGISTER. Other actions, not yet shown, can be initiated by setting a bit in the command register (e.g. abort transmission).

3.2.4.1. Interrupts

The interrupt sources are the WAKE-UP INTERRUPT (always enabled), the OVERRUN-, the ERROR-, the TRANSMIT- and the RECEIVE-INTERRUPT; the latter 4 can be enabled/disabled, which should be performed during the initialization. In order to present a complete description it is assumed that all interrupt sources are enabled, for other settings please refer to "Polling". A 82C200's interrupt request is acknowledged by the CPU by reading the contents of the 82C200's INTERRUPT REGISTER once; after reading this register, all its previously set bits are reset (low). Therefore, the CPU should analyse all the bits of the INTERRUPT REGISTER and perform the operations shown in table 5.

Note:
Where and how specific messages to be transmitted or received from the 82C200 are stored in the CPU's memory is dependent on the specific application. The data memories may be cyclic FIFOs or memories with ranges allocated to certain types of messages (i.e. corresponding to the message's identifier). It is also possible to operate directly on a message which has just been received without intermediately storing it in the RECEIVE BUFFER, e.g. to store it in a memory with a maximum capacity of 10 bytes. Also, whether or not to use the DATA LENGTH CODE included in each message, when the DATA BYTES of the message are read from the RECEIVE BUFFER into the CPU memory, depends on the application.

3.2.4.2. Polling

Polling the STATUS REGISTER provides the same interrupt information as that obtained by interrupt servicing, except for the WAKE-UP interrupt. Reading and using the contents of the STATUS REGISTER enables the message information to be coordinated and controlled. Analysing the contents of the STATUS REGISTER is very similar to analysing the contents of the INTERRUPT REGISTER. A complete analysis is given in table 6, all of which may not be applicable to the actual implementation.

3.2.4.3. Abort transmission

refer to Transmission.

3.2.4.4. Sleep mode

A network enters the "sleep mode" when all its nodes enter the "sleep mode". A node enters the "sleep mode" when its CAN controller (i.e. the 82C200) enters the "sleep mode". On condition that no bus activity is present and the $\overline{INT}$ pin is set to a logic high (inactive state), an 82C200 enters the "sleep mode" through a GO TO SLEEP command. An 82C200 generates a WAKE-UP INTERRUPT either if it wakes up, or if it is unable to enter the "sleep mode" after a GO TO SLEEP command.

Set command bit GO TO SLEEP := "sleep"

The 82C200 exits from the "sleep mode" by:

- activity on the transmission medium,
- setting the $\overline{INT}$ pin of the 82C200 to a logic low,
- setting the GO TO SLEEP bit of the 82C200 to "wake-up"

3.2.4.5. Clock divider

The frequency output provided by the CLOCKOUT signal of the 82C200 can be used to drive a CPU. The frequency is determined by the value programmed into the CLOCK DIVIDER REGISTER (CDR). After a reset, the CDR contains a value of 0 or 5 if the MODE pin of the 82C200 is tied to V_{dd} or V_{ss} respectively.

Attention: The voltage on the MODE pin also defines the CPU interface (see section 2.1). The CLOCKOUT frequency is defined by (only the three LSBs are significant):

$f_{CLOCKOUT} = f_{CRYSTAL}/(((CDR + 1) \cdot 2) \text{ modulo } 15)$.

The CLOCK DIVIDER REGISTER can be accessed at any time.

Write CLOCK DIVIDER REGISTER: (only the three LSBs are significant)

Table 5. Flow chart of INTERRUPT REGISTER data evaluation

read INTERRUPT REGISTER and store in the CPU memory

if (WAKE-UP INTERRUPT = "set")

then:

if (<CPU state> = "just being awoken")

then:

(* the network was awoken by some CAN bus activity *)

Perform appropriate network wake up activities

else:

(* the just issued GOTO SLEEP command was not successful *)

Perform appropriate action

else: —

if (TRANSMIT INTERRUPT = "set")

then:

(* the TRANSMIT BUFFER is released *)

A next message may be written into the TRANSMIT BUFFER

if (<using the ABORT TRANSMISSION command>)

then:

if (TRANSMISSION COMPLETE STATUS = "complete")

then:

(* last requested transmission has been completed, no ABORT TRANSMISSION command has been executed *)

else:

(* last requested transmission has not been completed; the ABORT TRANSMISSION command was successful *)

else:

(* last requested transmission has been completed *)

else: —

if (RECEIVE INTERRUPT = "set")

then:

read RECEIVE BUFFER into CPU memory

set command bit RELEASE RECEIVE BUFFER := "released"

if (OVERRUN INTERRUPT = "set")

then:

an application may use this information to change its behaviour (e.g. faster reaction on a RECEIVE INTERRUPT)

set command bit CLEAR OVERRUN := "clear"

else: —

if (ERROR INTERRUPT = "set")

then:

read STATUS REGISTER and store in CPU memory

if (BUS STATUS = "on bus")

then:

(* 82C200 takes part in bus activities *)

if (ERROR STATUS = "ok")

then:

(* the CAN bus is presently not severely disturbed *)

else:

(* the CAN bus is presently severely disturbed *)

else:

(* 82C200 does not take part in bus activities *)

if (<restart 82C200 required>)

then:

set control bit RESET REQUEST := "absent"

(* now the 82C200 waits for 128 · 11 consecutive recessive bits before going "on-bus" again *)

else:

(* 82C200 is left in "off-bus" and "reset" state *)

else: —

4. Development tools

For the 82C200 several powerful support tools can be supplied to assist during the design and test phases. These tools are:

- the PSCC evaluation board
- advanced tools[1]):

4.1. PSCC evaluation board

The PSCC evaluation board is a most-versatile aid consisting of a ready-to-use hardware and software module very

[1]) Philips has an agreement with I + ME (Gesellschaft für Informatik und Mikroelektronik, Wolfenbüttel, W. Germany) who are fully committed to

Table 6. Flow chart of STATUS REGISTER data evaluation (polling)

read STATUS REGISTER and store in CPU memory
(* use the copy of the STATUS REGISTER only *)

if (TRANSMIT BUFFER ACCESS = "released")

then	else
a next message may be written into the TRANSMIT BUFFER	

if (<using the ABORT TRANSMISSION command>)

then	else
if (TRANSMISSION COMPLETE STATUS = "complete")	(* last requested transmission has been completed *)

then	else
(* last requested transmission has been completed, no ABORT TRANSMISSION command has been executed *)	(* last requested transmission has not been completed due to an ABORT TRANSMISSION command *)

if (RECEIVE BUFFER STATUS = "full")

then	else
read RECEIVE BUFFER into CPU memory	
set command bit RELEASE RECEIVE BUFFER := "released"	
if (DATA OVERRUN = "overrun")	

then	else
an application may use this information to change its behavior (e.g. faster reaction on a RECEIVE INTERRUPT)	
set command bit CLEAR OVERRUN := "clear"	

if (BUS STATUS = "on-bus")

then	else
(* 82C200 takes part in bus activities *)	(* 82C200 does not take part in bus activities *)
if (ERROR STATUS = "ok")	if (<restart 82C200 required>)

then	else	then	else
(* the CAN bus is presently not severely disturbed *)	(* the CAN bus is presently severely disturbed *) some application-specific actions may be necessary	set control bit RESET REQUEST := "absent" (* now the 82C200 waits for 128 · 11 consecutive recessive bits before going "on-bus" again *)	perform application-specific default-mode operation

similar to a real CAN bus node. The PSCC evaluation board can be used without modification in a car since it has its own 5 V supply. An RS232 interface allows the PSCC evaluation board to be connected to a terminal or a PC with terminal emulation software.

4.1.1. PSCC evaluation board hardware

The PSCC evaluation board hardware is shown in figure 10. It consists of:

- 82C200 bus controller,
- 80C552 microcontroller with an external memory capacity of 32 KBytes for RAM and 32 KBytes for ROM storage,
- 5 V power supply with protection against car battery voltage fluctuations,
- two different, selectable, physical CAN bus interfaces:
  - Transceiver for high-speed applications
  - an RS232 interface,
- LEDs for demonstration purposes,
- wrap field for the user's specific circuitry.

4.1.2. PSCC evaluation board software

The software for the PSCC evaluation board is stored in an EPROM. The software is designed to assist users with different experience in CAN-based networks:

- A user with little experience is able to activate the demonstration software. A menu-driven software monitor allows the contents of the 82C200 registers to be altered and thereby enables the user to gain experience.
- A user with more experience will use the "download" facility; this allows the user to load new software on to the PSCC evaluation board.

The PSCC evaluation board is also ready to be used as a bus monitor, receiving messages from the bus for display

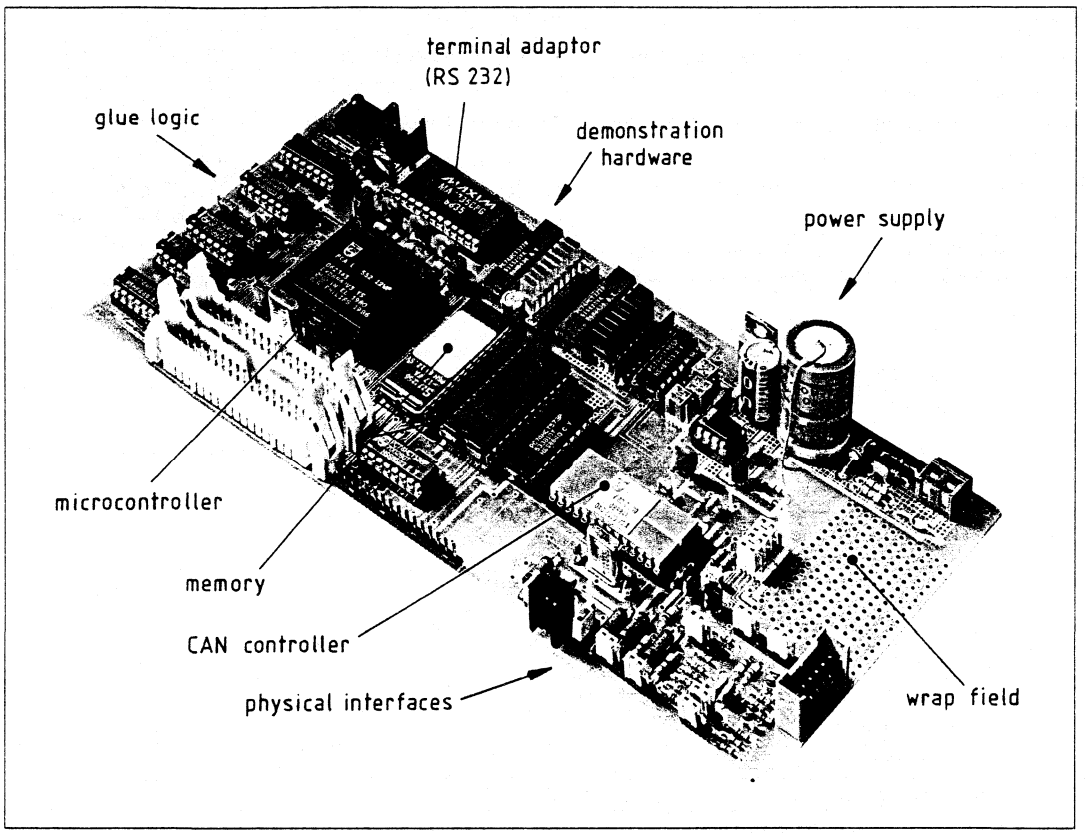


Figure 10. PSCC evaluation board

4.2. Advanced tools

In addition to the PSCC evaluation board, three other sophisticated development tools can be supplied. These were developed in co-operation with a sub-contractor, I + ME, Wolfenbüttel, West Germany. These tools are:

4.2.1. NetSim

NetSim (Network Simulator) is a software simulator for use with a Personal Computer. The CAN network is described using NetSim on the PC by:

- number of network nodes,
- data transmission rate,
- message identifiers/message length,
- noise.

The simulation is then started. NetSim provides information for various parameters, such as:

- delay in a defined message,
- bus load.

NetSim assists during the design phase to investigate these

4.2.2. NetAna

NetAna (Network Analyzer) is a combined hardware/software tool, operating in conjunction with a PC.

NetAna has two basic functions:

- to monitor the bus traffic and store the data on the hard disk in the PC for subsequent analysis,
- an event is triggered (identifier, bus error, etc.) and the messages around the trigger point are recorded.

NetAna assists to trace failures in an existing CAN network.

4.2.3. NetEmu

NetEmu (Network Emulator) enables the user to transmit defined messages into an operational CAN network. The resultant network response can then be analyzed by NetAna.

Weitere Informationen:

Philips Components
Unternehmensbereich der Philips GmbH
Burchardstraße 19, Postf. 10 63 23, 2000 Hamburg 1

CAN controller interface PCA82C250

FEATURES

- Fully compatible with the *"ISO/DIS 11898"* standard
- High speed (up to 1 Mbaud)
- Bus lines protected against transients in an automotive environment
- Slope control to reduce radio frequency interference (RFI)
- Differential receiver with wide common-mode range for high immunity against electromagnetic interference (EMI)
- Thermally protected
- Short-circuit proof to battery and ground
- Low current standby mode
- An unpowered node does not disturb the bus lines
- At least 110 nodes can be connected.

APPLICATIONS

- High-speed applications (up to 1 Mbaud) in cars.

GENERAL DESCRIPTION

The PCA82C250 is the interface between the CAN protocol controller and the physical bus. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5.5	V
I_{CC}	supply current		–	170	μA
$1/t_{bit}$	maximum transmission speed	non-return-to-zero	1	–	Mbaud
V_{CAN}	CANH, CANL input/output voltage		–8	+18	V
ΔV	differential bus voltage		1.5	3.0	V
t_{pd}	propagation delay	high-speed mode	–	50	ns
T_{amb}	operating ambient temperature		–40	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA82C250	8	DIP8	plastic	SOT97-1
PCA82C250T	8	SO8	plastic	SOT96-1

BLOCK DIAGRAM

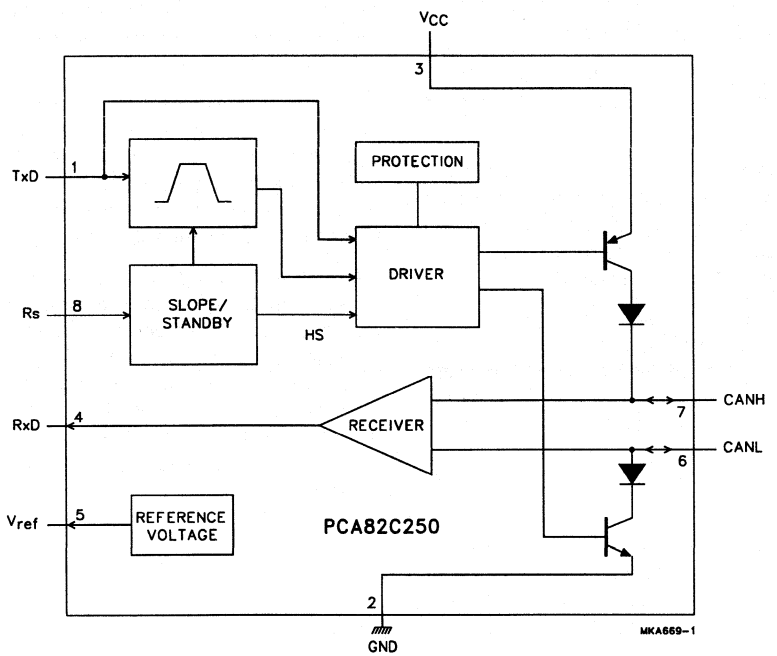


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TxD	1	transmit data input
GND	2	ground
V_{CC}	3	supply voltage
RxD	4	receive data output
V_{ref}	5	reference voltage output
CANL	6	LOW level CAN voltage input/output
CANH	7	HIGH level CAN voltage input/output
Rs	8	slope resistor input

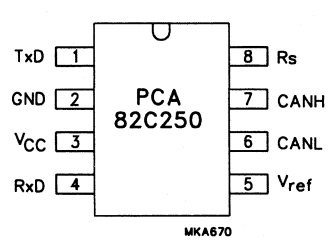


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The PCA82C250 is the interface between the CAN protocol controller and the physical bus. It is primarily intended for high-speed applications (up to 1 Mbaud) in cars. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller. It is fully compatible with the *"ISO/DIS 11898"* standard.

A current limiting circuit protects the transmitter output stage against short-circuit to positive and negative battery voltage. Although the power dissipation is increased during this fault condition, this feature will prevent destruction of the transmitter output stage.

If the junction temperature exceeds a value of approximately 160 °C, the limiting current of both transmitter outputs is decreased. Because the transmitter is responsible for the major part of the power dissipation, this will result in a reduced power dissipation and hence a lower chip temperature. All other parts of the IC will remain in operation. The thermal protection is particularly needed when a bus line is short-circuited.

The CANH and CANL lines are also protected against electrical transients which may occur in an automotive environment. Pin 8 (Rs) allows three different modes of operation to be selected: high-speed, slope control or standby.

For high-speed operation, the transmitter output transistors are simply switched on and off as fast as possible. In this mode, no measures are taken to limit the rise and fall slope. Use of a shielded cable is recommended to avoid RFI problems. The high-speed mode is selected by connecting pin 8 to ground.

For lower speeds or shorter bus length, an unshielded twisted pair or a parallel pair of wires can be used for the bus. To reduce RFI, the rise and fall slope should be limited. The rise and fall slope can be programmed with a resistor connected from pin 8 to ground. The slope is proportional to the current output at pin 8.

If a HIGH level is applied to pin 8, the circuit enters a low current standby mode. In this mode, the transmitter is switched off and the receiver is switched to a low current. If dominant bits are detected (differential bus voltage >0.9 V), RxD will be switched to a LOW level. The microcontroller should react to this condition by switching the transceiver back to normal operation (via pin 8). Because the receiver is slow in standby mode, the first message will be lost.

Table 1 Truth table of CAN transceiver.

SUPPLY	TxD	CANH	CANL	BUS STATE	RxD
4.5 to 5.5 V	0	HIGH	LOW	dominant	0
4.5 to 5.5 V	1 (or floating)	floating	floating	recessive	1
<2 V (not powered)	X	floating	floating	recessive	X
2 V < V_{CC} < 4.5 V	>0.75V_{CC}	floating	floating	recessive	X
2 V < V_{CC} < 4.5 V	X	floating if V_{Rs} > 0.75V_{CC}	floating if V_{Rs} > 0.75V_{CC}	recessive	X

Table 2 Rs (pin 8) summary.

CONDITION FORCED AT Rs	MODE	RESULTING VOLTAGE OR CURRENT AT Rs
V_{Rs} > 0.75V_{CC}	standby	I_{Rs} < |10 μA|
−10 μA < I_{Rs} < −200 μA	slope control	0.4V_{CC} < V_{Rs} < 0.6V_{CC}
V_{Rs} < 0.3V_{CC}	high-speed	I_{Rs} < −500 μA

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). All voltages are referenced to pin 2; positive input current.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		−0.3	+9.0	V
V_n	DC voltage at pins 1, 4, 5 and 8		−0.3	V_{CC} + 0.3	V
$V_{6,7}$	DC voltage at pins 6 and 7	0 V < V_{CC} < 5.5 V; no time limit	−8.0	+18.0	V
V_{trt}	transient voltage at pins 6 and 7	see Fig.8	−150	+100	V
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−40	+125	°C
T_{vj}	virtual junction temperature	note 1	−40	+150	°C

Note

1. In accordance with *"IEC 747-1"*.
   An alternative definition of virtual junction temperature T_{vj} is: $T_{vj} = T_{amb} + P_d \times R_{th\ vj\text{-}amb}$, where $R_{th\ vj\text{-}amb}$ is a fixed value to be used for the calculation of T_{vj}.
   The rating for T_{vj} limits the allowable combinations of power dissipation (P_d) and ambient temperature (T_{amb}).

HANDLING

Classification A: human body model; C = 100 pF; R = 1500 Ω; V = ±2000 V.
Classification B: machine model; C = 200 pF; R = 0 Ω; V = ±200 V.

QUALITY SPECIFICATION

Quality specification *"SNW-FQ-611 part E"* is applicable and can be found in the *"Quality reference pocket-book"* (ordering number 9398 510 34011).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	PCA82C250	100	K/W
	PCA82C250T	160	K/W

CHARACTERISTICS

V_{CC} = 4.5 to 5.5 V; T_{amb} = −40 to +125 °C; R_L = 60 Ω; I_8 > −10 μA; unless otherwise specified.
All voltages referenced to ground (pin 2); positive input current; all parameters are guaranteed over the ambient temperature range by design, but only 100% tested at +25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_3	supply current	dominant; V_1 = 1 V	–	–	70	mA
		recessive; V_1 = 4 V; R_8 = 47 kΩ	–	–	14	mA
		recessive; V_1 = 4 V; V_8 = 1 V	–	–	18	mA
		standby; T_{amb} < 90 °C; note 1	–	100	170	μA
DC bus transmitter						
V_{IH}	HIGH level input voltage	output recessive	$0.7V_{CC}$	–	V_{CC} + 0.3	V
V_{IL}	LOW level input voltage	output dominant	−0.3	–	$0.3V_{CC}$	V
I_{IH}	HIGH level input current	V_1 = 4 V	−200	–	+30	μA
I_{IL}	LOW level input voltage	V_1 = 1 V	100	–	600	μA
$V_{6,7}$	recessive bus voltage	V_1 = 4 V; no load	2.0	–	3.0	V
I_{LO}	off-state output leakage current	−2 V < (V_6,V_7) < 7 V	−2	–	+1	mA
		−5 V < (V_6,V_7) < 18 V	−5	–	+12	mA
V_7	CANH output voltage	V_1 = 1 V	2.75	–	4.5	V
V_6	CANL output voltage	V_1 = 1 V	0.5	–	2.25	V
$\Delta V_{6,7}$	difference between output voltage at pins 6 and 7	V_1 = 1 V	1.5	–	3.0	V
		V_1 = 1 V; R_L = 45 Ω; $V_{CC} \geq$ 4.9 V	1.5	–	–	V
		V_1 = 4 V; no load	−500	–	+50	mV
I_{sc7}	short-circuit CANH current	V_7 = −5 V; $V_{CC} \leq$ 5 V	–	–	105	mA
		V_7 = −5 V; V_{CC} = 5.5 V	–	–	120	mA
I_{sc6}	short-circuit CANL current	V_6 = 18 V	–	–	160	mA
DC bus receiver: V_1 = 4 V; pins 6 and 7 externally driven; −2 V < (V_6, V_7) < 7 V; unless otherwise specified						
$V_{diff(r)}$	differential input voltage (recessive)		−1.0	–	0.5	V
		−7 V < (V_6, V_7) < 12 V; not standby mode	−1.0	–	0.4	V
$V_{diff(d)}$	differential input voltage (dominant)		0.9	–	5.0	V
		−7 V < (V_6, V_7) < 12 V; not standby mode	1.0	–	5.0	V
$V_{diff(hys)}$	differential input hysteresis	see Fig.5	–	150	–	mV
V_{OH}	HIGH level output voltage (pin 4)	I_4 = −100 μA	$0.8V_{CC}$	–	V_{CC}	V
V_{OL}	LOW level output voltage (pin 4)	I_4 = 1 mA	0	–	$0.2V_{CC}$	V
		I_4 = 10 mA	0	–	1.5	V
R_i	CANH, CANL input resistance		5	–	25	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_{diff}	differential input resistance		20	–	100	kΩ
C_i	CANH, CANL input capacitance		–	–	20	pF
C_{diff}	differential input capacitance		–	–	10	pF
Reference output						
V_{ref}	reference output voltage	V_8 = 1 V; −50 μA < I_5 < 50 μA	0.45V_{CC}	–	0.55V_{CC}	V
		V_8 = 4 V; −5 μA < I_5 < 5 μA	0.4V_{CC}	–	0.6V_{CC}	V
Timing (see Figs 4, 6 and 7)						
t_{bit}	minimum bit time	V_8 = 1 V	–	–	1	μs
t_{onTxD}	delay TxD to bus active	V_8 = 1 V	–	–	50	ns
t_{offTxD}	delay TxD to bus inactive	V_8 = 1 V	–	40	80	ns
t_{onRxD}	delay TxD to receiver active	V_8 = 1 V	–	55	120	ns
t_{offRxD}	delay TxD to receiver inactive	V_8 = 1 V; V_{CC} < 5.1 V; T_{amb} < +85 °C	–	82	150	ns
		V_8 = 1 V; V_{CC} < 5.1 V; T_{amb} < +125 °C	–	82	170	ns
		V_8 = 1 V; V_{CC} < 5.5 V; T_{amb} < +85 °C	–	90	170	ns
		V_8 = 1 V; V_{CC} < 5.5 V; T_{amb} < +125 °C	–	90	190	ns
t_{onRxD}	delay TxD to receiver active	R_8 = 47 kΩ	–	390	520	ns
		R_8 = 24 kΩ	–	260	320	ns
t_{offRxD}	delay TxD to receiver inactive	R_8 = 47 kΩ	–	260	450	ns
		R_8 = 24 kΩ	–	210	320	ns
ISRI	differential output voltage slew rate	R_8 = 47 kΩ	–	14	–	V/μs
t_{WAKE}	wake-up time from standby (via pin 8)		–	–	20	μs
t_{dRxDL}	bus dominant to RxD LOW	V_8 = 4 V; standby mode	–	–	3	μs
Standby/slope control (pin 8)						
V_8	input voltage for high-speed		–	–	0.3V_{CC}	V
I_8	input current for high-speed	V_8 = 0 V	–	–	−500	μA
V_{stb}	input voltage for standby mode		0.75V_{CC}	–	–	V
I_{slope}	slope control mode current		−10	–	−200	μA
V_{slope}	slope control mode voltage		0.4V_{CC}	–	0.6V_{CC}	V

Note

1. $I_1 = I_4 = I_5 = 0$ mA; 0 V < V_6 < V_{CC}; 0 V < V_7 < V_{CC}; $V_8 = V_{CC}$.

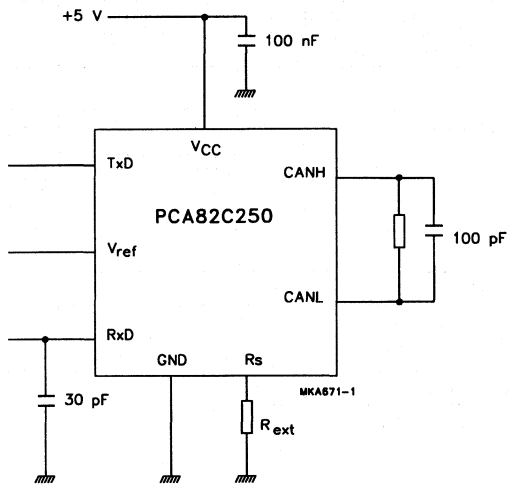


Fig.3 Test circuit for characteristics.

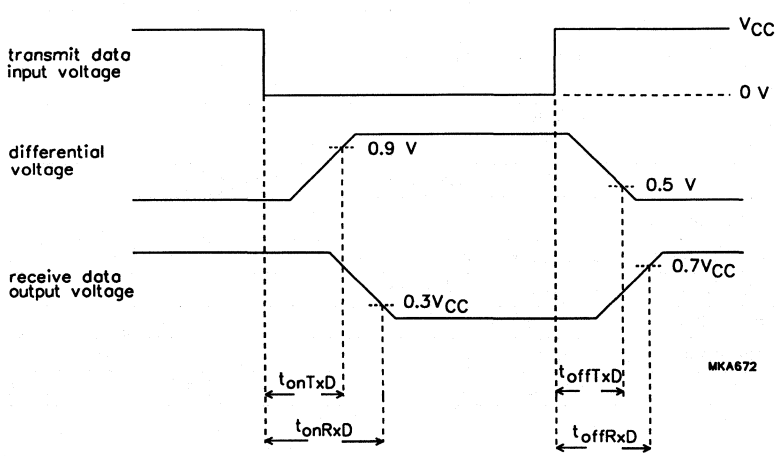


Fig.4 Timing diagram for dynamic characteristics.

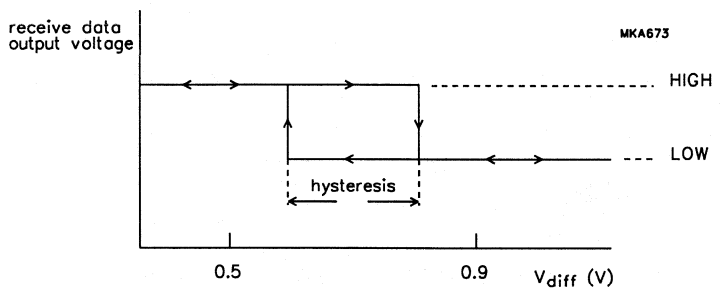
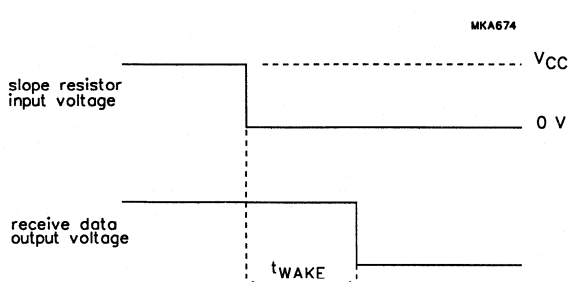
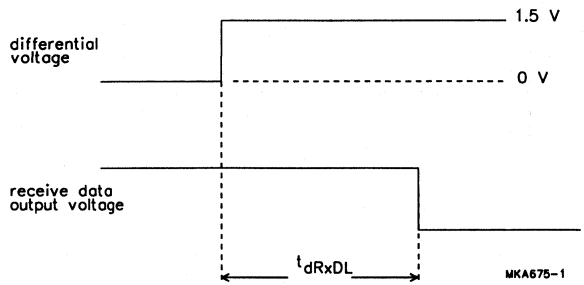


Fig.5 Hysteresis.



V_1 = 1 V.

Fig.6 Timing diagram for wake-up from standby.



$V_1 = 4$ V; $V_8 = 4$ V.

Fig.7 Timing diagram for bus dominant to RxD LOW.

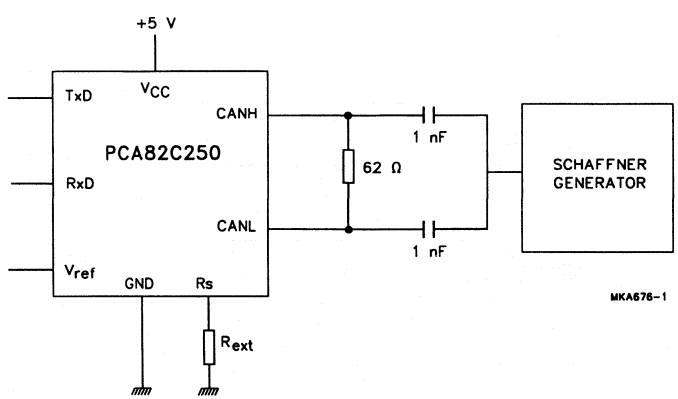


Fig.8 Test circuit for Schaffner pulses.

APPLICATION INFORMATION

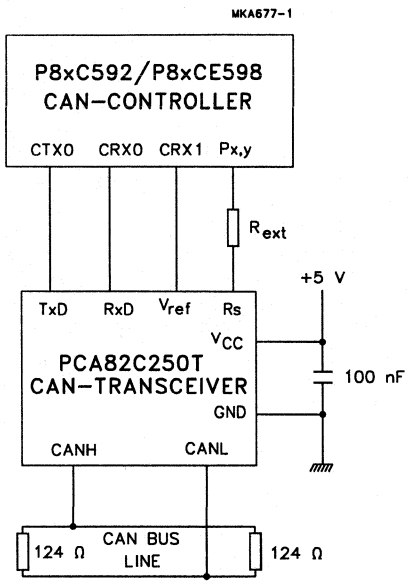


Fig.9 Application of the CAN transceiver.

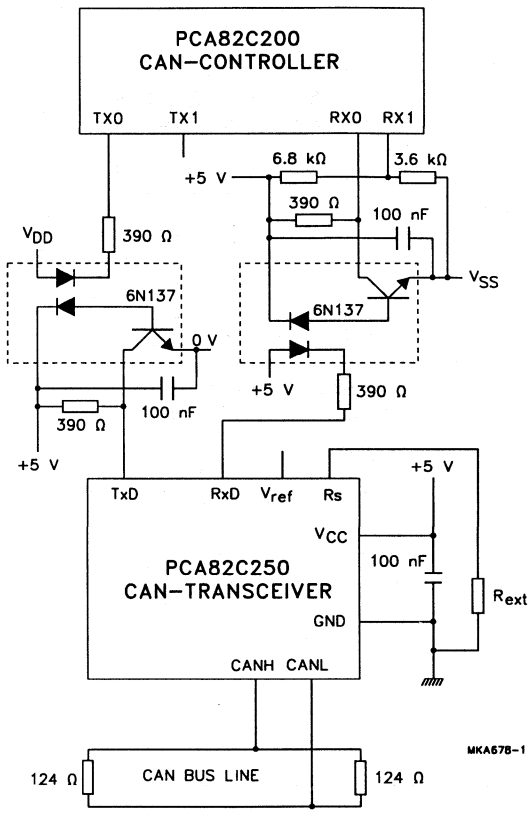


Fig.10 Application with galvanic isolation.

INTERNAL PIN CONFIGURATION

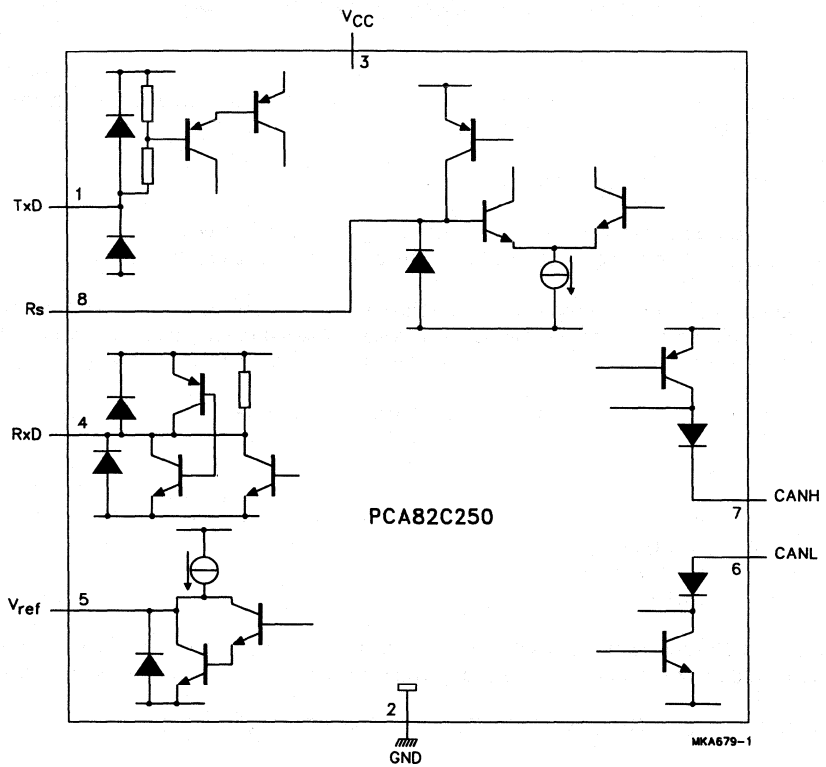


Fig.11 Internal pin configuration.

Application Hints on Using the Slope-Control Function of the PCA 82C250 CAN Transceiver

The 82C250 CAN transceiver provides a slope-control function where the slew rate can be adjusted via an optional external resistor connected to pin 8 of the device.

Using this feature can provide the following advantages

- o Reduction of electromagnetic emission, i.e. to support unshielded bus wires
- o Increase of allowed drop cable length, i.e. for connection of the nodes to the trunk line

The slew rate is approximately proportional to the current flowing out of the pin "Rs" (= pin 8) of the 82C250. The current flowing out of the pin "Rs" is determined by the internally generated voltage at Rs of 0.5 Vcc typically in slope-control mode and the external resistance to ground potential (= pin 2).

Consequently the following formula is valid for the 82C250 CAN transceiver:

$$R_{ext} = (Vcc/2) / (k_{SR} * SR)$$

R_{ext}	external resistor connected between pins Rs and GND (= pin 8 and pin 2)
Vcc	supply voltage, typically 5V
SR	typical slew rate of transmitter
k_{SR}	slew rate constant

According to the 82C250 specification a slew rate of 14 V/us typ. is obtained by using an external resistor of 47kΩ (see data sheet, page 7, April 1994). Thus the constant k_{SR} is calculated as follows:

$$k_{SR} = (Vcc/2) / (R_{ext14} * SR_{14}) = 2.5V / (47k\Omega * 14V/us) = 3.8 * 10^{-3}\ us/k\Omega$$

Example

Let SR = **20 V/us** be the desired slew rate. Here is the calculation of the corresponding resistance to be connected to pin 8

$$R_{ext20} = (Vcc/2) / (k_{SR} * SR) = 2.5V / (3.8 * 10^{-3}\ us/k\Omega * 20\ V/us) = \mathbf{33\ k\Omega}$$

Note 1: The recommended range for R_{ext} is $16.5\ k\Omega < R_{ext} < 140\ k\Omega$

Note 2: It is recommended to provide short tracks (PCB-layout) for pin 8 to optimize EMC performance.

Note 3: When the slope-control function is used the internal delay time increases. This corresponds to a reduction of the maximum bus line length at a given bit rate. Compared to the high-speed mode the maximum bus length is reduced by approx. 30m at R_{ext} = 24kΩ or approx. 70m at R_{ext} = 47kΩ.

CAN transceiver for 24 V systems PCA82C251

FEATURES

- Fully compatible with the *"ISO 11898 - 24 V"* standard
- Slope control to reduce RFI
- Thermally protected
- Short-circuit proof to battery and ground in 24 V powered systems
- Low current standby mode
- An unpowered node does not disturb the bus lines
- At least 110 nodes can be connected
- High speed (up to 1 Mbaud)
- High immunity against electromagnetic interference.

GENERAL DESCRIPTION

The PCA82C251 is the interface between the CAN protocol controller and the physical bus. It is primarily intended for applications (up to 1 MBaud) in trucks and buses. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5.5	V
I_{CC}	supply current	standby mode	–	275	µA
$1/t_{bit}$	maximum transmission speed	non-return-to-zero	1	–	MBaud
V_{CAN}	CANH, CANL input/output voltage		–40	+40	V
V_{diff}	differential bus voltage		1.5	3.0	V
T_{amb}	operating ambient temperature		–40	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	CODE
PCA82C251	SO8	plastic small outline package; 8 leads body width 3.9 mm	SOT96-1
PCA82C251T	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1

BLOCK DIAGRAM

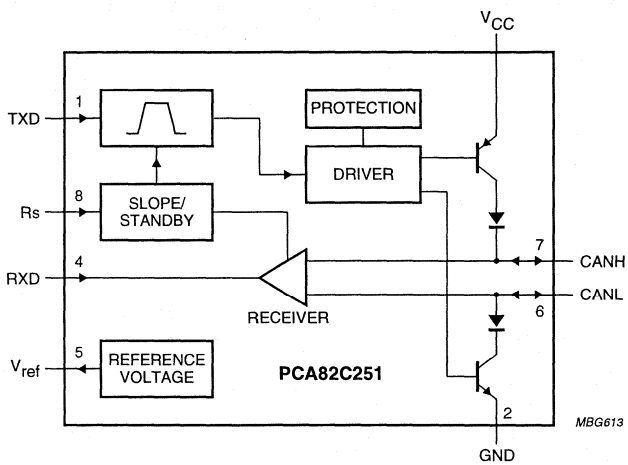


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TXD	1	transmit data input
GND	2	ground
V_{CC}	3	supply voltage
RXD	4	receive data output
V_{ref}	5	reference voltage output
CANL	6	LOW level CAN voltage input/output
CANH	7	HIGH level CAN voltage input/output
Rs	8	slope resistor input

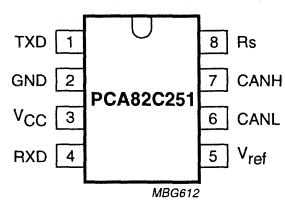


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The PCA82C251 is the interface between the CAN protocol controller and the physical bus. It is primarily intended for applications up to 1 MBaud in trucks and buses. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller. It is fully compatible with the *"ISO 11898-24 V"* standard.

A current limiting circuit protects the transmitter output stage against short-circuit to positive and negative battery voltage. Although the power dissipation is increased during this fault condition, this feature will prevent destruction of the transmitter output stage.

If the junction temperature exceeds a value of approximately 160 °C, the limiting current of both transmitter outputs is decreased. Because the transmitter is responsible for the major part of the power dissipation, this will result in a reduced power dissipation and hence a lower chip temperature. All other parts of the IC will remain operating. The thermal protection is particularly needed when a bus line is short-circuited.

The CANH and CANL lines are also protected against electrical transients which may occur in an automotive environment.

Pin 8 (Rs) allows three different modes of operation to be selected, high-speed, slope control or standby.

For high-speed operation, the transmitter output transistors are simply switched on and off as fast as possible. In this mode, no measures are taken to limit the rise and fall slope. Use of a shielded cable is recommended to avoid RFI problems. The high-speed mode is selected by connecting pin 8 to ground.

The slope control mode allows the use of an unshielded twisted pair or a parallel pair of wires as bus lines. To reduce RFI, the rise and fall slope should be limited. The rise and fall slope can be programmed with a resistor connected from pin 8 to ground. The slope is proportional to the current output at pin 8.

If a logic HIGH level is applied to pin 8, the circuit enters a low current standby mode. In this mode, the transmitter is switched off and the receiver is switched to a low current. If dominant bits are detected (differential bus voltage >0.9 V), RXD will be switched to a LOW level.

The microcontroller should react to this condition by switching the transceiver back to normal operation (via pin 8). Because the receiver is slower in standby mode, the first message will be lost at higher bit rates.

Table 1 Truth table of the CAN transceiver

V_{CC}	TXD	CANH	CANL	BUS STATE	RXD
4.5 to 5.5 V	0	HIGH	LOW	dominant	0
4.5 to 5.5 V	1 (or floating)	floating	floating	recessive	1[2]
$4.5 < V_{CC} < 5.5$ V	X[1]	floating if $V_{Rs} > 0.75V_{CC}$	floating if $V_{Rs} > 0.75V_{CC}$	floating	1[2]
$0 < V_{CC} < 4.5$ V	floating	floating	floating	floating	X[1]

Notes

1. Where X = don't care.
2. If another bus node is transmitting a dominant bit, then RXD is logic 0.

Table 2 Pin Rs summary

CONDITION FORCED AT PIN Rs	MODE	RESULTING VOLTAGE OR CURRENT AT PIN Rs
$V_{Rs} > 0.75V_{CC}$	standby	$-I_{Rs} < 10\ \mu A$
$10\ \mu A < -I_{Rs} < 200\ \mu A$	slope control	$0.4V_{CC} < V_{Rs} < 0.6V_{CC}$
$V_{Rs} < 0.3V_{CC}$	high-speed	$-I_{Rs} < 500\ \mu A$

RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134). All voltages are referenced to pin 2; positive input current.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		−0.3	+7.0	V
V_n	DC voltage at pins 1, 4, 5 and 8	0 V < V_{CC} < 5.5 V,	−0.3	V_{CC} + 0.3	V
$V_{6,7}$	DC voltage on pins 6 and 7	no time limit	−40	+40	V
V_{tr}	transient voltage on pins 6 and 7	see Fig.8	−200	+200	V
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−40	+125	°C
T_{vj}	virtual junction temperature	note 1	−40	+150	°C
V_{esd}	electrostatic discharge	note 2	−2500	+2500	V
		note 3	−250	+250	V

Note

1. In accordance with *"IEC 747-1"*.
   An alternative definition of virtual junction temperature T_{vj} is: $T_{vj} = T_{amb} + P_d \times R_{th\ vj\text{-}amb}$, where $R_{th\ vj\text{-}amb}$ is a fixed value to be used for the calculation of T_{vj}.
   The rating for T_{vj} limits the allowable combinations of power dissipation (P_d) and ambient temperature (T_{amb}).
2. Classification A: human body model; C = 100 pF; R = 1500 Ω; V = ±2500 V.
3. Classification B: machine model; C = 200 pF; R = 0 Ω; V = ±250 V.

QUALITY SPECIFICATION

Quality specification *"SNW-FQ-611 part E"* is applicable and can be found in the *"Quality reference pocket-book"* (ordering number 9398 510 34011).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SO8	160	K/W
	DIP8	100	K/W

CHARACTERISTICS

V_{CC} = 4.5 to 5.5 V; T_{amb} = –40 to + 125 °C; R_L = 60 Ω; I_8 > –10 μA; unless otherwise specified.
All voltages referenced to ground (pin 2); positive input current; all parameters are guaranteed over the ambient temperature range by design, but only 100% tested at +25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_3	supply current	dominant; V_1 = 1 V; V_{CC} < 5.1 V	–	–	78	mA
		dominant; V_1 = 1 V; V_{CC} < 5.25 V	–	–	80	mA
		dominant; V_1 = 1 V; V_{CC} < 5.5 V	–	–	85	mA
		recessive; V_1 = 4 V; R_8 = 47 kΩ	–	–	10	mA
		standby; note 1	–	–	275	μA
DC-bus transmitter						
V_{IH}	HIGH level input voltage	output recessive	0.7V_{CC}	–	V_{CC} + 0.3	V
V_{IL}	LOW level input voltage	output dominant	–0.3	–	0.3V_{CC}	V
I_{IH}	HIGH level input current	V_1 = 4 V	–200	–	+30	μA
I_{IL}	LOW level input voltage	V_1 = 1 V	100	–	600	μA
$V_{6,7}$	recessive bus voltage	V_1 = 4 V; no load	2.0	–	3.0	V
I_{LO}	off-state output leakage current	–2 V< (V_6,V_7) < 7 V	–2	–	+2	mA
		–5 V< (V_6,V_7) < 36 V	–10	–	+10	mA
V_7	CANH output voltage	V_1 = 1 V; V_{CC} = 4.75 to 5.5 V	3.0	–	4.5	V
		V_1 = 1 V; V_{CC} = 4.5 to 4.75 V	2.75	–	4.5	V
V_6	CANL output voltage	V_1 = 1 V	0.5	–	2.0	V
$\Delta V_{6,7}$	difference between output voltage at pins 6 and 7	V_1 = 1 V	1.5	–	3.0	V
		V_1 = 1 V; R_L = 45 Ω	1.5	–	–	V
		V_1 = 4 V; no load	–500	–	+50	mV
I_{sc7}	short-circuit CANH current	V_7 = –5 V	–	–	–200	mA
		V_7 = –36 V	–	–100	–	mA
I_{sc6}	short-circuit CANL current	V_6 = 36 V	–	–	200	mA
DC bus receiver [V_1 = 4 V; pins 6 and 7 externally driven; –2 V < (V6, V7) < 7 V; unless otherwise specified]						
$V_{diff(r)}$	differential input voltage (recessive)	note 2	–1.0	–	+0.5	V
		note 2; –7 V < (V_6, V_7) < 12 V	–1.0	–	+0.4	V
$V_{diff(d)}$	differential input voltage (dominant)		0.9	–	5.0	V
		–7 V < (V_6, V_7) < 12 V	1.0	–	5.0	V
		standby mode	0.97	–	5.0	V
		standby mode; V_{CC} = 4.5 to 5.25 V	0.91	–	5.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{diff(hys)}$	differential input hysteresis	see Fig.5	–	150	–	mV
V_{OH}	HIGH level output voltage (pin 4)	$I_4 = -100\ \mu A$	$0.8V_{CC}$	–	V_{CC}	V
V_{OL}	LOW level output voltage (pin 4)	$I_4 = 1$ mA	0	–	$0.2V_{CC}$	V
		$I_4 = 10$ mA	0	–	1.5	V
R_i	CANH, CANL input resistance		5	–	25	kΩ
R_{diff}	differential input resistance		20	–	100	kΩ
Reference output						
V_{ref}	reference output voltage	$V_8 = 1$ V; $I_5 < 50\ \mu A$	$0.45V_{CC}$	–	$0.55V_{CC}$	V
		$V_8 = 4$ V; $I_5 < 5\ \mu A$	$0.4V_{CC}$	–	$0.6V_{CC}$	V
Timing ($R_L = 60\ \Omega$; $C_L = 100$ pF; see Figs 3 and 4)						
t_{bit}	minimum bit time	$R_8 = 0\ \Omega$	–	–	1	µs
t_{onTXD}	delay TXD to bus active	$R_8 = 0\ \Omega$	–	–	50	ns
t_{offTXD}	delay TXD to bus inactive	$R_8 = 0\ \Omega$	–	40	80	ns
t_{onRXD}	delay TXD to receiver active	$R_8 = 0\ \Omega$	–	55	120	ns
t_{offRXD}	delay TXD to receiver inactive	$R_8 = 0\ \Omega$; $T_{amb} < +85$ °C; $V_{CC} = 4.5$ to 5.1 V	–	80	150	ns
		$R_8 = 0\ \Omega$; $V_{CC} = 4.5$ to 5.1 V	–	80	170	ns
		$R_8 = 0\ \Omega$; $T_{amb} < +85$ °C	–	90	170	ns
		$R_8 = 0\ \Omega$	–	90	190	ns
		$R_8 = 47\ k\Omega$	–	290	400	ns
t_{onRXD}	delay TXD to receiver active	$R_8 = 47\ k\Omega$	–	440	550	ns
$\|SR\|$	CANH, CANL slew rate	$R_8 = 47\ k\Omega$	–	7	–	V/µs
t_{WAKE}	wake-up time from standby (via pin 8)	see Fig.6	–	–	20	µs
t_{dRXDL}	bus dominant to RXD LOW	$V_8 = 4$ V; see Fig.7	–	–	3	µs
Standby/slope control (pin 8)						
V_{stb}	input voltage for standby mode		$0.75V_{CC}$	–	–	V
I_{slope}	slope control mode current		–10	–	–200	µA
V_{slope}	slope control mode voltage		$0.4V_{CC}$	–	$0.6V_{CC}$	V

Notes

1. $I_1 = I_4 = I_5 = 0$ mA; $0\ V < V_6 < V_{CC}$; $0\ V < V_7 < V_{CC}$; $V_8 = V_{CC}$; $T_{amb} < 90$ °C.
2. This is valid for the receiver in all modes, high-speed, slope control and standby.

TEST AND APPLICATION INFORMATION

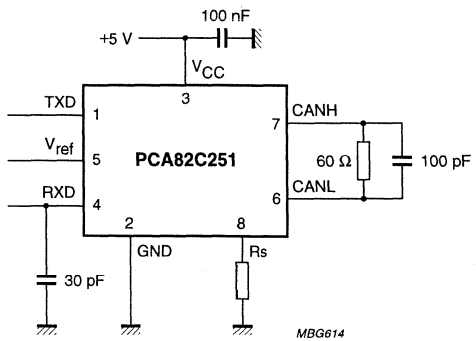


Fig.3 Test circuit for dynamic characteristics.

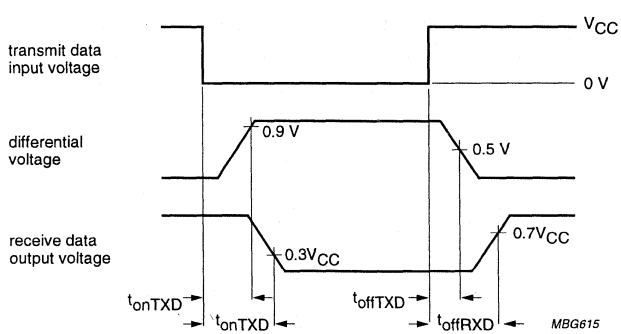


Fig.4 Timing diagram for dynamic characteristics.

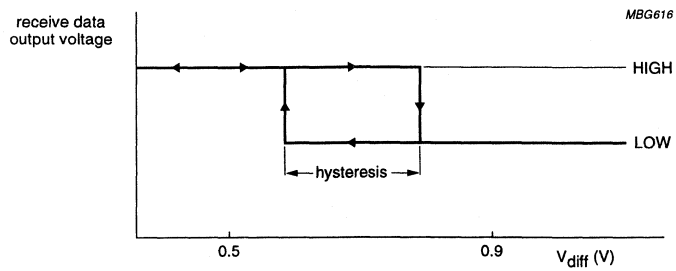
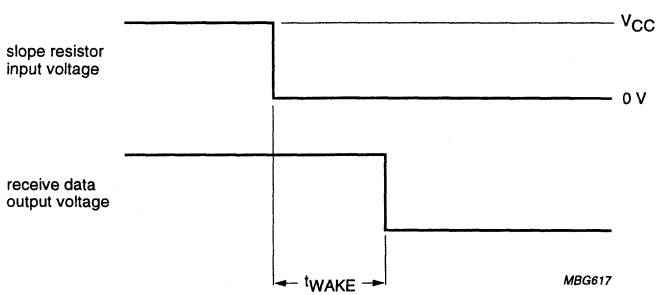
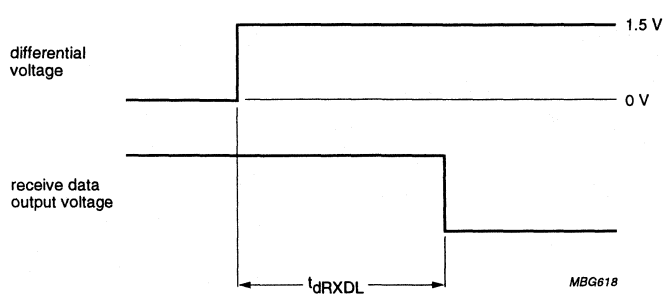


Fig.5 Hysteresis.



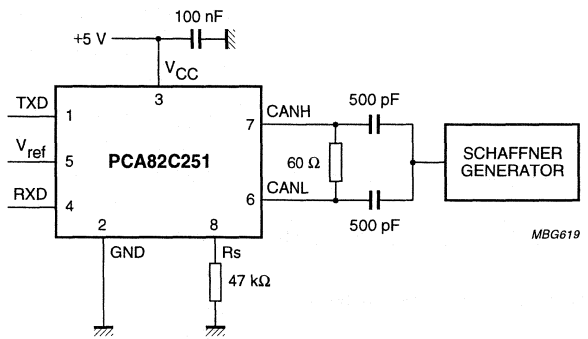
V_{TXD} = 1 V.

Fig.6 Timing diagram for wake up from standby.



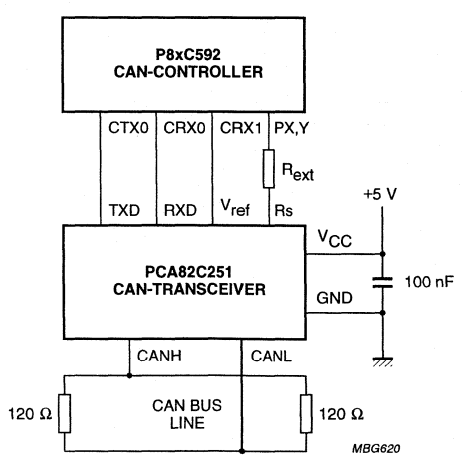
V_{Rs} = 4 V; V_{TXD} = 4 V.

Fig.7 Timing diagram for bus dominant to RXD low.



The wave forms of the applied transients shall be in accordance with *ISO 7637 part 1*, test pulses 1, 2, 3a and 3b.

Fig.8 Test circuit for automotive transients.



(1) The output control register of the P8xC592 should be programmed to 1AH (push-pull operation, dominant = LOW)
(2) If no slope control is desired; $R_{ext} = 0$.

Fig.9 Application of the PCA82C251 CAN Transceiver.

Fault-tolerant CAN transceiver PCA82C252

FEATURES

Optimized for in-car low-speed communication

- Baud rate up to 125 kBaud
- Up to 32 nodes can be connected
- Supports unshielded bus wires
- Low RFI due to built-in slope control function
- Fully integrated receiver filters.

Bus failure management

- Supports one-wire transmission modes with ground offset voltages up to 1.5 V
- Automatic switching to single-wire mode in the event of bus failure
- Automatic reset to differential mode if bus failure is removed.

Protection

- Short-circuit proof to battery and ground in 12 V powered systems
- Thermally protected
- Bus lines protected against transients in an automotive environment
- An unpowered node does not disturb the bus lines.

Support for low-power modes

- Low current sleep/standby mode with wake-up via the bus lines
- Wake-up via bus even without 5 V supply
- Output line for switching off/on external 5 V voltage regulator during sleep/wake-up mode.

GENERAL DESCRIPTION

The PCA82C252 is the interface between the CAN protocol controller and the physical bus. It is primarily intended for low-speed applications, up to 125 kBaud, in passenger cars. The device provides differential transmit capability but will switch in error conditions to a single-wire transmitter and/or receiver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MIN.	UNIT
V_{CC}	supply voltage		4.75	–	5.25	V
V_{BAT}	battery voltage	no time limit	–0.3	–	+27	V
		operating	6.0	–	27	V
		load dump	–	–	40	V
I_{sleep}	sleep mode current	V_{CC} = 0 V; V_{BAT} = 12 V	–	–	125	µA
$V_{11, 12}$	CANH, CANL input/output voltage pins 11 and 12	V_{CC} = 0 to 5.5 V; no time limit	–10	–	+27	V
V_{CANH}	CANH transmitter drop voltage	I_{CANH} = 50 mA	–	–	1.4	V
V_{CANL}	CANL transmitter drop voltage	I_{CANL} = 50 mA	–	–	1.4	V
t_{PD}	propagation delay	TXD to RXD	–	1	–	µs
t_r	bus output rise time	10% to 90%	–	0.5	–	µs
t_f	bus output fall time	90% to 10%	–	0.5	–	µs
T_{amb}	operating ambient temperature		–40	–	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA82C252	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

BLOCK DIAGRAM

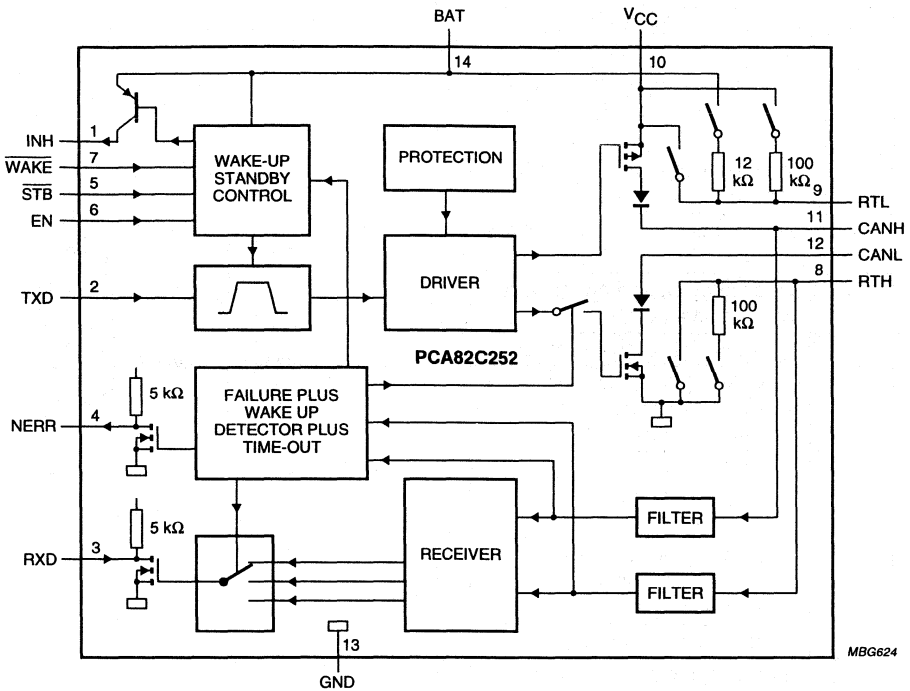


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
INH	1	inhibit output for switching external 5 V regulator
TXD	2	transmit data input, when LOW bus data will be dominant, when HIGH bus data will be recessive
RXD	3	receive data output, when LOW bus data will be dominant
NERR	4	error output pin, when LOW a bus error exists
$\overline{STB}$	5	not standby digital control input signal (active LOW)
EN	6	enable digital control input signal
$\overline{WAKE}$	7	not wake input signal, when pulled down INH becomes active for wake-up (active LOW)
RTH	8	termination resistor, CANH line will be high-impedance with certain bus errors
RTL	9	termination resistor, CANL line will be high-impedance with certain bus errors
V_{CC}	10	supply voltage (+5 V)
CANH	11	high voltage bus line, will be HIGH in dominant state
CANL	12	low voltage bus line, will be LOW in dominant state
GND	13	ground
BAT	14	battery voltage

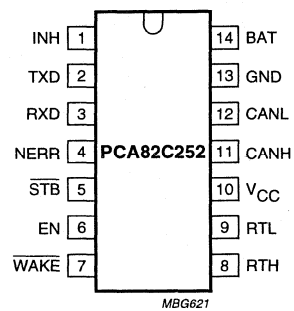


Fig.2 Pin configuration.

16-bit microcontroller with on-chip CAN XA-C3

DESCRIPTION

The XA-C3 device is a member of Philips' 80C51 XA (eXtended Architecture) family of high performance 16-bit single-chip microcontrollers, and is intended for industrial control applications.

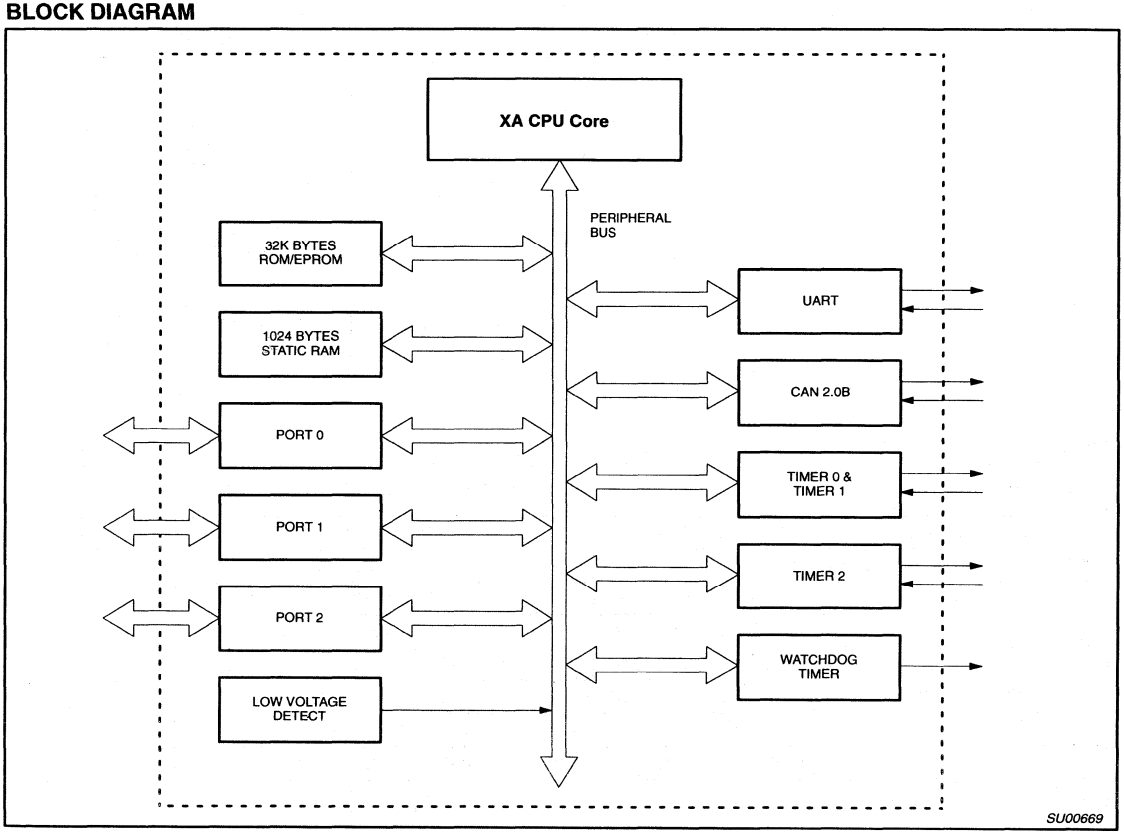
The XA-C3 device supports the full Controller Area Network (CAN) 2.0B. It supports both 11-bit and 29-bit identifiers (ID) at up to 1Mbit/s data rate. It is further optimized for DeviceNet™ applications.

The performance of the XA architecture supports the comprehensive bit-oriented operations of the 80C51 while incorporating support for multi-tasking operating systems and high-level languages such as C. The speed of the XA architecture, at 10 to 100 times that of the 80C51, gives designers an easy path to truly high performance embedded control, while maintaining great flexibility to adapt software to specific requirements.

Specific Features of the XA-C3

- 2.7V to 5.5V operation
- 32K bytes of on-chip EPROM/ROM program memory
- 1024 bytes of on-chip data RAM
- CAN block supporting full CAN2.0B, with 11-/29-bit ID and up to 1Mbit/s
- Three standard counter/timers with enhanced features (equivalent to 80C51 T0, T1, and T2) with outputs
- Watchdog timer with output
- 1 UART
- Low voltage detect
- Three 8-bit I/O ports with 4 programmable output configurations
- EPROM/OTP versions can be programmed in circuit
- 25MHz operating frequency at 4.5 – 5.5V V_{CC} over commercial operating conditions; 16MHz at 2.7V – 3.6V V_{CC}
- 40-pin DIP, 44-pin PLCC, and 44-pin QFP packages

BLOCK DIAGRAM



DeviceNet™ is a trademark of Open DeviceNet Vendor Association (OVDA).

CMOS single-chip 8-bit microcontroller — 80C575/83C575/87C575

DESCRIPTION

The Philips 80C575/83C575/87C575 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity.

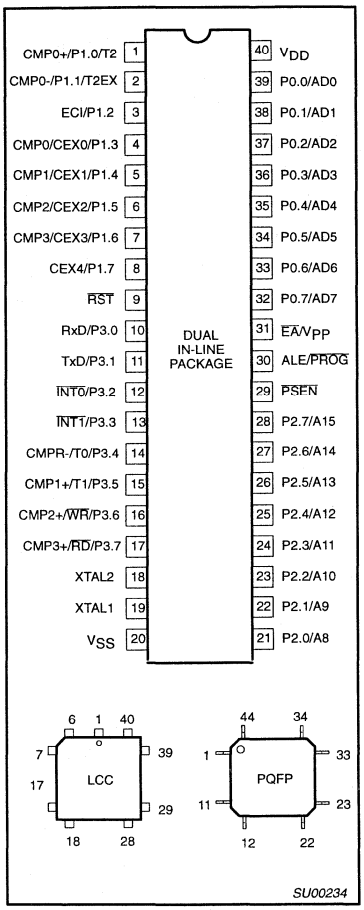
The 8XC575 contains an 8k × 8 ROM (83C575) EPROM (87C575), a 256 × 8 RAM, 32 I/O lines, three 16-bit counter/timers, a Programmable Counter Array (PCA), a seven-source, two-priority level nested interrupt structure, an enhanced UART, four analog comparators, power-fail detect and oscillator fail detect circuits, and on-chip oscillator and clock circuits.

In addition, the 8XC575 has a low active reset, and the port pins are reset to a low level. There is also a fully configurable watchdog timer, and internal power on clear circuit. The part includes idle mode and power-down mode states for reduced power consumption.

FEATURES

- 80C51 based architecture
  - 8k × 8 ROM (83C575)
  - 8k × 8 EPROM (87C575)
  - ROMless (80C575)
  - 256 × 8 RAM
  - Three 16-bit counter/timers
  - Programmable Counter Array
  - Enhanced UART
  - Boolean processor
  - Oscillator fail detect
  - Low active reset
  - Asynchronous low port reset
  - Schmitt trigger inputs
  - 4 analog comparators
  - Watchdog timer
  - Low V_{CC} detect
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- 4.0 to 16MHz
- Extended temperature ranges
- OTP package available

PIN CONFIGURATIONS

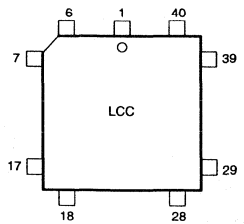


ORDERING INFORMATION

ROMless	ROM	EPROM[1]		TEMPERATURE RANGE °C AND PACKAGE	FREQ (MHz)	DRAWING NUMBER
P80C575EBPN	P83C575EBPN	P87C575EBPN	OTP	0 to +70, 40-Pin Plastic Dual In-line Package	16	SOT129-1
P80C575EBAA	P83C575EBAA	P87C575EBAA	OTP	0 to +70, 44-Pin Plastic Leaded Chip Carrier	16	SOT187-2
		P87C575EBFFA	UV	0 to +70, 40-Pin Ceramic Dual In-line Package	16	0590B
		P87C575EBLKA	UV	0 to +70, 44-Pin Ceramic Leaded Chip Carrier	16	1472A
P80C575EHPN	P83C575EHPN	P87C575EHPN	OTP	–40 to +125, 40-Pin Plastic Dual In-line Package	16	SOT129-1
P80C575EHAA	P83C575EHAA	P87C575EHAA	OTP	–40 to +125, 44-Pin Plastic Leaded Chip Carrier	16	SOT187-2
		P87C575EHFFA	UV	–40 to +125, 40-Pin Ceramic Dual In-line Package	16	0590B
		P87C575EHLKA	UV	–40 to +125, 44-Pin Ceramic Leaded Chip Carrier	16	1472A
P80C575EBBB	P83C575EBBB	P87C575EBBB	OTP	0 to +70, 44-Pin Plastic Quad Flat Pack	16	SOT307-2

NOTE:
1. OTP - One Time Programmable EPROM. UV - Erasable EPROM

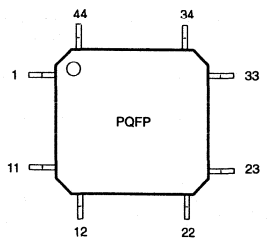
CERAMIC AND PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS



Pin	Function	Pin	Function
1	NC	23	NC
2	T2/P1.0/CMP0+	24	P2.0/A8
3	T2EX/P1.1/CMP0–	25	P2.1/A9
4	P1.2/ECI	26	P2.2/A10
5	P1.3/CMP0/CEX0	27	P2.3/A11
6	P1.4/CMP1/CEX1	28	P2.4/A12
7	P1.5/CMP2/CEX2	29	P2.5/A13
8	P1.6/CMP3/CEX3	30	P2.6/A14
9	P1.7/CEX4	31	P2.7/A15
10	$\overline{RST}$	32	$\overline{PSEN}$
11	RxD/P3.0	33	ALE/$\overline{PROG}$
12	NC	34	NC
13	TxD/P3.1	35	$\overline{EA}$/V_{PP}
14	$\overline{INT0}$/P3.2	36	P0.7/AD7
15	$\overline{INT1}$/P3.3	37	P0.6/AD6
16	T0/P3.4/CMPR–	38	P0.5/AD5
17	T1/P3.5/CMP1+	39	P0.4/AD4
18	$\overline{WR}$/P3.6/CMP2+	40	P0.3/AD3
19	$\overline{RD}$/P3.7/CMP3+	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	V_{SS}	44	V_{CC}

SU00235

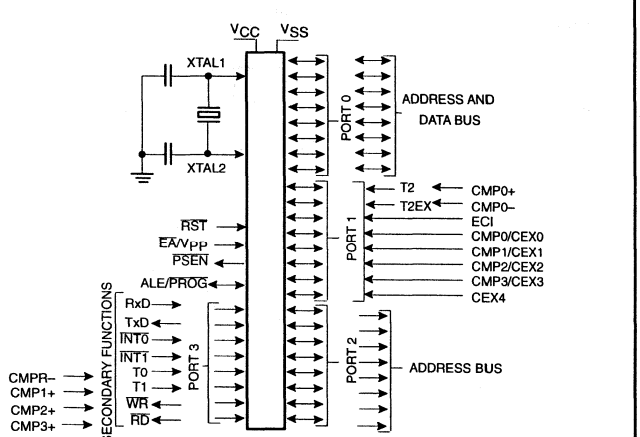
PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function
1	P1.5/CMP2/CEX2	23	P2.5/A13
2	P1.6/CMP3/CEX3	24	P2.6/A14
3	P1.7/CEX4	25	P2.7/A15
4	$\overline{RST}$	26	$\overline{PSEN}$
5	RxD/P3.0	27	ALE/$\overline{PROG}$
6	NC	28	NC
7	TxD/P3.1	29	$\overline{EA}$/V_{PP}
8	$\overline{INT0}$/P3.2	30	P0.7/AD7
9	$\overline{INT1}$/P3.3	31	P0.6/AD6
10	T0/P3.4/CMPR–	32	P0.5/AD5
11	T1/P3.5/CMP1+	33	P0.4/AD4
12	$\overline{WR}$/P3.6/CMP2+	34	P0.3/AD3
13	$\overline{RD}$/P3.7CMP3+	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	V_{SS}	38	V_{CC}
17	NC	39	NC
18	P2.0/A8	40	T2/P1.0/CMP0+
19	P2.1/A9	41	T2EX/P1.1/CMP0–
20	P2.2/A10	42	P1.2/ECI
21	P2.3/A11	43	P1.3/CMP0/CEX0
22	P2.4/A12	44	P1.4/CMP1/CEX1

SU00236

LOGIC SYMBOL



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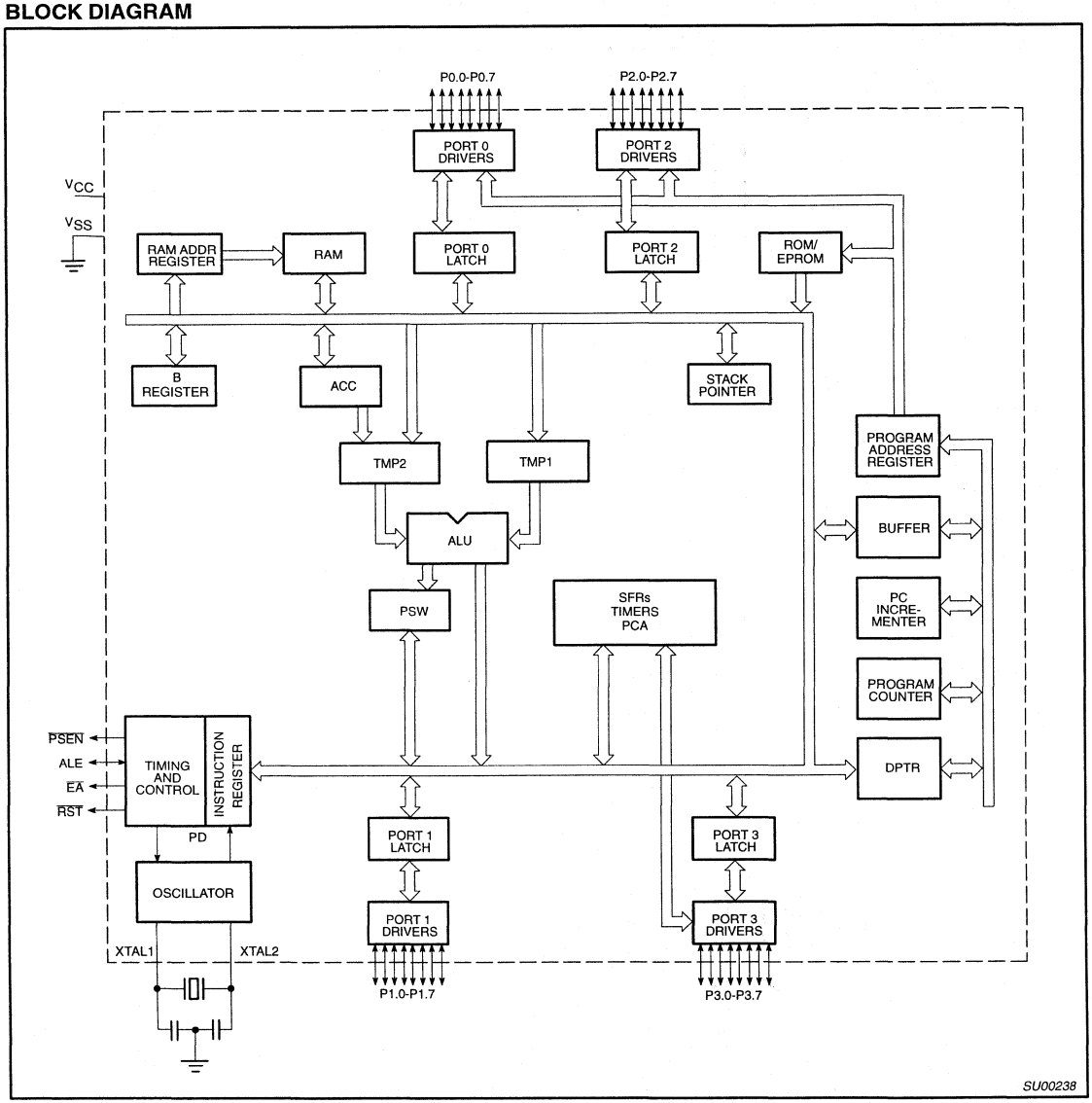
BLOCK DIAGRAM



PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER DIP	LCC	QFP	TYPE	NAME AND FUNCTION
V_{SS}	20	22	16	I	**Ground:** 0V reference.
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0-0.7	39-32	43-36	37-30	I/O	**Port 0:** Port 0 is an open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also receives code bytes during EPROM programming and outputs code bytes during program verification. External pull-ups are required during program verification. During reset, port 0 will be asynchronously driven low and will remain low until written to by software. All port 0 pins have Schmitt trigger inputs with 200mV hysteresis. A weak pulldown on port 0 guarantees positive leakage current (see DC Electrical Characteristics: I_{L1}).
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port. Port 1 pins have internal pull-ups such that pins that have 1s written to them can be used as inputs but will source current when externally pulled low (see DC Electrical Characteristics: I_{IL}). Port 1 receives the low-order address byte during program memory verification and EPROM programming. During reset, port 1 will be asynchronously driven low and will remain low until written to by software. All port 1 pins have Schmitt trigger inputs with 50mV hysteresis. Port 1 pins also serve alternate functions as follows:
	1	2	40	I/O	**P1.0** **T2** Timer 2 external I/O **CMP0+** Comparator 0 positive input
	2	3	41	I	**P1.1** **T2EX** Timer 2 capture input **CMP0-** Comparator 0 negative input
	3	4	42	I	**P1.2** **ECI** PCA count input
	4	5	43	I/O	**P1.3** **CEX0** PCA module 0 external I/O **CMP0** Comparator 0 output
	5	6	44	I/O	**P1.4** **CEX1** PCA module 1 external I/O **CMP1** Comparator 1 output
	6	7	1	I/O	**P1.5** **CEX2** PCA module 2 external I/O **CMP2** Comparator 2 output
	7	8	2	I/O	**P1.6** **CEX3** PCA module 3 external I/O **CMP3** Comparator 3 output
	8	9	3	I/O	**P1.7** **CEX4** PCA module 4 external I/O
P2.0-P2.7	21-28	24-31	18-25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them can be used as inputs, but will source current when externally pulled low (see DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during accesses to external program and data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. Port 2 receives the high-order address byte during program verification and EPROM programming. During reset, port 2 will be asynchronously driven low and will remain low until written to by software. Port 2 can be made open drain by writing to the P2OD register (AIH). In open drain mode, weak pulldowns on port 2 guarantee positive leakage current (see DC Electrical Characteristics I_{L1}).
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins except P3.1 that have 1s written to them can be used as inputs but will source current when externally pulled low (see DC Electrical Characteristics: I_{IL}). P3.1 will be a high impedance pin except while transmitting serial data, in which case the strong pull-up will remain on continuously when outputting a 1 level. The P3.1 output drive level when transmitting can be set to one of two levels by the writing to the P3.1 register bit. During reset all pins (except P3.1) will be asynchronously driven low and will remain low until written to by software. All port 3 pins have Schmitt trigger inputs with 200mV hysteresis, except P3.2 and P3.3, which have 50mV hysteresis. Port 3 pins serve alternate functions as follows:

PIN DESCRIPTIONS (Continued)

MNEMONIC	PIN NUMBER DIP	LCC	QFP	TYPE	NAME AND FUNCTION
					Port 3: (continued)
	10	11	5	I	**P3.0 RxD** Serial receive port
	11	13	7	O	**P3.1 TxD** Serial transmit port enabled only when transmitting serial data
	12	14	8	I	**P3.2 $\overline{INT0}$** External interrupt 0
	13	15	9	I	**P3.3 $\overline{INT1}$** External interrupt 1
	14	16	10	I	**P3.4 T0** Timer/counter 0 input **CMPR-** Common - reference to comparators 1, 2, 3
	15	17	11	I	**P3.5 T1** Timer/counter 1 input **CMP1+** Comparator 1 positive input
	16	18	12	O	**P3.6 $\overline{WR}$** External data memory write strobe **CMP2+** Comparator 2 positive input
	17	19	13	O	**P3.7 $\overline{RD}$** External data memory read strobe **CMP3+** Comparator 3 positive input
$\overline{RST}$	9	10	4	I	**Reset:** A low on this pin asynchronously resets all port pins to a low state except P3.1. The pin must be held low with the oscillator running for 24 oscillator cycles to initialize the internal registers. An internal diffused resistor to V_{CC} permits a power on reset using only an external capacitor to V_{SS}. RST has a Schmitt trigger input stage to provide additional noise immunity with a slow rising input voltage.
ALE/$\overline{PROG}$	30	33	27	I/O	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. ALE is switched off if the bit 0 in the AUXR register (8EH) is set. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming.
$\overline{PSEN}$	29	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
$\overline{EA}$/V_{PP}	31	35	29	I	**External Access Enable/Programming Supply Voltage:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H to 1FFFH. If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 1FFFH. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

Table 1. 87C575 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB							LSB	RESET VALUE
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
AUXR#	Auxiliary	8EH	–	–	–	–	–	–	LO	AO	xxxxxx00B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
CCAP0H#	Module 0 Capture High	FAH									xxxxxxxxB
CCAP1H#	Module 1 Capture High	FBH									xxxxxxxxB
CCAP2H#	Module 2 Capture High	FCH									xxxxxxxxB
CCAP3H#	Module 3 Capture High	FDH									xxxxxxxxB
CCAP4H#	Module 4 Capture High	FEH									xxxxxxxxB
CCAP0L#	Module 0 Capture Low	EAH									xxxxxxxxB
CCAP1L#	Module 1 Capture Low	EBH									xxxxxxxxB
CCAP2L#	Module 2 Capture Low	ECH									xxxxxxxxB
CCAP3L#	Module 3 Capture Low	EDH									xxxxxxxxB
CCAP4L#	Module 4 Capture Low	EEH									xxxxxxxxB
CCAPM0#	Module 0 Mode	DAH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM1#	Module 1 Mode	DBH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM2#	Module 2 Mode	DCH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM3#	Module 3 Mode	DDH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM4#	Module 4 Mode	DEH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
			DF	DE	DD	DC	DB	DA	D9	D8	
CCON*#	PCA Counter Control	D8H	CF	CR	–	CCF4	CCF3	CCF2	CCF1	CCF0	00x00000B
CH#	PCA Counter High	F9H									00H
CL#	PCA Counter Low	E9H									00H
CMOD#	PCA Counter Mode	D9H	CIDL	WDTE	–	–	–	CPS1	CPS0	ECF	00xxx000B
			EF	EE	ED	EC	EB	EA	E9	E8	
CMP*#	Comparator	E8H	EC3DP	EC2DP	EC1DP	EC0DP	C3RO	C2RO	C1RO	C0RO	00H
CMPE#	Comparator Enable	91H	EC3TDC	EC2TDC	EC1TDC	EC0TDC	EC3OD	EC2OD	EC1OD	EC0OD	00H
DPTR:	Data Pointer (2 bytes)										
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*	Interrupt Enable	A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0	00H
			BF	BE	BD	BC	BB	BA	B9	B8	
IP*	Interrupt Priority	B8H	–	PPC	PT2	PS	PT1	PX1	PT0	PX0	x0000000B
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	00H
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	CEX4	CEX3	CEX2	CEX1	CEX0	EXI	T2EX	T2	00H
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	00H
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TxD	RxD	00H

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.

Table 1. 87C575 Special Function Registers (Continued)

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB LSB								RESET VALUE
P2OD#	Port 2 Pullup Disable	A1H									00H
PCON	Power Control	87H	SMOD1	SMOD0	OSF[1]	POF[1]	LVF[1]	GF0	PD	IDL	00xxx000B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	00H
RACAP2H#	Timer 2 Capture High	CBH									00H
RACAP2L#	Timer 2 Capture Low	CAH									00H
SADDR#	Slave Address	A9H									00H
SADEN#	Slave Address Mask	B9H									00H
SBUF	Serial Data Buffer	99H									xxxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial Control	98H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SP	Stack Pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IE0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON*	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00H
T2MOD#	Timer 2 Mode Control	C9H	–	–	–	–	–	–	–	DCEN	xxxxxxx0B
TH0	Timer High 0	8CH									00H
TH1	Timer High 1	8DH									00H
TH2#	Timer High 2	CDH									00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low 1	8BH									00H
TL2#	Timer Low 2	CCH									00H
TMOD	Timer Mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H
			C7	C6	C5	C4	C3	C2	C1	C0	
WDCON*#	Watchdog Timer Control	C0H	PRE2	PRE1	PRE0	LVRE	OFRE	WDRUN	WDTOF	WDMOD	11111101B
WDL#	Watchdog Timer Reload	C1H									00H
WFEED1#	Watchdog Feed 1	C2H									xxH
WFEED2#	Watchdog Feed 2	C3H									xxH

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.
1. Reset value depends on reset source.

POWER ON CLEAR/ POWER ON FLAG

An on-chip Power On Detect Circuit resets the 8XC575 and sets the Power Off Flag (PCON.4) on power up or if V_{CC} drops to zero momentarily. The POF can only be cleared by software. The RST pin is not driven by the power on detect circuit. The POF can be read by software to determine that a power failure has occurred and can also be set by software.

LOW VOLTAGE DETECT

An on-chip Low Voltage Detect circuit sets the Low Voltage Flag (PCON.3) if V_{CC} drops below V_{LOW} (see DC Electrical Characteristics) and resets the 8XC575 if the Low Voltage Reset Enable bit (WDCON.4) is set. If the LVRE is cleared, the reset is disabled but LVF will still be set if V_{CC} is low. The RST pin is not driven by the low voltage detect circuit. The LVF can be read by software to determine that V_{CC} was low. The LVF can be set or cleared by software.

OSCILLATOR FAIL DETECT

An on-chip Oscillator Fail Detect circuit sets the Oscillator Fail Flag (PCON.5) if the oscillator frequency drops below OSCF for one or more cycles (see AC Electrical Characteristics: OSCF) and resets the 8XC575 if the Oscillator Fail Reset Enable bit (WDCON.3) is set. If OFRE is cleared, the reset is disabled but OSF will still be set if the oscillator fails. The RST pin is not driven by the oscillator fail detect circuit. The OSF can be read by software to determine that an oscillator failure has occurred. The OSF can be set or cleared by software.

LOW ACTIVE RESET

One of the most notable features on this part is the low active reset. At this time this is the only 80C51 derivative available that has low active reset. This feature makes it easier to interface the 8XC575 into an application to accommodate the power-on and low voltage conditions that can occur. The low active reset operates exactly the same as high active reset with the exception that the part is put into the reset mode by applying a low level to the reset pin. For power-on reset it is also necessary to invert the power-on reset circuit; connecting the 8.2K resistor from the reset pin to V_{CC} and the 10µf capacitor from the reset pin to ground. Figure 1 shows all of the reset related circuitry.

When reset the port pins on the 87C575 are driven low asynchronously. This is different from all other 80C51 derivatives.

The 8XC575 also has Low voltage detection circuitry that will, if enabled, force the part to reset when V_{CC} (on the part) fails below a set level. Low Voltage Reset is enabled by a normal reset. Low Voltage Reset can be disabled by clearing LVRE (bit 4 in the WDCON SFR) then executing a watchdog feed sequence (A5H to WFEED1 followed immediately by 5A to WFEED2). In addition there is a flag (LVF) that is set if a low voltage condition is detected. The LVF flag is set even if the Low Voltage detection circuitry is disabled. Notice that the Low voltage detection circuitry does not drive the RST# pin so the LVF flag is the only way that the microcontroller can determine if it has been reset due to a low voltage condition.

The 8XC575 has an on-chip power-on detection circuit that sets the POF (PCON.4) flag on power up or if the V_{CC} level momentarily drops to 0V. This flag can be used to determine if the part is being started from a power-on (cold start) or if a reset has occurred due to another condition (warm start).

TIMERS

The 87C575 has four on-chip timers.

Timers 0 and 1 are identical in every way to Timers 0 and 1 on the 80C51.

Timer 2 on the 8XC575 is identical to the 80C52 Timer 2 (described in detail in the 80C52 overview) with the exception that it is an up or down counter. To configure the Timer to count down the DCEN bit in the T2MOD special function register must be set and a low level must be present on the T2EX pin (P1.1).

The Watchdog timer operation and implementation is the same as that for the 8XC550 (described in the 8XC550 overview) with the exception that the reset values of the WDCON and WDL special function registers have been changed. The changes in these registers cause the watchdog timer to be enabled with a timeout of 98304 × T_{OSC} when the part is reset. The watchdog can be disabled by executing a valid feed sequence and then clearing WDRUN (bit 2 in the WDCON SFR).

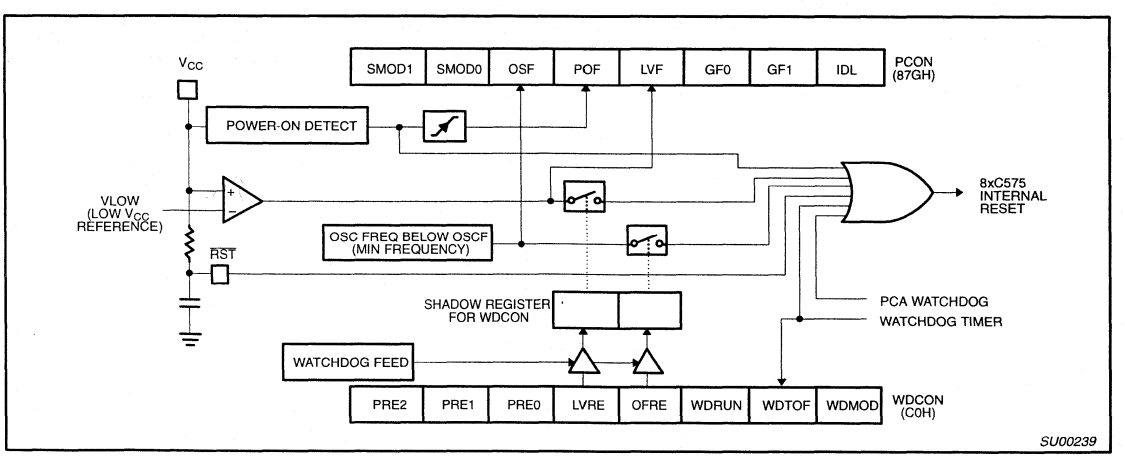


Figure 1. Reset Circuitry

PROGRAMMABLE COUNTER ARRAY (PCA)

The Programmable Counter Array is a special Timer that has five 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. Each module has a pin associated with it in port 1. Module 0 is connected to P1.3(CEX0), module 1 to P1.4(CEX1), etc.. The basic PCA configuration is shown in Figure 2.

The PCA timer is a common time base for all five modules and can be programmed to run at: 1/12 the oscillator frequency, 1/4 the oscillator frequency, the Timer 0 overflow, or the input on the ECI pin (P1.2). The timer count source is determined from the CPS1 and CPS0 bits in the CMOD SFR as follows (see Figure 3):

CPS1	CPS0	PCA Timer Count Source
0	0	1/12 oscillator frequency
0	1	1/4 oscillator frequency
1	0	Timer 0 overflow
1	1	External Input at ECI pin

In the CMOD SFR are three additional bits associated with the PCA. They are CIDL which allows the PCA to stop during idle mode, WDTE which enables or disables the watchdog function on module 4, and ECF which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows. These functions are shown in Figure 3.

The watchdog timer function is implemented in module 4 as implemented in other parts that have a PCA that are available on the market. However, if a watchdog timer is required in the target application, it is recommended to use the hardware watchdog timer that is implemented on the 87C575 separately from the PCA (see Figure 14).

The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (refer to Figure 6). To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set, The CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software. The PCA interrupt system shown in Figure 4.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (see Figure 7). The registers contain the bits that control the mode that each module will operate in. The ECCF bit (CCAPMn.0 where n=0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module. PWM (CCAPMn.1) enables the pulse width modulation mode. The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register. The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition. The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function. Figure 8 shows the CCAPMn settings for the various PCA functions.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output.

PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated. Refer to Figure 9.

16-bit Software Timer Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (see Figure 10).

High Speed Output Mode

In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (see Figure 11).

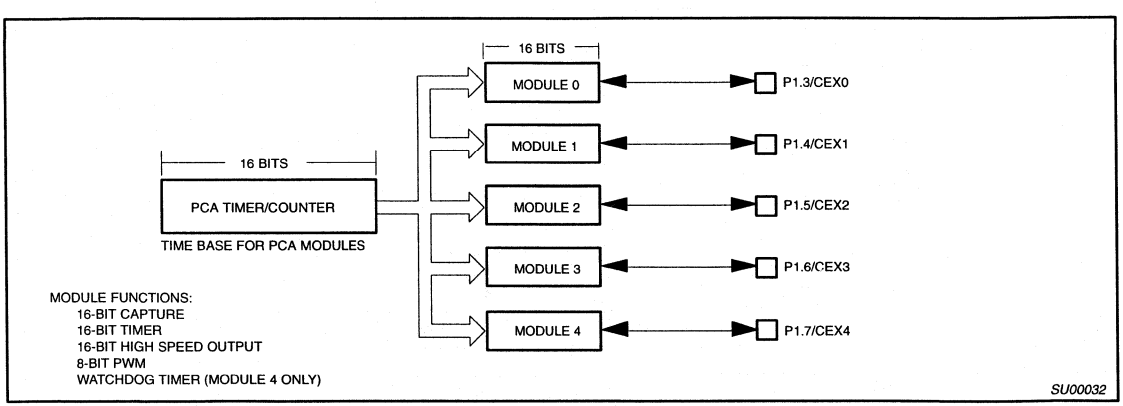


Figure 2. Programmable Counter Array (PCA)

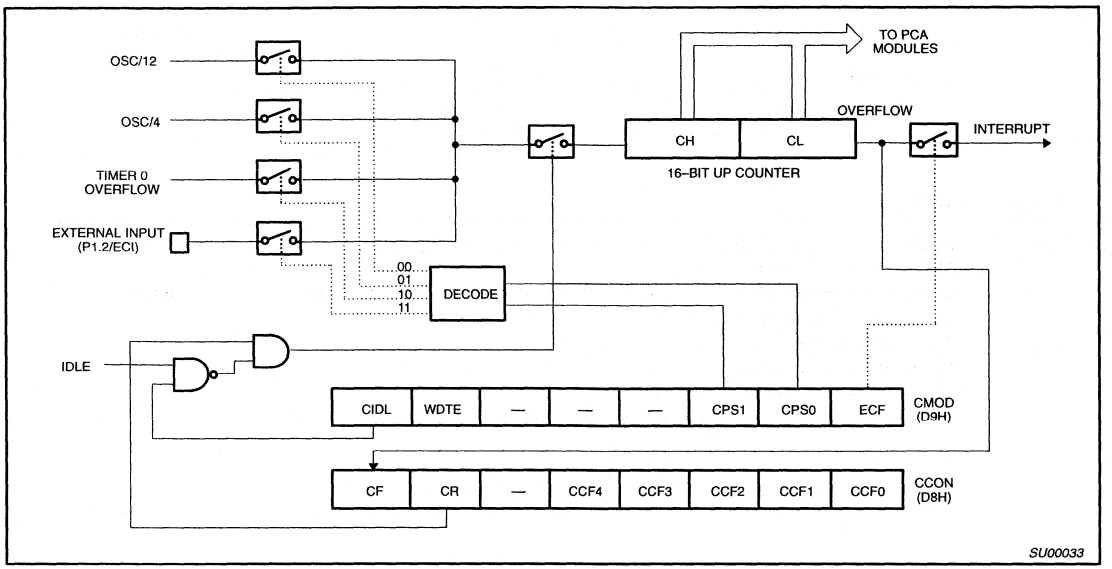


Figure 3. PCA Timer/Counter

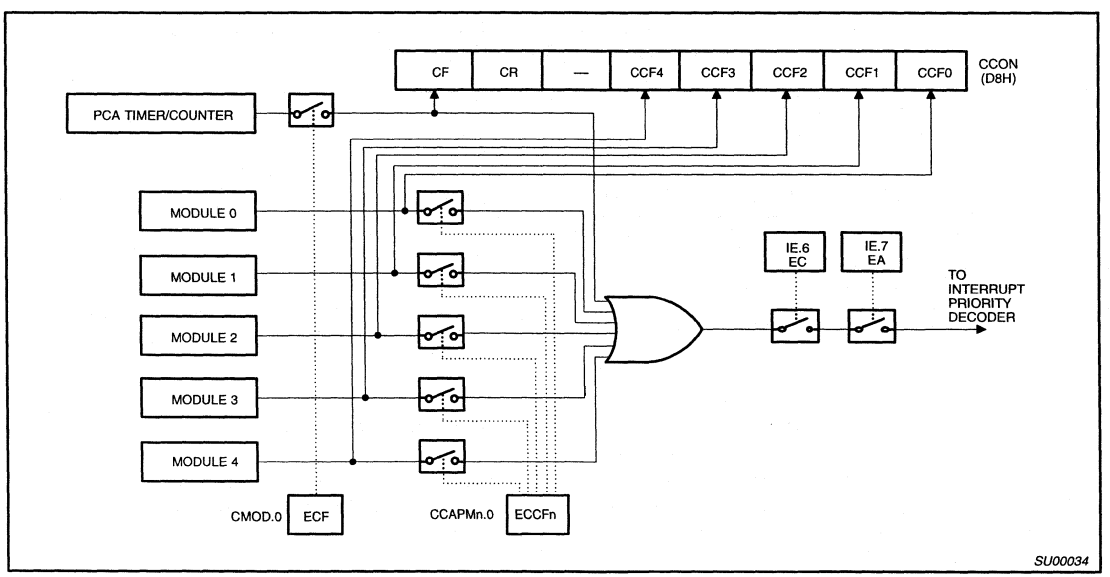


Figure 4. PCA Interrupt System

CMOD Address = OD9H Reset Value = 00XX X000B

Bit Addressable

CIDL	WDTE	–	–	–	CPS1	CPS0	ECF
7	6	5	4	3	2	1	0

Bit:

Symbol	Function
CIDL	Counter Idle control: CIDL = 0 programs the PCA Counter to continue functioning during idle Mode. CIDL = 1 programs it to be gated off during idle.
WDTE	Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA Module 4. WDTE = 1 enables it.
–	Not implemented, reserved for future use.*
CPS1	PCA Count Pulse Select bit 1.
CPS0	PCA Count Pulse Select bit 0.

CPS1	CPS0	Selected PCA Input**	
0	0	0	Internal clock, Fosc ÷ 12
0	1	1	Internal clock, Fosc ÷ 4
1	0	2	Timer 0 overflow
1	1	3	External clock at ECI/P1.2 pin (max. rate = Fosc ÷ 8)

ECF	PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.

NOTE:
* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.
** –Fosc = oscillator frequency

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Figure 5. CMOD: PCA Counter Mode Register

CCON Address = OD8H Reset Value = 00X0 0000B

Bit Addressable

CF	CR	–	CCF4	CCF3	CCF2	CCF1	CCF0
7	6	5	4	3	2	1	0

Bit:

Symbol	Function
CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
CR	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
–	Not implemented, reserved for future use*.
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

NOTE:
* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

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Figure 6. CCON: PCA Counter Control Register

CCAPMn Address CCAPM0 0DAH
CCAPM1 0DBH
CCAPM2 0DCH
CCAPM3 0DDH
CCAPM4 0DEH

Reset Value = X000 0000B

Not Bit Addressable

	–	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Bit:	7	6	5	4	3	2	1	0

Symbol	Function
–	Not implemented, reserved for future use*.
ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.
MATn	Match. When MATn = 1, a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.
PWMn	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.
ECCFn	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

NOTE:
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

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Figure 7. CCAPMn: PCA Modules Compare/Capture Registers

–	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	MODULE FUNCTION
X	0	0	0	0	0	0	0	No operation
X	X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	X	0	1	0	0	0	X	16-bit capture by a negative trigger on CEXn
X	X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
X	1	0	0	1	0	0	X	16-bit Software Timer
X	1	0	0	1	1	0	X	16-bit High Speed Output
X	1	0	0	0	0	1	0	8-bit PWM
X	1	0	0	1	X	0	X	Watchdog Timer

Figure 8. PCA Module Modes (CCAPMn Register)

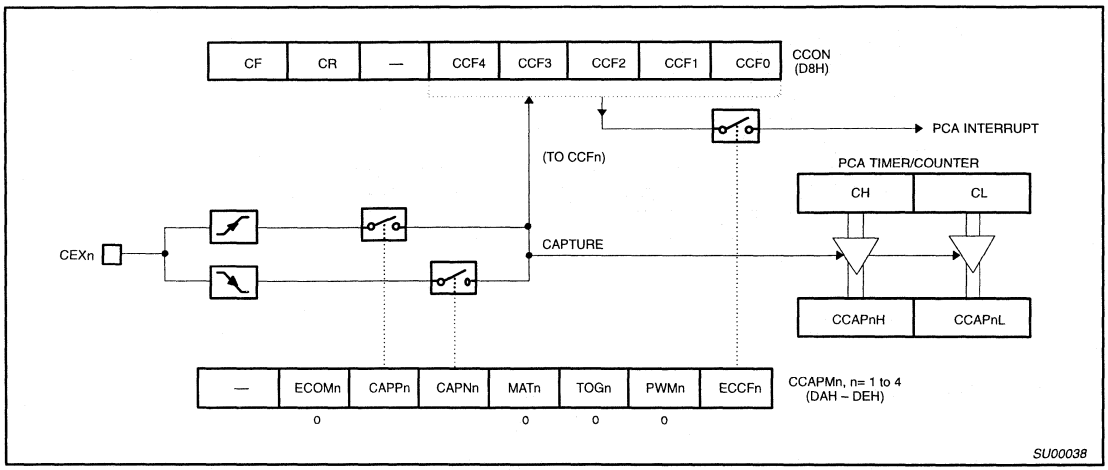


Figure 9. PCA Capture Mode

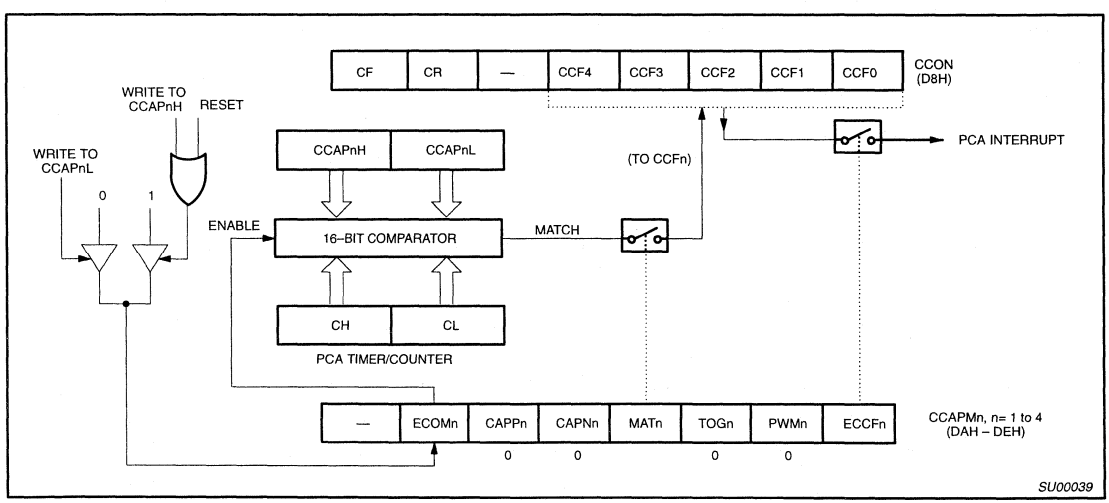


Figure 10. PCA Compare Mode

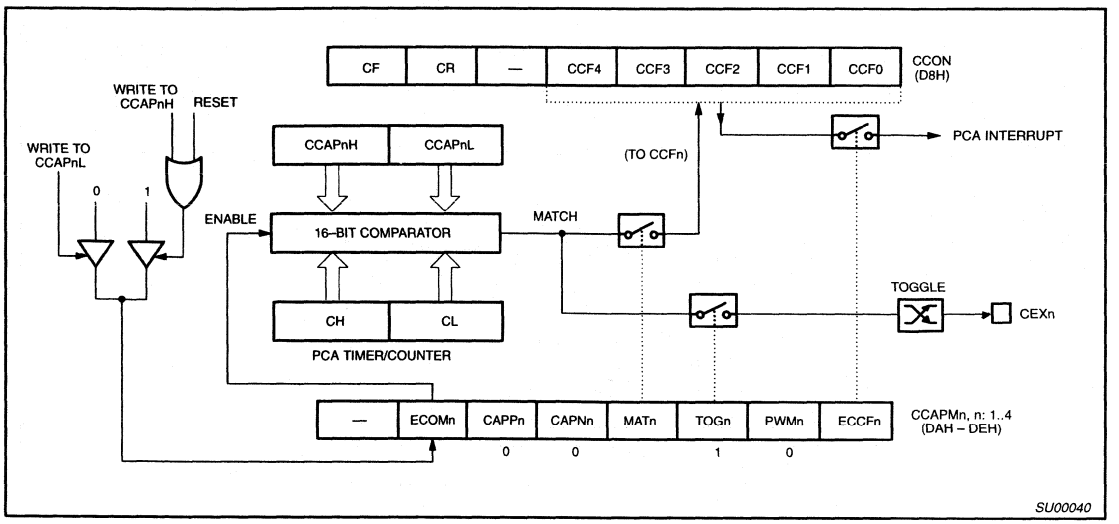


Figure 11. PCA High Speed Output Mode

Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. Figure 12 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. the allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.

WATCHDOG TIMER

The watchdog timer is not directly loadable by the user. Instead, the value to be loaded into the main timer is held in an autoload register or is part of the mask ROM programming. In order to cause the main timer to be loaded with the appropriate value, a special sequence of software action must take place. This operation is referred to as feeding the watchdog timer.

To feed the watchdog, two instructions must be sequentially executed successfully. No intervening instruction fetches are allowed, so interrupts should be disabled before feeding the watchdog. The instructions should move A5H to the WFEED1 register and then 5AH to the WFEED2 register. If WFEED1 is correctly loaded and WFEED2 is not correctly loaded, then an immediate underflow will occur.

The watchdog timer subsystem has two modes of operation. Its principal function is a watchdog timer. In this mode it protects the system from incorrect code execution by causing a system reset when the watchdog timer underflows as a result of a failure of software to feed the timer prior to the timer reaching its terminal count. If the user does not employ the watchdog function, the watchdog subsystem can be used as a timer. In this mode, reaching the terminal count sets a flag. In most other respects, the timer mode possesses the characteristics of the watchdog mode. This is done to protect the integrity of the watchdog function.

The watchdog timer subsystem consists of a prescaler and a main counter. The prescaler has 8 selectable taps off the final stages and the output of a selected tap provides the clock to the main counter. The main counter is the section that is loaded as a result of the software feeding the watchdog and it is the section that causes the system reset (watchdog mode) or time-out flag to be set (timer mode) if allowed to reach its terminal count.

Programming the Watchdog Timer

Both the EPROM and ROM devices have a set of SFRs for holding the watchdog autoload values and the control bits. The watchdog time-out flag is present in the watchdog control register and operates the same in all versions. In the EPROM device, the watchdog parameters (autoload value and control) are always taken from the SFRs. In the ROM device, the watchdog parameters can be mask programmed or taken from the SFRs. The selection to take the watchdog parameters from the SFRs or from the mask programmed values is controlled by EA (external access). When EA is high (internal ROM access), the watchdog parameters are taken from the mask programmed values. If the watchdog is mask programmed to the timer mode, then the autoload values and the pre-scaler taps are taken from the SFRs. When EA is low (external access), the watchdog parameters are taken from the SFRs. The user should be able to leave code in his program which initializes the watchdog SFRs even though he has migrated to the mask ROM part. This allows no code changes from EPROM prototyping to ROM coded production parts.

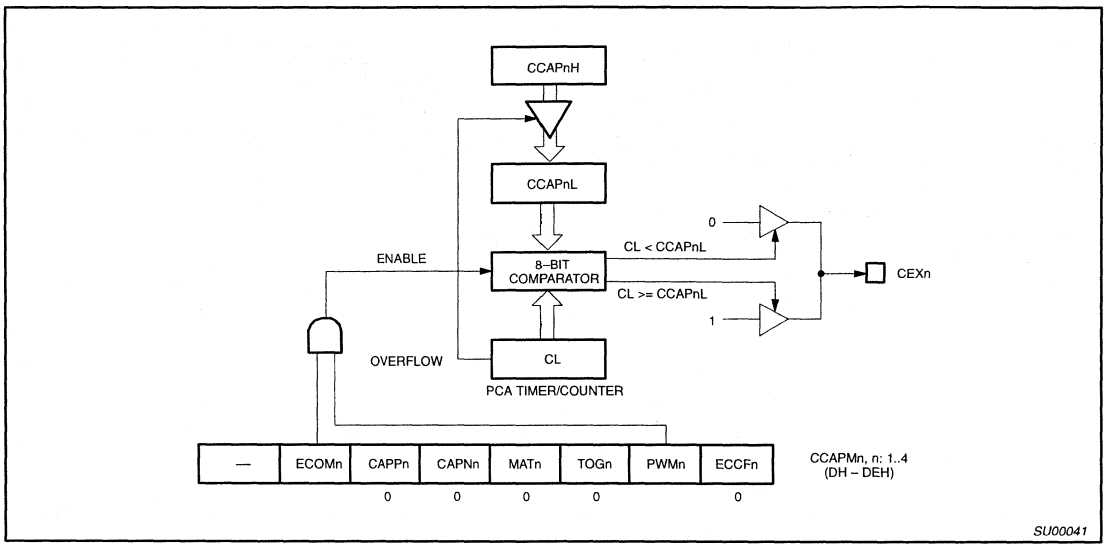


Figure 12. PCA PWM Mode

Watchdog Detailed Operation

EPROM Device (and ROMless Operation: $\overline{EA}$ = 0)

In the ROMless operation (ROM part, $\overline{EA}$ = 0) and in the EPROM device, the watchdog operates in the following manner (see Figure 14).

Whether the watchdog is in the watchdog or timer mode, when external RESET is applied, the following takes place:

- Watchdog mode bit set to watchdog mode.
- Watchdog run control bit set to ON.
- Autoload register set to 00 (min. count).
- Watchdog time-out flag cleared.
- Prescaler is cleared.
- Prescaler tap set to the highest divide.
- Autoload takes place.

The watchdog can be fed even though it is in the timer mode.

Note that the operational concept is for the watchdog mode of operation, when coming out of a hardware reset, the software should load the autoload registers, set the mode to watchdog, and then feed the watchdog (cause an autoload). The watchdog will now be starting at a known point.

If the watchdog is in the watchdog mode and running and happens to underflow at the time the external RESET is applied, the watchdog time-out flag will be cleared.

When the watchdog is in the watchdog mode and the watchdog underflows, the following action takes place (see Figure 16):

- Autoload takes place.
- Watchdog time-out flag is set
- Mode bit unchanged.
- Watchdog run bit unchanged.
- Autoload register unchanged.
- Prescaler tap unchanged.
- All other device action same as external reset.

Note that if the watchdog underflows, the program counter will start from 00H as in the case of an external reset. The watchdog time-out flag can be examined to determine if the watchdog has caused the reset condition. The watchdog time-out flag bit can be cleared by software.

When the watchdog is in the timer mode and the timer software underflows, the following action takes place:

- Autoload takes place.
- Watchdog time-out flag is set
- Mode bit unchanged.
- Watchdog run bit unchanged.
- Autoload register unchanged.
- Prescaler tap unchanged.

Mask ROM Device ($\overline{EA}$ = 1)

In the mask ROM device, the watchdog mode bit (WDMOD) is mask programmed and the bit in the watchdog command register is read only and reflects the mask programmed selection. If the mask programmed mode bit selects the timer mode, then the watchdog run bit (WDRUN) operates as described under EPROM Device. If the mask programmed bit selects the watchdog mode, then the watchdog run bit has no effect on the timer operation (see Figure 15).

Watchdog Function

The watchdog consists of a programmable prescaler and the main timer. The prescaler derives its clock from the on-chip oscillator. The prescaler consists of a divide by 12 followed by a 13 stage counter with taps from stage 6 through stage 13. This is shown in Figure 17. The tap selection is programmable. The watchdog main counter is a down counter clocked (decremented) each time the programmable prescaler underflows. The watchdog generates an underflow signal (and is autoloaded) when the watchdog is at count 0 and the clock to decrement the watchdog occurs. The watchdog is 8 bits long and the autoload value can range from 0 to FFH. (The

autoload value of 0 is permissible since the prescaler is cleared upon autoload).

This leads to the following user design equations. Definitions :t_{OSC} is the oscillator period, N is the selected prescaler tap value, W is the main counter autoload value, t_{MIN} is the minimum watchdog time-out value (when the autoload value is 0), t_{MAX} is the maximum time-out value (when the autoload value is FFH), t_D is the design time-out value.

$t_{MIN} = t_{OSC} \times 12 \times 64$

$t_{MAX} = t_{MIN} \times 128 \times 256$

$t_D = t_{MIN} \times 2^{PRESCALER} \times (W + 1)$
(where prescaler = 0, 1, 2, 3, 4, 5, 6, or 7)

Note that the design procedure is anticipated to be as follows. A t_{MAX} will be chosen either from equipment or operation considerations and will most likely be the next convenient value higher than t_D. (If the watchdog were inadvertently to start from FFH, an overflow would be guaranteed, barring other anomalies, to occur within t_{MAX}). Then the value for the prescaler would be chosen from:

prescaler = log2 (t_{MAX} / ($t_{OSC} \times 12 \times 256$)) - 6

This then also fixes t_{MIN}. An autoload value would then be chosen from:

$W = t_D / t_{MIN} - 1$

The software must be written so that a feed operation takes place every t_D seconds from the last feed operation. Some tradeoffs may need to be made. It is not advisable to include feed operations in minor loops or in subroutines unless the feed operation is a specific subroutine.

Watchdog Control Register (WDCON) (Bit Addressable) Address C0
The following bits of this register are read only in the ROM part when $\overline{EA}$ is high: WDMOD, PRE0, PRE1, and PRE2. That is, the register will reflect the mask programmed values. In the ROM part with $\overline{EA}$ high, these bits are taken from mask coded bits and are not readable by the program. WDRUN is read only in the ROM part when $\overline{EA}$ is high and WDMOD is in the watchdog mode. When WDMOD is in the timer mode, WDRUN functions normally.

The parameters written into WDMOD, PRE0, PRE1, and PRE2 by the program are not applied directly to the watchdog timer subsystem. The watchdog timer subsystem is directly controlled by a second register which stores these bits. The transfer of these bits from the user register (WDMOD) to the second control register takes place when the watchdog is fed. This prevents random code execution from directly foiling the watchdog function. This does not affect the operation where these bits are taken from mask coded values.

The reset values of the WDCON and WDL registers will be such that the timer resets to the watchdog mode with a timeout period of $12 \times 64 \times 128 \times t_{OSC}$. The watchdog timer will not generate an interrupt. Additional bits in WDCON are used to disable reset generation by the oscillator fail and low voltage detect circuits. WDCON can be written by software only by executing a valid watchdog feed sequence.

WDCON Register Bit Definitions

WDCON.7	PRE2	Prescaler Select 2, reset to 1
WDCON.6	PRE1	Prescaler Select 1, reset to 1
WDCON.5	PRE0	Prescaler Select 0, reset to 1
WDCON.4	LVRE	Low Voltage Reset Enable, reset to 1 (enabled)
WDCON.3	OFRE	Oscillator Fail Reset Enable, reset to 1 (enabled)
WDCON.2	WDRUN	Watchdog Run, reset to 1 (enabled)
WDCON.1	WDTOF	Watchdog Timeout Flag, reset to 0
WDCON.0	WDMOD	Watchdog Mode, reset to 1 (watchdog mode)

Enhanced UART

The UART operates in all of the usual modes that are described in the first section of this book for the 80C51. In addition the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The 87C575 UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 19). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 18.

Automatic Address Recognition
Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 20.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

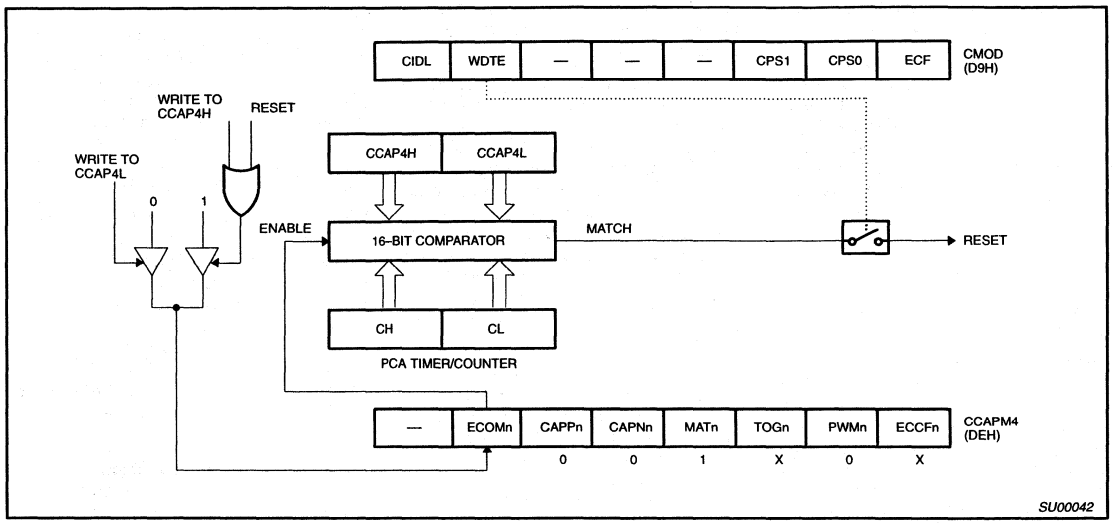


Figure 13. PCA Watchdog Timer

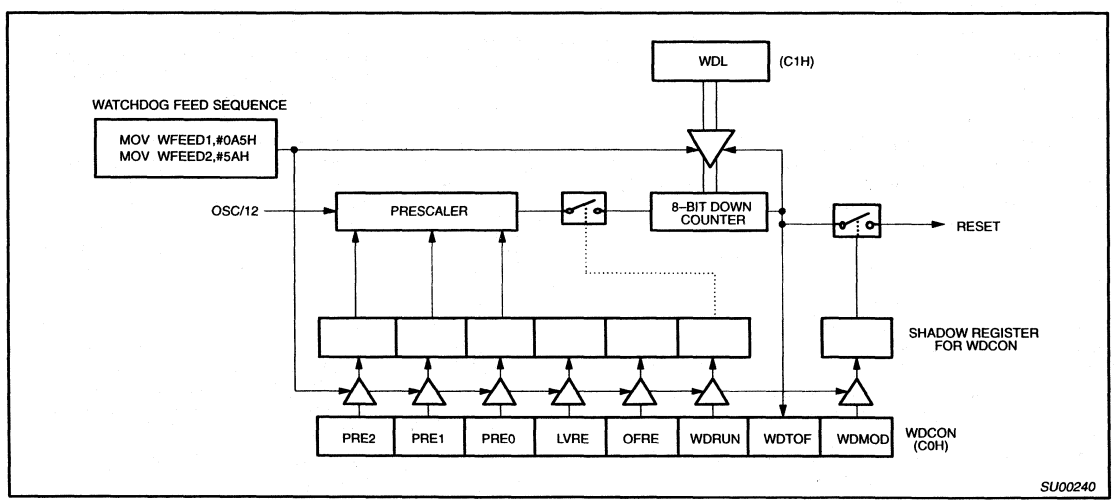


Figure 14. Watchdog Timer in 87C575 and 80C575 / 83C575 (EA = 0)

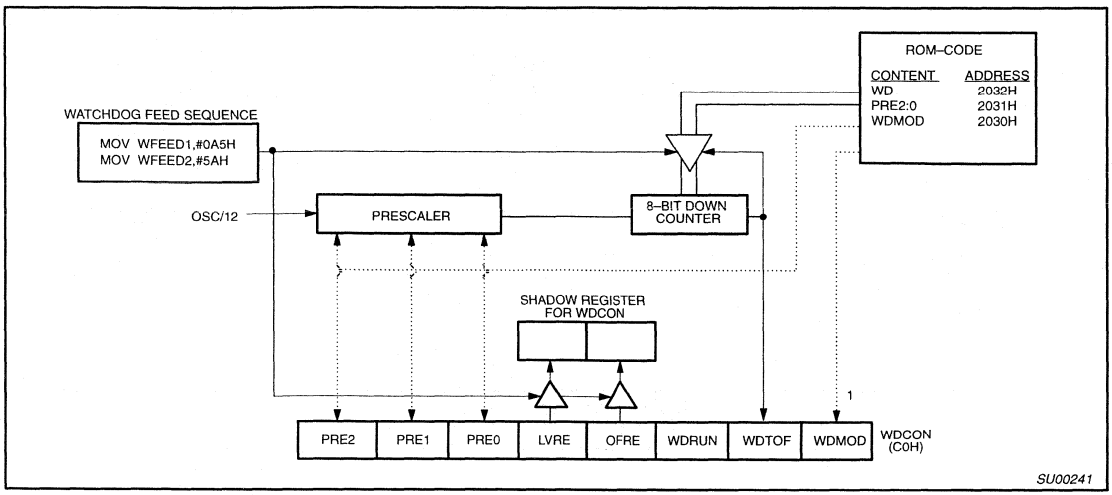


Figure 15. Watchdog Timer of 83C575 in Watchdog Mode (EA = 1, WDMOD = 1)

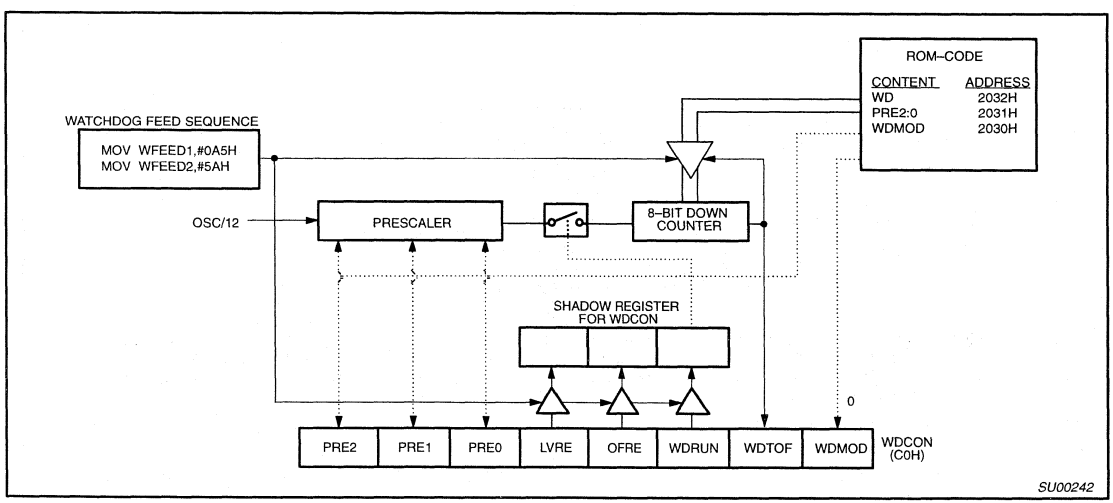


Figure 16. Watchdog Timer of 83C575 in Timer Mode (EA = 1, WDMOD = 0)

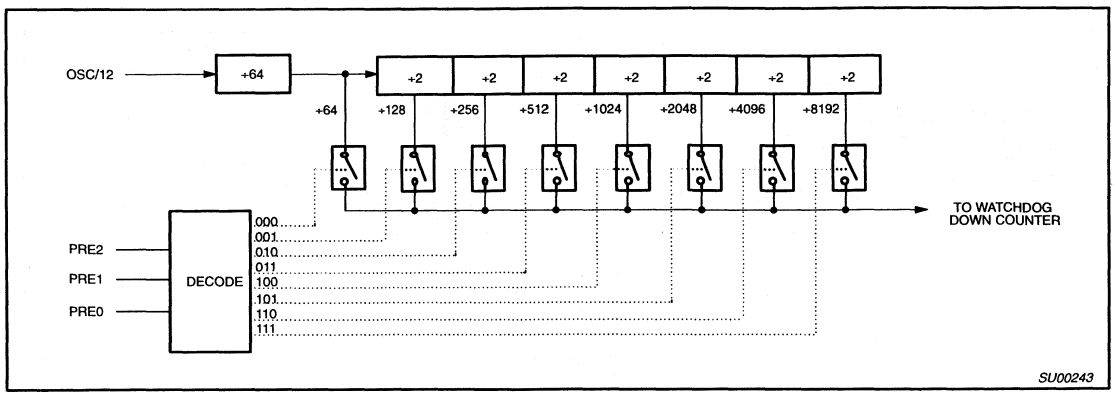


Figure 17. Watchdog Prescaler

SCON Address = 98H Reset Value = 0000 0000B

Bit Addressable

	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
Bit:	7	6	5	4	3	2	1	0

(SMOD0 = 0/1)*

Symbol	Function
FE	Framing Error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit.
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)
SM1	Serial Port Mode Bit 1

SM0	SM1	Mode	Description	Baud Rate**
0	0	0	shift register	Fosc/12
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	Fosc/64 or Fosc/32
1	1	3	9-bit UART	variable

SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
RB8	In modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

NOTE:
*SMOD0 is located at PCON6.
**Fosc = oscillator frequency

SU00043

Figure 18. SCON: Serial Port Control Register

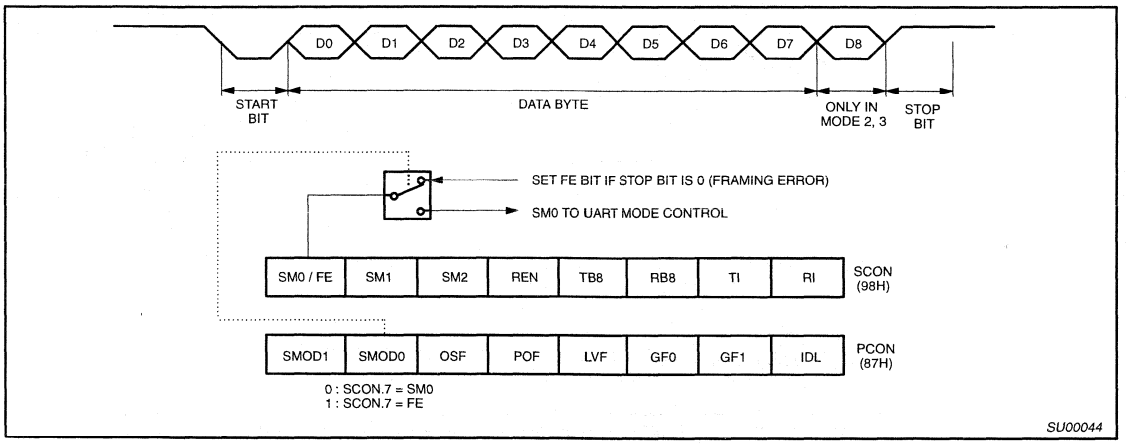


Figure 19. UART Framing Error Detection

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to b used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0	SADDR	=	1100 0000
	SADEN	=	1111 1101
	Given	=	1100 00X0
Slave 1	SADDR	=	1100 0000
	SADEN	=	1111 1110
	Given	=	1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0	SADDR	=	1100 0000
	SADEN	=	1111 1001
	Given	=	1100 0XX0
Slave 1	SADDR	=	1110 0000
	SADEN	=	1111 1010
	Given	=	1110 0X0X
Slave 2	SADDR	=	1110 0000
	SADEN	=	1111 1100
	Given	=	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary t make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are leaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". this effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

Analog Comparators

Four analog comparators are provided on chip. Three comparators have a common negative reference CMPR- and independent positive inputs CMP1+, CMP2+, CMP3+ on port 3. The fourth comparator has independent positive and negative inputs CMP0+ and CMP0- on port 1. The CMP register contains an output and enable bit for each comparator. The CMP register is bit addressable and is located at SFR address E8H. Figure 21 shows the connection of the comparators.

Pullups at the comparator input pins will be disabled by hardware when the comparator is enabled. In addition, to make inputs high impedance, the corresponding port SFR bits must be set by software to disable the pulldowns.

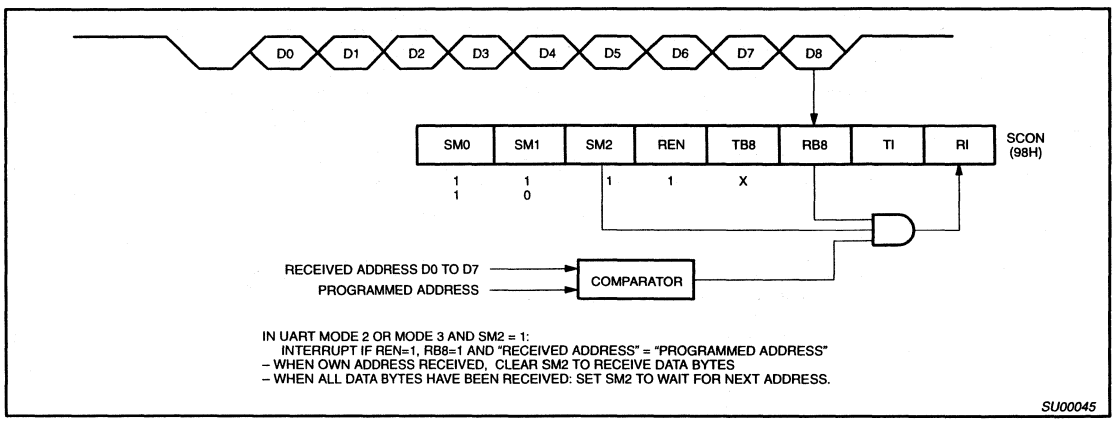


Figure 20. UART Multiprocessor Communication, Automatic Address Recognition

CMP Register Bit Definitions

CMP.7 enable comparator 3, disable pullups at P3.4, P3.7
CMP.6 enable comparator 2, disable pullups at P3.4, P3.6
CMP.5 enable comparator 1, disable pullups at P3.4, P3.5
CMP.4 enable comparator 0, disable pullups at P1.0, P1.1
CMP.3 comparator 3 output (read only)
CMP.2 comparator 2 output (read only)
CMP.1 comparator 1 output (read only)
CMP.0 comparator 0 output (read only)

All comparators are disabled automatically in power down mode, in idle mode unused comparators should be disabled by software to save power. A comparator can generate an interrupt that will terminate idle mode.

The CMPE register contains bits to enable each comparator to drive external output pins or internal PCA capture inputs. Pullups at the output pins are disabled by hardware when the external comparator output is enabled. The comparator output is wire-ORed with the corresponding port SFR bit, so the SFR bit must also be set by software to enable the output.

CMPE Register Bit Definitions

CMPE.7 enables comparator 3 to drive CEX3
CMPE.6 enables comparator 2 to drive CEX2
CMPE.5 enables comparator 1 to drive CEX1
CMPE.4 enables comparator 0 to drive CEX0
CMPE.3 enables comparator 3 output on P1.6 (open drain)
CMPE.2 enables comparator 2 output on P1.5 (open drain)
CMPE.1 enables comparator 1 output on P1.4 (open drain)
CMPE.0 enables comparator 0 output on P1.3 (open drain)

When 1s are written to CMPE bits 7-4, the comparator outputs will drive the corresponding capture input. (This function is not available in the idle or power-down mode.) When 1s are written to CMPE bits 3-0 the comparator output will also drive the corresponding port 1 pin. (This function **is** available in idle mode.) If the comparator's enabled to drive the capture input but not the port pin, then the port pin can be used for general purpose I/O. When a comparator output is enabled, pullups at the output pin are disabled and the output becomes open drain. The comparator output can be used to trigger a capture input in idle mode by programming the CMPE register to drive the pin from the comparator output to have the pin supply the capture trigger.

There are two special function registers associated with the comparators. They are CMP which contains the comparator enables and a bit that can be read by software to determine the state of each comparator's output, and CMPE which controls whether the output from each comparator drives the associated output pin or a capture input associated with one of the PCA modules.

The CMP registers bits 0–3 can be read by software to determine the state of the output of each comparator. To do this the associated comparator must be enabled but the output in port 1 can be disabled. This allows easy polling of the comparator output value without the need to use up a port pin.

The CMPE register allows the comparator to drive the associated PCA module capture input, so that on compare a capture can be generated in the PCA. Bits 0–3 of this register enable the comparator output to drive the associated port 1 output circuitry. Used as a comparator output this circuitry is open drain. To enable the comparator output to drive to port 1, the corresponding port bit must also be set to disable the pulldown. If the comparator is not enabled to drive the port 1 circuitry, the associated port 1 pin can be used for other I/O. This includes when a comparator is enabled to drive the capture input to a PCA module.

Reduced EMI Mode

There are two bits in the AUXR register that can be set to reduce the internal clock drive and disable the ALE output. AO (AUXR.0) when set turns off the ALE output. LO (AUXR.1) when set reduces the drive of the internal clock circuitry. Both bits are cleared on Reset. With LO set the 87C575 will still operate at 12MHz, but will have reduced EMI in the range above 100MHz.

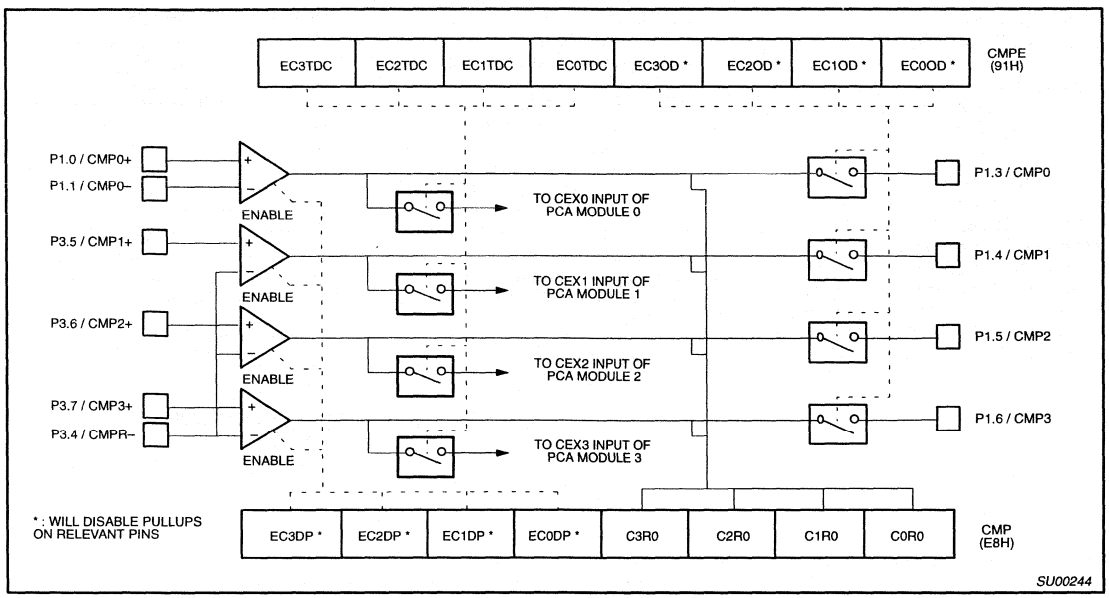


Figure 21. Analog Comparators

8XC575 Reduced EMI Mode

AUXR (0X8E)

–	–	–	–	–	–	LO	AO

AO: Turns off ALE output.

LO: Reduces drive of internal clock circuitry. 8XC575 spec'd to 12MHz when LO set.

INTERNAL RESET

Internal resets generated by the power on, low voltage, and oscillator fail detect circuits are self timed to guarantee proper initialization of the 8XC575. Reset will be held approximately 24 oscillator periods after normal conditions are detected by all enabled detect circuits. Internal resets do not drive $\overline{RST}$ but will cause missing pulses on ALE.

Interrupt Enable (IE) Register

EA	IE.7	enable all interrupts
EC	IE.6	enable PCA interrupt
ET2	IE.5	enable Timer 2 interrupt
ES	IE.4	enable Serial I/O interrupt
ET1	IE.3	enable Timer 1 interrupt
EX1	IE.2	enable External interrupt 1
ET0	IE.1	enable Timer 0 interrupt
EX0	IE.0	enable External interrupt 0

Interrupt Priority (IP) Register

	IP.7	reserved
PPC	IP.6	PCA interrupt priority
PT2	IP.5	Timer 2 interrupt priority
PS	IP.4	Serial I/O interrupt priority
PT1	IP.3	Timer 1 interrupt priority
PX1	IP.2	External interrupt 1 priority
PT0	IP.1	Timer 0 interrupt priority
PX0	IP.0	External interrupt 0 priority

Priority	Source	Flag	Vector
1	INT0	IE0	03H highest priority
2	Timer 0	TF0	0BH
3	INT1	IE1	13H
4	Timer 1	TF1	1BH
5	PCA	CF,CCFn	33H
6	Serial I/O	RI,TI	23H
7	Timer 2	TF2/EXF2	2BH lowest priority

Power Control (PCON) Register

SMOD1	PCON.7	double baud rate bit
SMOD0	PCON.6	SCON.7 access control
OSF	PCON.5	oscillator fail flag
POF	PCON.4	power off flag
LVF	PCON.3	low voltage flag
GF0	PCON.2	general purpose flag
PD	PCON.1	power down mode bit
IDL	PCON.0	idle mode bit

Auxiliary Register Bit Definitions (AUXR = 8EH)

AO	AUXR.0	ALE Off, when set turns off ALE
LO	AUXR.1	Low Speed, reduces internal clock drive

Port 2 Pullup Disable Register (P2OD = 0A1H)

Port 2 pullups can be disabled by writing ones to P2OD. Each bit in P2OD controls the corresponding bit in P2. P2OD resets to all zeros enabling Port 2 pullups. Writing one to a P2OD bit disables pullups at the corresponding port 2 bit making the output open drain.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the Logic Symbol, page 3.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

IDLE MODE

In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. The control bits for the reduced power modes are in the special function register PCON. Power-down mode can be terminated with either a hardware reset or external interrupt. With an external interrupt $\overline{INT0}$ or $\overline{INT1}$ must be enabled and configured as level sensitive. Holding the pin low restarts to oscillator and bringing the pin back high completes the exit.

If the watchdog is enabled (WDRUN = 1), then power-down mode is disabled.

DESIGN CONSIDERATIONS

At power-on, the voltage on V_{CC} must come up with $\overline{RST}$ low for a proper start-up.

Table 2 shows the state of I/O ports during low current operating modes.

Table 2. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

ROM CODE SUBMISSION

When submitting ROM code for the 83C575, the following must be specified:

1. 8k byte user ROM data
2. 32 byte ROM encryption key
3. ROM security bits
4. The watchdog timer parameters.

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 1FFFH	DATA	7:0	User ROM Data
2000H to 201FH	KEY	7:0	ROM Encryption Key FFH = no encryption
2020H	Reserved Security Bit 2 Security Bit 1	2 1 0	Must = 1 0 = enable, 1 = disable 0 = enable, 1 = disable
2030H	Reserved	7:0	Must = FFH
2031H	Reserved	7:0	Must = FFH
2032H	WDL [1]	7:0	Watchdog reload value (see specification)
2033H	WDCON [1]	7:5	PRE2:0
2033H	WDCON [1]	4	LVRE
2033H	WDCON [1]	3	OFRE
2033H	WDCON [1]	2	WDRUN=0, not ROM coded
2033H	WDCON [1]	1	WDTOF=0, not ROM coded
2033H	WDCON [1]	0	WDMOD

NOTES:

1. See Watchdog Timer Specification for definition of WDL and WDCON bits.

Security Bit 1: When programmed, this bit has two effects on masked ROM parts:

1. External MOVC is disabled, and
2. EA# is latched on Reset.

Security Bit 2: When programmed, this bit inhibits Verify User ROM.

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Operating temperature under bias	–55 to +125	°C
Storage temperature range	–65 to +150	°C
Voltage on $\overline{EA}/V_{PP}$ pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS}	–0.5 to +6.5	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C and –40°C to +125°C, V_{CC} = 5V ±20%, V_{SS} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
V_{IL}	Input low voltage (Ports 0, 2, 3, except 3.2, 3.3)		–0.5		$0.5V_{CC}$–0.6	V
V_{IL1}	Input low voltage (Ports 1, 3.2, 3.3)		–0.5		$0.65V_{CC}$–0.5	V
V_{IL2}	Input low voltage ($\overline{EA}$)		0		$0.2V_{CC}$–0.45	V
V_{IL3}	Input low voltage (XTAL1, RST)		–0.5		$0.2V_{CC}$–0.1	V
V_{IH}	Input high voltage (Ports 0, 2, 3, except 3.2, 3.3)		$0.5V_{CC}$+0.8		V_{CC}+0.5	V
V_{IH1}	Input high voltage (Ports 1, 3.2, 3.3)		$0.8V_{CC}$+0.3		V_{CC}+0.5	V
V_{IH2}	Input high voltage ($\overline{EA}$)		$0.2V_{CC}$+0.9		V_{CC}+0.5	V
V_{IH3}	Input high voltage (XTAL1, RST)		$0.7V_{CC}$		V_{CC}+0.5	V
HYS	Hysteresis (Ports 0, 2, 3, except 3.2, 3.3)		200			mV
HYS1	Hysteresis (Ports 1, 3.2, 3.3)		50			mV
V_{OL}	Output voltage low (Ports 1, 2, 3, except 3.1)	I_{OL} = 1.6mA			0.45	V
V_{OL1}	Output voltage low (Ports 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2mA			0.45	V
V_{OL2}	Output voltage low P3.1 with bit cleared P3.1 with bit set	 I_{OL} = 10.0mA I_{OL} = 1.6mA			 0.50 0.45	 V V
V_{OH}	Output voltage high (Ports 1, 2, 3, except P3.1)	I_{OH} = –30µA I_{OH} = –10µA	V_{CC}–0.7 V_{CC}–0.3			V V
V_{OH1}	Output voltage high (Port 0 in external bus mode, ALE, $\overline{PSEN}$)	I_{OH} = –3.2mA I_{OH} = –200µA	V_{CC}–0.7 V_{CC}–0.3			V V
V_{OH2}	Output voltage high P3.1 with bit cleared P3.1 with bit set	 I_{OH} = –10.0mA I_{OH} = –1.6mA	 V_{CC}–1.5 V_{CC}–1.5			 V V
V_{IO}	Offset voltage comparator inputs		–35		+35	mV
V_{CR}	Common mode range comparator inputs		0		V_{CC}	V
I_{IL}	Logical 0 input current (Ports 1, 2, 3, except 3.1)	V_{IN} = 0.45V			–75	µA
I_{TL}	Logical 1-to-0 transition current (Ports 2, 3, except 3.1, 3.2, 3.3) [4]	See Note 4			–600	µA
I_{TL1}	Logical 1-to-0 transition current (Ports 1, 3.2, 3.3)	See Note 4			–450	µA
I_{L1}	Input leakage current (Port 0, Port2 in open drain mode)[9]	0.45 < V_{IN} < V_{CC}	2		40	µA
I_{L2}	Input leakage current ($\overline{EA}$, P3.1)	0.45 < V_{IN} < V_{CC}	–10		+10	µA
I_{LC}	Input leakage current comparator inputs	0 < V_{IN} < V_{CC}	–1.0		+1.0	µA
I_{CC}	Power supply current:[7] Active mode @ 16MHz[5] Idle mode @ 16MHz Power-down mode	See note 6		 20 8 5	 30 12 75	 mA mA µA
R_{RST}	Internal reset pull-up resistor	V_{IN} = 0V	50		200	kΩ
V_{LOW}	Low V_{CC} detect voltage		4.0		4.45	V
C_{IO}	Pin capacitance[10]	f = 1MHz			10	pF

NOTES: (SEE NEXT PAGE)

NOTES TO THE DC ELECTRICAL CHARACTERISTICS TABLE:

1. Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
2. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
3. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
4. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is between V_{IH} and V_{IL}.
5. I_{CC}MAX at other frequencies can be determined from Figure 29.
6. See Figures 30 through 33 for I_{CC} test conditions.
7. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
8. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum total I_{OL} for all outputs: 71mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
9. Specification applies to Port 2 when P2OD bit is set.
10. 15pF MAX for the $\overline{EA}/V_{PP}$ and P0.0 pins.

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C and –40°C to +125°C, V_{CC} = 5V ±20%, V_{SS} = 0V[1, 2]

SYMBOL	FIGURE	PARAMETER	VARIABLE CLOCK		UNIT
			MIN	MAX	
$1/t_{CLCL}$	22	Oscillator frequency: **Speed Versions** 8XC575 E	6	16	MHz
OSCF		Oscillator fail detect frequency	0.6	5.5	MHz
TR		Comparator response time		10	µs
t_{LHLL}	22	ALE pulse width	$2t_{CLCL}$–40		ns
t_{AVLL}	22	Address valid to ALE low	t_{CLCL}–25		ns
t_{LLAX}	22	Address hold after ALE low	t_{CLCL}–25		ns
t_{LLIV}	22	ALE low to valid instruction in		$4t_{CLCL}$–75	ns
t_{LLPL}	22	ALE low to $\overline{PSEN}$ low	t_{CLCL}–25		ns
t_{PLPH}	22	$\overline{PSEN}$ pulse width	$3t_{CLCL}$–45		ns
t_{PLIV}	22	$\overline{PSEN}$ low to valid instruction in		$3t_{CLCL}$–70	ns
t_{PXIX}	22	Input instruction hold after $\overline{PSEN}$	0		ns
t_{PXIZ}	22	Input instruction float after $\overline{PSEN}$		t_{CLCL}–25	ns
t_{AVIV}	22	Address to valid instruction in		$5t_{CLCL}$–85	ns
t_{PLAZ}	22	$\overline{PSEN}$ low to address float		10	ns
Data Memory					
t_{RLRH}	23, 24	$\overline{RD}$ pulse width	$6t_{CLCL}$–100		ns
t_{WLWH}	23, 24	$\overline{WR}$ pulse width	$6t_{CLCL}$–100		ns
t_{RLDV}	23, 24	$\overline{RD}$ low to valid data in		$5t_{CLCL}$–110	ns
t_{RHDX}	23, 24	Data hold after $\overline{RD}$	0		ns
t_{RHDZ}	23, 24	Data float after $\overline{RD}$		$2t_{CLCL}$–28	ns
t_{LLDV}	23, 24	ALE low to valid data in		$8t_{CLCL}$–150	ns
t_{AVDV}	23, 24	Address to valid data in		$9t_{CLCL}$–165	ns
t_{LLWL}	23, 24	ALE low to $\overline{RD}$ or $\overline{WR}$ low	$3t_{CLCL}$–50	$3t_{CLCL}$+50	ns
t_{AVWL}	23, 24	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	$4t_{CLCL}$–75		ns
t_{QVWX}	23, 24	Data valid to $\overline{WR}$ transition	t_{CLCL}–30		ns
t_{WHQX}	23, 24	Data hold after $\overline{WR}$	t_{CLCL}–25		ns
t_{RLAZ}	23, 24	$\overline{RD}$ low to address float		0	ns
t_{WHLH}	23, 24	$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{CLCL}–25	t_{CLCL}+25	ns
External Clock					
t_{CHCX}	26	High time	12		ns
t_{CLCX}	26	Low time	12		ns
t_{CLCH}	26	Rise time		20	ns
t_{CHCL}	26	Fall time		20	ns
Shift Register					
t_{XLXL}	25	Serial port clock cycle time	$12t_{CLCL}$		ns
t_{QVXH}	25	Output data setup to clock rising edge	$10t_{CLCL}$–133		ns
t_{XHQX}	25	Output data hold after clock rising edge	$2t_{CLCL}$–60		ns
t_{XHDX}	25	Input data hold after clock rising edge	0		ns
t_{XHDV}	25	Clock rising edge to input data valid		$10t_{CLCL}$–133	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. Interfacing the 80C32/52 to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE
P – $\overline{PSEN}$
Q – Output data
R – $\overline{RD}$ signal
t – Time
V – Valid
W – $\overline{WR}$ signal
X – No longer a valid logic level
Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
t_{LLPL} = Time for ALE low to $\overline{PSEN}$ low.

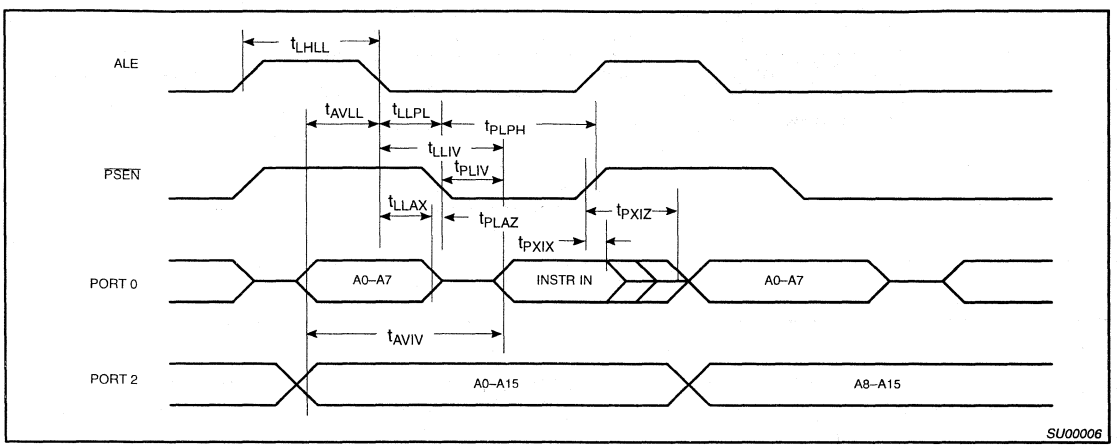


Figure 22. External Program Memory Read Cycle

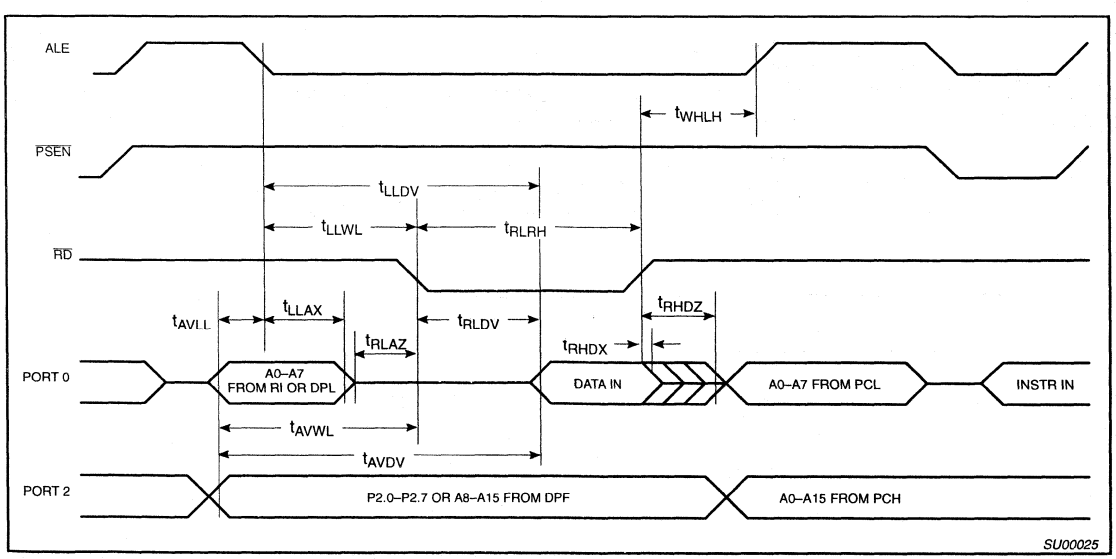


Figure 23. External Data Memory Read Cycle

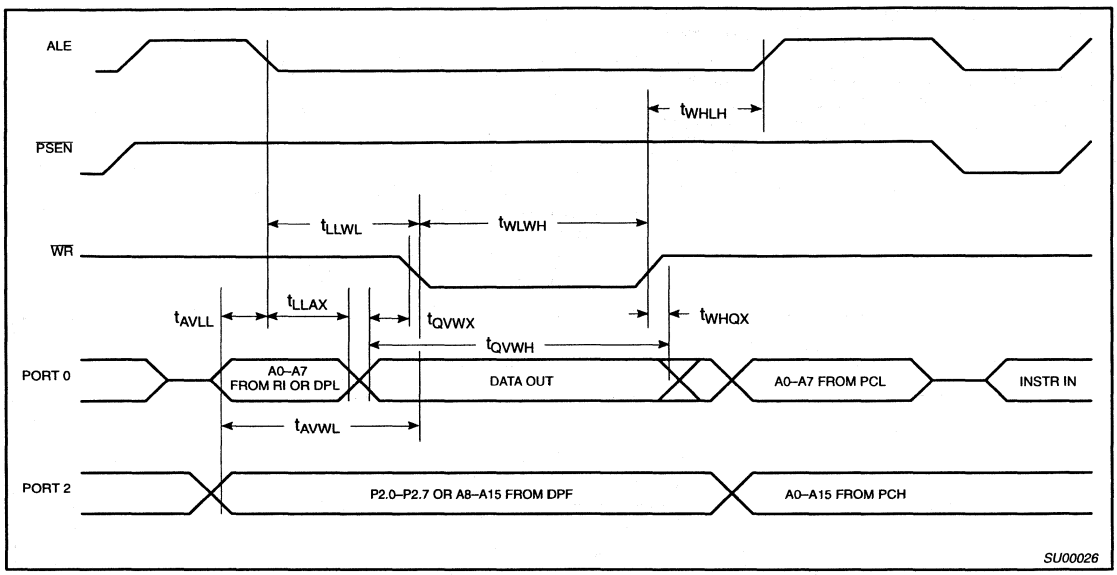


Figure 24. External Data Memory Write Cycle

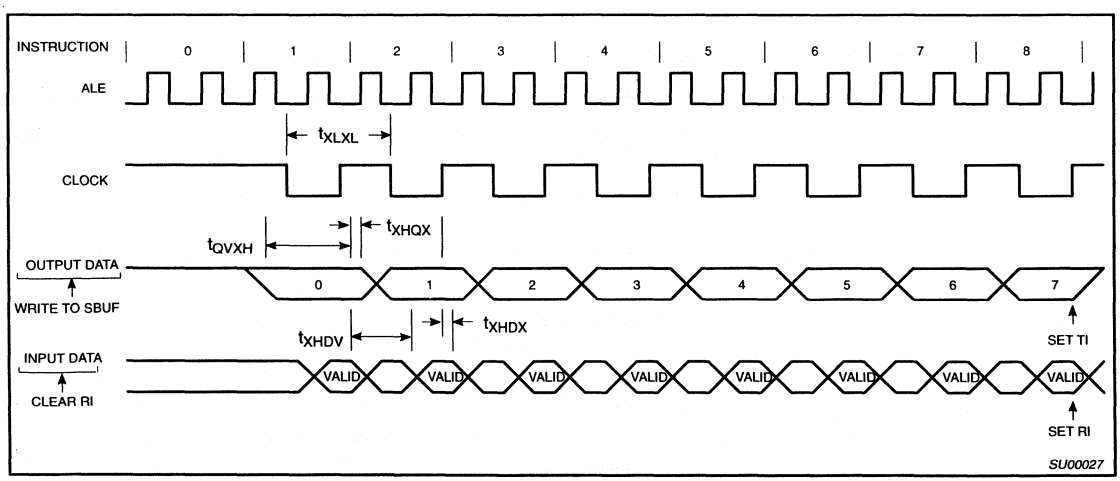


Figure 25. Shift Register Mode Timing

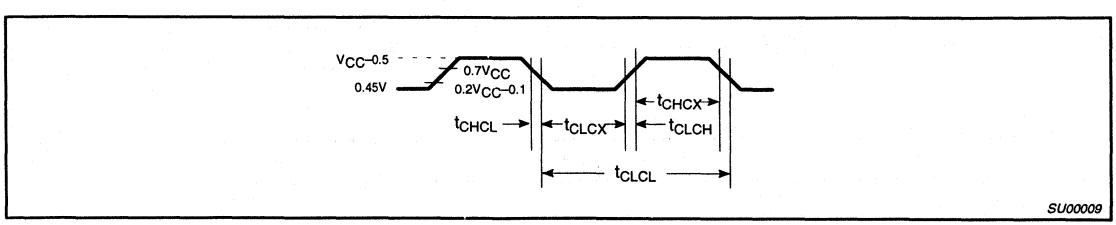
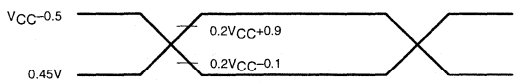


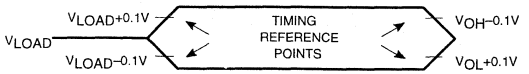
Figure 26. External Clock Drive



NOTE:
AC inputs during testing are driven at V_{CC} –0.5 for a logic '1' and 0.45V for a logic '0'.
Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

SU00010

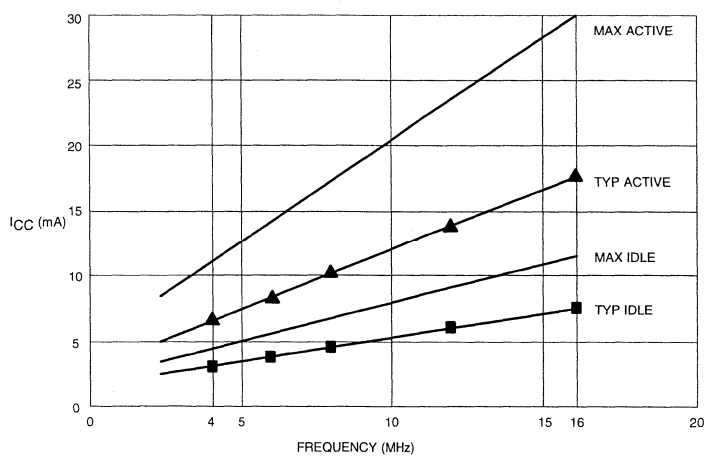
Figure 27. AC Testing Input/Output



NOTE:
For timing purposes, a port is no longer floating when a 100mV change from load voltage occurs, and begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OH}/I_{OL} \geq \pm 20$mA.

SU00011

Figure 28. Float Waveform



SU00245

Figure 29. I_{CC} vs. FREQ
Valid only within frequency specifications of the device under test

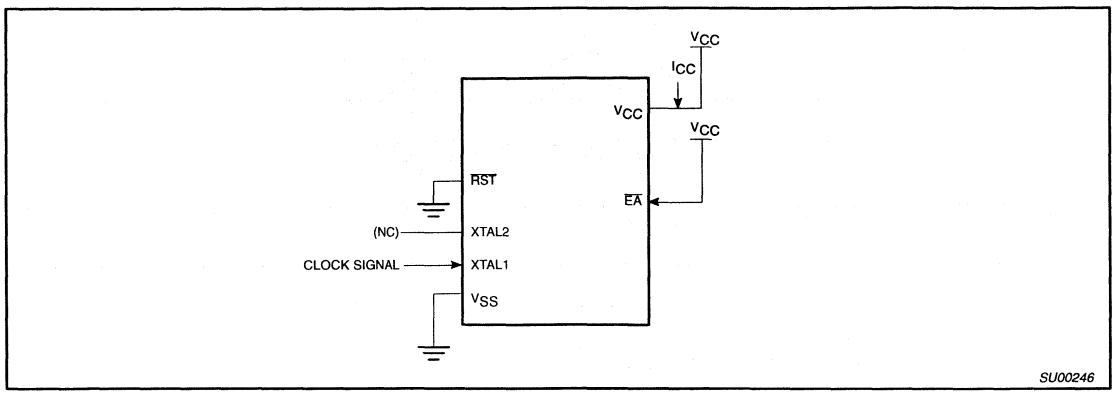


Figure 30. I_{CC} Test Condition, Active Mode
All other pins are disconnected

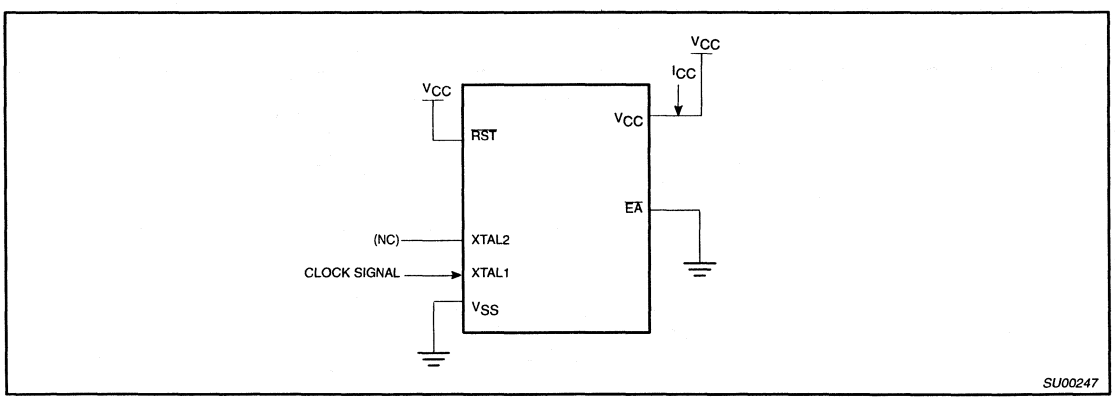


Figure 31. I_{CC} Test Condition, Idle Mode
All other pins are disconnected

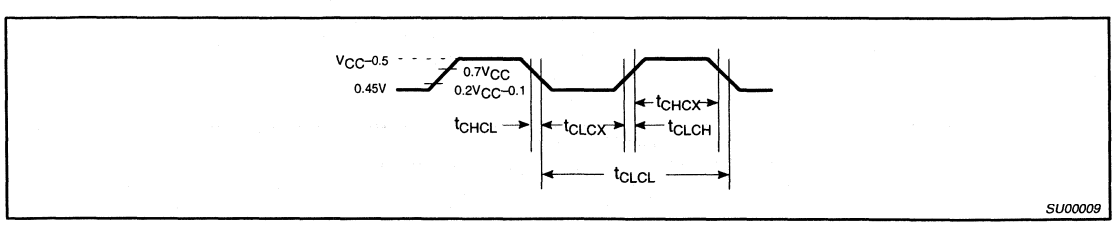


Figure 32. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
$t_{CLCH} = t_{CHCL} = 5ns$

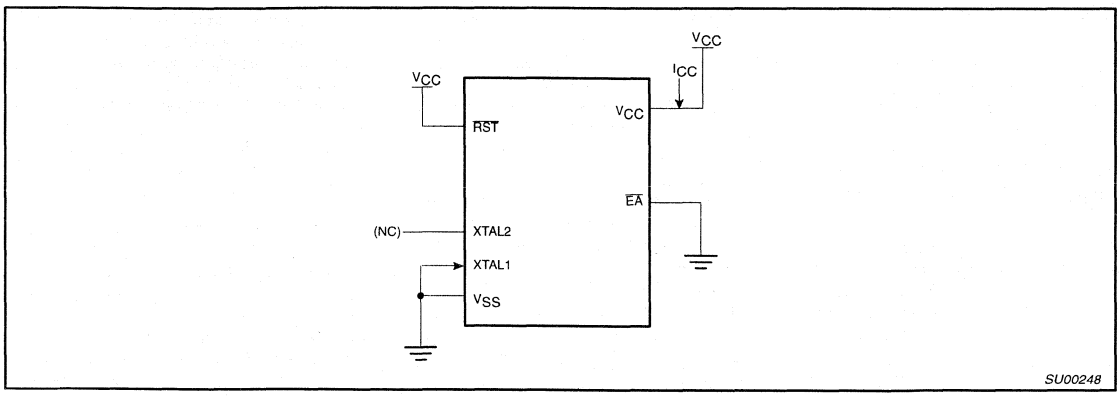


Figure 33. I_{CC} Test Condition, Power Down Mode
All other pins are disconnected. V_{CC} = 2V to 5.5V

EPROM CHARACTERISTICS

To put the 87C575 in the EPROM programming mode, PSEN must be held high during power up, then driven low with reset active. The 87C575 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses.

The 87C575 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C575 manufactured by Philips.

Table 3 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 34 and 35. Figure 36 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 34. Note that the 87C575 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 34. The code byte to be programmed into that location is applied to port 0. RST, $\overline{PSEN}$ and pins of ports 2 and 3 specified in Table 3 are held at the 'Program Code Data' levels indicated in Table 3. The ALE/$\overline{PROG}$ is pulsed low 25 times as shown in Figure 35.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the 25 pulse programming sequence using the 'Pgm Security Bit' levels. After one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bit can still be programmed.

Note that the $\overline{EA}$/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If security bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 36. The other pins are held at the 'Verify Code Data' levels indicated in Table 3. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips

(B0H) = 97H indicates 87C575

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345–5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-s/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000µW/cm^2 rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Table 3. EPROM Programming Modes

MODE	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.7	P2.6	P3.7	P3.6
Read signature	0	0	1	1	0	0	0	0
Program code data	0	0	0*	V_{PP}	1	0	1	1
Verify code data	0	0	1	1	0	0	1	1
Pgm encryption table	0	0	0*	V_{PP}	1	0	1	0
Pgm security bit 1	0	0	0*	V_{PP}	1	1	1	1
Pgm security bit 2	0	0	0*	V_{PP}	1	1	0	0

NOTES:

1. '0' = Valid low for that pin, '1' = valid high for that pin.
2. V_{PP} = 12.75V ±0.25V.
3. V_{CC} = 5V±10% during programming and verification.

* ALE/$\overline{PROG}$ receives 25 programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 100µs (±10µs) and high for a minimum of 10µs.

™Trademark phrase of Intel Corporation.

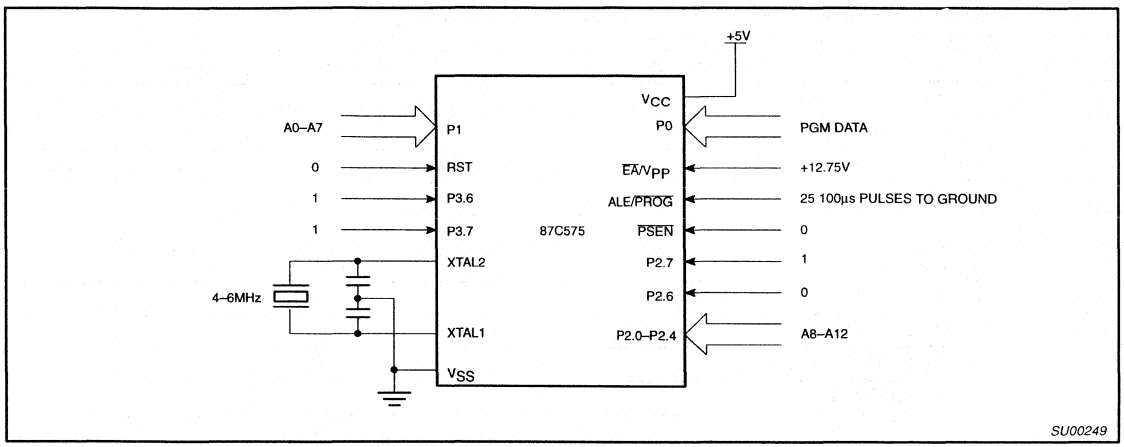


Figure 34. Programming Configuration

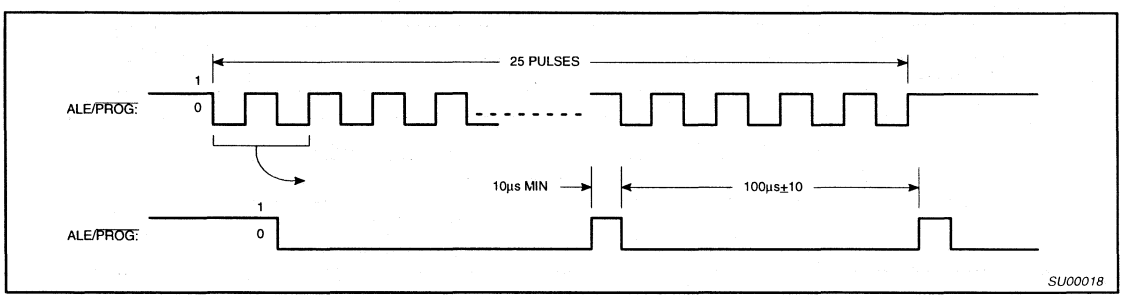


Figure 35. PROG Waveform

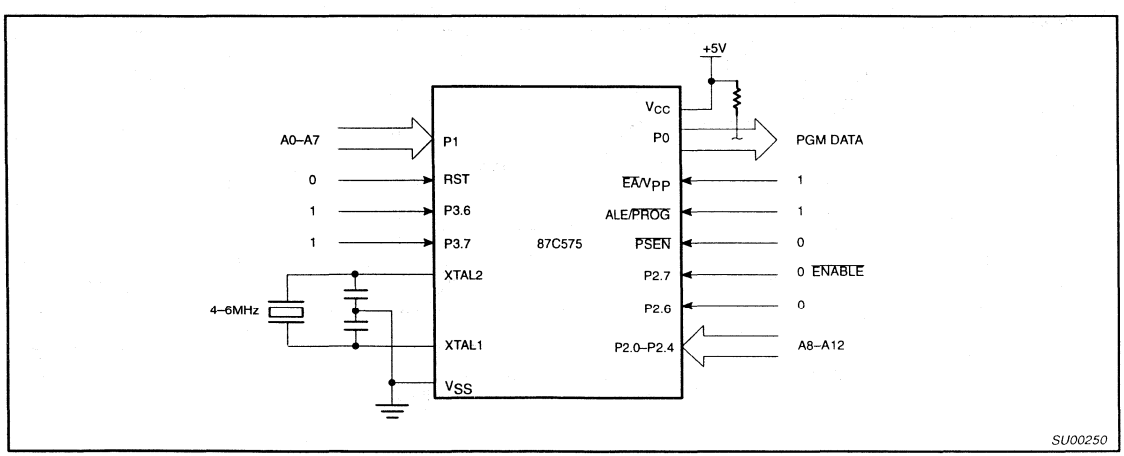
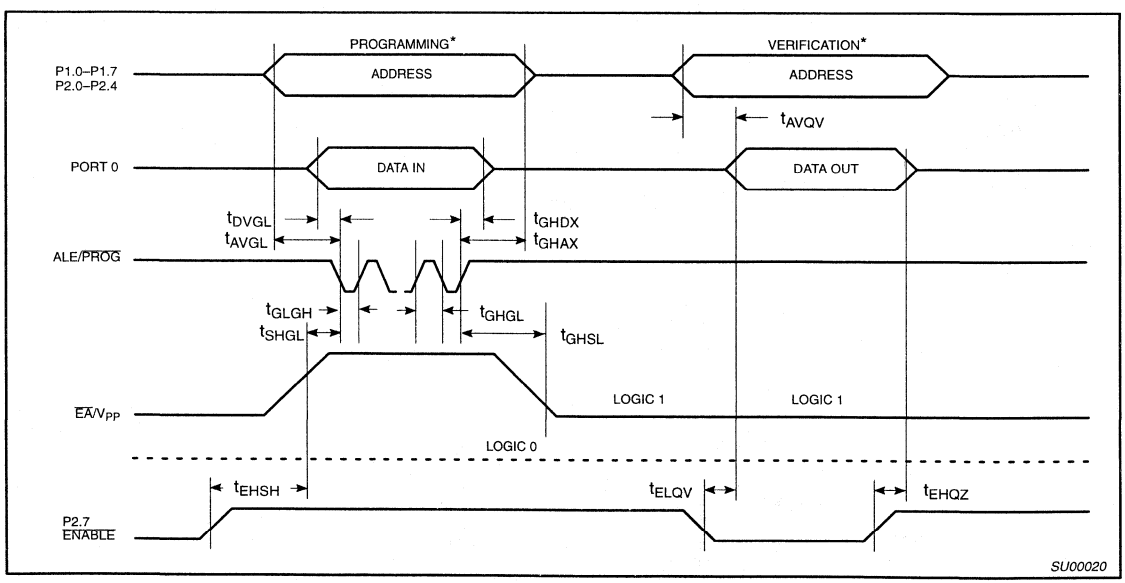


Figure 36. Program Verification

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_{amb} = 21°C to +27°C, V_{CC} = 5V±10%, V_{SS} = 0V (See Figure 37)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHAX}	Address hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHDX}	Data hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to $\overline{PROG}$ low	10		µs
t_{GHSL}	V_{PP} hold after $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ width	90	110	µs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELQZ}	$\overline{ENABLE}$ low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHGL}	$\overline{PROG}$ high to $\overline{PROG}$ low	10		µs



* FOR PROGRAMMING VERIFICATION SEE FIGURE 34.
FOR VERIFICATION CONDITIONS SEE FIGURE 36.

Figure 37. EPROM Programming and Verification

CMOS single-chip 8-bit microcontroller 83C751/87C751

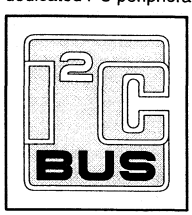
DESCRIPTION

The Philips 83C751/87C751 offers the advantages of the 80C51 architecture in a small package and at low cost.

The 8XC751 Microcontroller is fabricated with Philips high-density CMOS technology. Philips epitaxial substrate minimizes CMOS latch-up sensitivity.

The 8XC751 contains a 2k × 8 ROM (83C751) EPROM (87C751), a 64 × 8 RAM, 19 I/O lines, a 16-bit auto-reload counter/timer, a five-source, fixed-priority level interrupt structure, a bidirectional inter-integrated circuit (I^2C) serial bus interface, and an on-chip oscillator.

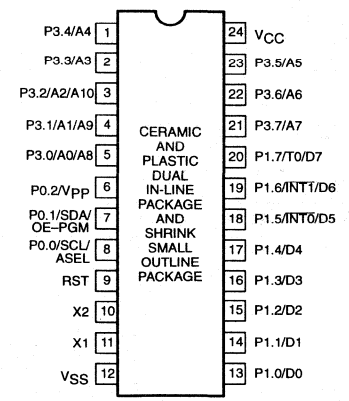
The on-board inter-integrated circuit (I^2C) bus interface allows the 8XC751 to operate as a master or slave device on the I^2C small area network. This capability facilitates I/O and RAM expansion, access to EEPROM, processor-to-processor communication, and efficient interface to a wide variety of dedicated I^2C peripherals.

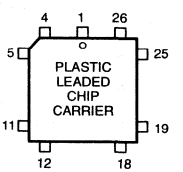


FEATURES

- 80C51 based architecture
- Inter-Integrated Circuit (I^2C) serial bus interface
- Small package sizes
  - 24-pin DIP (300 mil "skinny DIP")
  - 24-pin Shrink Small Outline Package
  - 28-pin PLCC
- 87C751 available in erasable quartz lid or one-time programmable plastic packages
- Wide oscillator frequency range
- Low power consumption:
  - Normal operation: less than 11mA @ 5V, 12MHz
  - Idle mode
  - Power-down mode
- 2k × 8 ROM (83C751)
  2k × 8 EPROM (87C751)
- 64 × 8 RAM
- 16-bit auto reloadable counter/timer
- Fixed-rate timer
- Boolean processor
- CMOS and TTL compatible
- Well suited for logic replacement, consumer and industrial applications
- LED drive outputs

PIN CONFIGURATIONS





Pin	Function	Pin	Function
1	P3.4/A4	15	P1.0/D0
2	P3.3/A3	16	P1.1/D1
3	P3.2/A2/A10	17	P1.2/D2
4	P3.1/A1/A9	18	P1.3/D3
5	N.C.	19	P1.4/D4
6	P3.0/A0/A8	20	P1.5/INT0/D5
7	P0.2/VPP	21	N.C.
8	P0.1/SDA/OE-PGM	22	N.C.
9	P0.0//SCLASEL	23	P1.6/INT1/D6
10	N.C.	24	P1.7/T0/D7
11	RST	25	P3.7/A7
12	X2	26	P3.6/A6
13	X1	27	P3.5/A5
14	VSS	28	VCC

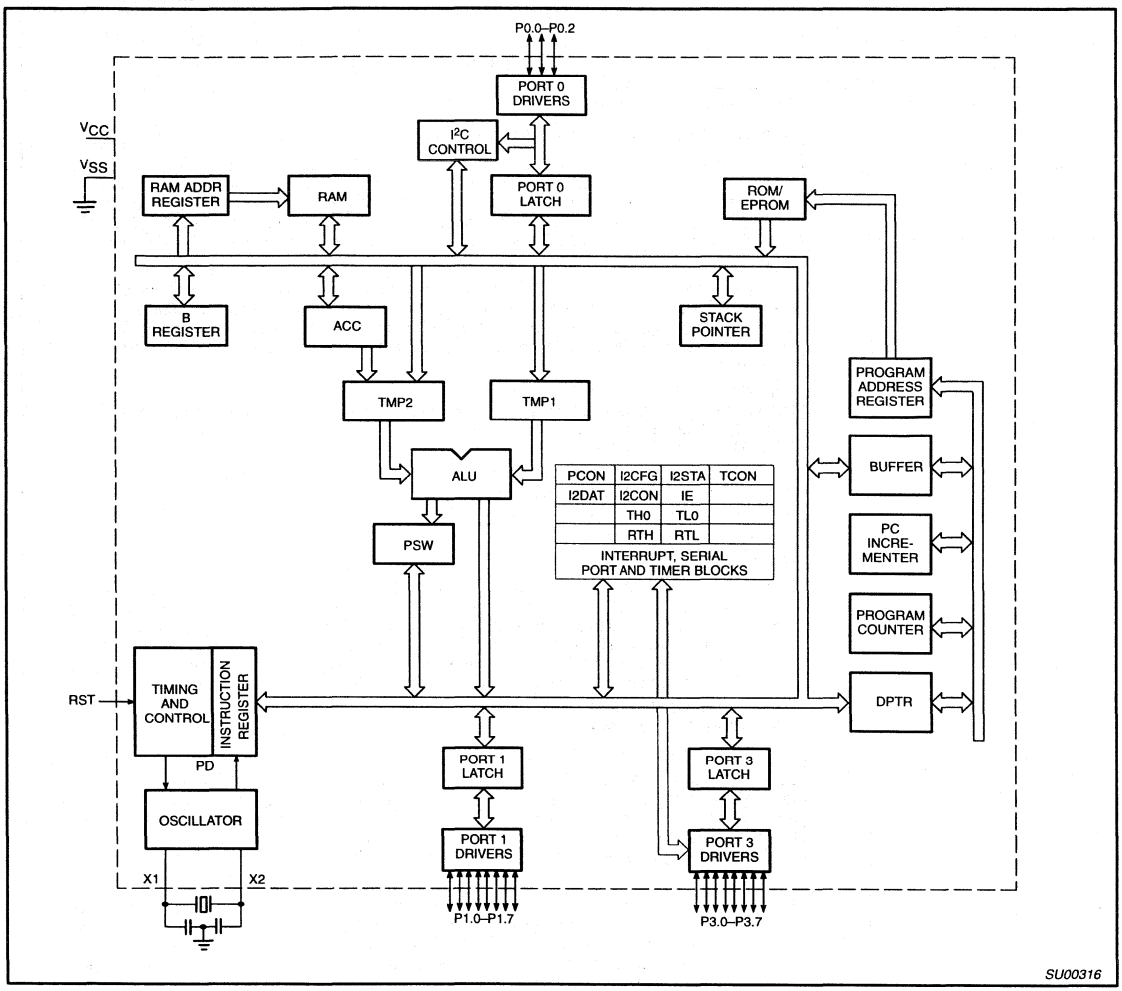
SU00315

ORDERING INFORMATION

ROM	EPROM[1]		TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY	DRAWING NUMBER
	S87C751–1F24	UV	0 to +70, Ceramic Dual In-line Package	3.5 to 12MHz	0586B
	S87C751–2F24	UV	–40 to +85, Ceramic Dual In-line Package	3.5 to 12MHz	0586B
	S87C751–4F24	UV	0 to +70, Ceramic Dual In-line Package	3.5 to 16MHz	0586B
	S87C751–5F24	UV	–40 to +85, Ceramic Dual In-line Package	3.5 to 16MHz	0586B
S83C751–1N24	S87C751–1N24	OTP	0 to +70, Plastic Dual In-line Package	3.5 to 12MHz	SOT222-1
S83C751–2N24	S87C751–2N24	OTP	–40 to +85, Plastic Dual In-line Package	3.5 to 12MHz	SOT222-1
S83C751–4N24	S87C751–4N24	OTP	0 to +70, Plastic Dual In-line Package	3.5 to 16MHz	SOT222-1
S83C751–5N24	S87C751–5N24	OTP	–40 to +85, Plastic Dual In-line Package	3.5 to 16MHz	SOT222-1
S83C751–1A28	S87C751–1A28	OTP	0 to +70, Plastic Leaded Chip Carrier	3.5 to 12MHz	SOT261-3
S83C751–2A28	S87C751–2A28	OTP	–40 to +85, Plastic Leaded Chip Carrier	3.5 to 12MHz	SOT261-3
S83C751–4A28	S87C751–4A28	OTP	0 to +70, Plastic Leaded Chip Carrier	3.5 to 16MHz	SOT261-3
S83C751–5A28	S87C751–5A28	OTP	–40 to +85, Plastic Leaded Chip Carrier	3.5 to 16MHz	SOT261-3
S83C751–1D24	S87C751–1D24	OTP	0 to +70, Shrink Small Outline Package	3.5 to 12MHz	SOT340-1
S83C751-2 DB	S87C751-2 DB	OTP	–40 to +85, Shrink Small Outline Package	3.5 to 12MHz	SOT340-1
S83C751–4D24	S87C751–4D24	OTP	0 to +70, Shrink Small Outline Package	3.5 to 16MHz	SOT340-1
S83C751-5 DB	S87C751-5 DB	OTP	–40 to +85, Shrink Small Outline Package	3.5 to 16MHz	SOT340-1

NOTE:
1. OTP = One Time Programmable EPROM. UV = UV Erasable EPROM.

BLOCK DIAGRAM



PIN DESCRIPTIONS

MNEMONIC	PIN NO. DIP/ SSOP	PIN NO. LCC	TYPE	NAME AND FUNCTION
V_{SS}	12	14	I	**Circuit Ground Potential**
V_{CC}	24	28	I	**Supply voltage during normal, idle, and power-down operation.**
P0.0–P0.2	8–6	9–7	I/O	**Port 0:** Port 0 is a 3-bit open-drain, bidirectional port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 also serves as the serial I^2C interface. When this feature is activated by software, SCL and SDA are driven low in accordance with the I^2C protocol. These pins are driven low if the port register bit is written with a 0 or if the I^2C subsystem presents a 0. The state of the pin can always be read from the port register by the program. To comply with the I^2C specification, P0.0 and P0.1 are open drain bidirectional I/O pins with the electrical characteristics listed in the tables that follow. While these differ from "standard TTL" characteristics, they are close enough for the pins to still be used as general-purpose I/O in non-I^2C applications. Port 0 also provides alternate functions for programming the EPROM memory as follows:
	6	7	N/A	**V_{PP} (P0.2)** – Programming voltage input.
	7	8	I	**OE/PGM (P0.1)** – Input which specifies verify mode (output enable) or the program mode. OE/PGM = 1 output enabled (verify mode). OE/PGM = 0 program mode.
	8	9	I	**ASEL (P0.0)** – Input which indicates which bits of the EPROM address are applied to port 3. ASEL = 0 low address byte available on port 3. ASEL = 1 high address byte available on port 3 (only the three least significant bits are used).
	7	8	I/O	**SDA (P0.1)** – I^2C data.
	8	9	I/O	**SCL (P0.0)** – I^2C clock.
P1.0–P1.7	13–20	15–20, 23, 24	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 serves to output the addressed EPROM contents in the verify mode and accepts as inputs the value to program into the selected address during the program mode. Port 1 also serves the special function features of the 80C51 family as listed below:
	18	20	I	**$\overline{INT0}$ (P1.5):** External interrupt.
	19	23	I	**$\overline{INT1}$ (P1.6):** External interrupt.
	20	24	I	**T0 (P1.7):** Timer 0 external input.
P3.0–P3.7	5–1, 23–21	6, 4–1, 27–25	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also functions as the address input for the EPROM memory location to be programmed (or verified). The 11-bit address is multiplexed into this port as specified by P0.0/ASEL.
RST	9	11	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on RESET using only an external capacitor to V_{CC}. After the device is reset, a 10-bit serial sequence, sent LSB first, applied to RESET, places the device in the programming state allowing programming address, data and V_{PP} to be applied for programming or verification purposes. The RESET serial sequence must be synchronized with the X1 input.
X1	11	13	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. X1 also serves as the clock to strobe in a serial bit stream into RESET to place the device in the programming state.
X2	10	12	O	**Crystal 2:** Output from the inverting oscillator amplifier.

ABSOLUTE MAXIMUM RATINGS[1, 2]

PARAMETER	RATING	UNIT
Storage temperature range	–65 to +150	°C
Voltage from V_{CC} to V_{SS}	–0.5 to +6.5	V
Voltage from any pin to V_{SS} (except V_{PP})	–0.5 to V_{CC} + 0.5	V
Power dissipation	1.0	W
Voltage on V_{PP} pin to V_{SS}	0 to +13.0	V
Maximum I_{OL} per I/O pin	10	mA

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±10% for 87C751, V_{CC} = 5V ±10% for 83C751, V_{SS} = 0V[1]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{IL}	Input low voltage, except SDA, SCL		–0.5	$0.2V_{DD}$–0.1	V
V_{IH}	Input high voltage, except X1, RST		$0.2V_{CC}$+0.9	V_{CC}+0.5	V
V_{IH1}	Input high voltage, X1, RST		$0.7V_{CC}$	V_{CC}+0.5	V
	SDA, SCL, P0.2				
V_{IL1}	Input low voltage		–0.5	$0.3V_{CC}$	V
V_{IH2}	Input high voltage		$0.7V_{CC}$	V_{CC}+0.5	V
V_{OL}	Output low voltage, ports 1 and 3	I_{OL} = 1.6mA[2]		0.45	V
V_{OL1}	Output low voltage, port 0.2	I_{OL} = 3.2mA[2]		0.45	V
V_{OH}	Output high voltage, ports 1 and 3	I_{OH} = –60µA	2.4		V
		I_{OH} = –25µA	$0.75V_{CC}$		V
		I_{OH} = –10µA	$0.9V_{CC}$		V
	Port 0.0 and 0.1 (I^2C) – Drivers				
V_{OL2}	Output low voltage	I_{OL} = 3mA		0.4	V
	Driver, receiver combined:	(over V_{CC} range)			
C	Capacitance			10	pF
I_{IL}	Logical 0 input current, ports 1 and 3	V_{IN} = 0.45V		–50	µA
I_{TL}	Logical 1 to 0 transition current, ports 1 and 3[3]	V_{IN} = 2V (0 to 70°C)		–650	µA
		V_{IN} = 2V (–40 to +85°C)		–750	µA
I_{LI}	Input leakage current, port 0	0.45 < V_{IN} < V_{CC}		±10	µA
R_{RST}	Internal pull-down resistor		25	175	kΩ
C_{IO}	Pin capacitance	Test freq = 1MHz, T_{amb} = 25°C		10	pF
I_{PD}	Power-down current[4]	V_{CC} = 2 to V_{CC} max		50	µA
V_{PP}	V_{PP} program voltage (for 87C751 only)	V_{SS} = 0V V_{CC} = 5V±10% T_{amb} = 21°C to 27°C	12.5	13.0	V
I_{PP}	Program current (for 87C751 only)	V_{PP} = 13.0V		50	mA
I_{CC}	Supply current (see Figure 2)				

NOTES TO DC ELECTRICAL CHARACTERISTICS ON NEXT PAGE

NOTES TO DC ELECTRICAL CHARACTERISTICS:

1. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
2. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10mA (NOTE: This is 85°C spec.)
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum total I_{OL} for all outputs: 67mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
3. Pins of ports 1 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
4. Power-down I_{CC} is measured with all output pins disconnected; port 0 = V_{CC}; X2, X1 n.c.; RST = V_{SS}.
5. Active I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = 5ns, V_{IL} = V_{SS} + 0.5V, V_{IH} = V_{CC} – 0.5V; X2 n.c.; RST = port 0 = V_{CC}. I_{CC} will be slightly higher if a crystal oscillator is used.
6. Idle I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = 5ns, V_{IL} = V_{SS} + 0.5V, V_{IH} = V_{CC} – 0.5V; X2 n.c.; port 0 = V_{CC}; RST = V_{SS}.

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±10% for 87C751, V_{CC} = 5V ±10% for 83C751, V_{SS} = 0V[1, 2]

SYMBOL	PARAMETER	12MHz CLOCK		VARIABLE CLOCK		UNIT
		MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	Oscillator frequency:			3.5 3.5	12 16	MHz MHz
External Clock (Figure 1)						
t_{CHCX}	High time	20		20		ns
t_{CLCX}	Low time	20		20		ns
t_{CLCH}	Rise time		20		20	ns
t_{CHCL}	Fall time		20		20	ns

NOTES:

1. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
2. Load capacitance for ports = 80pF.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

C – Clock
D – Input data
H – Logic level high
L – Logic level low
Q – Output data
T – Time
V – Valid
X – No longer a valid logic level
Z – Float

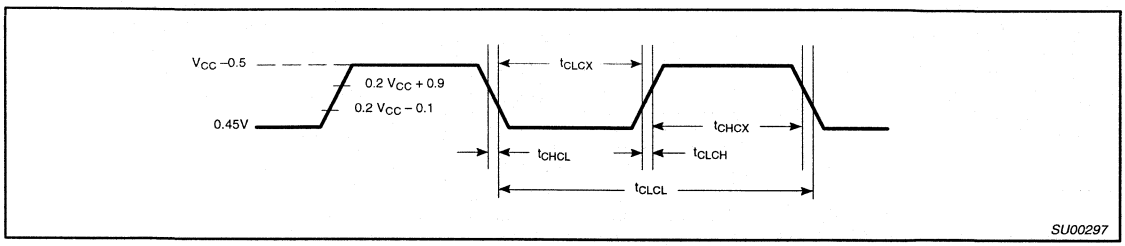


Figure 1. External Clock Drive

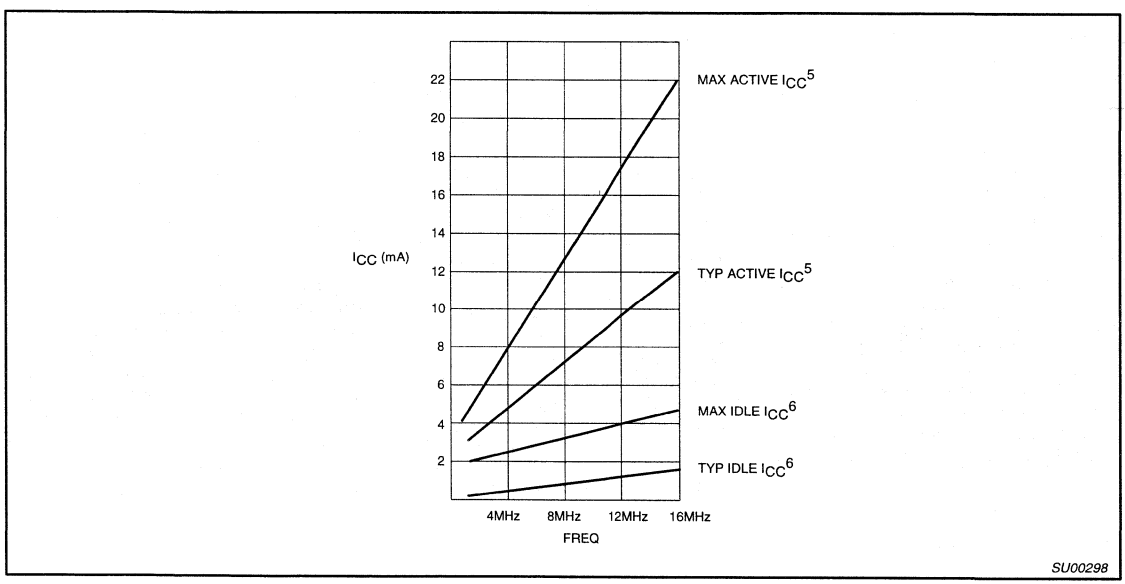


Figure 2. I_{CC} vs. FREQ
Maximum I_{CC} values taken at V_{CC} max and worst case temperature.
Typical I_{CC} values taken at V_{CC} = 5.0V and 25°C.
Notes 5 and 6 refer to DC Electrical Characteristics.

OSCILLATOR CHARACTERISTICS

X1 and X2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, X1 should be driven while X2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-up, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.

IDLE MODE

In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. the control bits for the reduced power modes are in the special function register PCON.

Table 1. External Pin Status During Idle and Power-Down Modes

MODE	Port 0	Port 1	Port 2
Idle	Data	Data	Data
Power-down	Data	Data	Data

DIFFERENCES BETWEEN THE 8XC751 AND THE 80C51

Memory Organization

The central processing unit (CPU) manipulates operands in two address spaces as shown in Figure 3. The part's internal memory space consists of 2k bytes of program memory, and 64 bytes of data RAM overlapped with the 128-byte special function register area. The differences from the 80C51 are in RAM size (64 bytes vs. 128 bytes), in external RAM access (not available on the 83C751), in internal ROM size (2k bytes vs. 4k bytes), and in external program memory expansion (not available on the 83C751). The 128-byte special function register (SFR) space is accessed as on the 80C51 with some of the registers having been changed to reflect changes in the 83C751 peripheral functions. The stack may be located anywhere in internal RAM by loading the 8-bit stack pointer (SP). It should be noted that stack depth is limited to 64 bytes, the amount of available RAM. A reset loads the stack pointer with 07 (which is pre-incremented on a PUSH instruction).

Program Memory

On the 8XC751, program memory is 2048 bytes long and is not externally expandable, so the 80C51 instructions MOVX, LJMP, and LCALL are not implemented. The only fixed locations in program memory are the addresses at which execution is taken up in response to reset and interrupts, which are as follows:

Event	Program Memory Address
Reset	000
External $\overline{INT0}$	003
Counter/timer 0	00B
External $\overline{INT1}$	013
Timer I	01B
I^2C serial	023

Counter/Timer Subsystem

The 8XC751 has one counter/timer called timer/counter 0. Its operation is similar to mode 2 operation on the 80C51, but is extended to 16 bits with 16 bits of autoload. The controls for this counter are centralized in a single register called TCON.

A watchdog timer, called Timer I, is for use with the I^2C subsystem. In I^2C applications, this timer is dedicated to time-generation and bus monitoring of the I^2C. In non-I^2C applications, it is available for use as a fixed time-base.

Counter Timer – Special Function Register

The counter/timer has only one mode of operation, so the TMOD SFR is not used. There is also only one counter/timer, so there is no need for the TL1 and TH1 SFRs found on the 80C51. These have been replaced on the 83C751 by RTL and RTH, the counter/timer reload registers. Table 3 shows the special function registers, their locations, and reset values.

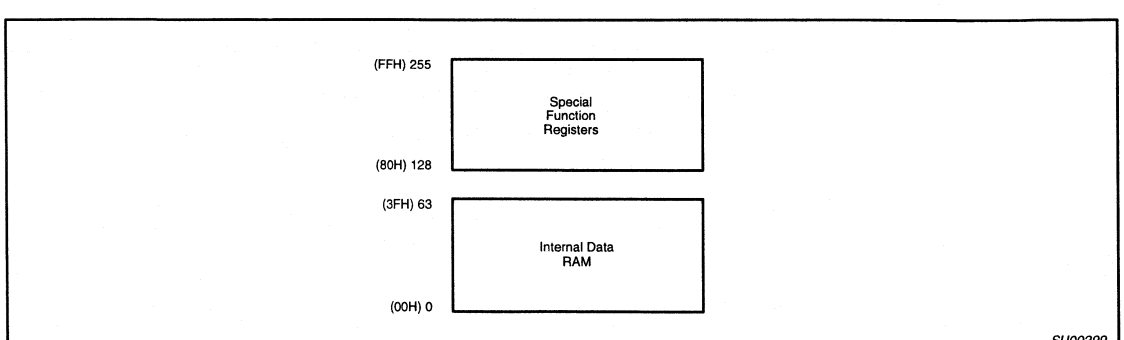


Figure 3. Memory Map

Interrupt Subsystem – Fixed Priority

The IP register and the 2-level interrupt system of the 80C51 are eliminated. Simultaneous interrupt conditions are resolved by a single-level, fixed priority as follows:

Highest priority:	Pin $\overline{INT0}$
	Counter/timer flag 0
	Pin $\overline{INT1}$
	Timer I
Lowest priority:	Serial I^2C

Special Function Register – Interrupt Subsystem

Because the interrupt structure is single level on the 83C751, there is no need for the IP SFR, so it is not used.

Serial Communications

The 8XC751 contains an I^2C serial communications port instead of the 80C51 UART. The I^2C serial port is a single bit hardware interface with all of the hardware necessary to support multimaster and slave operations. Also included are receiver digital filters and timer (timer I) for communication watch-dog purposes. The I^2C serial port is controlled through four special function registers; I^2C control, I^2C data, I^2C status, and I^2C configuration.

Special Function Register – Serial Communications

The 83C751 contains many of the special function registers (SFR) that are found on the 80C51. Due to the different peripheral features on the 83C751, there are several additional SFRs and several that have been changed.

Since the standard UART found on the 80C51 has been replaced by the I^2C serial interface, the UART SFRs, SCON, and SBUF have been replaced by I2CON and I2DAT, and two additional I^2C registers have been added (I2STA and I2CFG).

I/O Port Latches (P0, P1, P3)

The port latches function the same as those on the 80C51. Since there is no port 2 on the 83C751, the P2 latch is not used. Port 0 on the 83C751 has only 3 bits, so only 3 bits of the P0 SFR have a useful function.

Special Function Register – I/O Port Latches

There is no Port2 on the 8XC751, so P2 is not used. Also, only 3 bits of P0 SFR have a useful function.

Data Pointer (DPTR)

The data pointer (DPTR) consists of a high byte (DPH) and a low byte (DPL). In the 80C51 this register allows the access of external data memory using the MOVX instruction. Since the 83C751 does not support MOVX or external memory accesses, this register is generally used as a 16-bit offset pointer of the accumulator in a MOVC instruction. DPTR may also be manipulated as two independent 8-bit registers.

Table 2. I^2C Special Function Register Addresses

REGISTER ADDRESS			BIT ADDRESS							
NAME	SYMBOL	ADDRESS	MSB							LSB
I^2C control	I2CON	98	9F	9E	9D	9C	9B	9A	99	98
I^2C data	I2DAT	99	–	–	–	–	–	–	–	–
I^2C configuration	I2CFG	D8	DF	DE	DD	DC	DB	DA	D9	D8
I^2C status	I2STA	F8	FF	FE	FD	FC	FB	FA	F9	F8

Table 3. 8XC751 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB							LSB	RESET VALUE
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR:	Data pointer (2 bytes)										
DPH	High byte	83H									00H
DPL	Low byte	82H									00H
			DF	DE	DD	DC	DB	DA	D9	D8	
I²CFG*#	I²C configuration	D8H/RD	SLAVEN	MASTRQ	0	TIRUN	–	–	CT1	CT0	0000xx00B
		WR	SLAVEN	MASTRQ	CLRTI	TIRUN	–	–	CT1	CT0	
			9F	9E	9D	9C	9B	9A	99	98	
I²CON*#	I²C control	98H/RD	RDAT	ATN	DRDY	ARL	STR	STP	MASTER	–	81H
		WR	CXA	IDLE	CDR	CARL	CSTR	CSTP	XSTR	XSTP	
I²DAT#	I²C data	99H/RD	RDAT	0	0	0	0	0	0	0	80H
		WR	XDAT	X	X	X	X	X	X	X	
			FF	FE	FD	FC	FB	FA	F9	F8	
I²STA*#	I²C status	F8H	–	IDLE	XDATA	XACTV	MAKSTR	MAKSTP	XSTR	XSTP	x0100000B
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*#	Interrupt enable	A8H	EA	–	–	EI2	ETI	EX1	ET0	EX0	00H
								82	81	80	
P0*#	Port 0	80H	–	–	–	–	–	–	SDA	SCL	xxxxx111B
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	T0	$\overline{INT1}$	$\overline{INT0}$	–	–	–	–	–	FFH
P3*	Port 3	B0H	B7	B6	B5	B4	B3	B2	B1	B0	FFH
PCON#	Power control	87H	–	–	–	–	–	–	PD	IDL	xxxxxx00B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	00H
SP	Stack pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*#	Timer/counter control	88H	GATE	C/T	TF	TR	IE0	IT0	IE1	IT1	00H
TL#	Timer low byte	8AH									00H
TH#	Timer high byte	8CH									00H
RTL#	Timer low reload	8BH									00H
RTH#	Timer high reload	8DH									00H

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.

I/O Port Structure

The 8XC751 has two 8-bit ports (ports 1 and 3) and one 3-bit port (port 0). All three ports on the 8XC751 are bidirectional. Each consists of a latch (special function register P0, P1, P3), an output driver, and an input buffer. Three port 1 pins and two port 0 pins are multifunctional. In addition to being port pins, these pins serve the function of special features as follows:

Port Pin	Alternate Function
P0.0	I^2C clock (SCL)
P0.1	I^2C data (SDA)
P1.5	INT0 (external interrupt 0 input)
P1.6	INT1 (external interrupt 1 input)
P1.7	T0 (timer 0 external input)

Ports 1 and 3 are identical in structure to the same ports on the 80C51. The structure of port 0 on the 8XC751 is similar to that of the 80C51 but does not include address/data input and output circuitry. As on the 80C51, ports 1 and 3 are quasi-bidirectional while port 0 is bidirectional with no internal pullups.

Timer/Counter

The 8XC751 has two timers: a 16-bit timer/counter and a 10-bit fixed-rate timer. The 16-bit timer/counter's operation is similar to mode 2 operation on the 80C51, but is extended to 16 bits. The timer/counter is clocked by either 1/12 the oscillator frequency or by transitions on the T0 pin. The C/T pin in special function register TCON selects between these two modes. When the TCON TR bit is set, the timer/counter is enabled. Register pair TH and TL are incremented by the clock source. When the register pair overflows, the register pair is reloaded with the values in registers RTH and RTL. The value in the reload registers is left unchanged. See the 83C751 counter/timer block diagram in Figure 4. The TF bit in special function register TCON is set on counter overflow and, if the interrupt is enabled, will generate an interrupt.

TCON Register

MSB LSB

GATE	C/T	TF	TR	IE0	IT0	IE1	IT1

GATE 1 – Timer/counter is enabled only when INT0 pin is high, and TR is 1.
0 – Timer/counter is enabled when TR is 1.

C/T 1 – Counter/timer operation from T0 pin.
0 – Timer operation from internal clock.

TF 1 – Set on overflow of TH.
0 – Cleared when processor vectors to interrupt routine and by reset.

TR 1 – Timer/counter enabled.
0 – Timer/counter disabled.

IE0 1 – Edge detected in $\overline{INT0}$.

IT0 1 – $\overline{INT0}$ is edge triggered.
0 – $\overline{INT0}$ is level sensitive.

IE1 1 – Edge detected on $\overline{INT1}$.

IT1 1 – $\overline{INT1}$ is edge triggered.
0 – $\overline{INT1}$ is level sensitive.

These flags are functionally identical to the corresponding 80C51 flags, except that there is only one timer on the 83C751 and the flags are therefore combined into one register.

Note that the positions of the IE0/IT0 and IE1/IT1 bits are transposed from the positions used in the standard 80C51 TCON register.

Timer I is used to control the timing of the I^2C bus and also to detect a "bus locked" condition, by causing an interrupt when nothing happens on the I^2C bus for an inordinately long period of time while a transmission is in progress. If the interrupt does not occur, the program can attempt to correct the fault and allow the last I^2C transmission to be repeated.

The I^2C watchdog timer, timer I, is also available as a general-purpose fixed-rate timer when the I^2C interface is not being used. A clock rate of 1/12 the oscillator frequency forms the input to the timer. Timer I has a timeout interval of 1024 machine cycles when used as a fixed-rate timer.

I^2C Serial Interface

The I^2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Bidirectional data transfer between masters and slaves
- Serial addressing of slaves (no added wiring)
- Acknowledgment after each transferred byte
- Multimaster bus
- Arbitration between simultaneously transmitting masters without corruption of serial data on bus
- The 82B715 extends communication distance to 100 feet (30M).

A large family of I^2C compatible ICs is available. See the I^2C section of this manual for more details on the bus and available ICs.

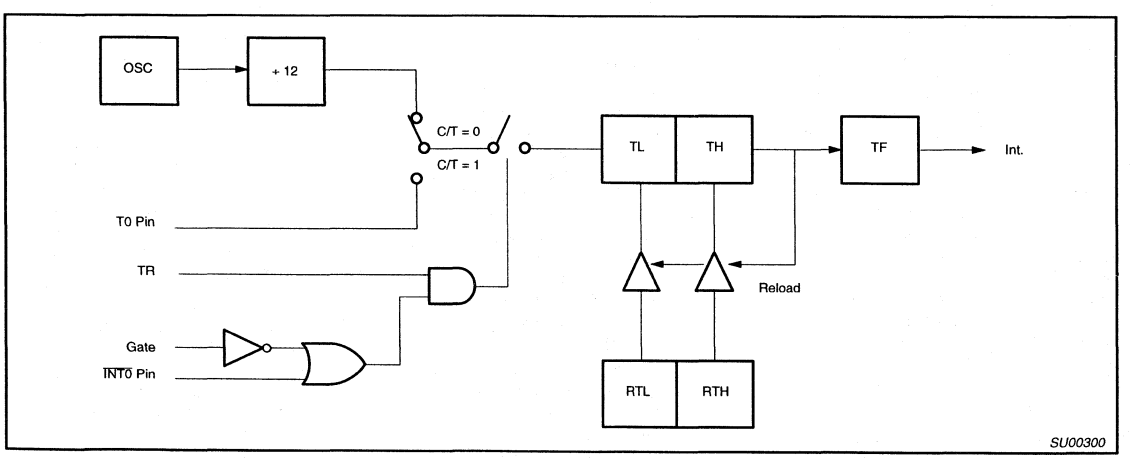


Figure 4. 83C751 Counter/Timer Block Diagram

The 83C751 I²C subsystem includes hardware to simplify the software required to drive the I²C bus. The hardware is a single bit interface which in addition to including the necessary arbitration and framing error checks, includes clock stretching and a bus timeout timer. The interface is synchronized to software either through polled loops or interrupts. Refer to the application note AN422, in Section 4, entitled "Using the 8XC751 Microcontroller as an I²C Bus Master" for additional discussion of the 83C751 I²C interface and sample driver routines.

Six time spans are important in I²C operation and are insured by timer I:

- The MINIMUM HIGH time for SCL when this device is the master.
- The MINIMUM LOW time for SCL when this device is a master. This is not very important for a single-bit hardware interface like this one, because the SCL low time is stretched until the software responds to the I²C flags. The software response time normally meets or exceeds the MIN LO time. In cases where the software responds within MIN HI + MIN LO) time, timer I will ensure that the minimum time is met.
- The MINIMUM SCL HIGH TO SDA HIGH time in a stop condition.
- The MINIMUM SDA HIGH TO SDA LOW time between I²C stop and start conditions (4.7µs, see spec.).
- The MINIMUM SDA LOW TO SCL LOW time in a start condition.
- The MAXIMUM SCL CHANGE time while an I²C frame is in progress. A frame is in progress between a start condition and the following stop condition. This time span serves to detect a lack of software response on this 8XC751 as well as external I²C problems. SCL "stuck low" indicates a faulty master or slave. SCL "stuck high" may mean a faulty device, or that noise induced onto the I²C bus caused all masters to withdraw from I²C arbitration.

The first five of these times are 4.7µs (see I²C specification) and are covered by the low order three bits of timer I. Timer I is clocked by the 8XC751 oscillator, which can vary in frequency from 0.5 to 16MHz. Timer I can be preloaded with one of four values to optimize timing for different oscillator frequencies. At lower frequencies, software response time is increased and will degrade maximum performance of the I²C bus. See special function register I2CFG description for prescale values (CT0, CT1).

The MAXIMUM SCL CHANGE time is important, but its exact span is not critical. The complete 10 bits of timer I are used to count out the maximum time. When I²C operation is enabled, this counter is cleared by transitions on the SCL pin. The timer does not run between I²C frames (i.e., whenever reset or stop occurred more recently than the last start). When this counter is running, it will carry out after 1020 to 1023 machine cycles have elapsed since a change on SCL. A carry out causes a hardware reset of the 83C751 I²C interface and generates an interrupt if the timer I interrupt is enabled. In cases where the bus hangup is due to a lack of software response by this 83C751, the reset releases SCL and allows I²C operation among other devices to continue.

I²C Interrupts

If I²C interrupts are enabled (EA and EI2 are both set to 1), an I²C interrupt will occur whenever the ATN flag is set by a start, stop, arbitration loss, or data ready condition (refer to the description of ATN following). In practice, it is not efficient to operate the I²C interface in this fashion because the I²C interrupt service routine would somehow have to distinguish between hundreds of possible conditions. Also, since I²C can operate at a fairly high rate, the software may execute faster if the code simply waits for the I²C interface.

Typically, the I²C interrupt should only be used to indicate a start condition at an idle slave device, or a stop condition at an idle master device (if it is waiting to use the I²C bus). This is accomplished by enabling the I²C interrupt only during the aforementioned conditions.

I²C Register I2CON

	7	6	5	4	3	2	1	0
Read	RDAT	ATN	DRDY	ARL	STR	STP	MASTER	–
Write	CXA	IDLE	CDR	CARL	CSTR	CSTP	XSTR	XSTP

Reading I2CON

RDAT The data from SDA is captured into "Receive DATa" whenever a rising edge occurs on SCL. RDAT is also available (with seven low-order zeros) in the I2DAT register. The difference between reading it here and there is that reading I2DAT clears DRDY, allowing the I²C to proceed on to another bit. Typically, the first seven bits of a received byte are read from I2DAT, while the 8th is read here. Then I2DAT can be written to send the Ack bit and clear DRDY.

ATN "ATteNtion" is 1 when one or more of DRDY, ARL, STR, or STP is 1. Thus, ATN comprises a single bit that can be tested to release the I²C service routine from a "wait loop."

DRDY "Data ReaDY" (and thus ATN) is set when a rising edge occurs on SCL, except at idle slave. DRDY is cleared by writing CDR = 1, or by writing or reading the I2DAT register. The following low period on SCL is stretched until the program responds by clearing DRDY.

Checking ATN and DRDY

When a program detects ATN = 1, it should next check DRDY. If DRDY = 1, then if it receives the last bit, it should capture the data from RDAT (in I2DAT or I2CON). Next, if the next bit is to be sent, it should be written to I2DAT. One way or another, it should clear DRDY and then return to monitoring ATN. Note that if any of ARL, STR, or STP is set, clearing DRDY will not release SCL to high, so that the I²C will not go on to the next bit. If a program detects ATN = 1, and DRDY = 0, it should go on to examine ARL, STR, and STP.

ARL "Arbitration Loss" is 1 when transmit Active was set, but this 83C751 lost arbitration to another transmitter. Transmit Active is cleared when ARL is 1. There are four separate cases in which ARL is set.

1. If the program sent a 1 or repeated start, but another device sent a 0, or a stop, so that SDA is 0 at the rising edge of SCL. (If the other device sent a stop, the setting of ARL will be followed shortly by STP being set.)
2. If the program sent a 1, but another device sent a repeated start, and it drove SDA low before the 83C751 could drive SCL low. (This type of ARL is always accompanied by STR = 1.)
3. In master mode, if the program sent a repeated start, but another device sent a 1, and it drove SCL low before this 83C751 could drive SDA low.
4. In master mode, if the program sent stop, but it could not be sent because another device sent a 0.

STR "STaRt" is set to a 1 when an I²C start condition is detected at a non-idle slave or at a master. (STR is not set when an idle slave becomes active due to a start bit; the slave has nothing useful to do until the rising edge of SCL sets DRDY.)

STP "STOP" is set to 1 when an I²C stop condition is detected at a non-idle slave or at a master. (STP is not set for a stop condition at an idle slave.)

MASTER "MASTER" is 1 if this 83C751 is currently a master on the I²C. MASTER is set when MASTRQ is 1 and the bus is not busy (i.e., if a start bit hasn't been received since reset or a "Timer I" time-out, or if a stop has been received since the last start). MASTER is cleared when ARL is set, or after the software writes MASTRQ = 0 and then XSTP = 1.

Writing I2CON

Typically, for each bit in an I²C message, a service routine waits for ATN = 1. Based on DRDY, ARL, STR, and STP, and on the current bit position in the message, it may then write I2CON with one or more of the following bits, or it may read or write the I2DAT register.

CXA Writing a 1 to "Clear Xmit Active" clears the Transmit Active state. (Reading the I2DAT register also does this.)

Regarding Transmit Active

Transmit Active is set by writing the I2DAT register, or by writing I2CON with XSTR = 1 or XSTP = 1. The I²C interface will only drive the SDA line low when Transmit Active is set, and the ARL bit will only be set to 1 when Transmit Active is set. Transmit Active is cleared by reading the I2DAT register, or by writing I2CON with CXA = 1. Transmit Active is automatically cleared when ARL is 1.

IDLE Writing 1 to "IDLE" causes a slave's I²C hardware to ignore the I²C until the next start condition (but if MASTRQ is 1, then a stop condition will make the 83C751 into a master).

CDR Writing a 1 to "Clear Data Ready" clears DRDY. (Reading or writing the I2DAT register also does this.)

CARL Writing a 1 to "Clear Arbitration Loss" clears the ARL bit.

CSTR Writing a 1 to "Clear STaRt" clears the STR bit.

CSTP Writing a 1 to "Clear STOP" clears the STP bit. Note that if one or more of DRDY, ARL, STR, or STP is 1, the low time of SCL is stretched until the service routine responds by clearing them.

XSTR Writing 1s to "Xmit repeated STaRt" and CDR tells the I²C hardware to send a repeated start condition. This should only be at a master. Note that XSTR need not and should not be used to send an "initial" (nonrepeated) start; it is sent automatically by the I²C hardware. Writing XSTR = 1 includes the effect of writing I2DAT with XDAT = 1; it sets Transmit Active and releases SDA to high during the SCL low time. After SCL goes high, the I²C hardware waits for the suitable minimum time and then drives SDA low to make the start condition.

XSTP Writing 1s to "Xmit STOP" and CDR tells the I²C hardware to send a stop condition. This should only be done at a master. If there are no more messages to initiate, the service routine should clear the MASTRQ bit in I2CFG to 0 before writing XSTP with 1. Writing XSTP = 1 includes the effect of writing I2DAT with XDAT = 0; it sets Transmit Active and drives SDA low during the SCL low time. After SCL goes high, the I²C hardware waits for the suitable minimum time and then releases SDA to high to make the stop condition.

NOTE: Because of the manner in which register bit addressing is implemented in the 80C51 family, the I2CON register should never be altered by use of the SETB, CLR, CPL, MOV (bit), or JBC instructions. This is due to the fact that read and write functions of this register are different. Testing of I2CON bits via the JB and JNB instructions is supported.

I²C Register I2DAT

	7	6	5	4	3	2	1	0
Read	RDAT	0	0	0	0	0	0	0
Write	XDAT	X	X	X	X	X	X	X

RDAT "Receive DATa" is captured from SDA every rising edge of SCL. Reading I2DAT also clears DRDY and the Transmit Active state.

XDAT "Xmit Data" sets the data for the next bit. Writing I2DAT also clears DRDY and sets the Transmit Active state.

Regarding Software Response Time

Because the 83C751 can run at 16MHz, and because the I²C interface is optimized for high-speed operation, it is quite likely that an I²C service routine will sometimes respond to DRDY (which is set at a rising edge of SCL) and write I2DAT before SCL has gone low again. If XDAT were applied directly to SDA, this situation would produce an I²C protocol violation. The programmer need not worry about this possibility because XDAT is applied to SDA only when SCL is low.

Conversely, a program that includes an I²C service routine may take a long time to respond to DRDY. Typically, an I²C routine operates on a flag-polling basis during a message, with interrupts from other peripheral functions enabled. If an interrupt occurs, it will delay the response of the I²C service routine. The programmer need not worry about this very much either, because the I²C hardware stretches the SCL low time until the service routine responds. The only constraint on the response is that it must not exceed the Timer I time-out, which is at least 765 microseconds.

I²C Register I2CFG

	7	6	5	4	3	2	1	0
Read	SLAVEN	MASTRQ	0	TIRUN	–	–	CT1	CT0
Write	SLAVEN	MASTRQ	CLRTI	TIRUN	–	–	CT1	CT0

SLAVEN Writing a 1 to "SLAVe ENable" enables the slave functions of the I²C subsystem. If SLAVEN and MASTRQ are 0, the I²C hardware is disabled. This bit is cleared to 0 by reset and by an I²C time-out.

MASTRQ Writing a 1 to "MASTRQ" requests mastership of the I²C. If a frame from another master is in progress when this bit is changed from 0 to 1, action is delayed until a stop condition is detected. Then, or immediately if a frame is not in progress, a start condition is sent and DRDY is set (thus making ATN 1 and generating an I²C interrupt). When a master wishes to release mastership status of the I²C, it writes a 1 to XSTP in I2CON. MASTRQ is cleared by reset and by an I²C time-out.

CLRTI Writing a 1 to this bit clears the Timer I interrupt flag. This bit position always reads as a 0.

TIRUN Writing a 1 to this bit lets Timer I run; a zero stops and clears it. Together with SLAVEN, MASTRQ, and MASTER, this bit determines operational modes as shown in Table 4.

CT1,0 These two bits are programmed as a function of the OSC rate, to optimize the MIN HI and LO time of SCL when this 83C751 is a master on the I²C. The time value determined by these bits controls both of these parameters, and also the timing for stop and start conditions. These bits are cleared to 00 by reset.

Table 4. Interaction of TIRUN with SLAVEN, MASTRQ, and MASTER

SLAVEN, MASTRQ, MASTER	TIRUN	OPERATING MODE
All 0	0	The I^2C interface is disabled. Timer I is cleared and does not run. This is the state assumed after a reset. If an I^2C application wants to ignore the I^2C at certain times, it should write SLAVEN, MASTRQ, and TIRUN all to zero.
All 0	1	The I^2C interface is disabled. Timer I operates as a free-running time base. Use this mode only in non-I^2C applications.
Any or all 1	0	The I^2C interface is enabled. The 3 low-order bits of Timer I run for min-time generation, but the hi-order bits do not, so that there is no checking for I^2C being "hung." This configuration can be used for very slow I^2C operation.
Any or all 1	1	The I^2C interface is enabled. Timer I runs during frames on the I^2C, and is cleared by transitions on SCL, and by Start and Stop conditions. This is the normal state for I^2C operation.

Values to be used in the CT1 and CT0 bits are shown in Table 5. To allow the I^2C bus to run at the maximum rate for a particular oscillator frequency, compare the actual oscillator rate to the f_{OSC} max column in the table. The value for CT1 and CT0 is found in the first line of the table where f_{OSC} max is greater than or equal to the actual frequency.

The table also shows the osc/12 count for various settings of CT1/CT0. This allows calculation of the actual minimum high and low times for SCL as follows:

SCL min high/low time = $\frac{12 * \text{count}}{\text{osc (in MHz)}}$
(in microseconds)

For instance, at a 16MHz frequency, with CT1/CT0 set to 10, the minimum SCL high and low times will be 5.25µs

The table also shows the Timer I timeout period (given in machine cycles) for each CT1/CT0 combination. The timeout period varies because of the way in which minimum SCL high and low times are measured. When the I^2C interface is operating, Timer I is preloaded at every SCL transition with a value dependent upon CT1/CT0. The preload value is chosen such that a minimum SCL high or low time has elapsed when Timer I reaches a count of 008 (the actual value preloaded into Timer I is 8 minus the osc/12 count).

I^2C Register I2STA

Read only

7	6	5	4	3	2	1	0
–	IDLE	XDATA	XACTV	MAKSTR	MAKSTP	XSTR	XSTP

MSB LSB

This register is read only and reflects the internal status of the I^2C hardware. IDLE, XSTR, and XSTP reflect the status of the like named bits in the I2CON register.

XDATA The content of the transmitter buffer.

XACTV Transmitter active.

MAKSTR This bit is high while the hardware is effecting a start condition.

MAKSTP This bit is high while the hardware is effecting a stop condition.

XSTR This bit is active while the hardware is effecting a repeated start condition.

XSTP This bit is active while the hardware is effecting a repeated stop condition.

Interrupts

The interrupt structure is a five-source, one-level interrupt system. Interrupt sources common to the 80C51 are the external interrupts ($\overline{INT0}$, $\overline{INT1}$) and the timer/counter interrupt (ET0). The I^2C interrupt (EI2) and Timer I interrupt (ETI) are the other two interrupt sources. The interrupt sources are listed below in their order of polling sequence priority.

Upon interrupt or reset the program counter is loaded with specific values for the appropriate interrupt service routine in program memory. These values are:

Event	Program Memory Address	Priority
Reset	000	Highest
INT0	003	
Counter/Timer 0	00B	
INT1	013	
Timer I	01B	
I^2C	023	Lowest

The interrupt enable register (IE) is used to individually enable or disable the five sources. Bit $\overline{EA}$ in the interrupt enable register can be used to globally enable or disable all interrupt sources. The interrupt enable register is described below. All other interrupt details are based on the 80C51 interrupt architecture.

Table 5. CT1, CT0 Values

CT1, CT0	OSC/12 COUNT	f_{OSC} MAX	TIMEOUT PERIOD
10	7	16.8MHz	1023 cycles
01	6	14.4MHz	1022 cycles
00	5	12.0MHz	1021 cycles
11	4	9.6MHz	1020 cycles

Interrupt Enable Register

$\overline{EA}$	X	X	EI2	ETI	EX1	ET0	EX0

Symbol	Position	Function
$\overline{EA}$	IE.7	Disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit
–	IE.6	Reserved
–	IE.5	Reserved
EI2	IE.4	Enables or disables the I^2C interrupt. If EI2 = 0, the I^2C interrupt is disabled
ETI	IE.3	Enables or disables the Timer I overflow interrupt. If ETI = 0, the Timer I interrupt is disabled.
EX1	IE.2	Enables or disables external interrupt 1. If EX1 = 0, external interrupt 1 is disabled.
ET0	IE.1	Enables or disables the Timer 0 overflow interrupt. If ET0 = 0, theTimer 0 interrupt is disabled.
EX0	IE.0	Enables or disables external interrupt 0. If EX0 = 0, external interrupt 0 is disabled.

87C751 PROGRAMMING CONSIDERATIONS

EPROM Characteristics

The 87C751 is programmed by using a modified Quick-Pulse Programming algorithm similar to that used for devices such as the 87C451 and 87C51. It differs from these devices in that a serial data stream is used to place the 87C751 in the programming mode.

Figure 5 shows a block diagram of the programming configuration for the 87C751. Port pin P0.2 is used as the programming voltage supply input (V_{PP} signal). Port pin P0.1 is used as the program (PGM/) signal. This pin is used for the 25 programming pulses.

Port 3 is used as the address input for the byte to be programmed and accepts both the high and low components of the eleven bit address. Multiplexing of these address components is performed using the ASEL input. The user should drive the ASEL input high and then drive port 3 with the high order bits of the address. ASEL should remain high for at least 13 clock cycles. ASEL may then be driven low which latches the high order bits of the address internally. the high address should remain on port 3 for at least two clock cycles after ASEL is driven low. Port 3 may then be driven with the low byte of the address. The low address will be internally stable 13 clock cycles later. The address will remain stable provided that the low byte placed on port 3 is held stable and ASEL is kept low. **Note:** ASEL needs to be pulsed high only to change the high byte of the address.

Port 1 is used as a bidirectional data bus during programming and verify operations. During programming mode, it accepts the byte to be programmed. During verify mode, it provides the contents of the EPROM location specified by the address which has been supplied to Port 3.

The XTAL1 pin is the oscillator input and receives the master system clock. This clock should be between 1.2 and 6MHz.

The RESET pin is used to accept the serial data stream that places the 87C751 into various programming modes. This pattern consists of a 10-bit code with the LSB sent first. Each bit is synchronized to the clock input, X1.

Programming Operation

Figures 6 and 7 show the timing diagrams for the program/verify cycle. RESET should initially be held high for at least two machine cycles. P0.1 (PGM/) and P0.2 (V_{PP}) will be at V_{OH} as a result of the RESET operation. At this point, these pins function as normal quasi-bidirectional I/O ports and the programming equipment may pull these lines low. However, prior to sending the 10-bit code on the RESET pin, the programming equipment should drive these pins high (V_{IH}). The RESET pin may now be used as the serial data input for the data stream which places the 87C751 in the programming mode. Data bits are sampled during the clock high time and thus should only change during the time that the clock is low. Following transmission of the last data bit, the RESET pin should be held low.

Next the address information for the location to be programmed is placed on port 3 and ASEL is used to perform the address multiplexing, as previously described. At this time, port 1 functions as an output.

A high voltage V_{PP} level is then applied to the V_{PP} input (P0.2). (This sets Port 1 as an input port). The data to be programmed into the EPROM array is then placed on Port 1. This is followed by a series of programming pulses applied to the PGM/ pin (P0.1). These pulses are created by driving P0.1 low and then high. This pulse is repeated until a total of 25 programming pulses have occurred. At the conclusion of the last pulse, the PGM/ signal should remain high.

The V_{PP} signal may now be driven to the V_{OH} level, placing the 87C751 in the verify mode. (Port 1 is now used as an output port). After four machine cycles (48 clock periods), the contents of the addressed location in the EPROM array will appear on Port 1.

The next programming cycle may now be initiated by placing the address information at the inputs of the multiplexed buffers, driving the V_{PP} pin to the V_{PP} voltage level, providing the byte to be programmed to Port1 and issuing the 26 programming pulses on the PGM/ pin, bringing V_{PP} back down to the V_C level and verifying the byte.

Programming Modes

The 87C751 has four programming features incorporated within its EPROM array. These include the USER EPROM for storage of the application's code, a 16-byte encryption key array and two security bits. Programming and verification of these four elements are selected by a combination of the serial data stream applied to the RESET pin and the voltage levels applied to port pins P0.1 and P0.2. The various combinations are shown in Table NO TAG.

Encryption Key Table

The 87C751 includes a 16-byte EPROM array that is programmable by the end user. The contents of this array can then be used to encrypt the program memory contents during a program memory verify operation. When a program memory verify operation is performed, the contents of the program memory location is XNOR'ed with one of the bytes in the 16-byte encryption table. The resulting data pattern is then provided to port 1 as the verify data. The encryption mechanism can be disable, in essence, by leaving the bytes in the encryption table in their erased state (FFH) since the XNOR product of a bit with a logical one will result in the original bit. The encryption bytes are mapped with the code memory in 16-byte groups. the first byte in code memory will be encrypted with the first byte in the encryption table; the second byte in code memory will be encrypted with the second byte in the encryption table and so forth up to and including the 16the byte. The encryption repeats in 16-byte groups; the 17th byte in the code memory will be encrypted with the first byte in the encryption table, and so forth.

Security Bits

Two security bits, security bit 1 and security bit 2, are provided to limit access to the USER EPROM and encryption key arrays. Security bit 1 is the program inhibit bit, and once programmed performs the following functions:

1. Additional programming of the USER EPROM is inhibited.
2. Additional programming of the encryption key is inhibited.
3. Verification of the encryption key is inhibited.
4. Verification of the USER EPROM and the security bit levels may still be performed.

(If the encryption key array is being used, this security bit should be programmed by the user to prevent unauthorized parties from reprogramming the encryption key to all logical zero bits. Such programming would provide data during a verify cycle that is the logical complement of the USER EPROM contents).

Security bit 2, the verify inhibit bit, prevents verification of both the USER EPROM array and the encryption key arrays. The security bit levels may still be verified.

Programming and Verifying Security Bits

Security bits are programmed employing the same techniques used to program the USER EPROM and KEY arrays using serial data streams and logic levels on port pins indicated in Table NO TAG. When programming either security bit, it is not necessary to provide address or data information to the 87C751 on ports 1 and 3.

Verification occurs in a similar manner using the RESET serial stream shown in Table NO TAG. Port 3 is not required to be driven and the results of the verify operation will appear on ports 1.6 and 1.7.

Ports 1.7 contains the security bit 1 data and is a logical one if programmed and a logical zero if erased. Likewise, P1.6 contains the security bit 2 data and is a logical one if programmed and a logical zero if erased.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Flourless part number 2345–5 or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-s/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000µW/cm^2 rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Table 6. Implementing Program/Verify Modes

OPERATION	SERIAL CODE	P0.1 (PGM/)	P0.2 (V_{PP})
Program user EPROM	296H	–*	V_{PP}
Verify user EPROM	296H	V_{IH}	V_{IH}
Program key EPROM	292H	–*	V_{PP}
Verify key EPROM	292H	V_{IH}	V_{IH}
Program security bit 1	29AH	–*	V_{PP}
Program security bit 2	298H	–*	V_{PP}
Verify security bits	29AH	V_{IH}	V_{IH}

NOTE:
* Pulsed from V_{IH} to V_{IL} and returned to V_{IH}.

EPROM PROGRAMMING AND VERIFICATION

T_{amb} = 21°C to +27°C, V_{CC} = 5V ±10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	MAX	UNIT
$1/t_{CLCL}$	Oscillator/clock frequency	1.2	6	MHz
t_{AVGL}[1]	Address setup to P0.1 (PROG–) low	10µs + 24t_{CLCL}		
t_{GHAX}	Address hold after P0.1 (PROG–) high	48t_{CLCL}		
t_{DVGL}	Data setup to P0.1 (PROG–) low	38t_{CLCL}		
t_{GHDX}	Data hold after P0.1 (PROG–) high	36t_{CLCL}		
t_{SHGL}	V_{PP} setup to P0.1 (PROG–) low	10		µs
t_{GHSL}	V_{PP} hold after P0.1 (PROG–)	10		µs
t_{GLGH}	P0.1 (PROG–) width	90	110	µs
t_{AVQV}[2]	V_{PP} low (V_{CC}) to data valid		48t_{CLCL}	
t_{GHGL}	P0.1 (PROG–) high to P0.1 (PROG–) low	10		µs
t_{MASEL}	ASEL high time	13t_{CLCL}		
t_{HAHLD}	Address hold time	2t_{CLCL}		
t_{HASET}	Address setup to ASEL	13t_{CLCL}		
t_{ADSTA}	Low address to valid data		48t_{CLCL}	

NOTES:
1. Address should be valid at least 24t_{CLCL} before the rising edge of P0.2 (V_{PP}).
2. For a pure verify mode, i.e., no program mode in between, t_{AVQV} is 14t_{CLCL} maximum.

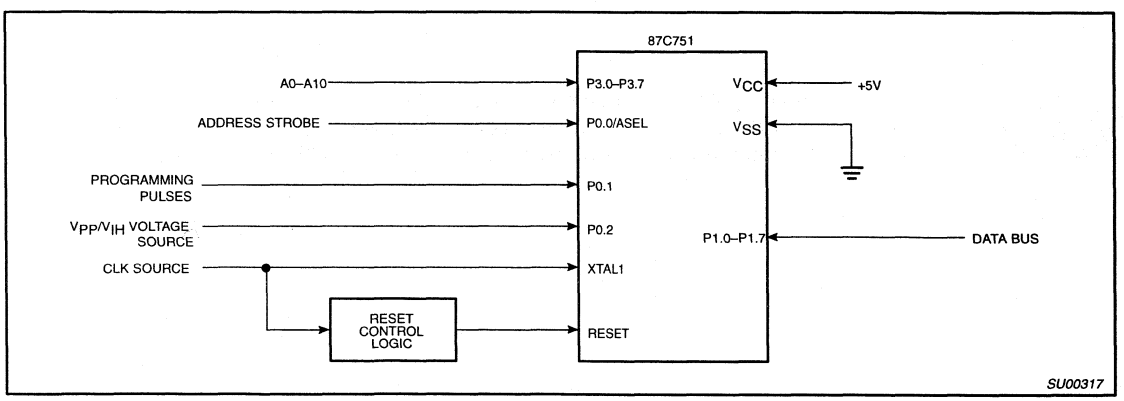


Figure 5. Programming Configuration

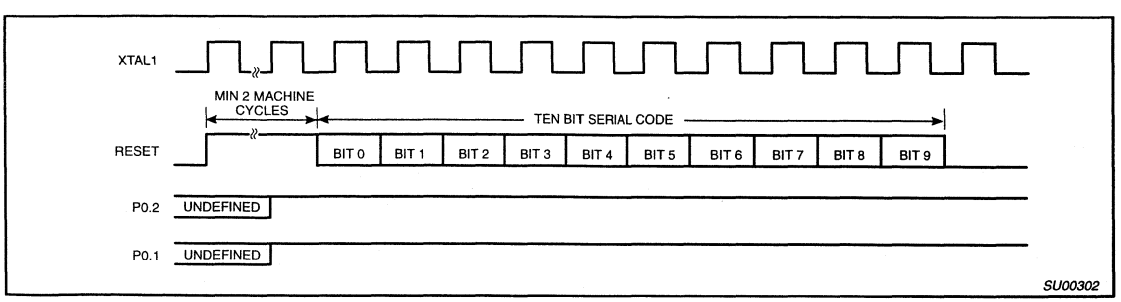


Figure 6. Entry into Program/Verify Modes

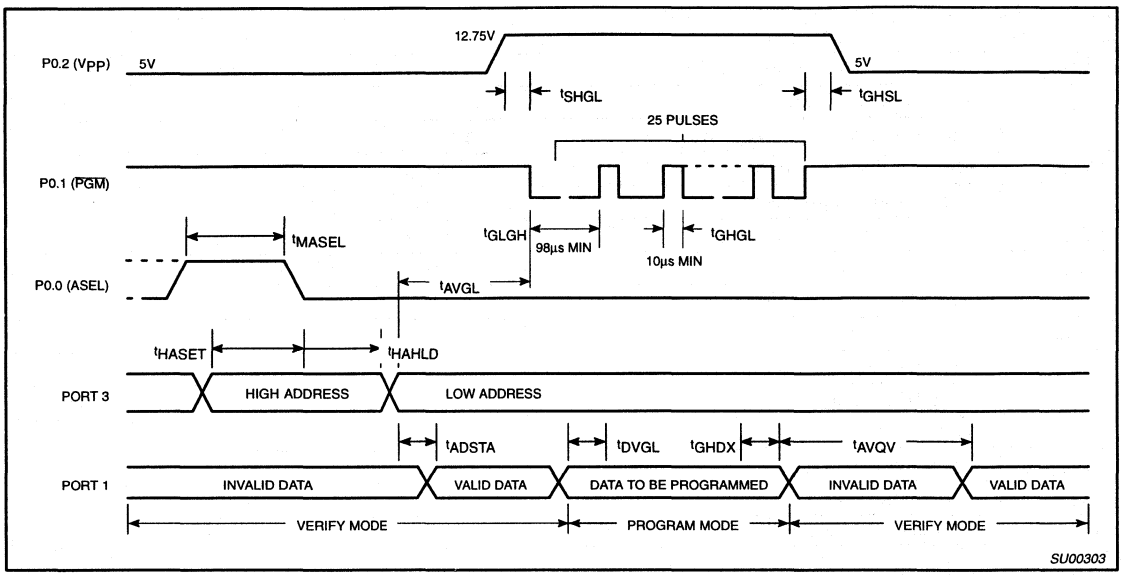


Figure 7. Program/Verify Cycle

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CMOS single-chip 8-bit microcontroller — 83C752/87C752

CMOS single-chip 8-bit microcontroller with A/D, PWM

DESCRIPTION

The Philips 83C752/87C752 offers many of the advantages of the 80C51 architecture in a small package and at low cost.

The 8XC752 Microcontroller is fabricated with Philips high-density CMOS technology. Philips epitaxial substrate minimizes CMOS latch-up sensitivity.

The 8XC752 contains a 2k × 8 ROM (83C752) EPROM (87C752), a 64 × 8 RAM, 21 I/O lines, a 16-bit auto-reload counter/timer, a fixed-priority level interrupt structure, a bidirectional inter-integrated circuit (I^2C) serial bus interface, an on-chip oscillator, a five channel multiplexed 8-bit A/D converter, and an 8-bit PWM output.

The onboard inter-integrated circuit (I^2C) bus interface allows the 8XC752 to operate as a master or slave device on the I^2C small area network. This capability facilitates I/O and RAM expansion, access to EEPROM, processor-to-processor communication, and efficient interface to a wide variety of dedicated I^2C peripherals.

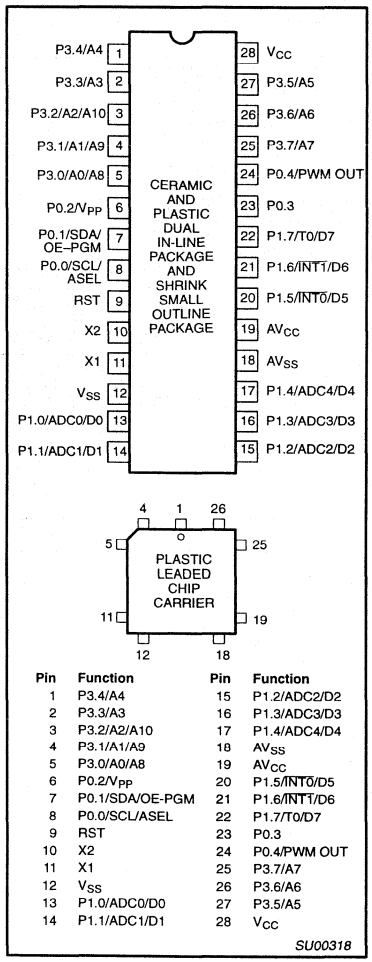
The EPROM version of this device, the 87C752, is also available in both quartz-lid erasable and plastic one-time programmable (OTP) packages. Once the array has been programmed, it is functionally equivalent to the masked ROM 83C752. Thus, unless explicitly stated otherwise, all references made to the 83C752 apply equally to the 87C752.

The 83C752 supports two power reduction modes of operation referred to as the idle mode and the power-down mode.

FEATURES

- Available in erasable quartz lid or One-Time Programmable plastic packages
- 80C51 based architecture
- Inter-integrated Circuit (I^2C) serial bus interface
- Small package sizes
  - 28-pin DIP
  - 28-pin PLCC
  - 28-pin SSOP
- Wide oscillator frequency range
- Low power consumption:
  - Normal operation: less than 11mA @ 5V, 12MHz
  - Idle mode
  - Power-down mode
- 2k × 8 ROM (83C752) EPROM (87C752)
- 64 × 8 RAM
- 16-bit auto reloadable counter/timer
- 5-channel 8-bit A/D converter
- 8-bit PWM output/timer
- Fixed-rate timer
- Boolean processor
- CMOS and TTL compatible
- Well suited for logic replacement, consumer and industrial applications

PIN CONFIGURATION



Pin	Function	Pin	Function
1	P3.4/A4	15	P1.2/ADC2/D2
2	P3.3/A3	16	P1.3/ADC3/D3
3	P3.2/A2/A10	17	P1.4/ADC4/D4
4	P3.1/A1/A9	18	AV_{SS}
5	P3.0/A0/A8	19	AV_{CC}
6	$P0.2/V_{PP}$	20	P1.5/$\overline{INT0}$/D5
7	P0.1/SDA/OE-PGM	21	P1.6/$\overline{INT1}$/D6
8	P0.0/SCL/ASEL	22	P1.7/T0/D7
9	RST	23	P0.3
10	X2	24	P0.4/PWM OUT
11	X1	25	P3.7/A7
12	V_{SS}	26	P3.6/A6
13	P1.0/ADC0/D0	27	P3.5/A5
14	P1.1/ADC1/D1	28	V_{CC}

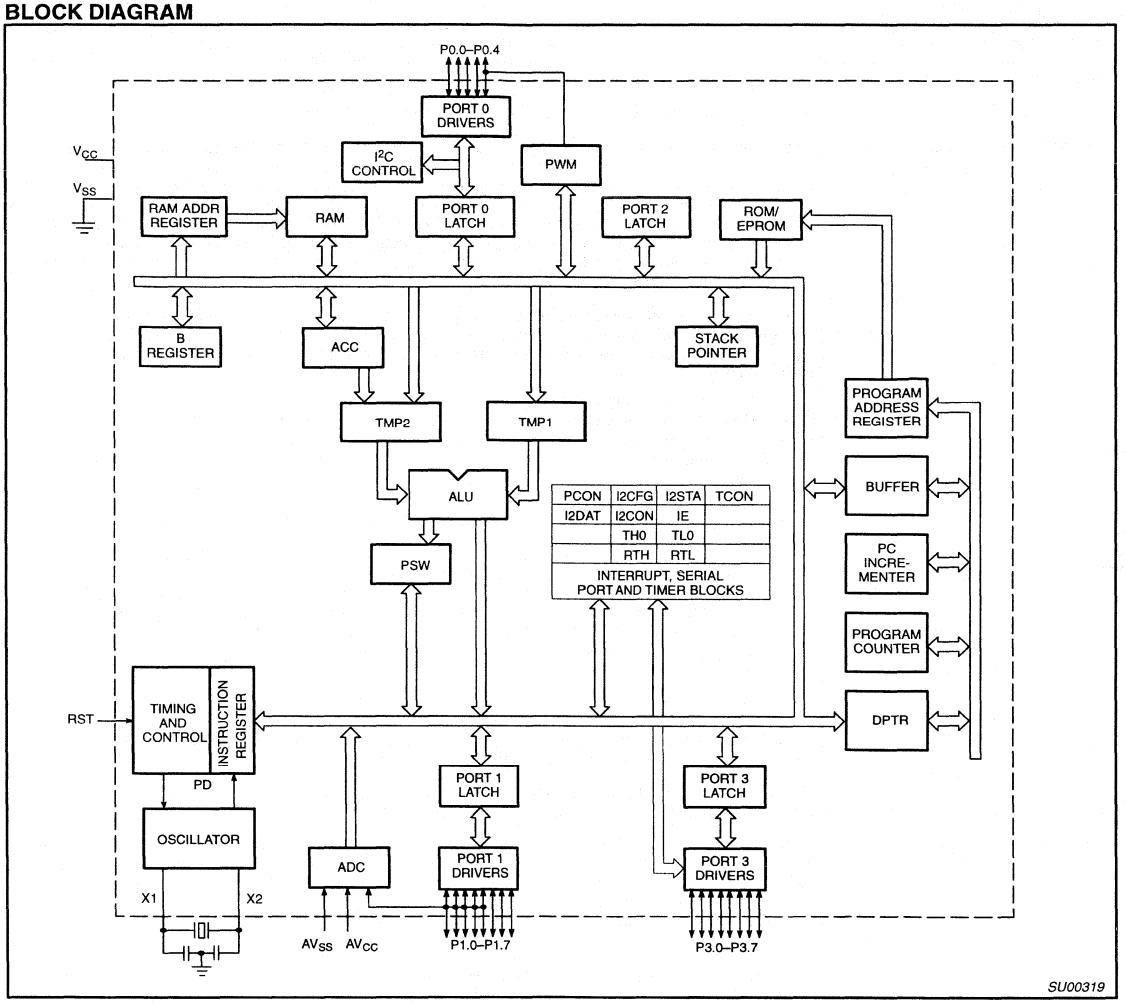
SU00318

PART NUMBER SELECTION

ROM	EPROM		TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY	DRAWING NUMBER
	S87C752–1F28	UV	0 to +70, 28-pin Ceramic Dual In-line Package	3.5 to 12MHz	0589B
	S87C752–2F28	UV	–40 to +85, 28-pin Ceramic Dual In-line Package	3.5 to 12MHz	0589B
	S87C752–4F28	UV	0 to +70, 28-pin Ceramic Dual In-line Package	3.5 to 16MHz	0589B
	S87C752–5F28	UV	–40 to +85, 28-pin Ceramic Dual In-line Package	3.5 to 16MHz	0589B
S83C752–1DB	S87C752–1DB	OTP	0 to +70, 28-pin Plastic Shrink Small Outline Package	3.5 to 12MHz	SOT341-1
S83C752–1N28	S87C752–1N28	OTP	0 to +70, 28-pin Plastic Dual In-line Package	3.5 to 12MHz	SOT117-2
S83C752–2N28	S87C752–2N28	OTP	–40 to +85, 28-pin Plastic Dual In-line Package	3.5 to 12MHz	SOT117-2
S83C752–4DB	S87C752–4DB	OTP	0 to +70, 28-pin Plastic Shrink Small Outline Package	3.5 to 12MHz	SOT341-1
S83C752–4N28	S87C752–4N28	OTP	0 to +70, 28-pin Plastic Dual In-line Package	3.5 to 16MHz	SOT117-2
S83C752–5N28	S87C752–5N28	OTP	–40 to +85, 28-pin Plastic Dual In-line Package	3.5 to 16MHz	SOT117-2
S83C752–1A28	S87C752–1A28	OTP	0 to +70, 28-pin Plastic Leaded Chip Carrier	3.5 to 12MHz	SOT261-3
S83C752–2A28	S87C752–2A28	OTP	–40 to +85, 28-pin Plastic Leaded Chip Carrier	3.5 to 12MHz	SOT261-3
S83C752–4A28	S87C752–4A28	OTP	0 to +70, 28-pin Plastic Leaded Chip Carrier	3.5 to 16MHz	SOT261-3
S83C752–5A28	S87C752–5A28	OTP	–40 to +85, 28-pin Plastic Leaded Chip Carrier	3.5 to 16MHz	SOT261-3
S83C752–6A28	S87C752–6A28	OTP	–55 to +125, 28-pin Plastic Leaded Chip Carrier	3.5 to 12MHz	SOT261-3
S83C752–6N28	S87C752–6N28	OTP	–55 to +125, 28-pin Plastic Dual In-line Package	3.5 to 12MHz	SOT117-2

NOTE:
1. OTP = One Time Programmable EPROM. UV = UV Erasable EPROM.

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
V_{SS}	12	I	**Circuit Ground Potential.**
V_{CC}	28	I	**Supply voltage during normal, idle, and power-down operation.**
P0.0–P0.4	8–6 23, 24	I/O	**Port 0:** Port 0 is a 5-bit bidirectional port. Port 0.0–P0.2 are open drain. Port 0.0–P0.2 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. P0.3–P0.4 are bidirectional I/O port pins with internal pull-ups. Port 0 also serves as the serial I^2C interface. When this feature is activated by software, SCL and SDA are driven low in accordance with the I^2C protocol. These pins are driven low if the port register bit is written with a 0 or if the I^2C subsystem presents a 0. The state of the pin can always be read from the port register by the program. Port 0.3 and 0.4 have internal pull-ups that function identically to port 3. Pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. To comply with the I^2C specification, P0.0 and P0.1 are open drain bidirectional I/O pins with the electrical characteristics listed in the tables that follow. While these differ from "standard TTL" characteristics, they are close enough for the pins to still be used as general-purpose I/O in non-I^2C applications.
	6	I	**V_{PP} (P0.2)** – Programming voltage input.
	7	I	**OE/PGM (P0.1)** – Input which specifies verify mode (output enable) or the program mode. OE/PGM = 1 output enabled (verify mode). OE/PGM = 0 program mode.
	8	I	**ASEL (P0.0)** – Input which indicates which bits of the EPROM address are applied to port 3. ASEL = 0 low address byte available on port 3. ASEL = 1 high address byte available on port 3 (only the three least significant bits are used).
P1.0–P1.7	13–17, 20–22	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. P0.3–P0.4 pins are bidirectional I/O port pins with internal pull-ups. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 also serves the special function features of the SC80C51 family as listed below:
	20	I	**$\overline{INT0}$ (P1.5):** External interrupt.
	21	I	**$\overline{INT1}$ (P1.6):** External interrupt.
	22	I	**T0 (P1.7):** Timer 0 external input.
	13–17	I	**ADC0 (P1.0)–ADC4 (P1.4):** Port 1 also functions as the inputs to the five channel multiplexed A/D converter. These pins can be used as outputs only if the A/D function has been disabled. These pins can be used as inputs while the A/D converter is enabled. Port 1 serves to output the addressed EPROM contents in the verify mode and accepts as inputs the value to program into the selected address during the program mode.
P3.0–P3.7	5–1, 27–25	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also functions as the address input for the EPROM memory location to be programmed (or verified). The 11-bit address is multiplexed into this port as specified by P0.0/ASEL.
RST	9	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits a power-on RESET using only an external capacitor to V_{CC}. After the device is reset, a 10-bit serial sequence, sent LSB first, applied to RESET, places the device in the programming state allowing programming address, data and V_{PP} to be applied for programming or verification purposes. The RESET serial sequence must be synchronized with the X1 input.
X1	11	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. X1 also serves as the clock to strobe in a serial bit stream into RESET to place the device in the programming state.
X2	10	O	**Crystal 2:** Output from the inverting oscillator amplifier.
AV_{CC} [1]	19	I	**Analog supply voltage and reference input.**
AV_{SS} [1]	18	I	**Analog supply and reference ground.**

NOTE:
1. AV_{SS} (reference ground) must be connected to 0V (ground). AV_{CC} (reference input) cannot differ from V_{CC} by more than ±0.2V, and must be in the range 4.5V to 5.5V.

OSCILLATOR CHARACTERISTICS

X1 and X2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, X1 should be driven while X2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

IDLE MODE

The 8XC752 includes the 80C51 power-down and idle mode features. In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals except the A/D and PWM stay active. The functions that continue to run while in the idle mode are Timer 0, the I^2C interface including Timer I, and the interrupts. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset. Upon powering-up the circuit, or exiting from idle mode, sufficient time must be allowed for stabilization of the internal analog reference voltages before an A/D conversion is started.

Special Function Registers

The special function registers (directly addressable only) contain all of the 8XC751 registers except the program counter and the four register banks. Most of the 21 special function registers are used to control the on-chip peripheral hardware. Other registers include arithmetic registers (ACC, B, PSW), stack pointer (SP) and data pointer registers (DPH, DPL). Nine of the SFRs are bit addressable.

Data Pointer

The data pointer (DPTR) consists of a high byte (DPH) and a low byte (DPL). In the 80C51 this register allows the access of external data memory using the MOVX instruction. Since the 83C752 does not support MOVX or external memory accesses, this register is generally used as a 16-bit offset pointer of the accumulator in a MOVC instruction. DPTR may also be manipulated as two independent 8-bit registers.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON.

Table 1. External Pin Status During Idle and Power-Down Modes

MODE	Port 0*	Port 1	Port 2
Idle	Data	Data	Data
Power-down	Data	Data	Data

* Except for PWM output (P0.4).

DIFFERENCES BETWEEN THE 8XC752 AND THE 80C51

Program Memory

On the 8XC752, program memory is 2048 bytes long and is not externally expandable, so the 80C51 instructions MOVX, LJMP, and LCALL are not implemented. If these instructions are executed, the appropriate number of instruction cycles will take place along with external fetches; however, no operation will take place. The LJMP may not respond to all program address bits. The only fixed locations in program memory are the addresses at which execution is taken up in response to reset and interrupts, which are as follows:

Event	Program Memory Address
Reset	000
External $\overline{INT0}$	003
Counter/timer 0	00B
External $\overline{INT1}$	013
Timer I	01B
I^2C serial	023
ADC	02B
PWM	033

Memory Organization

The 8XC752 manipulates operands in three memory address spaces. The first is the program memory space which contains program instructions as well as constants such as look-up tables. The program memory space contains 2k bytes in the 8XC752.

The second memory space is the data memory array which has a logical address space of 128 bytes. However, only the first 64 (0 to 3FH) are implemented in the 8XC752.

The third memory space is the special function register array having a 128-byte address space (80H to FFH). Only selected locations in this memory space are used (see Table 1). Note that the architecture of these memory spaces (internal program memory, internal data memory, and special function registers) is identical to the 80C51, and the 8XC752 varies only in the amount of memory physically implemented.

The 8XC752 does not directly address any external data or program memory spaces. For this reason, the MOVX instructions in the 80C51 instruction set are not implemented in the 83C752, nor are the alternate I/O pin functions $\overline{RD}$ and $\overline{WR}$.

I/O Ports

The I/O pins provided by the 83C752 consist of port 0, port 1, and port 3.

Port 0

Port 0 is a 5-bit bidirectional I/O port and includes alternate functions on some pins of this port. Pins P0.3 and P0.4 are provided with internal pullups while the remaining pins (P0.0, P0.1, and P0.2) have open drain output structures. The alternate functions for port 0 are:

P0.0 SCL – the I^2C bus clock
P0.1 SDA – the I^2C bus data
P0.4 PWM – the PWM output

If the alternate functions, I^2C and PWM, are not being used, then these pins may be used as I/O ports.

Port 1

Port 1 is an 8-bit bidirectional I/O port whose structure is identical to the 80C51, but also includes alternate input functions on all pins. The alternate pin functions for port 1 are:

P1.0-P1.4 - ADC0-ADC4 - A/D converter analog inputs
P1.5 $\overline{INT0}$ - external interrupt 0 input
P1.6 $\overline{INT1}$ - external interrupt 1 input
P1.7 - T0 - timer 0 external input

If the alternate functions $\overline{INT0}$, $\overline{INT1}$, or T0 are not being used, these pins may be used as standard I/O ports. It is necessary to connect AV_{CC} and AV_{SS} to V_{CC} and V_{SS}, respectively, in order to use these pins as standard I/O pins. When the A/D converter is enabled, the analog channel connected to the A/D may not be used as a digital input; however, the remaining analog inputs may be used as digital inputs. They may not be used as digital outputs. While the A/D is enabled, the analog inputs are floating.

Port 3

Port 3 is an 8-bit bidirectional I/O port whose structure is identical to the 80C51. Note that the alternate functions associated with port 3 of the 80C51 have been moved to port 1 of the 83C752 (as applicable). See Figure 1 for port bit configurations.

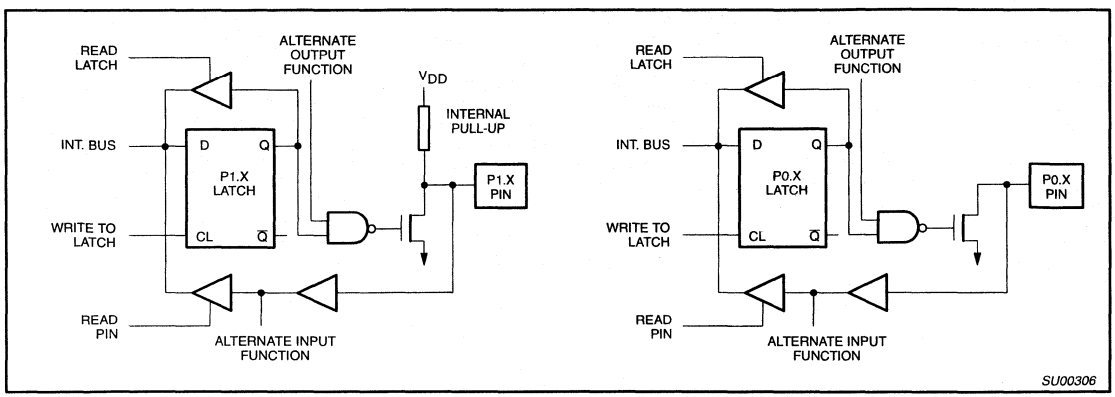


Figure 1. Port Bit Latches and I/O Buffers

Counter/Timer Subsystem

The 8XC752 has one counter/timer called timer/counter 0. Its operation is similar to mode 2 operation on the 80C51, but is extended to 16 bits with 16 bits of autoload. The controls for this counter are centralized in a single register called TCON.

A watchdog timer, called Timer I, is for use with the I²C subsystem. In I²C applications, this timer is dedicated to time-generation and bus monitoring of the I²C. In non-I²C applications, it is available for use as a fixed time-base.

Interrupt Subsystem—Fixed Priority

The IP register and the 2-level interrupt system of the 80C51 are eliminated. The interrupt structure is a seven-source, one-level interrupt system similar to the 8XC751. Simultaneous interrupt conditions are resolved by a single-level, fixed priority as follows:

Highest priority:	Pin $\overline{INT0}$
	Counter/timer flag 0
	Pin $\overline{INT1}$
	PWM
	Timer I
	Serial I²C
Lowest priority:	ADC

The vector addresses are as follows:

Source	Vector Address
INT0	0003H
TF0	000BH
INT1	0013H
TIMER I	001BH
SIO	0023H
ADC	002BH
PWM	0033H

Interrupt Control Registers

The 80C51 interrupt enable register is modified to take into account the different interrupt sources of the 8XC752.

Interrupt Enable Register

MSB LSB

EA	EAD	ETI	ES	EPWM	EX1	ET0	EX0

Position	Symbol	Function
IE.7	EA	Global interrupt disable when EA = 0
IE.6	EAD	A/D conversion complete
IE.5	ETI	Timer I
IE.4	ES	I²C serial port
IE.3	EPWM	PWM counter overflow
IE.2	EX1	External interrupt 1
IE.1	ET0	Timer 0 overflow
IE.0	EX0	External interrupt 0

Serial Communications

The 8XC752 contains an I²C serial communications port instead of the 80C51 UART. The I²C serial port is a single bit hardware interface with all of the hardware necessary to support multimaster and slave operations. Also included are receiver digital filters and timer (timer I) for communication watch-dog purposes. The I²C serial port is controlled through four special function registers; I²C control, I²C data, I²C status, and I²C configuration.

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main technical features of the bus are:

- Bidirectional data transfer between masters and slaves
- Serial addressing of slaves
- Acknowledgment after each transferred byte
- Multimaster bus
- Arbitration between simultaneously transmitting master without corruption of serial data on bus
- With 82B715, communication distance is extended to beyond 100 feet (30M)

A large family of I²C compatible ICs is available. See the I²C section for more details on the bus and available ICs.

The 83C752 I²C subsystem includes hardware to simplify the software required to drive the I²C bus. This circuitry is the same as that on the 83C751. (See the 83C751 section for a detailed discussion of this subsystem).

Pulse Width Modulation Output (P0.4)

The PWM outputs pulses of programmable length and interval. The repetition frequency is defined by an 8-bit prescaler which generates the clock for the counter. The prescaler register is PWMP. The prescaler and counter are not associated with any other timer. The 8-bit counter counts modulo 255, that is from 0 to 254 inclusive. The value of the 8-bit counter is compared to the contents of a compare register, PWM. When the counter value matches the contents of this register, the output of the PWM is set high. When the counter reaches zero, the output of the PWM is set low. The pulse width ratio (duty cycle) is defined by the contents of the compare register and is in the range of 0 to 1 programmed in increments of 1/255. The PWM output can be set to be continuously high by loading the compare register with 0 and the output can be set to be continuously low by loading the compare register with 255. The PWM output is enabled by a bit in a special function register, PWENA. When enabled, the pin output is driven with a fully active pull-up. That is, when the output is high, a strong pull-up is continuously applied. when disabled, the pin functions as a normal bidirectional I/O pin, however, the counter remains active.

The PWM function is disabled during RESET and remains disabled after reset is removed until re-enabled by software. The PWM output is high during power down and idle. The counter is disabled during idle. The repetition frequency of the PWM is given by:

$f_{PWM} = f_{OSC} / 2 (1 + PWMP) 255$

The low/high ratio of the PWM signal is PWM / (255 – PWM) for PWM not equal to 255. For PWM = 255, the output is always low.

The repetition frequency range is 92Hz to 23.5kHz for an oscillator frequency of 12MHz.

An interrupt will be asserted upon PWM counter overflow if the interrupt is not masked off.

The PWM output is an alternative function of P0.4. In order to use this port as a bidirectional I/O port, the PWM output must be disabled by clearing the enable/disable bit in PWENA. In this case, the PWM subsystem can be used as an interval timer by enabling the PWM interrupt.

Table 1. 8XC752 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB							LSB	RESET VALUE
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
ADAT#	A/D result	84H									00H
ADCON#	A/D control	A0H	–	–	ENADC	ADCI	ADCS	AADR2	AADR1	AADR0	C0H
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR:	Data pointer (2 bytes)										
DPL	Data pointer low	82H									00H
DPH	Data pointer high	83H									00H
			DF	DE	DD	DC	DB	DA	D9	D8	
I²CFG*#	I²C configuration	D8H/RD	SLAVEN	MASTRQ	0	TIRUN	–	–	CT1	CT0	0000xx00B
		WR	SLAVEN	MASTRQ	CLRTI	TIRUN	–	–	CT1	CT0	
			9F	9E	9D	9C	9B	9A	99	98	
I²CON*#	I²C control	98H/RD	RDAT	ATN	DRDY	ARL	STR	STP	MASTER	–	81H
		WR	CXA	IDLE	CDR	CARL	CSTR	CSTP	XSTR	XSTP	
I²DAT*#	I²C data	99H/RD	RDAT	0	0	0	0	0	0	0	80H
		WR	XDAT	X	X	X	X	X	X	X	
			FF	FE	FD	FC	FB	FA	F9	F8	
I²STA*#	I²C status	F8H	–	IDLE	XDATA	XACTV	MAKSTR	MAKSTP	XSTR	XSTP	x0100000B
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*#	Interrupt enable	A8H	EA	EAD	ETI	ES	EPWM	EX1	ET0	EX0	00H
			–	–	–	84	83	82	81	80	xxx11111B
P0*#	Port 0	80H	–	–	–	PWM0	–	–	SDA	SCL	
			97	96	95	94	93	92	91	90	FFH
P1*#	Port 1	90H	T0	$\overline{INT1}$	INT0	ADC4	ADC3	ADC2	ADC1	ADC0	
P3*	Port 3	B0H	B7	B6	B5	B4	B3	B2	B1	B0	FFH
PCON#	Power control	87H	–	–	–	–	–	–	PD	IDL	xxxx0000B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	00H
PWCM#	PWM compare	8EH									xxxxxxxxB
PWENA#	PWM enable	FEH	–	–	–	–	–	–	–	PWE	FEH
PWMP#	PWM prescaler	8FH									00H
RTL#	Timer low reload	8BH									00H
RTH#	Timer high reload	8DH									00H
SP	Stack pointer	81H									07H
TL#	Timer low	8AH									00H
TH#	Timer high	8CH									00H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*#	Timer control	88H	GATE	C/T	TF	TR	IE0	IT0	IE1	IT1	00H

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.

Special Function Register Addresses

Special function registers for the 8XC752 are identical to those of the 80C51, except for the changes listed below:

80C51 special function registers not present in the 8XC752 are TMOD (89), P2 (A0) and IP (B8). The 80C51 registers TH1, TL1, SCON, and SBUF are replaced with the 8XC752 registers RTH, RTL, I2CON, and I2DAT, respectively. Additional special function registers are I2CFG (D8) and I2STA (FB), ADCON (A0), ADAT (84), PWM (8E), PWMP (8F), and PWENA (FE). See Table 2.

A/D Converter

The analog input circuitry consists of a 5-input analog multiplexer and an A to D converter with 8-bit resolution. The conversion takes 40 machine cycles, i.e., 40µs at 12MHz oscillator frequency. The A/D converter is controlled using the ADCON control register. Input channels are selected by the analog multiplexer through ADCON register bits 0–2.

The 83C752 contains a five-channel multiplexed 8-bit A/D converter. The conversion requires 40 machine cycles (40µs at 12MHz oscillator frequency).

The A/D converter is controlled by the A/D control register, ADCON. Input channels are selected by the analog multiplexer by bits ADCON.0 through ADCON.2. The ADCON register is not bit addressable.

ADCON Register

MSB LSB

X	X	ENADC	ADCI	ADCS	AADR2	AADR1	AADR0

ADCI	ADCS	Operation
0	0	ADC not busy, a conversion can be started.
0	1	ADC busy, start of a new conversion is blocked.
1	0	Conversion completed, start of a new conversion is blocked.
1	1	Not possible.

INPUT CHANNEL SELECTION			
ADDR2	ADDR1	ADDR0	INPUT PIN
0	0	0	P1.0
0	0	1	P1.1
0	1	0	P1.2
0	1	1	P1.3
1	0	0	P1.4

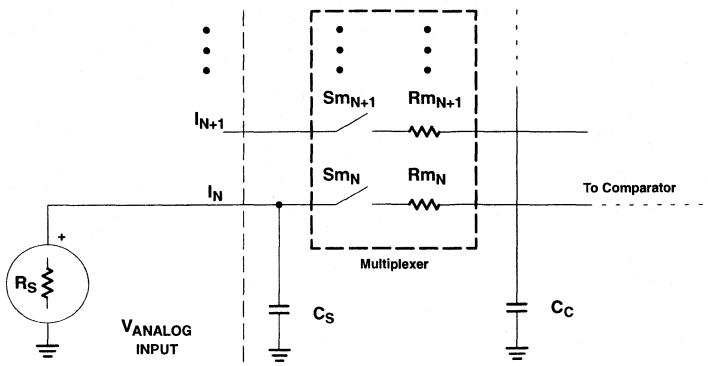
Position	Symbol	Function
ADCON.5	ENADC	Enable A/D function when ENADC = 1. Reset forces ENADC = 0.
ADCON.4	ADCI	ADC interrupt flag. This flag is set when an ADC conversion is complete. If IE.6 = 1, an interrupt is requested when ADCI = 1. The ADCI flag is cleared when conversion data is read. This flag is read only.
ADCON.3	ADCS	ADC start. Setting this bit starts an A/D conversion. Once set, ADCS remains high throughout the conversion cycle. On completion of the conversion, it is reset just before the ADCI interrupt flag is cleared. ADCS cannot be reset by software. ADCS should not be used to monitor the A/D converter status. ADCI should be used for this purpose.
ADCON.2	AADR2	Analog input select.
ADCON.1	AADR1	Analog input select.
ADCON.0	AADR0	Analog input select. This binary coded address selects one of the five analog input port pins of P1 to be input to the converter. It can only be changed when ADCI and ADCS are both low. AADR2 is the most significant bit.

The completion of the 8-bit ADC conversion is flagged by ADCI in the ADCON register, and the result is stored in the special function register ADAT.

An ADC conversion in progress is unaffected by an ADC start. The result of a completed conversion remains unaffected provided ADCI remains at a logic 1. While ADCS is a logic 1 or ADCI is a logic 1, a new ADC START will be blocked and consequently lost. An ADC conversion in progress is aborted when the idle or power-down mode is entered. The result of a completed conversion (ADCI = logic 1) remains unaffected when entering the idle mode. See Figure 2 for an A/D input equivalent circuit.

The analog input pins ADC0-ADC4 may be used as digital inputs and outputs when the A/D converter is disabled by a 0 in the ENADC bit in ADCON. When the A/D is enabled, the analog input channel that is selected by the ADDR2-ADDR0 bits in ADCON cannot be used as a digital input. Reading the selected A/D channel as a digital input will always return a 1. The unselected A/D inputs may always be used as digital inputs. Unselected analog inputs will be floating and may not be used as digital outputs.

The A/D reference inputs on the 8XC752 are tied together with the analog supply pins AV_{CC} and AV_{SS}. This means that the reference voltage on the A/D cannot be varied separately from the analog supply pins. AV_{SS} must be connected to 0V and AV_{CC} must be connected to a supply voltage between 4.5V and 5.5V. A/D measurements may be made in the range of 4.5V to 5.5V. Increasing the voltage on the A/D ground reference above 0V or reducing the voltage on the positive A/D reference below 4.5V is not permitted.



Rm = 0.5 - 3 kΩ
CS + CC = 15pF maximum
RS = Recommended < 9.6 kΩ for 1 LSB @ 12MHz

NOTE:
Because the analog to digital converter has a sampled-data comparator, the input looks capacitive to a source. When a conversion is initiated, switch Sm closes for 8tcy (8μs @ 12MHz crystal frequency) during which time capacitance Cs + Cc is charged. It should be noted that the sampling causes the analog input to present a varying load to an analog source.

SU00199

Figure 2. A/D Input: Equivalent Circuit

A/D CONVERTER PARAMETER DEFINITIONS

The following definitions are included to clarify some specifications given and do not represent a complete set of A/D parameter definitions.

Absolute Accuracy Error

Absolute accuracy error of a given output is the difference between the theoretical analog input voltage to produce a given output and the actual analog input voltage required to produce the same code. Since the same output code is produced by a band of input voltages, the "required input voltage" is defined as the midpoint of the band of input voltage that will produce that code. Absolute accuracy error not specified with a code is the maximum over all codes.

Nonlinearity

If a straight line is drawn between the end points of the actual converter characteristics such that zero offset and full scale errors are removed, then non-linearity is the maximum deviation of the code transitions of the actual characteristics from that of the straight line so constructed. This is also referred to as relative accuracy and also integral non-linearity.

Differential Non-Linearity

Differential non-linearity is the maximum difference between the actual and ideal code widths of the converter. The code widths are the differences expressed in LSB between the code transition points, as the input voltage is varied through the range for the complete set of codes.

Gain Error

Gain error is the deviation between the ideal and actual analog input voltage required to cause the final code transition to a full-scale output code after the offset error has been removed. This may sometimes be referred to as full scale error.

Offset Error

Offset error is the difference between the actual input voltage that causes the first code transition and the ideal value to cause the first code transition. This ideal value is 1/2 LSB above V_{ref-}.

Channel to Channel Matching

Channel to channel matching is the maximum difference between the corresponding code transitions of the actual characteristics taken from different channels under the same temperature, voltage and frequency conditions.

Crosstalk

Crosstalk is the measured level of a signal at the output of the converter resulting from a signal applied to one deselected channel.

Total Error

Maximum deviation of any step point from a line connecting the ideal first transition point to the ideal last transition point.

Relative Accuracy

Relative accuracy error is the deviation of the ADC's actual code transition points from the ideal code transition points on a straight line which connects the ideal first code transition point and the final code transition point, after nullifying offset error and gain error. It is generally expressed in LSBs or in percent of FSR.

COUNTER/TIMER

The 8XC752 counter/timer is designated Timer 0 and is separate from Timer I of the I²C serial port and from the PWM. Its operation is similar to mode 2 of the 80C51 counter/timer, extended to 16 bits. When Timer 0 is used in the external counter mode, the T0 input (P1.7) is sampled every S4P1. The counter/timer function is controlled using the timer control register (TCON).

TCON Register

MSB LSB

GATE	C/T	TF	TR	IE0	IT0	IE1	IT1

Position	Symbol	Function
TCON.7	GATE	1 – Timer 0 is enabled only when INT0 pin is high and TR is 1. 0 – Timer 0 is enabled only when TR is 1.
TCON.6	C/T	1 – Counter operation from T0 pin. 0 – Timer operation from internal clock.
TCON.5	TF	1 – Set on overflow of T0. 0 – Cleared when processor vectors to interrupt routine and by reset.
TCON.4	TR	1 – Enable timer 0 0 – Disable timer 0
TCON.3	IE0	1 – Edge detected on INT0
TCON.2	IT0	1 – INT0 is edge triggered. 0 – INT0 is level sensitive.
TCON.1	IE1	1 – Edge detected on INT1
TCON.0	IT1	1 – INT1 is edge triggered. 0 – INT1 is level sensitive.

These flags are functionally identical to the corresponding 80C51 flags except that there is only one of the 80C51 style timers, and the flags are combined into one register.

Note that the positions of the IE0/IT0 and IE1/IT1 bits are transposed from the positions used in the standard 80C51 TCON register.

A communications watchdog timer, Timer I, is described in the I²C section. In I²C applications, this timer is dedicated to time generation and bus monitoring for the I²C. In non-I²C applications, it is available for use as a fixed time base.

The 16-bit timer/counter's operation is similar to mode 2 operation on the 80C51, but is extended to 16 bits. The timer/counter is clocked by either 1/12 the oscillator frequency or by transitions on the T0 pin. The C/T pin in special function register TCON selects between these two modes. When the TCON TR bit is set, the timer/counter is enabled. Register pair TH and TL are incremented by the clock source. When the register pair overflows, the register pair is reloaded with the values in registers RTH and RTL. The value in the reload registers is left unchanged. The TF bit in special function register TCON is set on counter overflow and, if the interrupt is enabled, will generate an interrupt (see Figure 3).

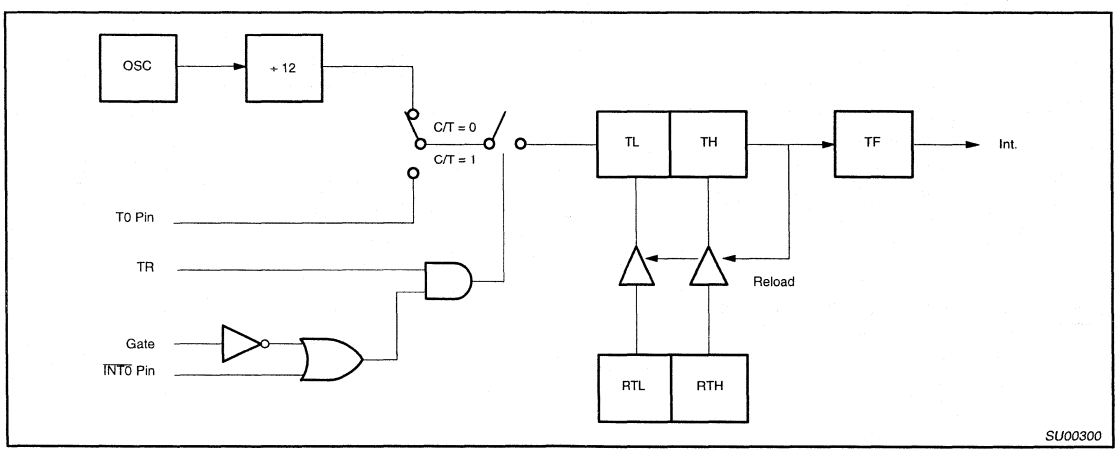


Figure 3. 83C752 Counter/Timer Block Diagram

Table 2. I²C Special Function Register Addresses

REGISTER ADDRESS			BIT ADDRESS							
NAME	SYMBOL	ADDRESS	MSB							LSB
I²C control	I2CON	98	9F	9E	9D	9C	9B	9A	99	98
I²C data	I2DAT	99	–	–	–	–	–	–	–	–
I²C configuration	I2CFG	D8	DF	DE	DD	DC	DB	DA	D9	D8
I²C status	I2STA	F8	FF	FE	FD	FC	FB	FA	F9	F8

ABSOLUTE MAXIMUM RATINGS[1, 3, 4]

PARAMETER	RATING	UNIT
Storage temperature range	–65 to +150	°C
Voltage from V_{CC} to V_{SS}	–0.5 to +6.5	V
Voltage from any pin to V_{SS} (except V_{PP})	–0.5 to V_{CC} + 0.5	V
Power dissipation	1.0	W
Voltage from V_{PP} pin to V_{SS}	–0.5 to + 13.0	V

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or –40°C to +85°C, AV_{CC} = 5V ±5, AV_{SS} = 0V[4]
V_{CC} = 5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS[4] MIN	Typical[1]	MAX	UNIT
I_{CC}	Supply current (see Figure 6)					
Inputs						
V_{IL}	Input low voltage, except SDA, SCL	(0 to 70°C) (–40 to +85°C)	–0.5 –0.5		$0.2V_{CC}$–0.1 $0.2V_{CC}$–0.15	V V
V_{IH}	Input high voltage, except X1, RST	(0 to 70°C) ($0.2V_{CC}$+1)	$0.2V_{CC}$+0.9 (–40 to +85°C)		V_{CC}+0.5 V_{CC}+0.5	V V
V_{IH1}	Input high voltage, X1, RST	(0 to 70°C) (–40 to +85°C)	$0.7V_{CC}$ $0.7V_{CC}$ to 0.1		V_{CC}+0.5 V_{CC}+0.5	V V
	SDA, SCL, P0.2					
V_{IL1}	Input low voltage	(0 to 70°C) (–40 to +85°C)	–0.5 –0.5		$0.3V_{CC}$ $0.3V_{CC}$–0.1	V V
V_{IH2}	Input high voltage	(0 to 70°C) (–40 to –85°C)	$0.7V_{CC}$ $0.7V_{CC}$+0.1		V_{CC}+0.5 V_{CC}+0.5	V
Outputs						
V_{OL}	Output low voltage, ports 1, 3, 0.3, and 0.4 (PWM disabled)	I_{OL} = 1.6mA[2]			0.45	V
V_{OL1}	Output low voltage, port 0.2	I_{OL} = 3.2mA[2]			0.45	V
V_{OH}	Output high voltage, ports 1, 3, 0.3, and 0.4 (PWM disabled)	I_{OH} = –60µA, I_{OH} = –25µA I_{OH} = –10µA I_{OH} = –400µA	2.4 $0.75V_{CC}$ $0.9V_{CC}$ 2.4			V V V V
V_{OH2}	Output high voltage, P0.4 (PWM enabled)	I_{OH} = –40µA	$0.9V_{CC}$			V
V_{OL2}	Port 0.0 and 0.1 (I^2C) – Drivers Output low voltage	I_{OL} = 3mA (over V_{CC} range)			0.4	V
C	Driver, receiver combined: Capacitance				10	pF
I_{IL}	Logical 0 input current, ports 1, 3, 0.3, and 0.4 (PWM disabled)[11]	V_{IN} = 0.45V (0 to 70°C) V_{IN} = 0.45V (0 to +85°C)			–50 –75	µA µA
I_{TL}	Logical 1 to 0 transition current, ports 1, 3, 0.3 and 0.4[11]	V_{IN} = 2V (0 to 70°C) V_{IN} = 2V (–40 to +85°C)			–650 –750	µA µA
I_{LI}	Input leakage current, port 0.0, 0.1 and 0.2	0.45 < V_{IN} < V_{CC}			±10	µA
R_{RST}	Reset pull-down resistor		25		175	kΩ
C_{IO}	Pin capacitance	Test freq = 1MHz, T_{amb} = 25°C			10	pF
I_{PD}	Power-down current[5]	V_{CC} = 2 to 5.5V V_{CC} = 2 to 6.0V (83C752)			50	µA
V_{PP}	V_{PP} program voltage (87C752 only)	V_{SS} = 0V V_{CC} = 5V±10% T_{amb} = 21°C to 27°C	12.5		13.0	V
I_{PP}	Program current (87C752 only)	V_{PP} = 13.0V			50	mA

DC ELECTRICAL CHARACTERISTICS (Continued)

T_{amb} = 0°C to +70°C or −40°C to +85°C, AV_{CC} = 5V ±5, AV_{SS} = 0V[4]
V_{CC} = 5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS[4]			UNIT
			MIN	Typical[1]	MAX	
Analog Inputs (A/D guaranteed only with quartz window covered.)						
AV_{CC}	Analog supply voltage[10]	$AV_{CC} = V_{CC}$±0.2V	4.5		5.5	V
AI_{CC}	Analog operating supply current	AV_{CC} = 5.12V			3[9]	mA
AV_{IN}	Analog input voltage		AV_{SS}–0.2		AV_{CC}+0.2	V
C_{IA}	Analog input capacitance				15	pF
t_{ADS}	Sampling time				$8t_{CY}$	s
t_{ADC}	Conversion time				$40t_{CY}$	s
R	Resolution				8	bits
E_{RA}	Relative accuracy				±1	LSB
OS_e	Zero scale offset				±1	LSB
G_e	Full scale gain error				0.4	%
M_{CTC}	Channel to channel matching				±1	LSB
C_t	Crosstalk	0–100kHz			–60	dB

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10mA (NOTE: This is 85°C spec.)
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum total I_{OL} for all outputs: 67mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
5. Power-down I_{CC} is measured with all output pins disconnected; port 0 = V_{CC}; X2, X1 n.c.; RST = V_{SS}.
6. I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = 5ns, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; X2 n.c.; RST = port 0 = V_{CC}. I_{CC} will be slightly higher if a crystal oscillator is used.
7. Idle I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = 5ns, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; X2 n.c.; port 0 = V_{CC}; RST = V_{SS}.
8. Load capacitance for ports = 80pF.
9. The resistor ladder network is not disconnected in the power down or idle modes. Thus, to conserve power, the user may remove AV_{CC}.
10. If the A/D function is not required, or if the A/D function is only needed periodically, AV_{CC} may be removed without affecting the operation of the digital circuitry. Contents of ADCON and ADAT are not guaranteed to be valid. If AV_{CC} is removed, the A/D inputs must be lowered to less than 0.5V. Digital inputs on P1.0–P1.4 will not function normally.
11. These parameters do not apply to P1.0–P1.4 if the A/D function is enabled.

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V[4, 8]

SYMBOL	PARAMETER	12MHz CLOCK		VARIABLE CLOCK		UNIT
		MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	Oscillator frequency:			3.5 3.5	12 16	MHz MHz
External Clock (Figure 4)						
t_{CHCX}	High time	20		20		ns
t_{CLCX}	Low time	20		20		ns
t_{CLCH}	Rise time		20		20	ns
t_{CHCL}	Fall time		20		20	ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

C – Clock
D – Input data
H – Logic level high
L – Logic level low
Q – Output data
T – Time
V – Valid
X – No longer a valid logic level
Z – Float

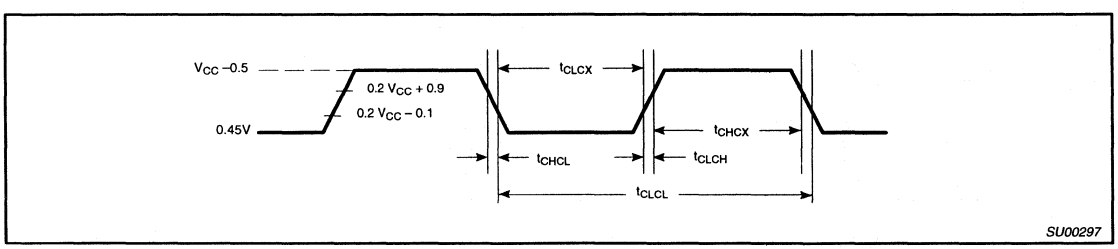


Figure 4. External Clock Drive

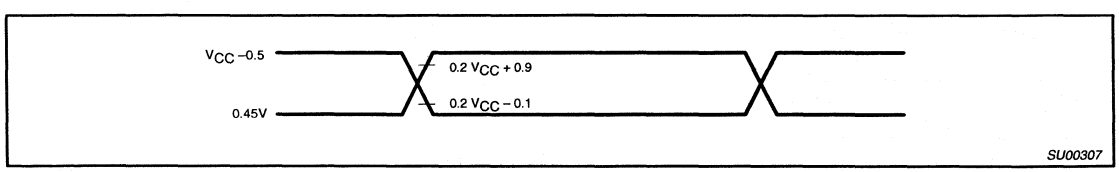


Figure 5. AC Testing Input/Output

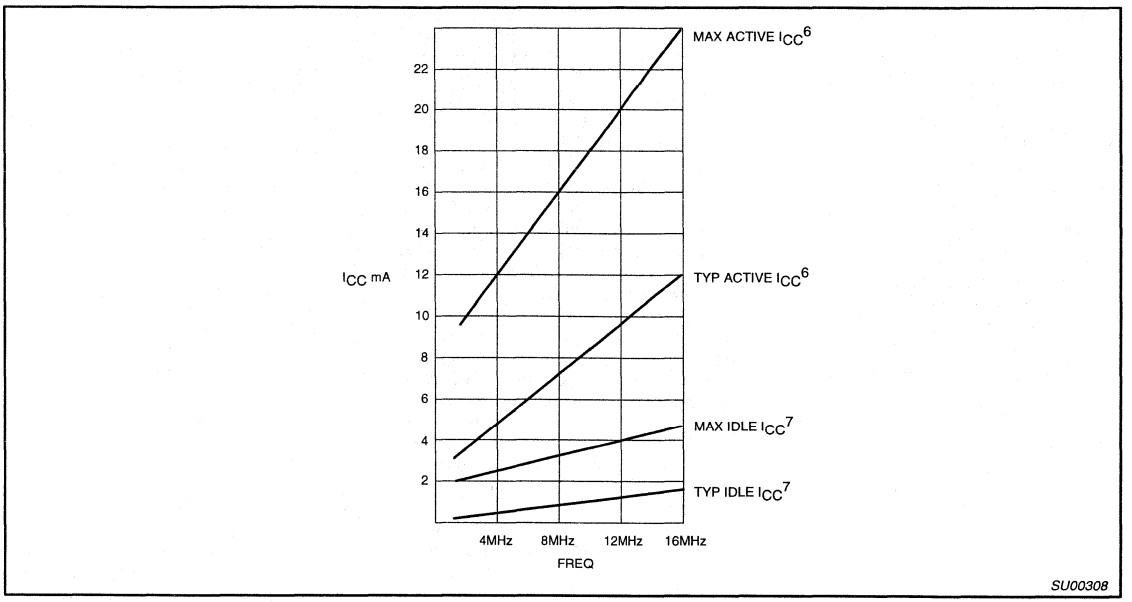


Figure 6. I_{CC} vs. FREQ
Maximum I_{CC} values taken at V_{CC} = 5.5V and worst case temperature.
Typical I_{CC} values taken at V_{CC} = 5.0V and 25°C.
Notes 6 and 7 refer to AC Electrical Characteristics.

PROGRAMMING CONSIDERATIONS

EPROM Characteristics

The 87C752 is programmed by using a modified Quick-Pulse Programming algorithm similar to that used for devices such as the 87C451 and 87C51. It differs from these devices in that a serial data stream is used to place the 87C752 in the programming mode.

Figure 7 shows a block diagram of the programming configuration for the 87C752. Port pin P0.2 is used as the programming voltage supply input (V_{PP} signal). Port pin P0.1 is used as the program (PGM/) signal. This pin is used for the 25 programming pulses.

Port 3 is used as the address input for the byte to be programmed and accepts both the high and low components of the eleven bit address. Multiplexing of these address components is performed using the ASEL input. The user should drive the ASEL input high and then drive port 3 with the high order bits of the address. ASEL should remain high for at least 13 clock cycles. ASEL may then be driven low which latches the high order bits of the address internally. The high address should remain on port 3 for at least two clock cycles after ASEL is driven low. Port 3 may then be driven with the low byte of the address. The low address will be internally stable 13 clock cycles later. The address will remain stable provided that the low byte placed on port 3 is held stable and ASEL is kept low. **Note:** ASEL needs to be pulsed high only to change the high byte of the address.

Port 1 is used as a bidirectional data bus during programming and verify operations. During programming mode, it accepts the byte to be programmed. During verify mode, it provides the contents of the EPROM location specified by the address which has been supplied to Port 3.

The XTAL1 pin is the oscillator input and receives the master system clock. This clock should be between 1.2 and 6MHz.

The RESET pin is used to accept the serial data stream that places the 87C752 into various programming modes. This pattern consists of a 10-bit code with the LSB sent first. Each bit is synchronized to the clock input, X1.

Programming Operation

Figures 8 and 9 show the timing diagrams for the program/verify cycle. RESET should initially be held high for at least two machine cycles. P0.1 (PGM/) and P0.2 (V_{PP}) will be at V_{OH} as a result of the RESET operation. At this point, these pins function as normal quasi-bidirectional I/O ports and the programming equipment may pull these lines low. However, prior to sending the 10-bit code on the RESET pin, the programming equipment should drive these pins high (V_{IH}). The RESET pin may now be used as the serial data input for the data stream which places the 87C752 in the programming mode. Data bits are sampled during the clock high time and thus should only change during the time that the clock is low. Following transmission of the last data bit, the RESET pin should be held low.

Next the address information for the location to be programmed is placed on port 3 and ASEL is used to perform the address multiplexing, as previously described. At this time, port 1 functions as an output.

A high voltage V_{PP} level is then applied to the V_{PP} input (P0.2). (This sets Port 1 as an input port). The data to be programmed into the EPROM array is then placed on Port 1. This is followed by a series of programming pulses applied to the PGM/ pin (P0.1). These pulses are created by driving P0.1 low and then high. This pulse is repeated until a total of 25 programming pulses have occurred. At the conclusion of the last pulse, the PGM/ signal should remain high.

The V_{PP} signal may now be driven to the V_{OH} level, placing the 87C752 in the verify mode. (Port 1 is now used as an output port). After four machine cycles (48 clock periods), the contents of the addressed location in the EPROM array will appear on Port 1.

The next programming cycle may now be initiated by placing the address information at the inputs of the multiplexed buffers, driving the V_{PP} pin to the V_{PP} voltage level, providing the byte to be programmed to Port1 and issuing the 26 programming pulses on the PGM/ pin, bringing V_{PP} back down to the V_C level and verifying the byte.

Programming Modes

The 87C752 has four programming features incorporated within its EPROM array. These include the USER EPROM for storage of the application's code, a 16-byte encryption key array and two security bits. Programming and verification of these four elements are selected by a combination of the serial data stream applied to the RESET pin and the voltage levels applied to port pins P0.1 and P0.2. The various combinations are shown in Table 3.

Encryption Key Table

The 87C752 includes a 16-byte EPROM array that is programmable by the end user. The contents of this array can then be used to encrypt the program memory contents during a program memory verify operation. When a program memory verify operation is performed, the contents of the program memory location is XNOR'ed with one of the bytes in the 16-byte encryption table. The resulting data pattern is then provided to port 1 as the verify data. The encryption mechanism can be disable, in essence, by leaving the bytes in the encryption table in their erased state (FFH) since the XNOR product of a bit with a logical one will result in the original bit. The encryption bytes are mapped with the code memory in 16-byte groups. the first byte in code memory will be encrypted with the first byte in the encryption table; the second byte in code memory will be encrypted with the second byte in the encryption table and so forth up to and including the 16the byte. The encryption repeats in 16-byte groups; the 17th byte in the code memory will be encrypted with the first byte in the encryption table, and so forth.

Security Bits

Two security bits, security bit 1 and security bit 2, are provided to limit access to the USER EPROM and encryption key arrays. Security bit 1 is the program inhibit bit, and once programmed performs the following functions:

1. Additional programming of the USER EPROM is inhibited.
2. Additional programming of the encryption key is inhibited.
3. Verification of the encryption key is inhibited.
4. Verification of the USER EPROM and the security bit levels may still be performed.

(If the encryption key array is being used, this security bit should be programmed by the user to prevent unauthorized parties from reprogramming the encryption key to all logical zero bits. Such programming would provide data during a verify cycle that is the logical complement of the USER EPROM contents).

Security bit 2, the verify inhibit bit, prevents verification of both the USER EPROM array and the encryption key arrays. The security bit levels may still be verified.

Programming and Verifying Security Bits

Security bits are programmed employing the same techniques used to program the USER EPROM and KEY arrays using serial data streams and logic levels on port pins indicated in Table 3. When programming either security bit, it is not necessary to provide address or data information to the 87C752 on ports 1 and 3.

Verification occurs in a similar manner using the RESET serial stream shown in Table 3. Port 3 is not required to be driven and the results of the verify operation will appear on ports 1.6 and 1.7.

Ports 1.7 contains the security bit 1 data and is a logical one if programmed and a logical zero if erased. Likewise, P1.6 contains the security bit 2 data and is a logical one if programmed and a logical zero if erased.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Flourless part number 2345–5 or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000uW/cm^2 rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Table 3. Implementing Program/Verify Modes

OPERATION	SERIAL CODE	P0.1 (PGM/)	P0.2 (V_{PP})
Program user EPROM	296H	–*	V_{PP}
Verify user EPROM	296H	V_{IH}	V_{IH}
Program key EPROM	292H	–*	V_{PP}
Verify key EPROM	292H	V_{IH}	V_{IH}
Program security bit 1	29AH	–*	V_{PP}
Program security bit 2	298H	–*	V_{PP}
Verify security bits	29AH	V_{IH}	V_{IH}

NOTE:
* Pulsed from V_{IH} to V_{IL} and returned to V_{IH}.

EPROM PROGRAMMING AND VERIFICATION

T_{amb} = 21°C to +27°C, V_{CC} = 5V ±10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	MAX	UNIT
$1/t_{CLCL}$	Oscillator/clock frequency	1.2	6	MHz
t_{AVGL}[1]	Address setup to P0.1 (PROG–) low	10µs + $24t_{CLCL}$		
t_{GHAX}	Address hold after P0.1 (PROG–) high	$48t_{CLCL}$		
t_{DVGL}	Data setup to P0.1 (PROG–) low	$38t_{CLCL}$		
t_{DVGL}	Data setup to P0.1 (PROG–) low	$38t_{CLCL}$		
t_{GHDX}	Data hold after P0.1 (PROG–) high	$36t_{CLCL}$		
t_{SHGL}	V_{PP} setup to P0.1 (PROG–) low	10		µs
t_{GHSL}	V_{PP} hold after P0.1 (PROG–)	10		µs
t_{GLGH}	P0.1 (PROG–) width	90	110	µs
t_{AVQV}[2]	V_{PP} low (V_{CC}) to data valid		$48t_{CLCL}$	
t_{GHGL}	P0.1 (PROG–) high to P0.1 (PROG–) low	10		µs
t_{SYNL}	P0.0 (sync pulse) low	$4t_{CLCL}$		
t_{SYNH}	P0.0 (sync pulse) high	$8t_{CLCL}$		
t_{MASEL}	ASEL high time	$13t_{CLCL}$		
t_{MAHLD}	Address hold time	$2t_{CLCL}$		
t_{HASET}	Address setup to ASEL	$13t_{CLCL}$		
t_{ADSTA}	Low address to address stable	$13t_{CLCL}$		

NOTES:
1. Address should be valid at least $24t_{CLCL}$ before the rising edge of P0.2 (V_{PP}).
2. For a pure verify mode, i.e., no program mode in between, t_{AVQV} is $14t_{CLCL}$ maximum.

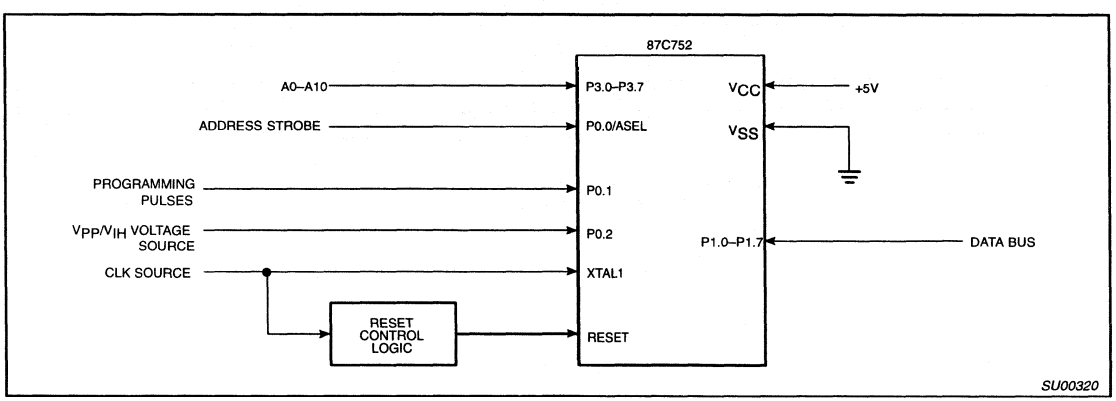


Figure 7. Programming Configuration

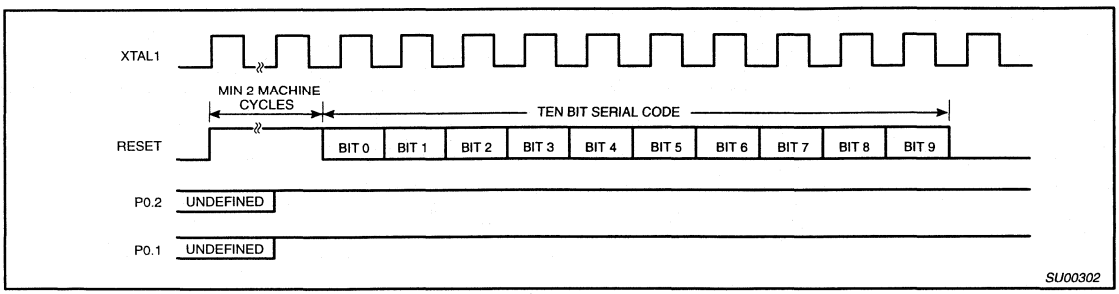


Figure 8. Entry into Program/Verify Modes

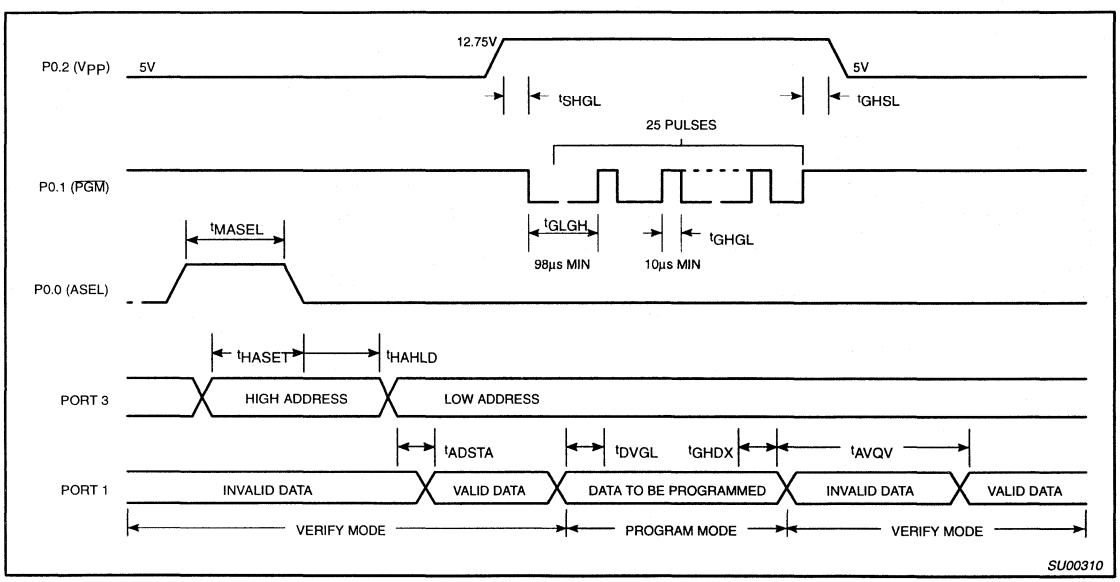


Figure 9. Program/Verify Cycle

SENSORS

QUICK REFERENCE DATA

FAMILY TYPE	R_{25} (Ω)	AVAILABLE TOLERANCE (ΔR)	T_{oper} RANGE (°C)	PACKAGE
KTY81-1	1000	±1% up to ±5%	−55 to 150	SOD70
KTY81-2	2000	±1% up to ±5%	−55 to 150	SOD70
KTY82-1	1000	±1% up to ±5%	−55 to 150	SOT23
KTY82-2	2000	±1% up to ±5%	−55 to 150	SOT23
KTY83-1	1000	±1% up to ±5%	−55 to 175	SOD68
KTY84-1	1000 (R_{100})	±3% up to ±5%	−40 to 300	SOD68
KTY85-1	1000	±1% up to ±5%	−40 to 125	SOD80
KTY86-2	2000	±0.5%	−40 to 150	SOD103
KTY87-2	2000(R_{25})	±0.5%	−40 to 125	SOD103
	3344(R_{100})			

GENERAL

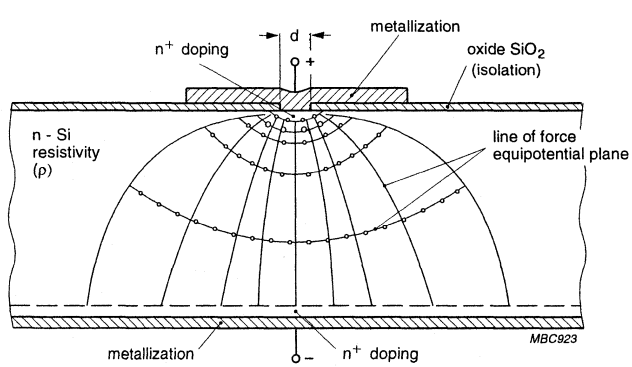
With their high accuracy and reliability, the KTY series of silicon temperature sensors in spreading resistance technology provide an attractive alternative to more conventional sensors using NTC or PTC thermistors. They have a positive temperature coefficient and a virtually linear temperature characteristic.

The sensors use n-type silicon with a doping level between 10^{14} and $10^{15}/cm^3$, providing a nominal resistance at 25 °C of about 1000 Ω (KTY81-1, KTY82-1, KTY83, KTY85) or 2000 Ω (KTY81-2, KTY82-2, KTY86, KTY87).

The nominal resistance of the KTY84 is also 1000 Ω, but specified at 100 °C.

Construction of the sensor: spreading resistance principle

The construction of the basic sensor chip is shown in Fig.1. The chip size is ≈500 × 500 × 240 μm. The upper plane of the chip is covered by an SiO_2 insulation layer, in which a metallized hole with a diameter of ≈20 μm has been cut out. The entire bottom plane is metallized.



The top plane is provided with a circular metal contact; the entire bottom plane is metallized.

$$R \approx \frac{\rho}{\pi} \times \frac{1}{d}.$$

Fig.1 Section through the crystal showing the spreading resistance principle and the electrode arrangement.

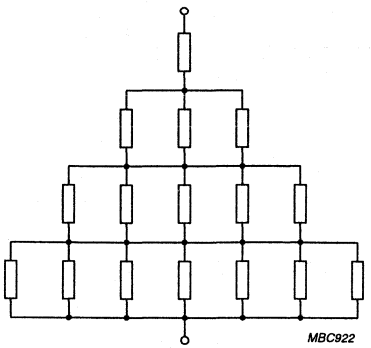


Fig.2 Equivalent circuit symbolically representing the spreading resistance principle shown in Fig.1.

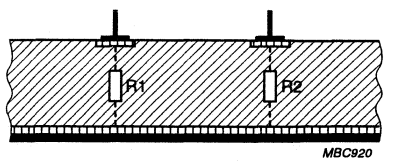


Fig.3 Setup consisting of two single sensors connected in series, but with opposite polarity.

This arrangement provides a conical current distribution through the crystal, hence the name 'spreading resistance' (see Fig.2). A major advantage of this arrangement is that the dependency of the sensor resistance on manufacturing tolerances is significantly reduced. An n^+ region, diffused into the crystal beneath the metallization reduces barrier-layer effects at the metal-semiconductor junctions.

Figure 3 shows a second arrangement, effectively consisting of two single sensors connected in series, but with opposite polarity. This twin-sensor arrangement has the advantage of providing a resistance that is independent of current direction, in contrast to the single-sensor arrangement of Fig.1, which, for larger currents and temperatures above 100 °C, gives a resistance that varies slightly with the current direction.

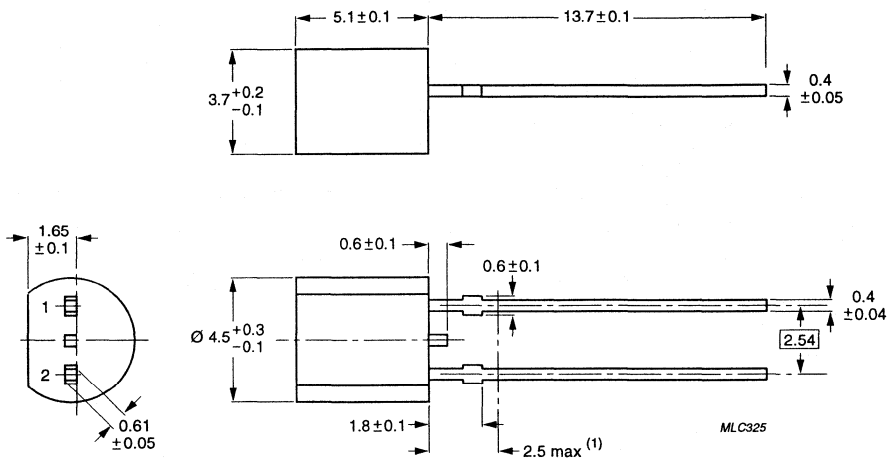
Normally, silicon temperature sensors have a temperature limit of ≈150 °C, imposed by the intrinsic semiconductor properties of silicon. If, however, the single-sensor device is biased with its metal contact positive, the onset of intrinsic semiconductor behaviour is shifted to a higher temperature. This stems from the fact that a positive voltage on the gold contact severely depletes the hole concentration in the upper n^+ diffusion layer, and so effectively insulates holes spontaneously generated within the body of the crystal (due to its intrinsic nature) preventing them from contributing to the total current, and hence from affecting the resistance.

The twin-sensor arrangement shown in Fig.3 has been applied in the KTY81 and KTY82 series. These sensors, in SOD70 (KTY81) and SOT23 (KTY82) packages (Figs 4 and 5), are therefore polarity independent.

The KTY83/84/85 series use the more basic single-sensor arrangement. The simplicity of this arrangement allows the sensors to be produced in the compact SOD68 (KTY83/84) and SOD80 (KTY85) packages (Figs 6 and 7, respectively).

In addition to simplicity, the single-sensor device has another important advantage: the potential for operation at temperatures up to 300 °C. The KTY84 makes use of this property, being specifically designed for operation at temperatures up to 300 °C.

The KTY86/87 temperature sensors consist of two KTY83 sensors in series, the resistance of the latter having been matched, in order to reduce tolerances. For the KTY86, the KTY83 sensors are matched at 25 °C; for the KTY87, at 25 and 100 °C (see Chapter "Quick reference data"). The package outline of the KTY86/87 sensors is given in Fig.8.



(1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

Fig.4 Outline of the KTY81 (SOD70).

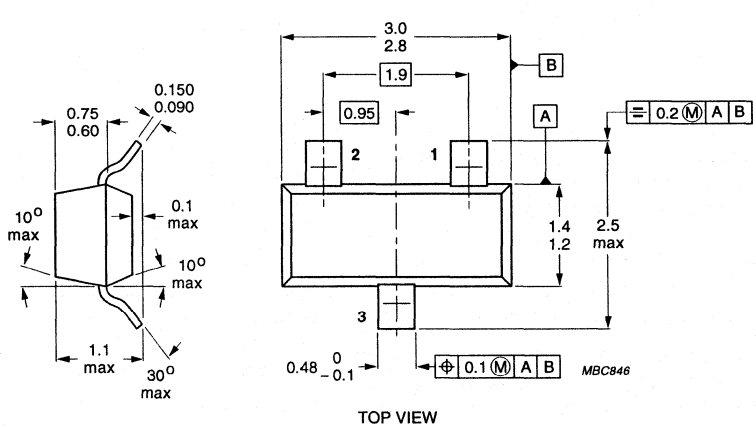


Fig.5 Outline of the KTY82 (SOT23).

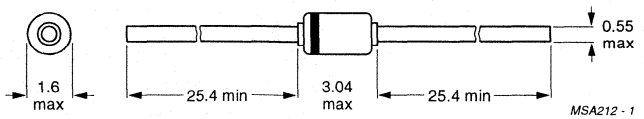
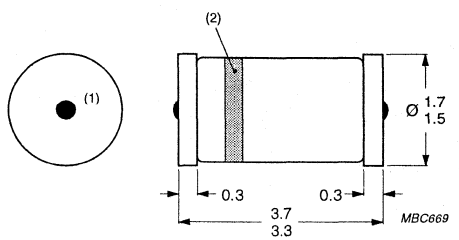


Fig.6 Outline of the KTY83/84 (SOD68).



(1) Area not tinned; small elevations are possible.
(2) Indication of polarity and type tape.

Fig.7 Outline of the KTY85 (SOD80).

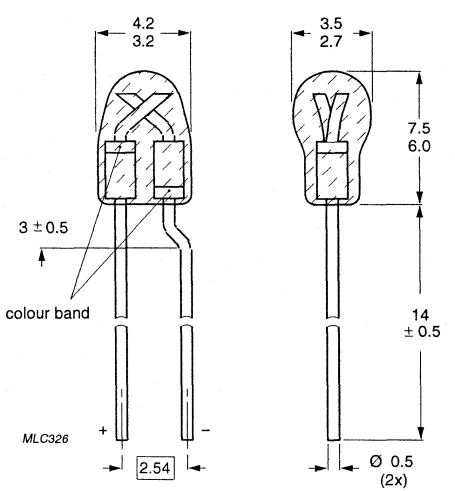


Fig.8 Outline of the KTY86/87 (SOD103).

TEMPERATURE DEPENDENCY

For the KTY83/85/86/87 series of temperature sensors, the mathematical expression for the sensor resistance 'R_T' as a function of temperature is given by:

$$R_T = R_{ref}\left[1 + A(T - T_{ref}) + B(T - T_{ref})^2\right] \quad (1)$$

where:

R_T is resistance at temperature T

R_{ref} is the nominal resistance at the reference temperature (T_{ref})

T_{ref} is reference temperature (100 °C for the KTY84, 25 °C for all other types)

A, B is type-dependent coefficients.

For the KTY81/82/84 series, the slope of the characteristic curve decreases slightly in the upper temperature range above a certain temperature T_I (point of inflection). Therefore, an additional term in equation (1) becomes necessary:

$$R_T = R_{ref}\left[1 + A(T - T_{ref}) + B(T - T_{ref})^2 - C(T - T_I)^D\right]$$

where:

T_I is temperature above which the slope of the characteristic curve starts to decrease (point of inflection).

C, D is type-dependent coefficients.

C is 0 for $T < T_I$.

For the types previously mentioned, the type-dependent constants 'A', 'B', 'C' and 'D', as well as 'T_I', are given in Table 1.

For high-precision applications, e.g. microcontroller-based control systems, the above expressions and the values in Table 1 can be used to generate a calibration table to store in a ROM for look-up and linear interpolation.

If a microcontroller is not used, the slight deviation from linearity can easily be compensated using a parallel resistor (if a constant current source is used), a series resistor (if a constant voltage source is used) or a suitable combination of both. This is discussed in Section "Linearization".

Table 1 Type dependent contstants

SENSOR TYPE	A (K^{-1})	B (K^{-2})	C(1) (K^{-D})	D	T_I (°C)
KTY81-1	7.874×10^{-3}	1.874×10^{-5}	3.42×10^{-8}	3.7	100
KTY81-2	7.874×10^{-3}	1.874×10^{-5}	1.096×10^{-6}	3.0	100
KTY82-1	7.874×10^{-3}	1.874×10^{-5}	3.42×10^{-8}	3.7	100
KTY82-2	7.874×10^{-3}	1.874×10^{-5}	1.096×10^{-6}	3.0	100
KTY83	7.635×10^{-3}	1.731×10^{-5}	–	–	–
KTY84	6.229×10^{-3}	1.159×10^{-5}	3.14×10^{-8}	3.6	250
KTY85	7.635×10^{-3}	1.731×10^{-5}	–	–	–
KTY86/87	7.646×10^{-3}	1.752×10^{-5}	–	–	–

Note

1. For $T < T_I$: C = 0.

RESISTANCE/TEMPERATURE CHARACTERISTICS

Manufacturing tolerances

Silicon temperature sensors are normally produced to quite fine tolerances: 'ΔR' between $\pm 0.5\%$ and $\pm 2\%$ (see Chapter "Quick reference data"). Figure 9 illustrates how these tolerances are specified, except for the KTY87. The tolerance on resistance quoted in our data sheets is given by the resistance spread 'ΔR' measured at 25 °C.

Because of spread in the slope of the resistance characteristics, 'ΔR' will increase each side of the 25 °C point, to produce the butterfly curve shown in Fig.9. To give an indication of this spread in slope, we also quote the ratio of resistance at two other temperatures (–55 °C and 100 °C) to the nominal resistance at 25 °C, i.e. 'R_{-55}/R_{25}' and 'R_{100}/R_{25}'; for the KTY84, we quote 'R_{25}/R_{100}' and 'R_{250}/R_{100}'.

The user, however, is usually more interested in the maximum expected temperature error '$\pm\Delta T$'. We also provide this in the data sheets, as a graph showing 'ΔT' as a function of 'T'. For the high temperature sensor KTY84, we specify the resistance spread at 100 °C.

The resistance of the KTY87 is specified with a close tolerance at 25 °C and 100 °C. This specification at two temperatures provides an essential improvement of measurement accuracy in this temperature range.

Current dependency of sensor resistance

The resistance of silicon temperature sensors is dependent on the operating current. In applications with an operating current deviating from the nominal current, a deviation of sensor resistance from the nominal values has to be taken into account.

For any application, an operating current ≥ 0.1 mA is recommended. For lower operating currents, the current dependency is additionally influenced by temperature.

For any application with operating currents above the nominal values, it should be noted, that an additional error caused by self-heating effects will influence the measurement accuracy.

Polarity of current

KTY83, 84, 85, 86 and 87 sensors are marked with a coloured band to indicate polarity. The published characteristics of the sensors will only be obtained if the current polarity is correct. In events where the current polarity is incorrect, the curve $R = f(T_{amb})$ differs in the upper temperature range significantly from the published form. Light, especially infrared, also has an influence.

Linearization

The resistance/temperature characteristics of the silicon temperature sensors are nearly linear, but in some applications further linearization becomes necessary, e.g. control systems requiring high accuracy.

A simple way to do this is to shunt the sensor resistance 'R_T' with a fixed resistor 'R_P' (see Fig.10a). The resistance '$R \times R_T/(R + R_T)$' of the parallel combination then effectively becomes a linear function of temperature, and the output voltage 'V_T' of the linearizing circuit can be used to regulate the control system.

If the circuit is powered by a constant-voltage source (see Fig.10a), a resistor R_S can be connected in series with the sensor. The voltages across the sensor and across the resistor will than again be approximately functions of temperature.

The value of the series or parallel resistor depends on the required operating temperature range of the sensor. A method for finding this resistance is described here, giving zero temperature error at three equidistant points T_a, T_b and T_c.

Consider the parallel arrangement. If the resistance of the sensor at the three points R_a, R_b and R_c, the requirement for linearity at the three points is:

$$R_{pa} - R_{pb} = R_{pb} - R_{pc}$$

i.e.

$$\frac{R \times R_a}{R + R_a} - \frac{R \times R_b}{R + R_b} = \frac{R \times R_b}{R + R_b} - \frac{R \times R_c}{R + R_c}$$

so

$$R = \frac{R_b \times (R_a + R_c) - 2R_a \times R_c}{R_a + R_c - 2R_b}.$$

The same resitor will also be suitable for the series arrangement.

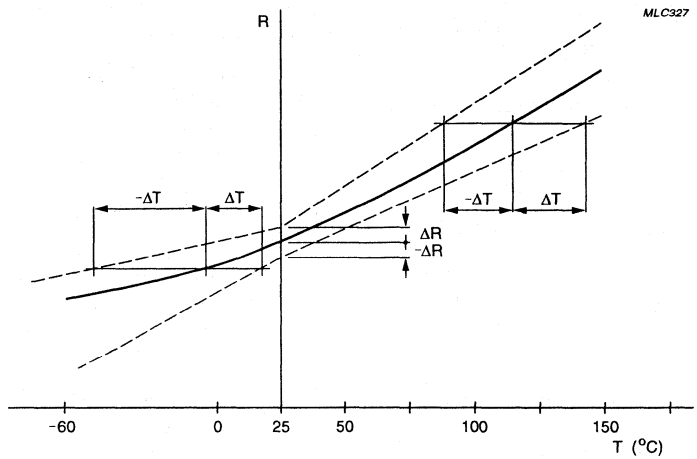
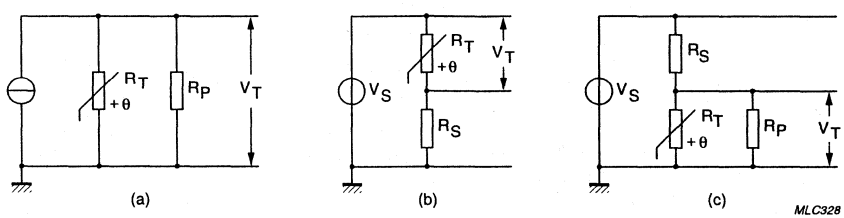


Fig.9 Butterfly curve.



(a) With a resistor 'R_P' shunted across the sensor.
(b) With a resistor 'R_S' in series with the sensor and system powered by a constant-voltage source.
(c) With a series 'R_S' and parallel resistor 'R_P' and system powered by a constant-voltage source.

Fig.10 Linearization of sensor characteristics.

In practice a current source is too expensive and a fixed supply voltage, e.g. 5 or 12 V is used for a specific operating current, e.g. 1 or 0.1mA. In this case, linearization can be achieved by series/parallel resistor combination to the sensor (see Fig.10c). The value of the parallel resistor R_P is equal to the value of R_S. Starting with the value of resistor R and with the desired current I_S through the sensor at a reference temperature T (preferable in the middle of the measured range), the resistor R_S and R_P can be calculated as follows:

$$\text{series resistor: } R_S = \frac{V_S}{I_S \times \left(\frac{R_T}{R} + 1\right)}$$

$$\text{parallel resistor: } R_P = \frac{1}{\frac{1}{R} - \frac{1}{R_S}}.$$

As an example, Fig.11 shows the deviation from linearity to be expected from a nominal KTY81 sensor, linearized over the temperature range 0 to 100 °C with a linearizing resistance of 2870 Ω.

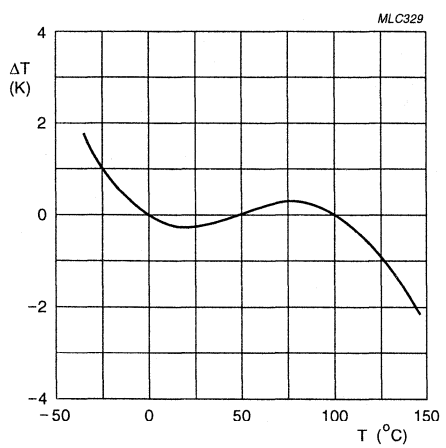
Figure 18 shows an application example using a series/parallel combination for the KTY81 (I_S = 1 mA) and Fig.19 shows an application example for the KTY87 (I_S = 0.1 mA).

Effect of tolerances on linearized sensor characteristics

In practical applications with an arbitrary sensor, the total uncertainty in the sensor reading will be a combination of spread due to manufacturing tolerances and linearization errors.

As an example, Fig.13 shows the combined effects of manufacturing tolerances and linearization errors for the KTY81 sensor linearized over the temperature range 0 to 100 °C. Calibration of the subsequent circuitry (op-amp, control circuitry, etc.) can reduce this error significantly.

Figure 14 shows the temperature error of the system with (linear) output circuitry calibrated at 50 °C, and Fig.15 shows the error of the same system calibrated at 0 and 100 °C.



Sensor linearized over the temperature range 0 to 100 °C (linearizing resistance 2870 Ω).

Fig.11 Linearization error 'ΔT' to be expected from a nominal KTY81.

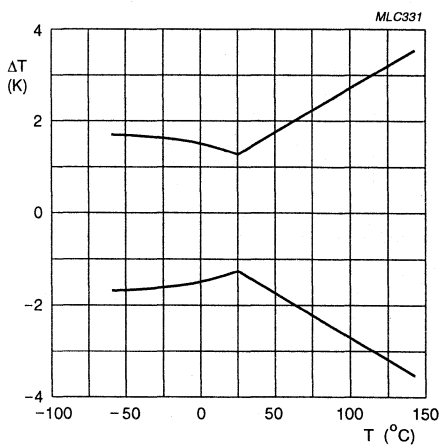


Fig.12 Maximum temperature error 'ΔT' due to manufacturing tolerances expected of a KTY81-1 sensor.

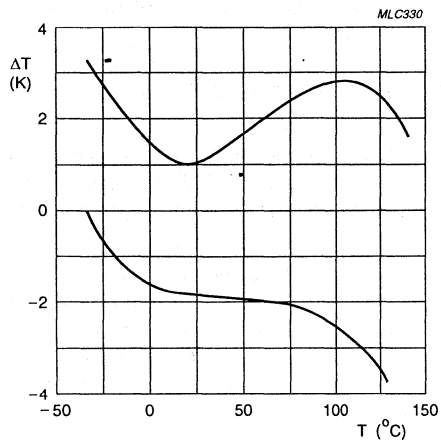


Fig.13 Combined effects of manufacturing tolerances and linearization errors for the KTY81 sensor.

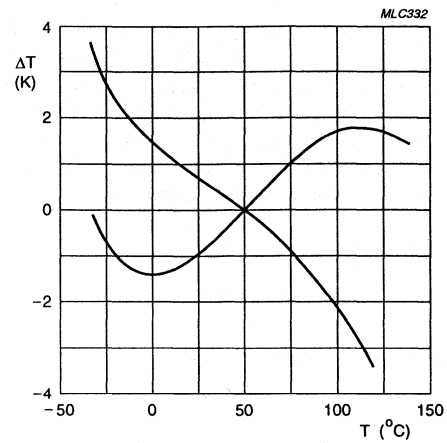


Fig.14 Maximum expected temperature error of a KTY81-1 sensor plus linearization resistor calibrated at 50 °C.

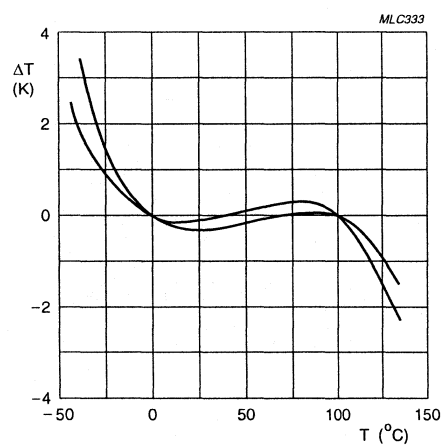


Fig.15 Error of a KTY81-1 sensor (same system as Fig.14) calibrated at 0 and 100 °C.

TEMPERATURE COMPENSATION

In many applications, it is necessary to compensate for the temperature dependency of electronic circuitry. For example, the sensitivity of many magnetic field sensors has a linear drift with temperature. To compensate for this drift, a temperature sensor with linear characteristics is required. The temperature sensors of the KTY series are well suited for this purpose and can be used for compensation of both positive and negative drift.

In many events, as with the magnetoresistive sensor KMZ10B, the temperature drift is negative. For this sensor, two circuits in SMD-technology, which include temperature compensation, are described below. The formulae given can be used to adapt the circuits to other conditions.

Figure 16 shows a simple setup using a single op-amp (NE5230D). The circuit provides the following facilities:

- Compensation of the **average** (sensor-to-sensor) sensitivity drift with temperature via a negative feedback loop incorporating a KTY82-210 silicon temperature sensor
- Offset adjustment by means of potentiometers 'R1' and 'R2'
- Gain adjustment by means of potentiometer 'R7'.

The temperature sensor is part of the amplifier's feedback loop and thus increases the amplification with increasing temperature.

With the resistor as shown in Fig.16 the temperature dependent amplification 'A' is given by:

$$A = \frac{R7}{R4 + \frac{R_B}{2}}\left(1 + 2\frac{R_T}{R_S}\right) \qquad (2)$$

and the temperature coefficient of the amplification can be calculated to be:

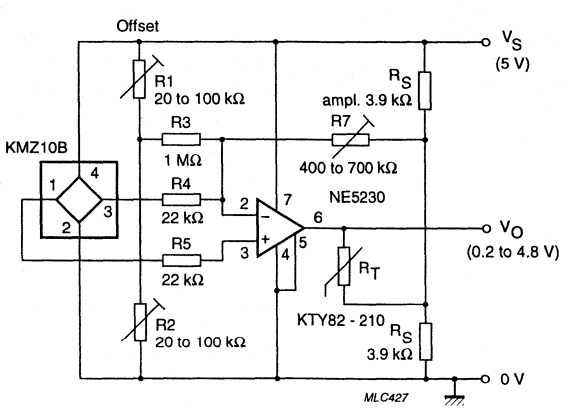
$$TC_A = \frac{R_T \times TC_{KTY}}{R_T + \frac{R_S}{2}}$$

with:

R_T = temperature dependent resistance of the KTY82.

TC_{KTY} = temperature coefficient of the KTY82 at reference temperature (0.79 %/K at 25 °C).

R_B = bridge resistance of the magnetoresistive sensor.



Example: A = 50 (typ.), $TC_A = 0.004\ K^{-1}$.

Fig.16 Temperature compensation circuit.

The temperature coefficient of amplification must be equal and opposite to the magnetic field sensor's 'TC' of sensitivity.

The value of the resistor 'R_S', which determines the positive 'TC' of the amplification is:

$$R_S = 2 \times R_T \left(\frac{TC_{KTY}}{TC_A} - 1 \right).$$

The resistance of the feedback resistor can be derived from equation (2):

$$R7 = R4 \times \left(\frac{A}{1 + 2\frac{R_T}{R_S}} \right).$$

The temperature dependent values 'R_T' and 'A' are taken for a certain reference temperature, usually 25 °C, but in other applications a different reference temperature may be more suitable.

Figure 17 shows an example with a commonly used instrumentation amplifier. The circuit can be divided into two stages: a differential amplifier stage that produces a symmetrical output signal derived from the magnetoresistive sensor, and an output stage that also provides a reference to ground for the amplification stage.

To compensate the negative sensor drift, the amplification is again given an equal but positive temperature coefficient by means of a KTY81-110 silicon temperature sensor in the feedback loop of the differential amplifier.

The amplification of the input stage ('OP1' and 'OP2') is given by:

$$A1 = 1 + \frac{R_T + R_B}{R_A}$$

and the amplification of the complete amplifier by:

$$A = A1 \times \frac{R14}{R10}.$$

The positive temperature coefficient of the amplification is:

$$TC_A = \frac{R_T \times TC_{KTY}}{R_A + R_B + R_T}.$$

For the given negative 'TC' of the magnetoresistive sensor and the required amplification of the input stage 'A1', the resistance 'R_A' and 'R_B' can be calculated by:

$$R_B = R_T \times \left(\frac{TC_{KTY}}{TC_A} \times \left(1 - \frac{1}{A1} \right) - 1 \right)$$

$$R_A = \frac{R_T + R_B}{A1 - 1}.$$

The circuit provides for adjustment of gain and offset voltage of the magnetic-field sensor. The calculated resistance 'R_A' consists of the fixed resistor 'R5' and trimming resistor 'R6' provided for amplification adjustment. Amplification adjustment only negligibly influences the 'TC' of the amplifier. The output stage 'OP3' gives an output voltage of $^2/_5$ of the supply voltage (2 V for V_S = 5 V) for zero output voltage of the magnetic field sensor and an output voltage of ±1 V for V_S = 5 V. For other supply voltages the circuit has a ratiometric behaviour.

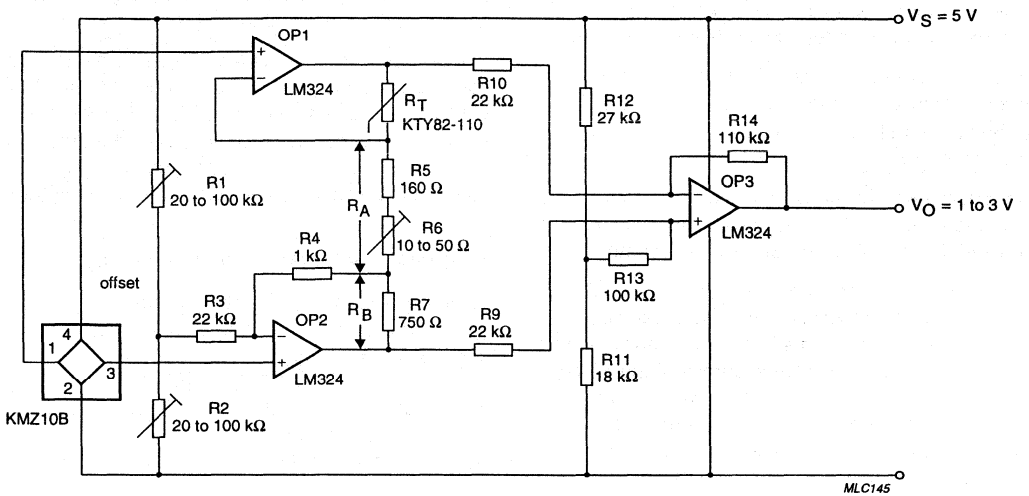
TYPICAL APPLICATION CIRCUIT

Figure 18 shows a typical and versatile temperature measuring circuit using silicon temperature sensors. This example is designed for the KTY81-110 (or the KTY82-110) and a temperature range from 0 to 100 °C.

With resistors 'R1' and 'R2', the sensor forms one arm of a bridge, the other arm being formed by resistor 'R3', potentiometer 'P1' and resistor 'R4'. The values of 'R1' and 'R2' are chosen to supply the sensor with the proper current of ≈1 mA, and to linearize the sensor characteristic over the temperature range of interest: in this event, between 0 and 100 °C. Over this temperature range, the output voltage V_O will vary linearly between $0.2V_S$ and $0.6V_S$, i.e. between 1 V and 3 V for a supply of V_S = 5 V.

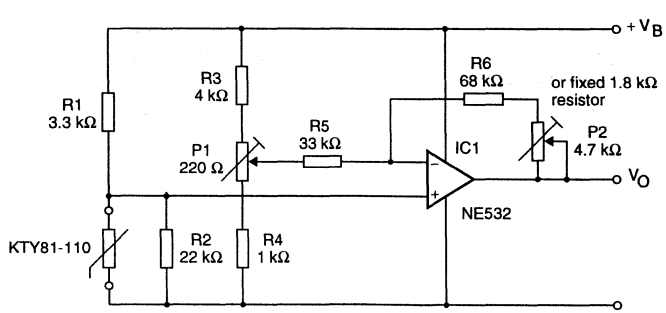
To calibrate the circuit, adjust 'P1' to set 'V_O' to 1 V, with the sensor at 0 °C. Then, at a temperature of 100 °C, adjust 'P2' to set 'V_O' to the corresponding output voltage, in this example 3 V. With this circuit, adjustment of 'P2' has no effect on the zero adjustment.

The measurement accuracy obtained by this two-point calibration is shown in Fig.15. If the application can tolerate a temperature deviation of ±2 K at the temperature extremes (see Fig.14), costs can be reduced by replacing 'P2' with a 1.8 kΩ fixed resistor and adjusting 'V_O' at one temperature (the middle of the range, for example), using 'P1'.



Example: A = 50 (typ.), TC_A = 0.004 K^{-1}.

Fig.17 KMZ10B evaluation circuit with instrumentation amplifier.



A KTY82-110 sensor would be equally suitable.
Temperature range 0 to 100 °C; V_O = 0.2V_S to 0.6V_S.
For V_S = 5 V: V_O = 1 to 3 V.
All resistors metal film; tolerance ±1%.

Fig.18 Temperature measuring circuit using a KTY81-110 sensor.

MEASURING CIRCUITS WITH KTY87

The advantages of the KTY87-205 silicon temperature sensor are its improved accuracy and replacement within an evaluation circuit without subsequent re-calibration.

The improved accuracy of the KTY87 is not only effective at one temperature, but over a wide temperature range due to the special series connection of two selected temperature sensors.

Within the temperature range 20 °C to 100 °C the KTY87 provides a less expensive alternative to Pt100 sensors if the somewhat reduced accuracy can be accepted.

Due to component tolerances and offset voltage of common operational amplifiers, the evaluation circuit for the temperature sensor normally has to be adjusted with respect to the sensor. The high accuracy of the KTY87 within the range 25 °C to 100 °C, however, makes it possible to adjust the electronic circuit with respect to nominal resistance sensor values. A sensor within the evaluation circuit can then be subsequently replaced without the need for re-calibration of the circuit. The overall measurement error is less than ±1 °C.

MICROCONTROLLER INTERFACE/GENERAL PURPOSE

The circuit in Fig.19, is effective for the temperature range 0 to 100 °C. It is a suitable preamplifier for AD converters or microcontrollers with ADC inputs of ratiometric behaviour. It may also be used as a general simple signal conditioning circuit for silicon temperature sensors.

Because of the high accuracy of the sensor, a precision operational amplifier with low offset drift and high temperature stable resistors should be used.

The calibration of this circuit as follows:

Replace the sensor by a fixed test resistor of 1 640 Ω (nominal value of KTY87 at 0 °C).

Adjust 'P1' to set 'V_O' to 0.5 V.

Replace the sensor with a test resistor of 3344 Ω (nominal value at 100 °C).

Set V_O = 4.5 V by 'P2'.

The circuit is now calibrated for a nominal KTY87 temperature sensor and can be used with any such sensor, giving a measurement accuracy of better than ±1 °C in the range of 20 to 100 °C.

If the circuit is to be matched to a specific sensor the calibration procedure has to be carried out with this sensor subjected to the test temperatures and should be carefully monitored e.g. by use of an accurate liquid thermostat. This method is more costly and gives an increase in measurement accuracy for this specific sensor only.

TWO WIRE TRANSMITTER (4 to 20 mA)

In industrial temperature control, current transmitters with the standardized current output of 4 to 20 mA, are commonly used. Figure 20 shows a two wire current transmitter with the KTY87; temperature measuring range is 0 to 100 °C. It consists of a wheatstone bridge with a preamplifier similar to that in Fig.19, a current transmitter output stage and voltage stabilization circuitry.

The calibration of this current transmitter is as follows:

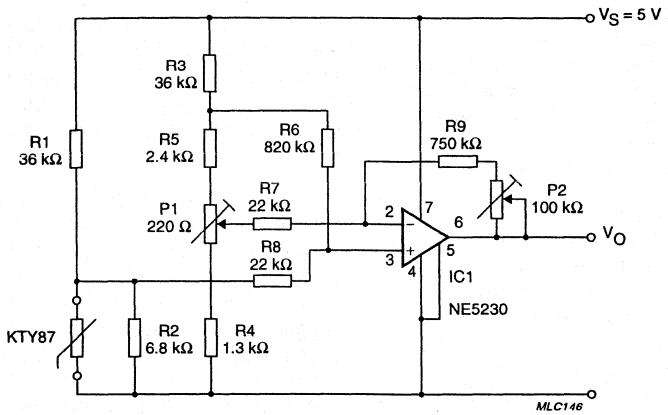
Set the supply voltage to ≈12 V.

Set the internal operating voltage to 5 V by potentiometer 'P3'.

Replace the temperature sensor by a fixed test resistor of 1640 Ω (nominal value of KTY87 at 0 °C) and set the output current to 4 mA by 'P1'.

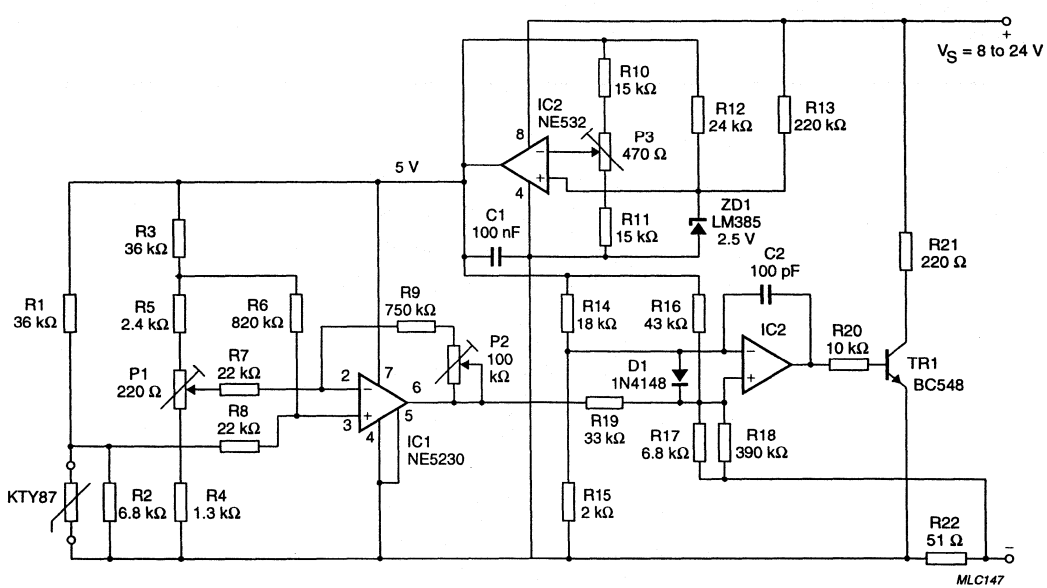
Replace the test resistor with a second test resistor of 3344 Ω inserted (nominal value at 100 °C) and set the output current to 20 mA by potentiometer 'P2'.

The calibration procedure can also be carried out with a specific temperature sensor subjected to the test temperatures 0 °C and 100 °C. The circuit then is calibrated to this specific sensor only.



All resistors: metalfilm, tolerance <±1%, TC < ±50 × 10^{-6} K^{-1}; measuring range: 0 to 100 °C; V_O = 0.5 to 4.5 V for V_S = 5.0 V; $V_O = 0.2V_S \times (0.5 + 0.04 \times TC)$.

Fig.19 Microcontroller interface for KTY87.



All resistors: metalfilm, tolerance <±1%, TC < ±50 × 10^{-6} K^{-1}; measuring range: 0 to 100 °C, I = 4 + T/6.25 with I in mA and T in °C.

Fig.20 Current transmitter (4 to 20 mA) for the KTY87.

HIGH TEMPERATURE MEASUREMENT WITH KTY84

The operating range of silicon temperature sensors normally is limited to about 150 °C (an exception is the KTY83 with an upper temperature limit of 175 °C). This is due to the temperature stability of the package and the increasing intrinsic conductivity of the silicon crystal above 150 °C. The measuring range of the KTY84 silicon temperature sensors is extended up to 300 °C.

The SOD68 diode housing together with special contacts between leads and sensor crystal give the necessary temperature resistivity for the envelope. The influence of the intrinsic conductivity can be suppressed by a sufficiently high operating current flowing in the correct direction.

Figure 21 shows the nominal characteristic for the recommended operating current of 2 mA and the effect of operating the sensor with a lower, and especially, a reverse current. The sensor resistance at the high temperature end makes it impossible to draw the current of 2 mA through the sensor in a common bridge circuit as in the previously suggested circuits. Reasons are the usually limited supply voltage and the fact that the value of the series resistor may not be less than the linearization resistor of ≈5 kΩ. A solution is to supply the sensor by a constant current source.

Figure 22 gives an example with internal voltage stabilization, a supply voltage of 8 to 24 V and for the full measuring range up to 300 °C. Operational amplifier 'OP1' and transistor 'TR1' form a current source to feed the temperature sensor. 'OP2' amplifies the bridge signal to the output voltage range. The circuit provides adjustment for a 'zero point', 100 °C equal V_O = 2 V ('P1'), and full range ('P2').

A second example for a KTY84 evaluation circuit takes into consideration that in some electronic systems a supply voltage of only 5 V may be used. Under such circumstances it would be impossible to obtain the recommended current of 2 mA. A compromise is suggested by the circuit in Fig.23. A low drop current source supplies the temperature sensor and the linearization resistor. The maximum attainable current at 300 °C is 1.5 mA. This value is below the nominal operating current, but as Fig.21 shows, at up to 250 °C this will not cause any additional measuring error. Between 250 °C and 300 °C, however, a slightly decreasing slope of the sensor characteristic has to be taken into account.

The KTY84 silicon temperature sensor is a reliable and cost effective alternative to more expensive options such as Pt100-resistors or thermocouplers.

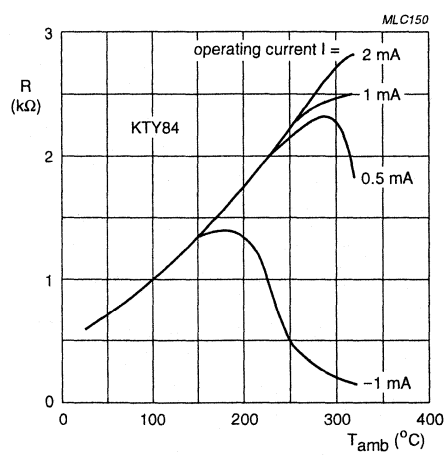


Fig.21 Sensor characteristic of the KTY84.

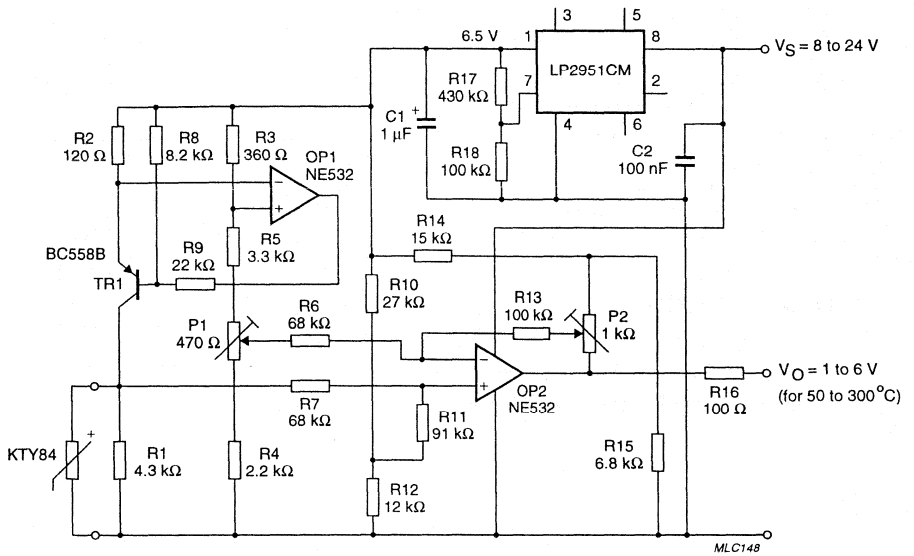


Fig.22 Evaluation circuit for KTY 84 with voltage regulation.

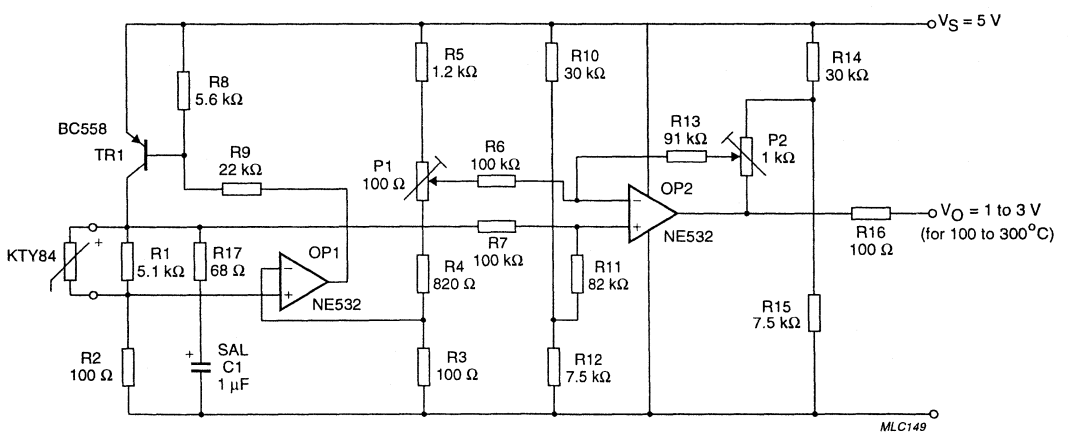


Fig.23 KTY84 evaluation circuit for 5 V power supply.

AD CONVERTER TEMPERATURE COMPENSATION

When an A/D converter is integrated with a microcontroller, temperature compensation is required.

Figure 24 shows a suitable configuration, using a KTY81-210 temperature sensor in series with linearization resistor R_S. This voltage divider provides a linear temperature dependent voltage V_T of between 1.127 V and 1.886 V over the range 0 to 100 °C. This voltage is used as a reference for the A/D converter. The linear slope 'S' of V_T = 7.59 mV/ K.

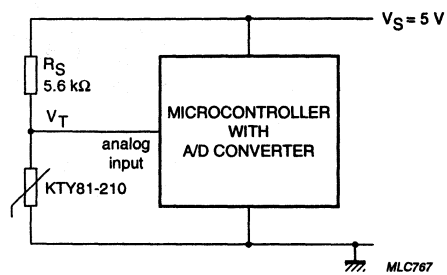


Fig.24 Temperature compensation for A/D converters.

ADDITIONAL TEMPERATURE SENSOR APPLICATIONS

Philips temperature sensors are also suitable for use in a number of other applications, for which information can be supplied on request:

- Electronic circuit protection
- Protection for power supplies
- Domestic appliances
- The white goods industry
- The automotive industry.

MOUNTING AND HANDLING RECOMMENDATIONS

Mounting

KTY81

When potting techniques for KTY81 sensors are used for assembling, care has to be taken to ensure that mechanical stress and temperature development during curing of epoxy resin do not overstress the devices.

KTY83, 84, 86 AND 87

Excessive forces applied to a sensor may cause serious damage. To avoid this, the following recommendations should be adhered to:

- no perpendicular forces must be applied to the body
- during bending, the leads must be supported
- bending close to the body must be done very carefully
- axial forces to the body can influence the accuracy of the sensor and should be avoided.

Handling

ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY

Electrostatic discharges above a certain energy can lead to irreversible changes of the sensor characteristic. In extreme events, sensors can even be destroyed. In accordance with the test methods described in IEC 47 (CO)955, temperature sensors are classified as sensitive components with respect to ESD. During handling (testing, transporting, fitting), the common rules for handling of ESD sensitive components should be observed.

If necessary, the ESD sensitivity in the practical application can be further reduced by connecting a 10 nF capacitor in parallel to the sensor.

Soldering

KTY81

The common rules for soldering components in TO-92 packages should be observed.

KTY 82

The common rules for soldering SMD components in SOT23 packages should be observed (see Chapter *"Mounting and soldering in Handbook SC10a"*).

KTY83, 86 AND 87

Avoid any force on the body or leads during, or just after, soldering. Do not correct the position of an already soldered sensor by pushing, pulling or twisting the body. Prevent fast cooling after soldering. For hand soldering, where mounting is not on a printed-circuit board, the soldering temperature should be <300 °C, the soldering time <3 s and the distance between body and soldering point >1.5 mm. For hand soldering, dip, wave or other bath soldering, mounted on a printed-circuit board, the soldering temperature should be <300 °C, the soldering time <5 s and the distance between body and soldering point >1.5 mm.

KTY85

The common rules for surface mounted devices in SOD80 packages should be observed. Hand soldering is not recommended, because there is a great risk of damaging the glass body or the inner construction by uncontrolled temperature and time.

Welding

The KTY84 sensors are manufactured with nickel plated leads suitable for welding. The distance between the body and the welding point should be >0.5 mm. Care should be taken to ensure that welding current never passes through the sensor.

SILICON TEMPERATURE SENSORS

These sensors have a positive temperature coefficient of resistance and are for use in measurement and control.

QUICK REFERENCE DATA

Resistance at T_{amb} = 25 °C
I_C = 1 mA

KTY81-110	R_{25}	990 - 1010 Ω
KTY81-120	R_{25}	980 - 1020 Ω
KTY81-121	R_{25}	980 - 1000 Ω
KTY81-122	R_{25}	1000 - 1020 Ω
KTY81-150	R_{25}	950 - 1050 Ω
KTY81-151	R_{25}	950 - 1000 Ω
KTY81-152	R_{25}	1000 - 1050 Ω

Operating ambient temperature range T_{amb} −55 to +150 °C

MECHANICAL DATA

Dimensions in mm

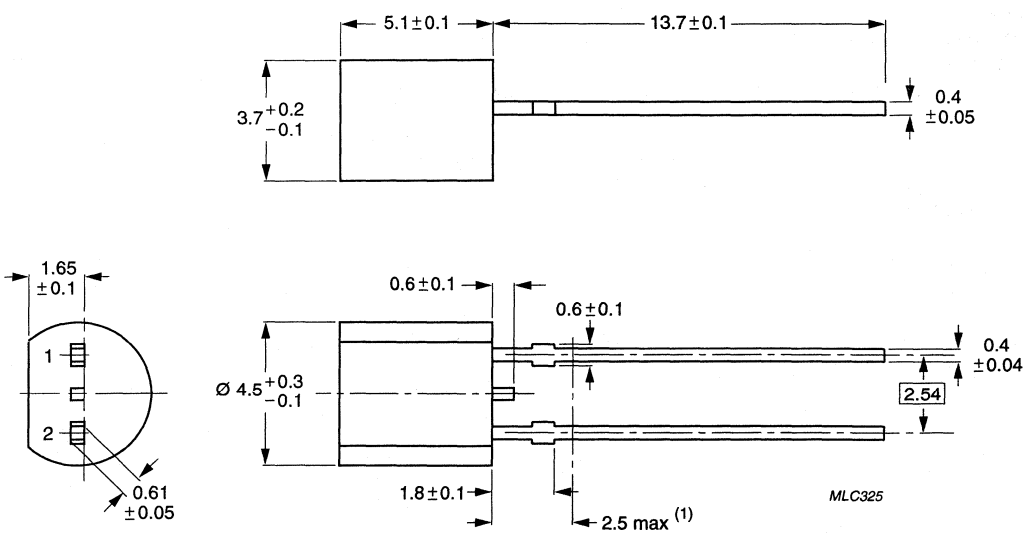


Fig. 1 SOD-70.

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Continuous sensor current in free air			
T_{amb} = 25 °C	I_C	max.	10 mA
T_{amb} = 150 °C	I_C	max.	2.0 mA

CHARACTERISTICS

(Based on the measurements in liquid at T_{amb} = 25 °C unless otherwise specified).

Resistance				
I_C = 1 mA	KTY81-110	R_{25}	990 - 1010 Ω	
	KTY81-120	R_{25}	980 - 1020 Ω	
	KTY81-121	R_{25}	980 - 1000 Ω	
	KTY81-122	R_{25}	1000 - 1020 Ω	
	KTY81-150	R_{25}	950 - 1050 Ω	
	KTY81-151	R_{25}	950 - 1000 Ω	
	KTY81-152	R_{25}	1000 - 1050 Ω	
Temperature coefficient			typ. 0.79	%/K
Resistance ratio		R100/R25	1.696 ± 0.020	
		R−55/R25	0.490 ± 0.010	
Thermal time constant*				
in still air			typ. 30	s
in still liquid**			typ. 5.0	s
in flowing liquid**			typ. 3.0	s
Measuring temperature range			−55 to +150	°C

T_{amb} °C	Resistance Ω
−55	490
−50	515
−40	567
−30	624
−20	684
−10	747
0	815
10	886
20	961
25	1000
30	1040
40	1122

T_{amb} °C	Resistance Ω
50	1209
60	1299
70	1392
80	1490
90	1591
100	1696
110	1805
120	1915
130	2023
140	2124
150	2211

Ambient temperature and corresponding average resistance values of sensor (I_C = 1 mA).

* The thermal time constant is the time the sensor needs to reach 63.2% of the total temperature difference. For instance, the time needed to reach a temperature of 72.4 °C, when a sensor with an initial temperature of 25 °C is put into an ambient with a temperature of 100 °C.

** Inert liquid FC43 of 3M company.

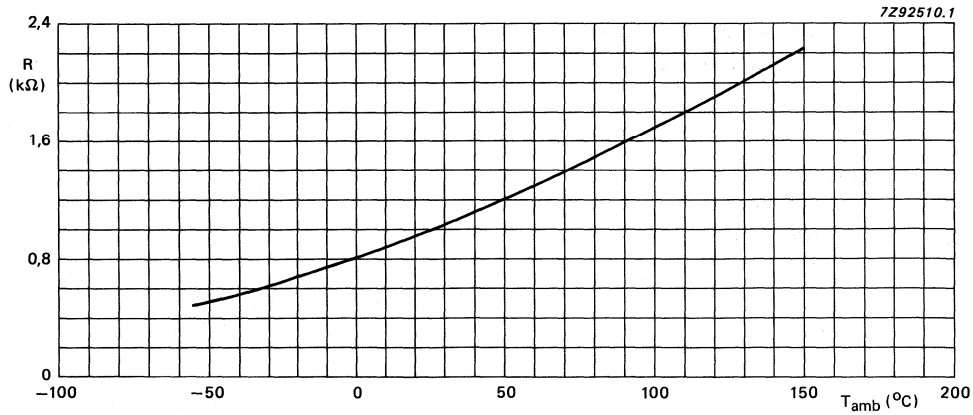


Fig. 2 Average resistance value of sensor at I_C = 1 mA as a function of temperature.

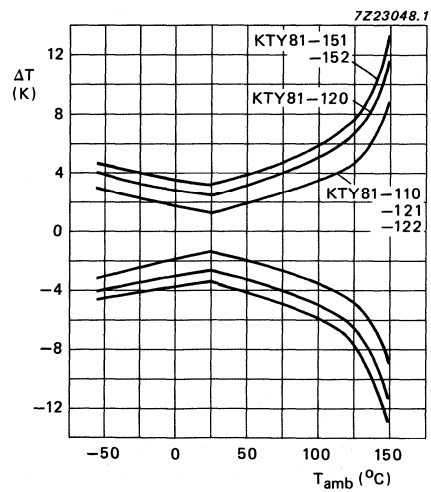


Fig. 3 Maximum expected temperature error ΔT.

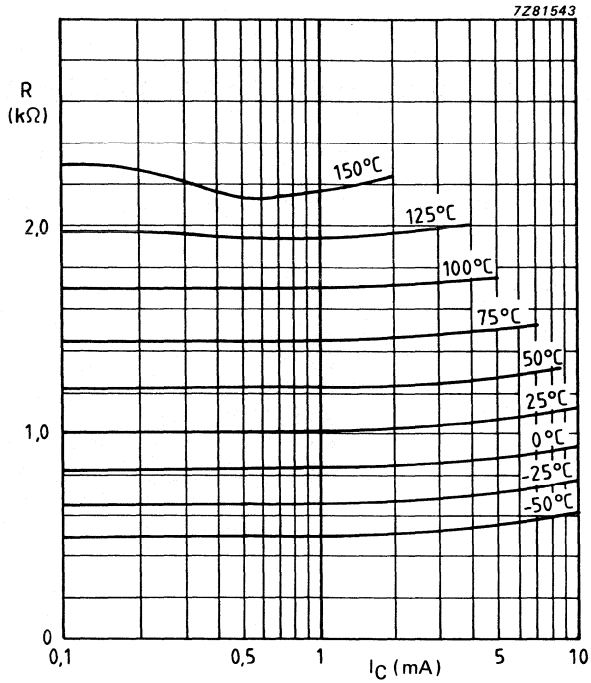


Fig. 4 Sensor resistance as a function of operating current (see Note).

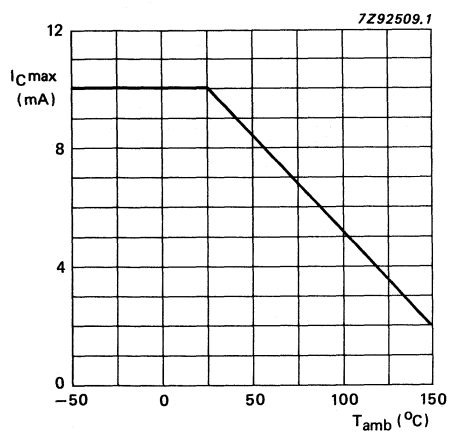


Fig. 5 Maximum operating current for safe operation.

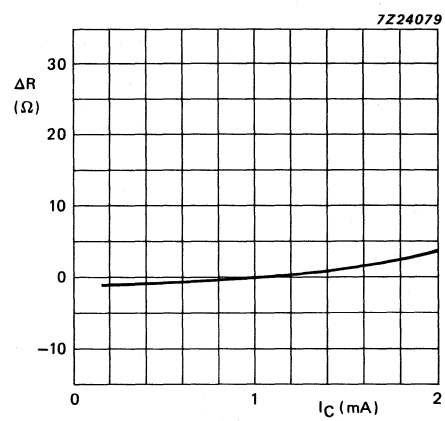


Fig. 6 Resistance deviation as a function of measuring current in still liquid; T_{amb} = 25 °C.

Note

To minimize temperature error, an operating current of I_C = 1 mA is recommended for temperatures above 100 °C.

SILICON TEMPERATURE SENSORS

These sensors have a positive temperature coefficient of resistance and are for use in measurement and control systems.

QUICK REFERENCE DATA

Resistance at T_{amb} = 25 °C
I_C = 1 mA

KTY81-210	R_{25}	1980 - 2020 Ω
KTY81-220	R_{25}	1960 - 2040 Ω
KTY81-221	R_{25}	1960 - 2000 Ω
KTY81-222	R_{25}	2000 - 2040 Ω
KTY81-250	R_{25}	1900 - 2100 Ω
KTY81-251	R_{25}	1900 - 2000 Ω
KTY81-252	R_{25}	2000 - 2100 Ω

Operating ambient temperature range T_{amb} −55 to +150 °C

MECHANICAL DATA

Dimensions in mm

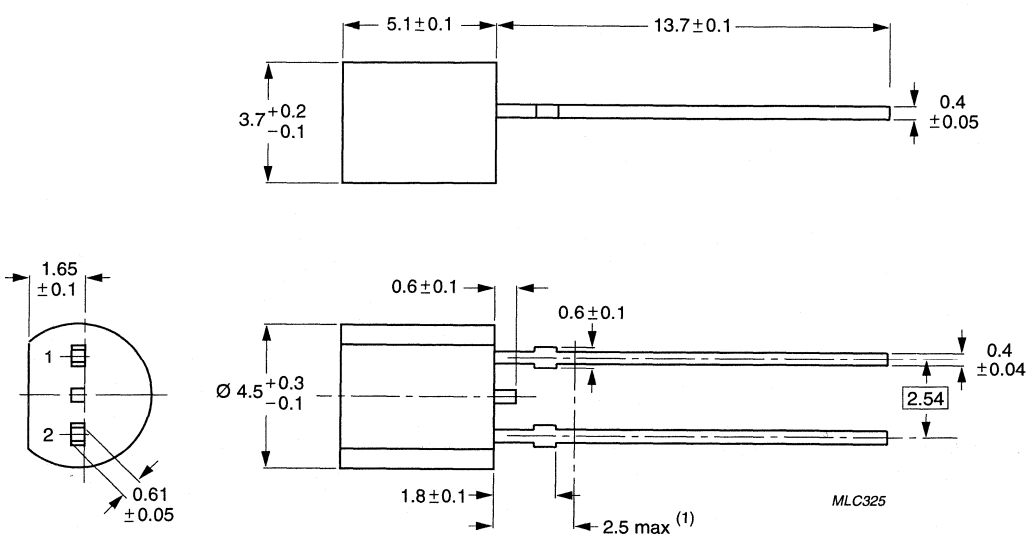


Fig. 1 SOD-70.

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Continuous sensor current in free air

T_{amb} = 25 °C	I_C	max.	10 mA
T_{amb} = 150 °C	I_C	max.	2.0 mA

CHARACTERISTICS

(Based on the measurements in liquid at T_{amb} = 25 °C unless otherwise specified).

Resistance

I_C = 1 mA

KTY81-210	R_{25}	1980 - 2020 Ω
KTY81-220	R_{25}	1960 - 2040 Ω
KTY81-221	R_{25}	1960 - 2000 Ω
KTY81-222	R_{25}	2000 - 2040 Ω
KTY81-250	R_{25}	1900 - 2100 Ω
KTY81-251	R_{25}	1900 - 2000 Ω
KTY81-252	R_{25}	2000 - 2100 Ω

Temperature coefficient		typ.	0.79 %/K
Resistance ratio	R100/R25		1.696 ± 0.020
	R-55/R25		0.490 ± 0.010

Thermal time constant*

in still air	typ.	30 s
in still liquid**	typ.	5 s
in flowing liquid	typ.	3 s

Measuring temperature range *** −55 to +150 °C

T_{amb} °C	Resistance Ω	T_{amb} °C	Resistance Ω
−55	980	50	2417
−50	1030	60	2597
−40	1135	70	2785
−30	1247	80	2980
−20	1367	90	3182
−10	1495	100	3392
0	1630	110	3607
10	1772	120	3817
20	1922	125	3915
25	2000	130	4008
30	2080	140	4166
40	2245	150	4280

Ambient temperatures and corresponding resistance values of sensor (I_C = 1 mA).

* The thermal time constant is the time the sensor needs to reach 63.2% of the total temperature difference. For instance, the time needed to reach a temperature of 72.4 °C, when a sensor with an initial temperature of 25 °C is put into an ambient with a temperature of 100 °C.

** Inert liquid FC43 of 3M company.

*** Restricted accuracy in the temperature range 125 °C to 150 °C.

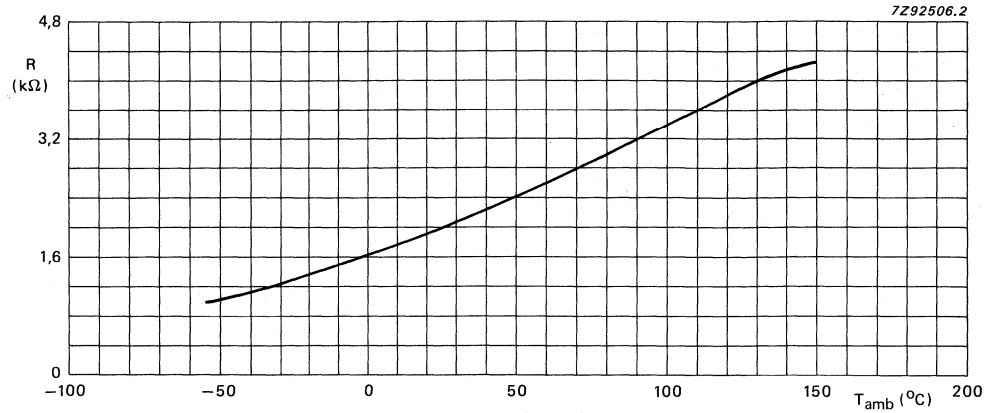


Fig. 2 Average resistance value of sensor at I_C = 1 mA as a function of temperature.

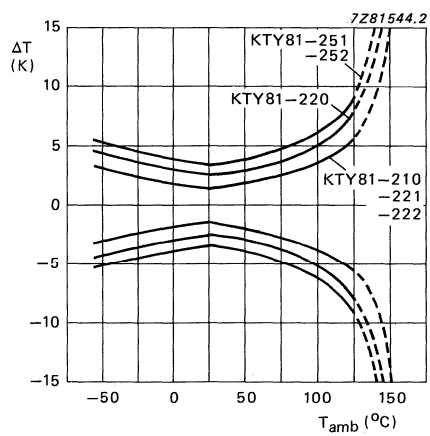


Fig. 3 Maximum expected temperature error ΔT.

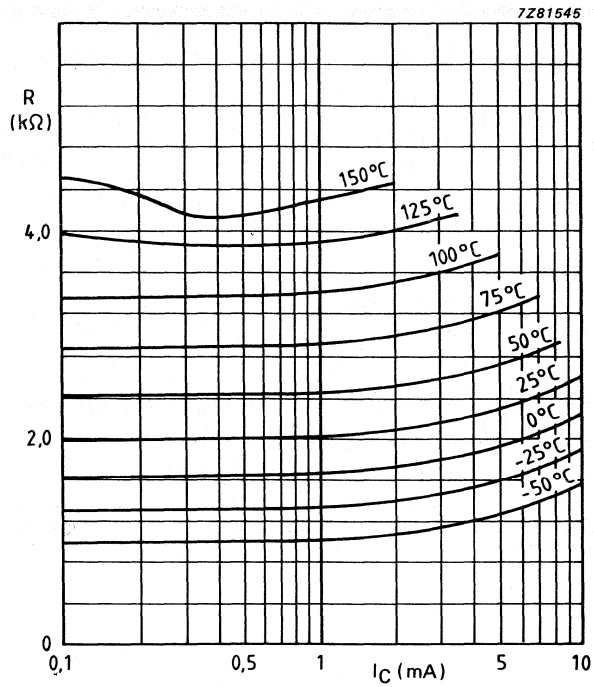


Fig. 4 Sensor resistance as a function of operating current (see Note).

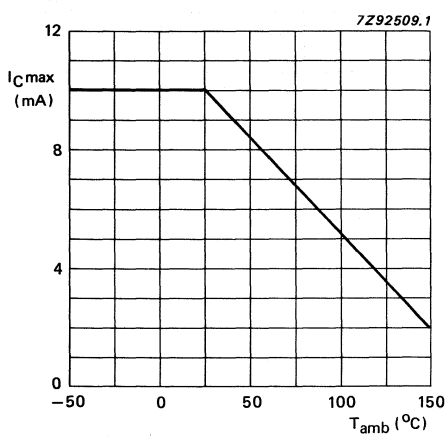


Fig. 5 Maximum operating current for safe operation.

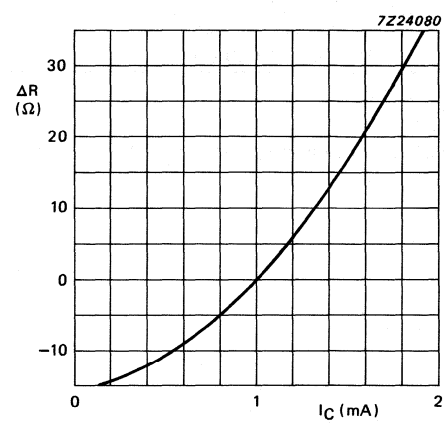


Fig. 6 Resistance deviation as a function of measuring current in still liquid; T_{amb} = 25 °C.

Note

To keep the temperature error low, an operating current of I_C = 1 mA is recommended for temperatures above 100 °C.

Silicon temperature sensors KTY82-1 series

DESCRIPTION

These temperature sensors have a positive temperature coefficient of resistance and are for use in measurement and control systems.

PINNING

PIN	DESCRIPTION
1	electrical contact
2	electrical contact
3	substrate (must remain potential free)

Marking codes:

KTY82-110: 110.
KTY82-120: 120.
KTY82-121: 121.
KTY82-122: 122.
KTY82-150: 150.
KTY82-151: 151.
KTY82-152: 152.

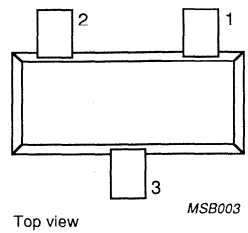


Fig.1 Simplified outline.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
R_{25}	sensor resistance	T_{amb} = 25 °C; I_{cont} = 1 mA			
	KTY82-110		990	1010	Ω
	KTY82-120		980	1020	Ω
	KTY82-121		980	1000	Ω
	KTY82-122		1000	1020	Ω
	KTY82-150		950	1050	Ω
	KTY82-151		950	1000	Ω
	KTY82-152		1000	1050	Ω
T_{amb}	ambient operating temperature range		−55	150	°C

Note

Tolerances of 0.5% or other special selections available on request.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{cont}	continuous sensor current	in free air; T_{amb} = 25 °C	–	10	mA
		in free air; T_{amb} = 150 °C	–	2	mA
T_{amb}	ambient operating temperature range		–55	150	°C

CHARACTERISTICS

T_{amb} = 25 °C, in liquid, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_{25}	sensor resistance	T_{amb} = 25 °C; I_{cont} = 1 mA				
	KTY82-110		990	–	1010	Ω
	KTY82-120		980	–	1020	Ω
	KTY82-121		980	–	1000	Ω
	KTY82-122		1000	–	1020	Ω
	KTY82-150		950	–	1050	Ω
	KTY82-151		950	–	1000	Ω
	KTY82-152		1000	–	1050	Ω
TC	temperature coefficient		–	0.79	–	%/K
R_{100}/R_{25}	resistance ratio	at T_{amb} = 100 °C and 25 °C	1.676	1.696	1.716	
R_{-55}/R_{25}	resistance ratio	at T_{amb} = –55 °C and 25 °C	0.480	0.490	0.500	
τ	thermal time constant (note 1)	in still air	–	7	–	s
		in still liquid (note 2)	–	1	–	s
		in flowing liquid	–	0.5	–	s
	rated temperature range		–55	–	150	°C

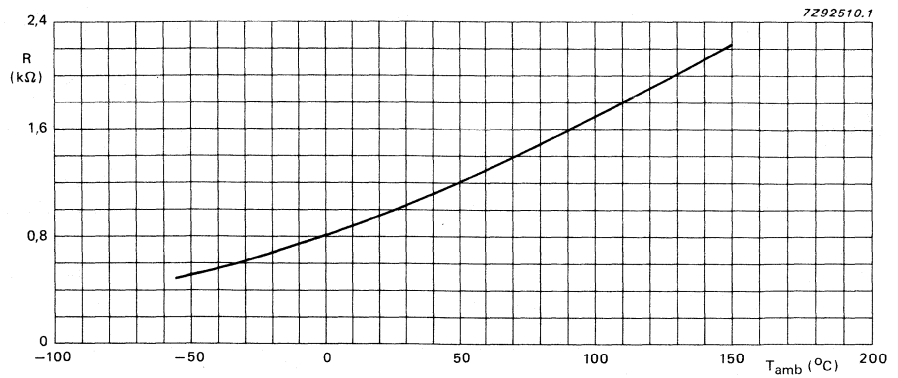
Notes

1. The thermal time constant is the time the sensor needs to reach 63.2% of the total temperature difference. For example, the time needed to reach a temperature of 72.4 °C, when a sensor with an initial temperature of 25 °C is put into an ambient with a temperature of 100 °C.
2. Inert liquid FC43 by 3M.

AMBIENT TEMPERATURES AND CORRESPONDING RESISTANCE OF SENSOR

I_{cont} = 1 mA.

AMBIENT TEMPERATURE (°C)	RESISTANCE (Ω)
−55	490
−50	515
−40	567
−30	624
−20	684
−10	747
0	815
10	886
20	961
25	1000
30	1040
40	1122
50	1209
60	1299
70	1392
80	1490
90	1591
100	1696
110	1805
120	1915
125	1969
130	2023
140	2124
150	2211



I_{cont} = 1 mA.

Fig.2 Average resistance value of sensor as a function of ambient temperature.

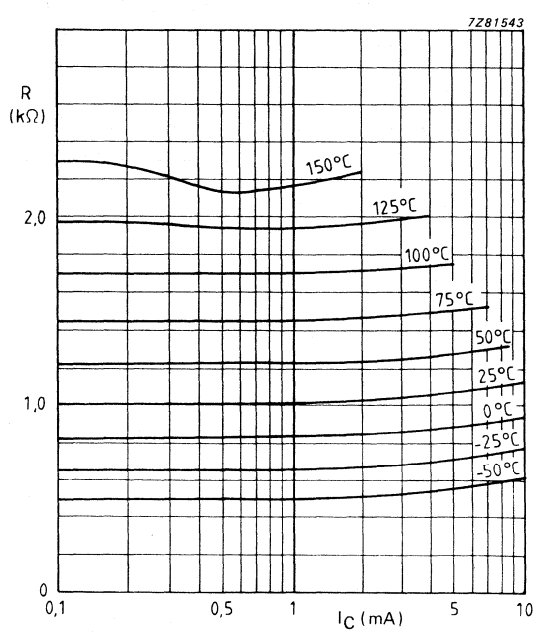


Fig.3 Sensor resistance as a function of operating current.

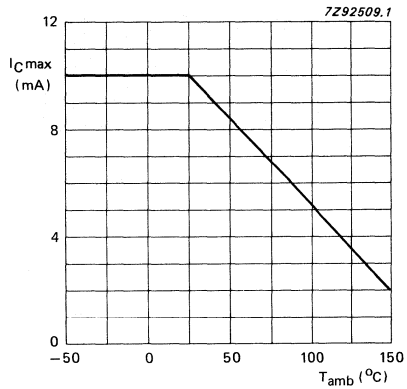
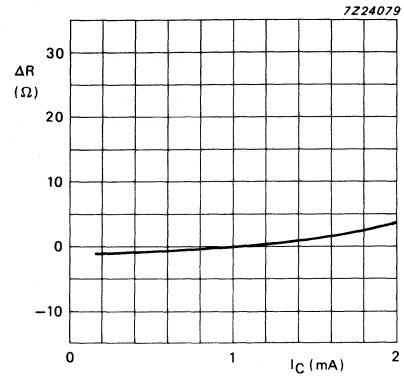


Fig.4 Maximum operating current for safe operation.



T_{amb} = 25 °C.

Fig.5 Deviation of sensor resistance as a function of operating current in still liquid.

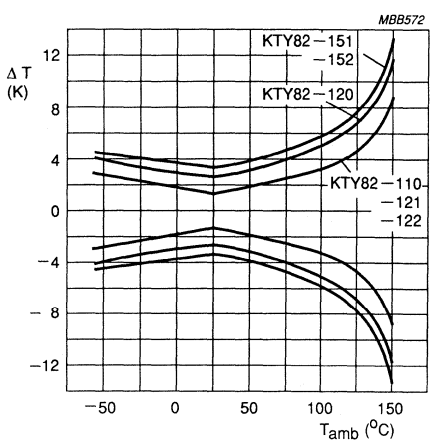


Fig.6 Maximum expected temperature error (ΔT).

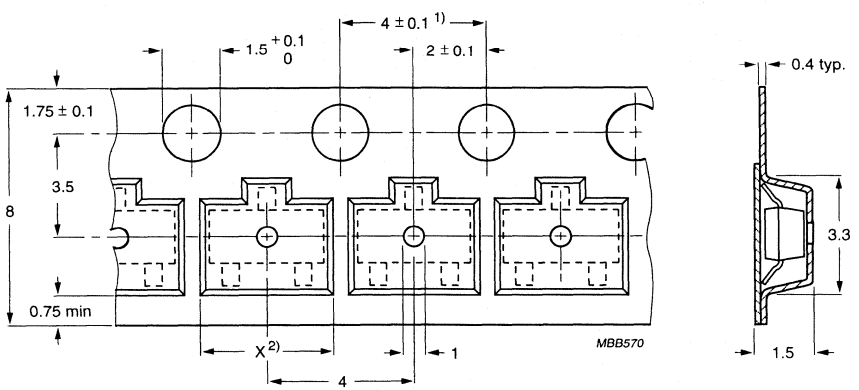
Note

To keep the temperature error low, an operating current of I_{cont} = 1 mA is recommended for temperatures above 100 °C.

PACKING DIMENSIONS

Tape specification

Sensors in SOT23 encapsulation are delivered in reel packing for automatic placement on hybrid circuits and printed circuit boards. The devices are placed with the mounting side downwards in compartments.



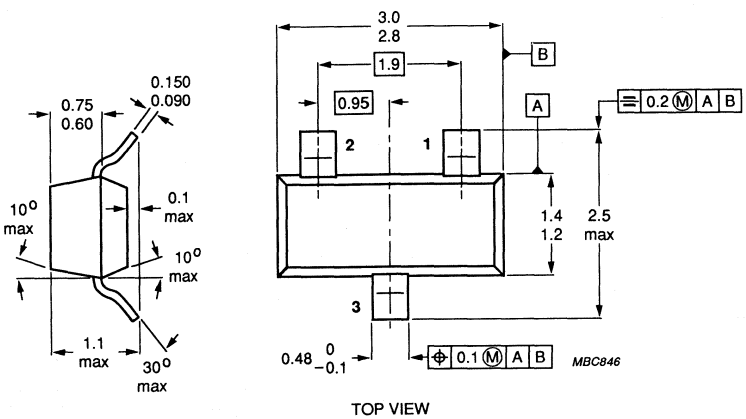
Dimensions in mm.

1) Tolerance over any 10 pitches: ±0.2 mm.

X = component length + 0.2 mm.

Fig.7 Configuration of bandolier.

PACKAGE OUTLINE



Dimensions in mm.

Weight: 0.01 g.

Fig.8 SOT23.

Silicon temperature sensors KTY82-2 series

DESCRIPTION

These temperature sensors have a positive temperature coefficient of resistance and are for use in measurement and control systems.

Marking codes:

KTY82-210: 210.
KTY82-220: 220.
KTY82-221: 221.
KTY82-222: 222.
KTY82-250: 250.
KTY82-251: 251.
KTY82-252: 252.

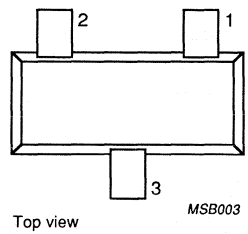


Fig.1 Simplified outline.

PINNING

PIN	DESCRIPTION
1	electrical contact
2	electrical contact
3	substrate (must remain potential free)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
R_{25}	sensor resistance	T_{amb} = 25 °C; I_{cont} = 1 mA			
	KTY82-210		1980	2020	Ω
	KTY82-220		1960	2040	Ω
	KTY82-221		1960	2000	Ω
	KTY82-222		2000	2040	Ω
	KTY82-250		1900	2100	Ω
	KTY82-251		1900	2000	Ω
	KTY82-252		2000	2100	Ω
T_{amb}	ambient operating temperature range		−55	150	°C

Note

Tolerances of 0.5% or other special selections available on request.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{cont}	continuous sensor current	in free air; T_{amb} = 25 °C	–	10	mA
		in free air; T_{amb} = 150 °C	–	2	mA
T_{amb}	ambient operating temperature range		–55	150	°C

CHARACTERISTICS

T_{amb} = 25 °C, in liquid, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_{25}	sensor resistance	T_{amb} = 25 °C; I_{cont} = 1 mA				
	KTY82-210		1980	–	2020	Ω
	KTY82-220		1960	–	2040	Ω
	KTY82-221		1960	–	2000	Ω
	KTY82-222		2000	–	2040	Ω
	KTY82-250		1900	–	2100	Ω
	KTY82-251		1900	–	2000	Ω
	KTY82-252		2000	–	2100	Ω
TC	temperature coefficient		–	0.79	–	%/K
R_{100}/R_{25}	resistance ratio	at T_{amb} = 100 °C and 25 °C	1.676	1.696	1.716	
R_{-55}/R_{25}	resistance ratio	at T_{amb} = –55 °C and 25 °C	0.480	0.490	0.500	
τ	thermal time constant (note 1)	in still air	–	7	–	s
		in still liquid (note 2)	–	1	–	s
		in flowing liquid	–	0.5	–	s
	rated temperature range (note 3)		–55	–	150	°C

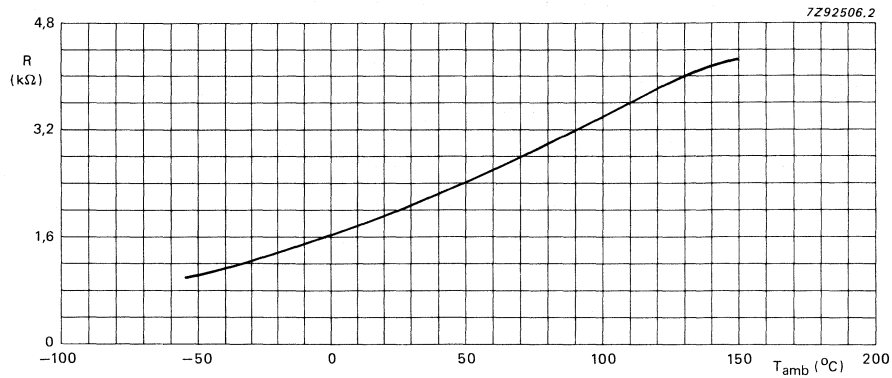
Notes

1. The thermal time constant is the time the sensor needs to reach 63.2% of the total temperature difference. For example, the time needed to reach a temperature of 72.4 °C, when a sensor with an initial temperature of 25 °C is put into an ambient with a temperature of 100 °C.
2. Inert liquid FC43 by 3M.
3. Restricted accuracy in the temperature range 125 to 150 °C.

AMBIENT TEMPERATURES AND CORRESPONDING RESISTANCE OF SENSOR

I_{cont} = 1 mA.

AMBIENT TEMPERATURE (°C)	RESISTANCE (Ω)
−55	980
−50	1030
−40	1135
−30	1247
−20	1367
−10	1495
0	1630
10	1772
20	1922
25	2000
30	2080
40	2245
50	2417
60	2597
70	2785
80	2980
90	3182
100	3392
110	3607
120	3817
125	3915
130	4008
140	4166
150	4280



I_{cont} = 1 mA.

Fig.2 Average resistance value of sensor as a function of ambient temperature.

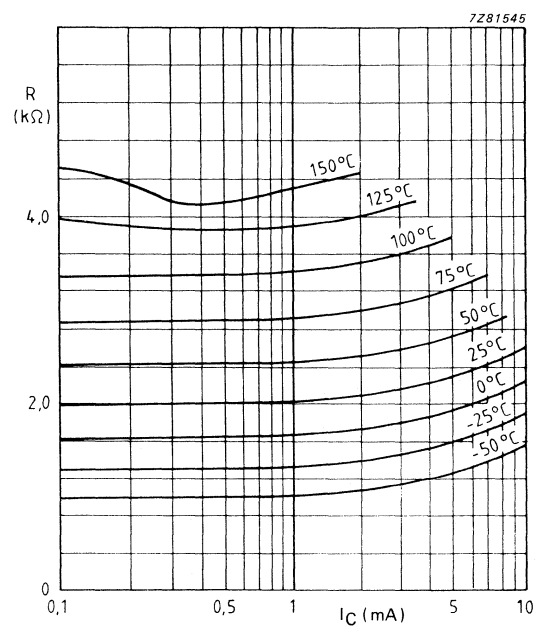


Fig.3 Sensor resistance as a function of operating current (ΔT).

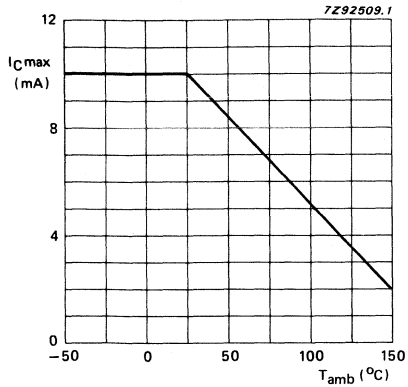
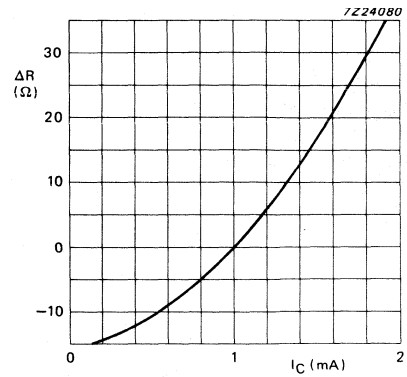


Fig.4 Maximum operating current for safe operation.



T_{amb} = 25 °C.

Fig.5 Deviation of sensor resistance as a function of operating current in still liquid.

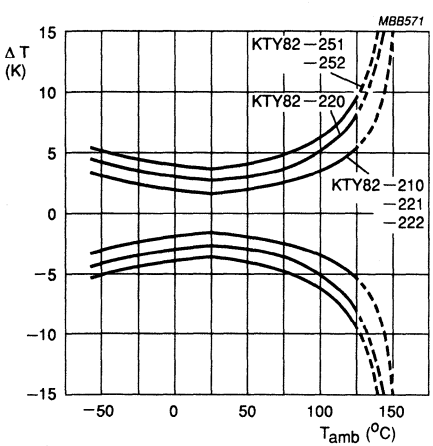


Fig.6 Maximum expected temperature error (ΔT).

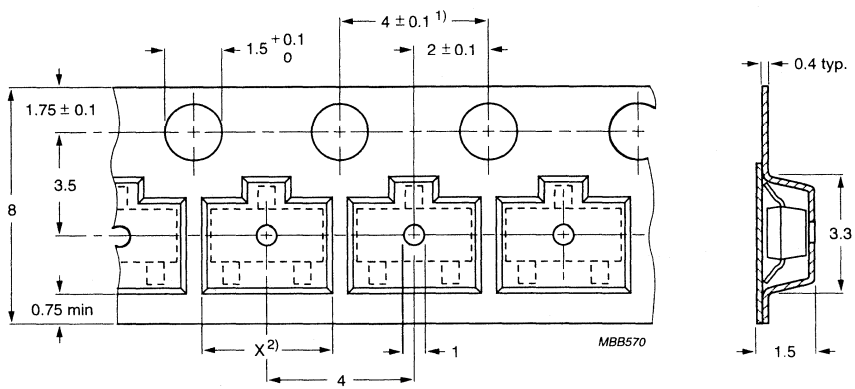
Note

To keep the temperature error low, an operating current of I_{cont} = 1 mA is recommended for temperatures above 100 °C.

PACKING DIMENSIONS

Tape specification

Sensors in SOT23 encapsulation are delivered in reel packing for automatic placement on hybrid circuits and printed circuit boards. The devices are placed with the mounting side downwards in compartments.



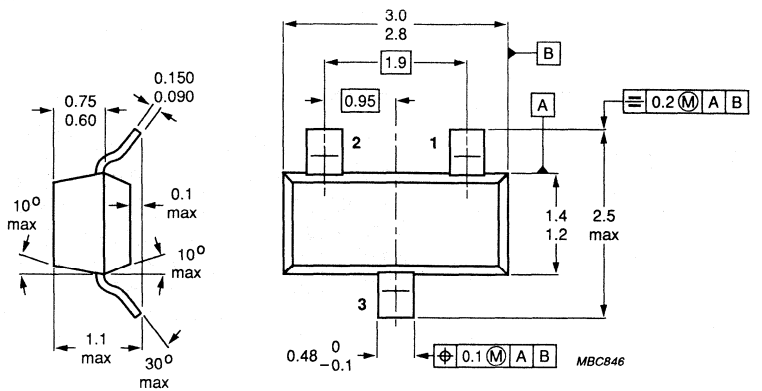
Dimensions in mm.

1) Tolerance over any 10 pitches: ±0.2 mm.

X = component length + 0.2 mm.

Fig.7 Configuration of bandolier.

PACKAGE OUTLINE



TOP VIEW

Dimensions in mm.

Weight: 0.01 g.

Fig.8 SOT23.

SILICON TEMPERATURE SENSORS

These sensors have a positive temperature coefficient of resistance and are for use in measurement and control.

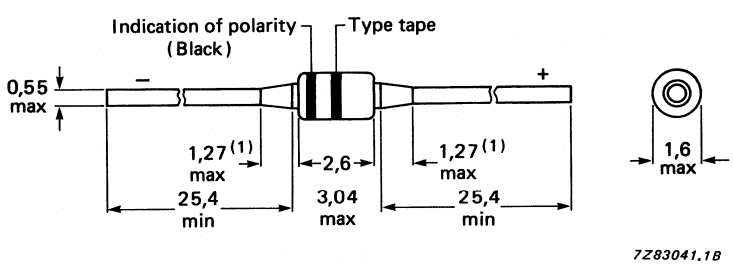
QUICK REFERENCE DATA

Resistance at T_{amb} = 25 °C I_C = 1 mA		Type tape (identification colour)
	KTY83-110	R_{25} = 990 - 1010 Ω; yellow
	KTY83-120	R_{25} = 980 - 1020 Ω; red
	KTY83-121	R_{25} = 980 - 1000 Ω; white
	KTY83-122	R_{25} = 1000 - 1020 Ω; green
	KTY83-150	R_{25} = 950 - 1050 Ω; grey
	KTY83-151	R_{25} = 950 - 1000 Ω; black
	KTY83-152	R_{25} = 1000 - 1050 Ω; blue

Operating ambient temperature range T_{amb} —55 to +175 °C

MECHANICAL DATA

Dimensions in mm



(1) Lead diameter in this zone uncontrolled

Fig.1 SOD68 (DO-34)

Note

The sensor has to be operated with the lower potential at the marked connection (black type).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Continuous sensor current in free air

T_{amb} = 25 °C	I_C	max.	10 mA
T_{amb} = 175 °C	I_C	max.	2.0 mA

CHARACTERISTICS

(Based on the measurements in liquid at T_{amb} = 25 °C unless otherwise specified)

Resistance

I_C = 1 mA

KTY83-110	R_{25} = 990 - 1010 Ω
KTY83-120	R_{25} = 980 - 1020 Ω
KTY83-121	R_{25} = 980 - 1000 Ω
KTY83-122	R_{25} = 1000 - 1020 Ω
KTY83-150	R_{25} = 950 - 1050 Ω
KTY83-151	R_{25} = 950 - 1000 Ω
KTY83-152	R_{25} = 1000 - 1050 Ω

Temperature coefficient		typ.	0.76 %/K
Resistance ratio	R100/R25		1.67 ± 0.02
	R-55/R25		0.50 ± 0.01
Thermal time constant*			
in still air		typ.	20 s
in still liquid**		typ.	1.0 s
in flowing liquid**		typ.	0.5 s
Measuring temperature range			−55 to +175 °C

T_{amb} °C	Resistance Ω
−55	500
−50	525
−40	577
−30	632
−20	691
−10	754
0	820
10	889
20	962
25	1000
30	1039
40	1118
50	1202
60	1288

T_{amb} °C	Resistance Ω
70	1379
80	1472
90	1569
100	1670
110	1774
120	1882
125	1937
130	1993
140	2107
150	2225
160	2346
170	2471
175	2535

Ambient temperatures and corresponding resistance values of sensor (I_C = 1 mA).

* The thermal time constant is the time the sensor needs to reach 63.2% of the total temperature difference. For instance, the time needed to reach a temperature of 72.4 °C, when a sensor with an initial temperature of 25 °C is put into an ambient with a temperature of 100 °C.

** Inert liquid FC43 of 3M company.

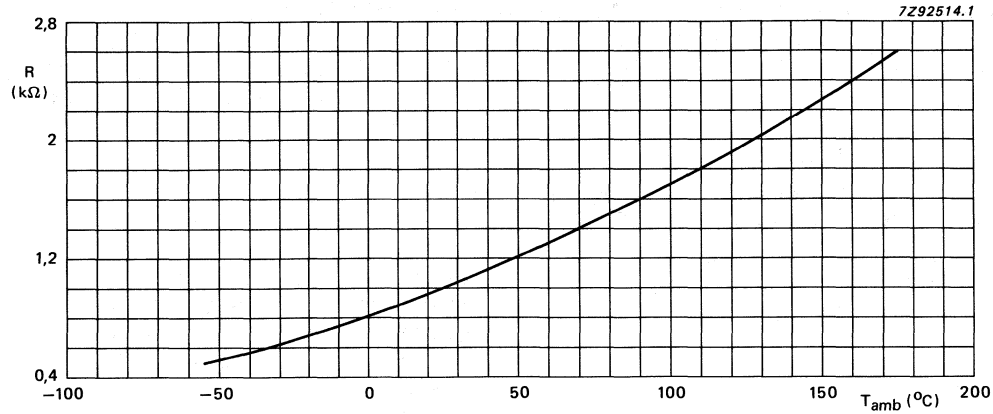


Fig. 2 Average resistance value of sensor at I_C = 1 mA as a function of temperature.

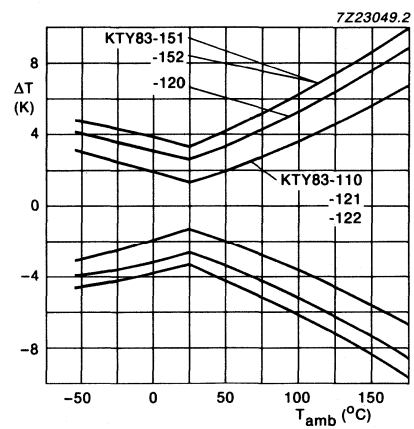


Fig. 3 Maximum expected temperature error ΔT.

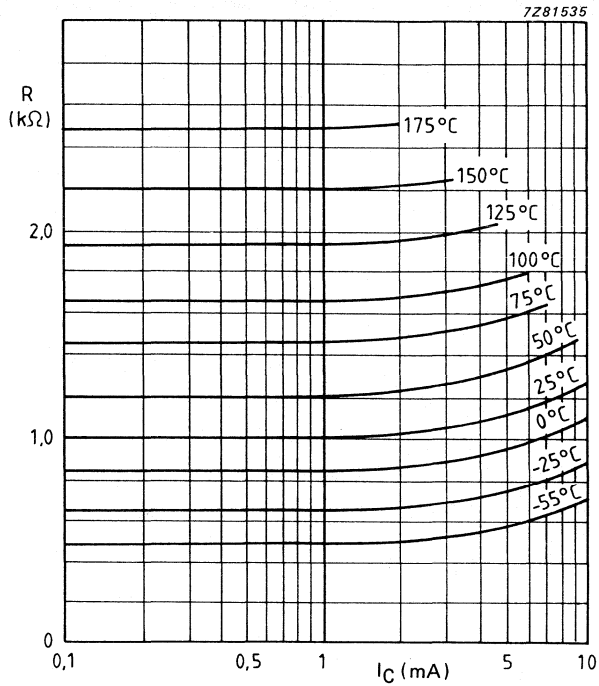


Fig. 4 Sensor resistance as a function of operating current.

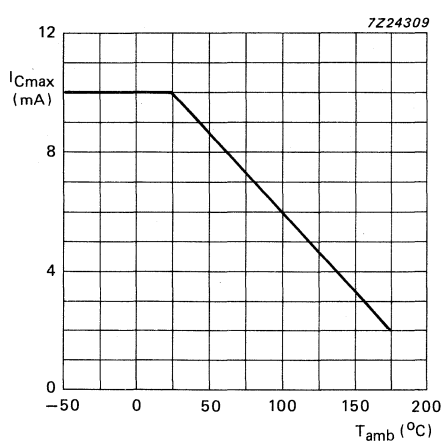


Fig. 5 Maximum operating current for safe operation.

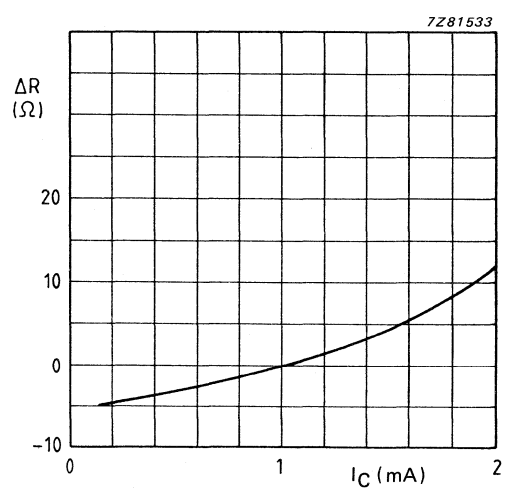


Fig. 6 Resistance deviation as a function of measuring current in still liquid; T_{amb} = 25 °C.

Silicon temperature sensors KTY84-130/150/151/152

DESCRIPTION

These temperature sensors have a positive temperature coefficient of resistance and are for use in measurement and control over a temperature range of –40 to +300 °C.

PACKAGE OUTLINE

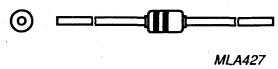


Fig.1 Simplified outline.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT	TYPE TAPE (IDENTIFICATION COLOUR)
R_{100}	resistance	T_{amb} = 100 °C;				
	KTY84-130	I_{cont} = 2 mA	970	1030	Ω	yellow
	KTY84-150		950	1050	Ω	grey
	KTY84-151		950	1000	Ω	black
	KTY84-152		1000	1050	Ω	blue

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{cont}	continuous sensor current	in free air; T_{amb} = 25 °C; (note 1)	–	10	mA
		in free air; T_{amb} = 300 °C	–	2	mA
T_{amb}	operating temperature range		–40	300	°C
T_{stg}	storage temperature range		–55	300	°C

Note

1. For temperatures greater than 200 °C, a sensor current of I_{cont} = 2 mA must be used.

CHARACTERISTICS

T_{amb} = 100 °C, in liquid, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_{100}	resistance	I_{cont} = 2 mA				
	KTY84-130		970	–	1030	Ω
	KTY84-150		950	–	1050	Ω
	KTY84-151		950	–	1000	Ω
	KTY84-152		1000	–	1050	Ω
TC	temperature coefficient		–	0.62	–	%/K
R_{250}/R_{100}	resistance ratio		2.140	2.195	2.250	
R_{25}/R_{100}	resistance ratio		0.590	0.598	0.606	
τ	thermal time constant (note 1)					
		in still air	–	20	–	s
		in still liquid (note 2)	–	1	–	s
		in flowing liquid (note 2)	–	0.5	–	s

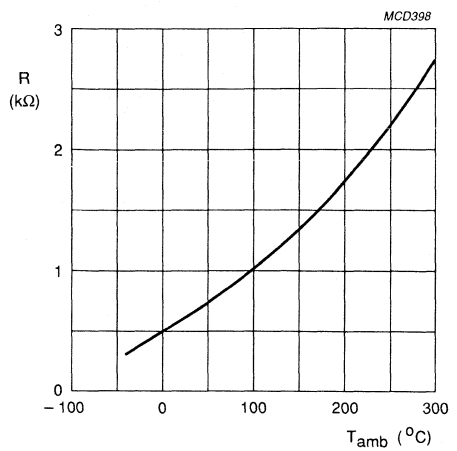
Notes

1. The thermal time constant is the time the sensor needs to reach 63.2% of the total temperature difference. For example, the time needed to reach a temperature of 72.4 °C, when a sensor with an initial temperature of 25 °C is put into an ambient with a temperature of 100 °C.
2. Inert liquid FC43 by 3M.

AMBIENT TEMPERATURES AND CORRESPONDING RESISTANCE OF SENSOR

I_{cont} = 2 mA.

AMBIENT TEMPERATURE (°C)	RESISTANCE (Ω)
−40	355
−30	386
−20	419
−10	455
0	493
10	533
20	576
25	598
30	621
40	668
50	718
60	769
70	824
80	880
90	939
100	1000
110	1063
120	1129
130	1197
140	1268
150	1340
160	1415
170	1493
180	1572
190	1654
200	1739
210	1825
220	1914
230	2006
240	2099
250	2195
260	2293
270	2392
280	2490
290	2584
300	2668



I_{cont} = 2 mA.

Fig.2 Resistance value of sensor as a function of ambient temperature.

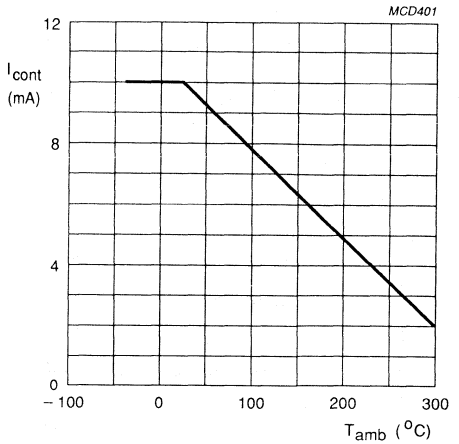
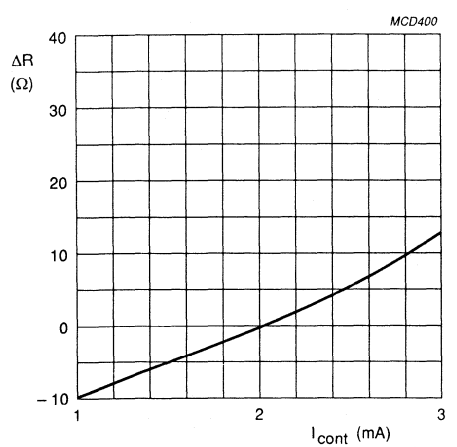


Fig.3 Maximum operating current for safe operation.



T_{amb} = 100 °C.

Fig.4 Deviation of sensor resistance as a function of operating current in still liquid.

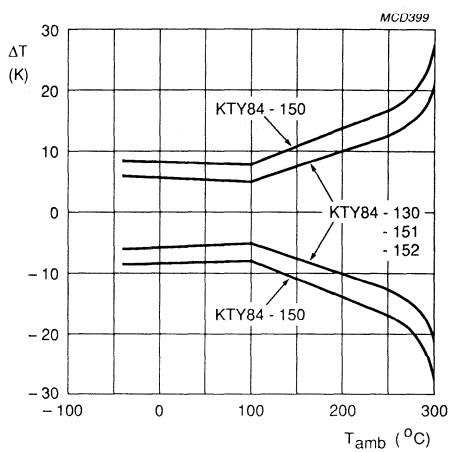
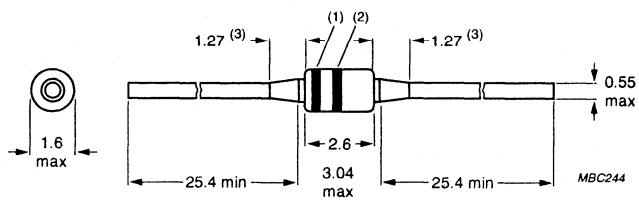


Fig.5 Maximum expected temperature error.



Dimensions in mm.

(1) Indication of polarity (green).

(2) Type tape.

(3) Lead diameter within this zone is not controlled.

Fig.6 SOD68 (DO-34).

SILICON TEMPERATURE SENSORS

These sensors have a positive temperature coefficient of resistance and are for use in measurement and control.

QUICK REFERENCE DATA

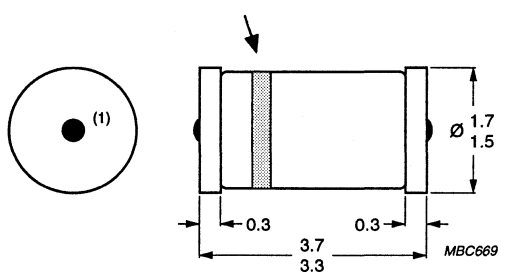
Resistance at T_{amb} = 25 °C I_C = 1 mA		Type tape (identification colour)
KTY85-110	R_{25} = 990 - 1010 Ω	yellow
KTY85-120	R_{25} = 980 - 1020 Ω	red
KTY85-121	R_{25} = 980 - 1000 Ω	white
KTY85-122	R_{25} = 1000 - 1020 Ω	green
KTY85-150	R_{25} = 950 - 1050 Ω	grey
KTY85-151	R_{25} = 950 - 1000 Ω	black
KTY85-152	R_{25} = 1000 - 1050 Ω	blue

Operating ambient temperature range T_{amb} —40 to +125 °C

MECHANICAL DATA

Dimensions in mm

Indication of polarity and type tape



(1) Area not tinned; small elevations are possible.

Fig. 1 SOD-80.

Note

The sensor has to be operated with the lower potential at the marked connection.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Continuous sensor current in free air			
T_{amb} = 25 °C	I_C	max.	10 mA
T_{amb} = 125 °C	I_C	max.	2.0 mA

CHARACTERISTICS

(Based on the measurements in liquid at T_{amb} = 25 °C unless otherwise specified)

Resistance			
I_C = 1 mA	KTY85-110	R_{25} = 990 - 1010 Ω	
	KTY85-120	R_{25} = 980 - 1020 Ω	
	KTY85-121	R_{25} = 980 - 1000 Ω	
	KTY85-122	R_{25} = 1000 - 1020 Ω	
	KTY85-150	R_{25} = 950 - 1050 Ω	
	KTY85-151	R_{25} = 950 - 1000 Ω	
	KTY85-152	R_{25} = 1000 - 1050 Ω	
Temperature coefficient		typ.	0.76 %/K
Resistance ratio		R100/R25	1.670 ± 0.020
		R-40/R25	0.577 ± 0.008
Thermal time constant*			
in still air		typ.	20 s
in still liquid**		typ.	1.0 s
in flowing liquid**		typ.	0.5 s
Measuring temperature range			−40 to +125 °C

* The thermal time constant is the time the sensor needs to reach 63.2% of the total temperature difference. For instance, the time needed to reach a temperature of 72.4 °C, when a sensor with an initial temperature of 25 °C is put into an ambient with a temperature of 100 °C.

** Inert liquid FC43 of 3M company.

T_{amb} °C	Resistance Ω
−40	577
−30	632
−20	691
−10	754
0	820
10	889
20	962
25	1000
30	1039
40	1118
50	1202
60	1288
70	1379
80	1472
90	1569
100	1670
110	1774
120	1882
125	1937

Ambient temperatures and corresponding resistance values of sensor (I_C = 1mA).

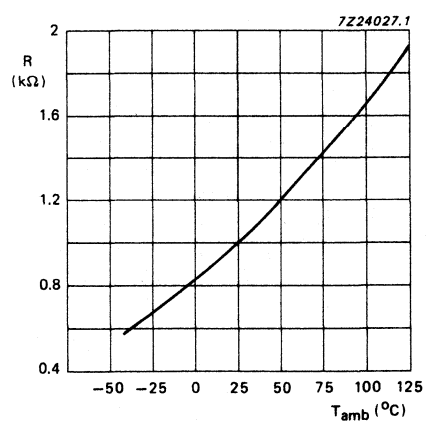


Fig. 2 Average resistance value of sensor at I_C = 1 mA as a function of ambient temperature.

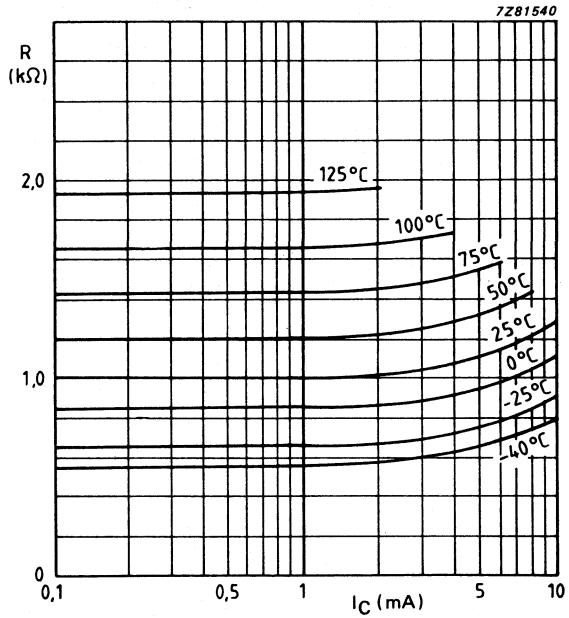


Fig. 3 Sensor resistance as a function of operating current.

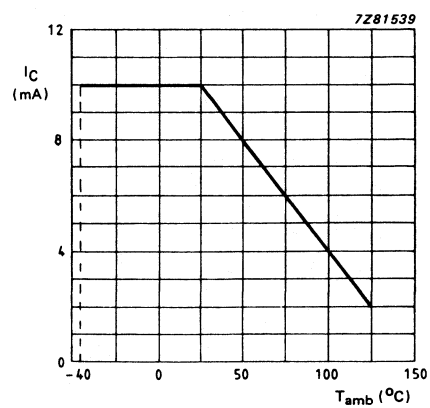


Fig. 4 Maximum operating current for safe operation.

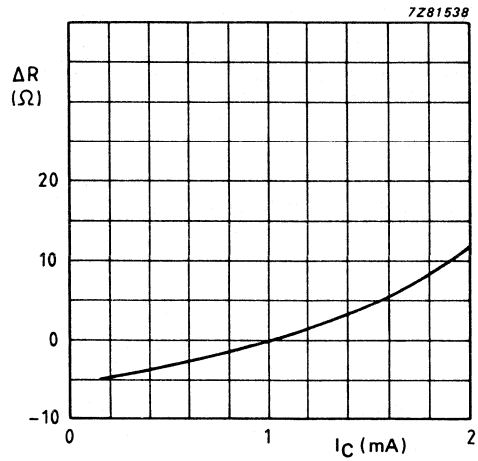


Fig. 5 Deviation of sensor resistance R as a function of operating current I_C in still liquid; T_{amb} = 25 °C.

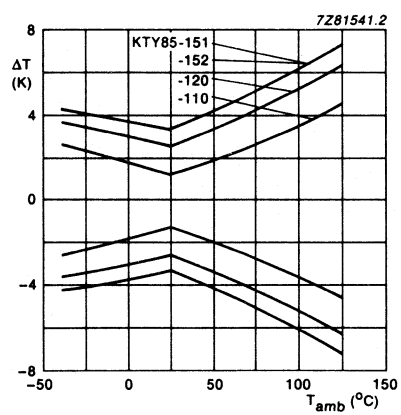


Fig. 6 Maximum expected temperature error ΔT.

SILICON TEMPERATURE SENSORS

These sensors are high accuracy temperature sensors with a positive temperature coefficient of resistance. Each sensor consists of a pair of 1000 Ω sensors in series and its main application fields are the measurement and control of temperature.

QUICK REFERENCE DATA

Resistance at T_{amb} = 25 °C I_C = 0.1 mA	KTY86-205	R_{25}	2000 ± 10 Ω
Operating ambient temperature range		T_{amb}	−40 to + 150 °C

MECHANICAL DATA

Dimensions in mm

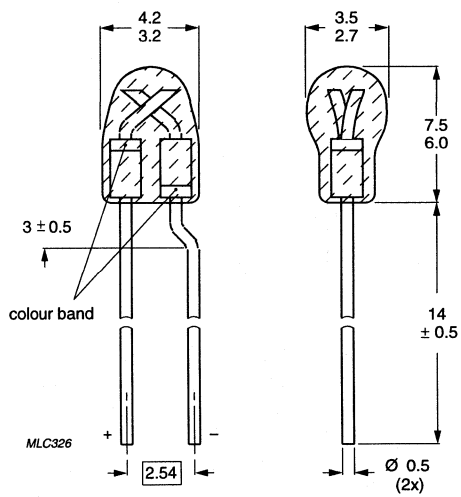


Fig.1 SOD103; colour band is white.

Note

The sensor has to be operated with the lower potential at the bent lead.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Continuous sensor current in free air			
T_{amb} = 25 °C	I_C	max.	10 mA
T_{amb} = 150 °C	I_C	max.	2.0 mA

CHARACTERISTICS

(Based on the measurements in liquid at T_{amb} = 25 °C; I_C = 0.1 mA unless otherwise specified).

Resistance	KTY86-205	R_{25} =	2000 ± 10	Ω
Resistance ratio				
$R_{100\ °C}/R_{25\ °C}$			1.672 ± 0.020	
$R_{-40\ °C}/R_{25\ °C}$			0.577 ± 0.008	
Temperature coefficient		α_{-40}	0.93	%/K
		α_{25}	0.76	%/K
		α_{100}	0.61	%/K
Thermal time constant*				
in still air		typ.	30	s
in still liquid**		typ.	2.2	s
in flowing liquid**		typ.	1.7	s
Measuring temperature range			−40 to +150	°C

* The thermal time constant is the time the sensor needs to reach 63.2% of the total temperature difference, for instance, the time needed to reach a temperature of 72.4 °C, when a sensor with an initial temperature of 25 °C is put into an ambient with a temperature of 100 °C.

** Inert liquid FC43 of 3M company.

T_{amb} °C	Resistance Ω
−40	1154
−30	1265
−20	1383
−10	1508
0	1640
10	1779
20	1924
25	2000
30	2077
40	2237
50	2404
60	2578
70	2759
80	2947
90	3142
100	3344
110	3553
120	3769
130	3992
140	4222
150	4459

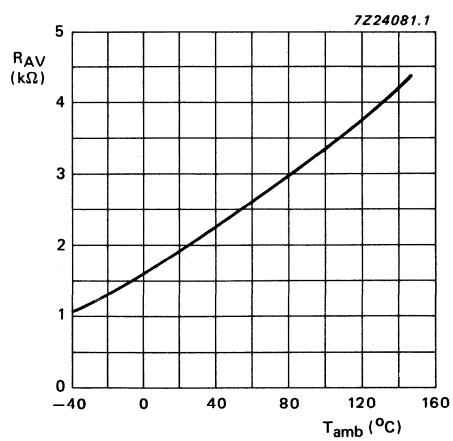


Fig. 2 Average resistance value of sensor at I_C = 0.1 mA as a function of ambient temperature.

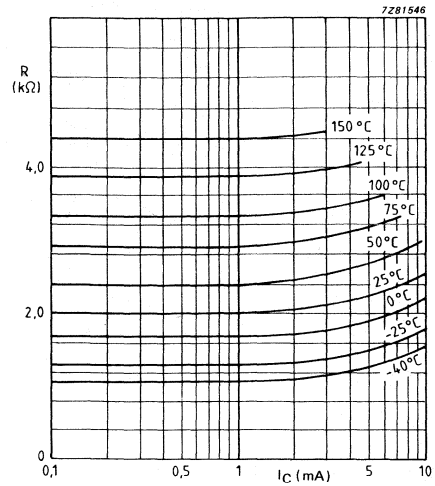


Fig. 3 Sensor resistance as a function of operating current.

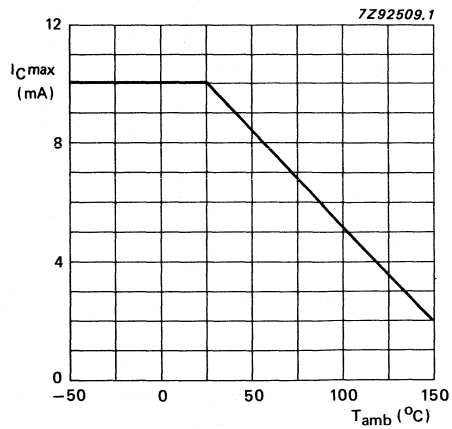


Fig. 4 Maximum operating current for safe operation.

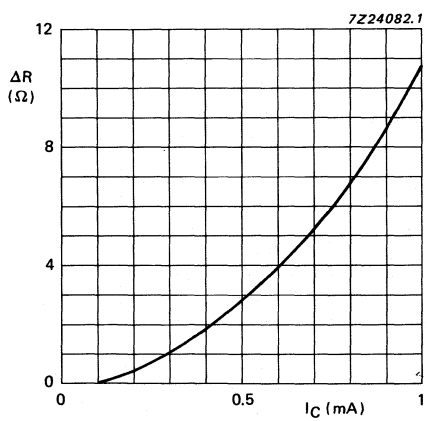


Fig. 5 Deviation of sensor resistance R as a function of operating current I_C in still liquid; T_{amb} = 25 °C.

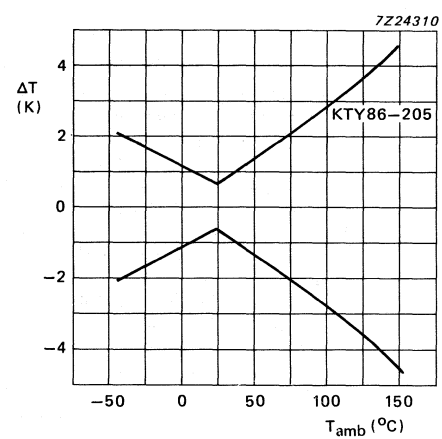


Fig. 6 Maximum expected temperature error ΔT.

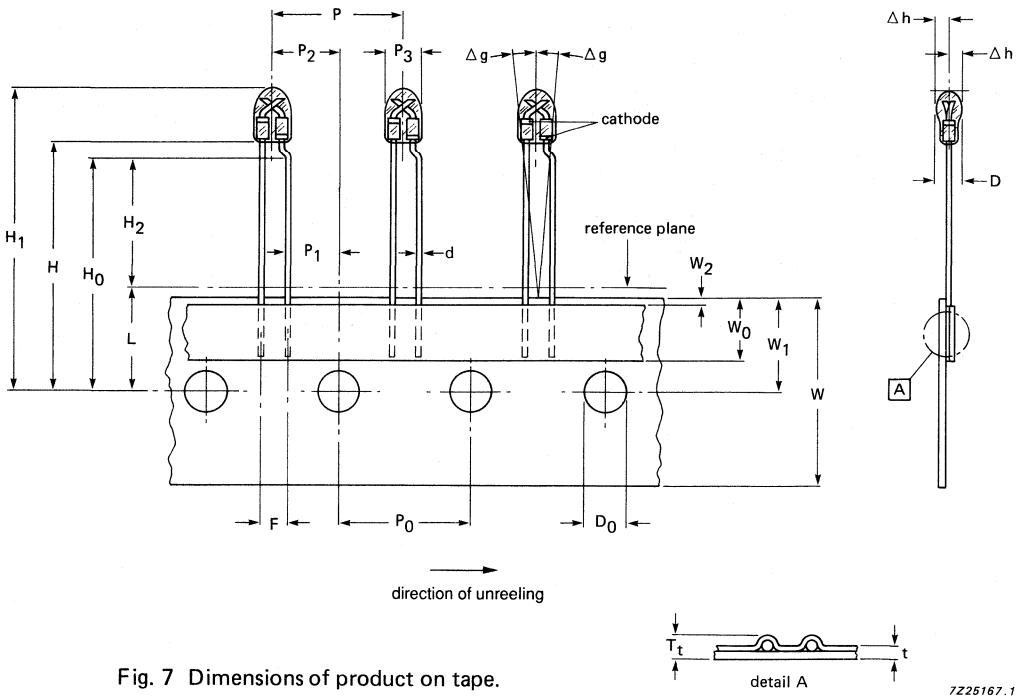


Fig. 7 Dimensions of product on tape.

Table 1 Dimensions of product on tape

symbol	dimensions
D	2.7 - 3.5
D_0	4.0 ± 0.2
d	0.48 - 0.55
F	2.54 + 0.4/−0.1
Δg	0 + 5°
H	24.5 max.
H_0	22.0 max.
H_1	32.0 max.
H_2	12.0 max.
Δh	± 2.0
L	10.0 max.

symbol	dimensions
P	12.7 ± 1.0
P_0	12.7 ± 0.3
P_1	5.09 ± 0.7
P_2	5.95 ± 1.0
P_3	3.2 - 4.2
Tt	1.5 max.
t	0.7 ± 0.2
W	18.0 ± 1.0/−0.5
W_0	6.0 min.
W_1	9.0 ± 0.5
W_2	0 - 1.5

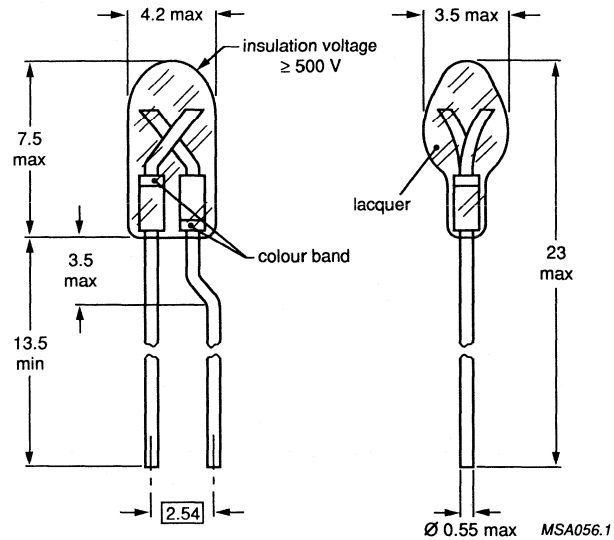


Fig.8 Dimensions of product cut out of tape.

SILICON TEMPERATURE SENSORS

The KTY87 are high precision temperature sensors with a positive temperature coefficient of resistance for temperature measuring and temperature control. In the temperature range 10 °C to 110 °C the measuring accuracy is better than ± 1 °C.

QUICK REFERENCE DATA

Resistance at I_C = 0.1 mA	
T_{amb} = 25 °C	R_{25} = 2000 ± 10 Ω
T_{amb} = 100 °C	R100 = 3344 ± 17 Ω
Operating temperature range	−40 to + 125 °C

MECHANICAL DATA

Dimensions in mm

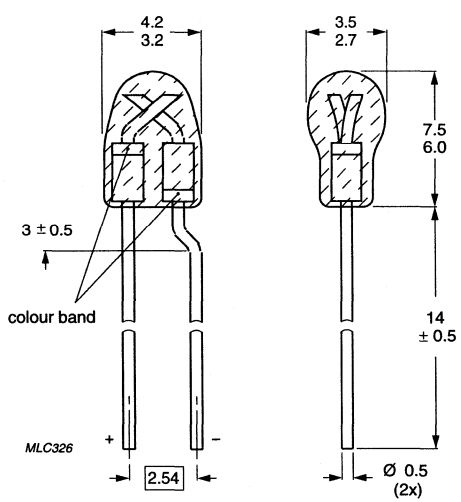


Fig.1 SOD103; colour band is green.

Notes

1. The sensor has to be operated with the lower potential at the bent lead.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Continuous sensor current in free air				
T_{amb} = 25 °C	I_C	max.	10	mA
T_{amb} = 125 °C	I_C	max.	2.0	mA

CHARACTERISTICS

(Based on the measurements in liquid at T_{amb} = 25 °C; I_C = 0.1 mA unless otherwise specified)

Resistance				
T_{amb} = 100 °C	R25	=	2000 ± 10	Ω
	R100	=	3344 ± 17	Ω
Temperature coefficient	at −40 °C	=	0.93	%/K
	at 25 °C	=	0.75	%/K
	at 100 °C	=	0.61	%/K
Resistance ratio	R−40/R25	=	0.577 ± 0.008	
Thermal time constant*				
in still air		typ.	30	s
in still liquid**		typ.	2.2	s
in flowing liquid**		typ.	1.7	s
Operating temperature range			−40 to + 125	°C

* The thermal time constant is the time the sensor needs to reach 63.2% of the total temperature difference. For instance, the time needed to reach a temperature of 72.4 °C, when a sensor with an initial temperature of 25 °C is put into an ambient with a temperature of 100 °C.

** Inert liquid FC43 of 3M company.

T_{amb} °C	Resistance Ω
−40	1154
−30	1265
−20	1383
−10	1508
0	1640
10	1779
20	1924
25	2000
30	2077
40	2237
50	2404
60	2578
70	2759
80	2947
90	3142
100	3344
110	3553
120	3769
125	3880

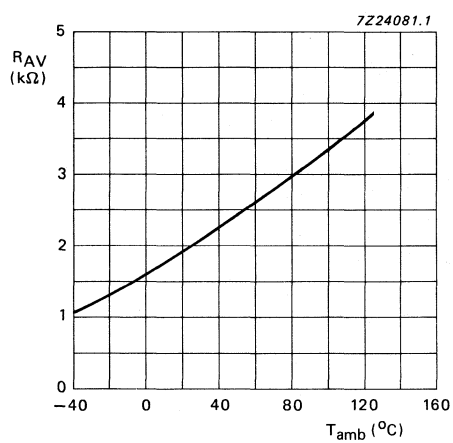


Fig. 2 Average resistance value of sensor at I_C = 0.1 mA as a function of ambient temperature.

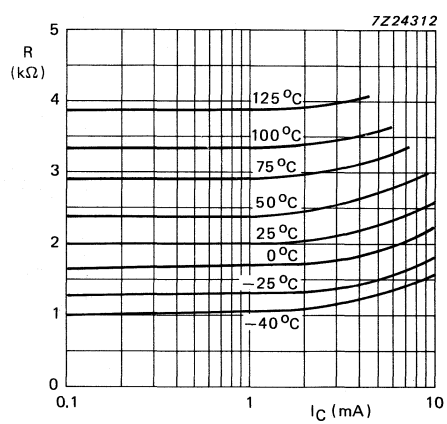


Fig. 3 Sensor resistance as a function of operating current.

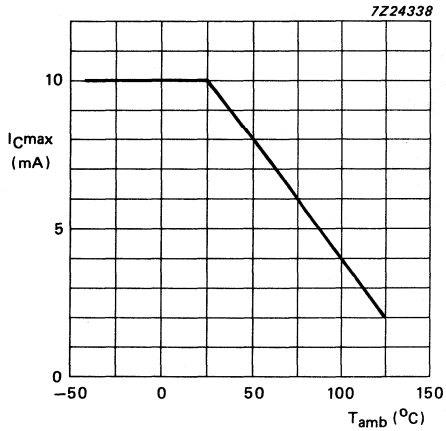


Fig. 4 Maximum operating current for safe operation.

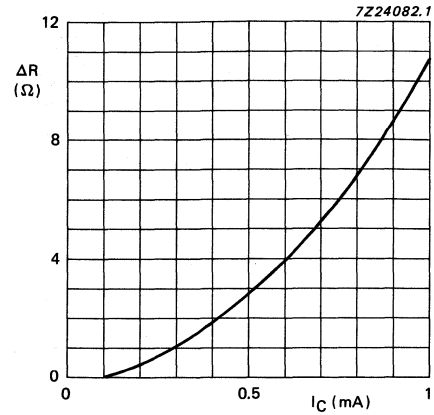


Fig. 5 Deviation of sensor resistance R versus operating current I_C in still liquid.

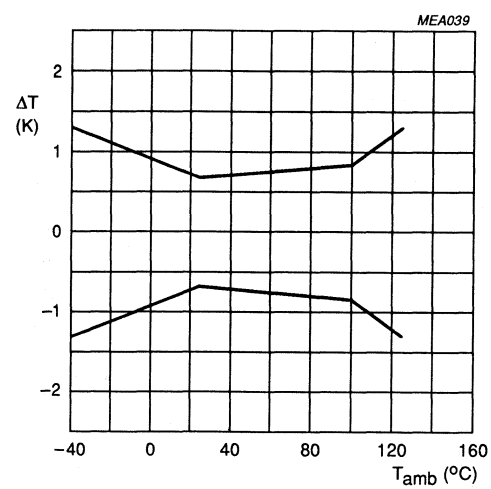


Fig. 6 Maximum temperature error ΔT.

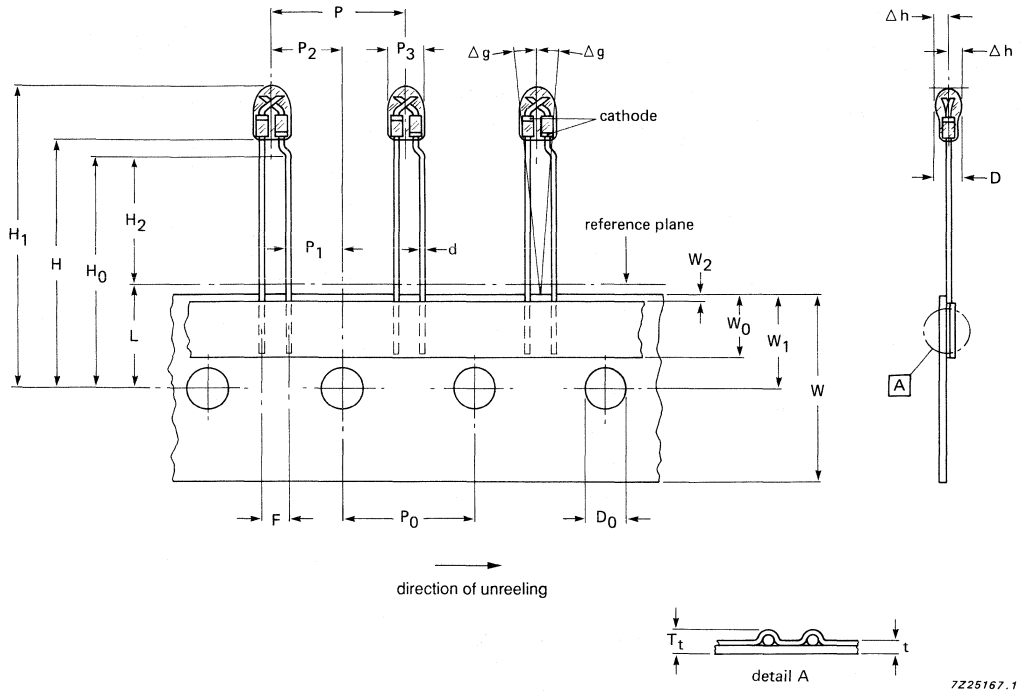


Table 1 Dimensions of product on tape

symbol	dimensions
D	2.7 – 3.5
D_0	4.0 ±0.2
d	0.48 – 0.55
F	2.54 +0.4/–0.1
Δg	0 +5°
H	24.5 max.
H_0	22.0 max.
H_1	32.0 max.
H_2	12.0 max.
Δh	±2.0
L	10.0 max
P	12.7 ±1.0
P_0	12.7 ±0.3
P_1	5.09 ±0.7
P_2	5.95 ±1.0
P_3	3.2 – 4.2
Tt	1.5 max
t	0.7 ±0.2
W	18.0 + 1.0/–0.5
W_0	6.0 min
W_1	9.0 ±0.5
W_2	0 – 1.5

Fig. 7 Dimensions of product on tape.

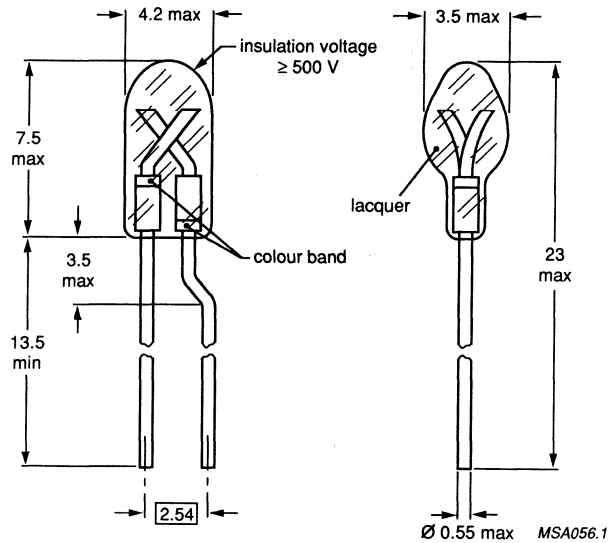


Fig.8 Dimensions of product cut out of tape.

INTRODUCTION

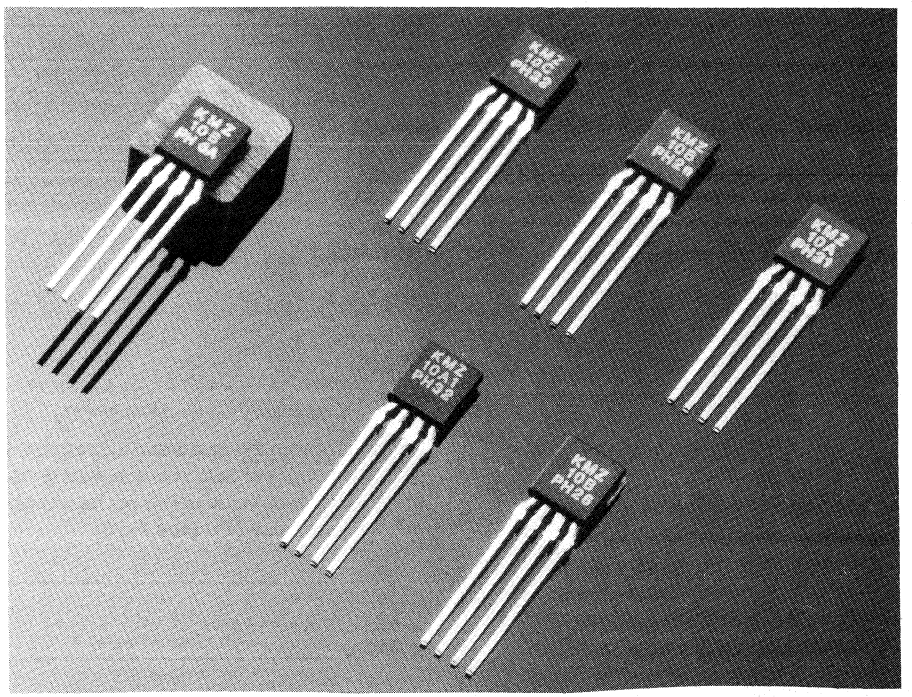


Fig.1 The KMZ magnetoresistive sensors.

The KMZ range of magnetoresistive sensors is characterized by high sensitivity, a wide operating temperature range, a low and stable offset and low sensitivity to mechanical stress. They therefore provide an excellent means of measuring both linear and angular displacement under extreme environmental conditions. This is because a quite small movement of actuating components in e.g. cars or machinery (gear wheels, metal rods, cogs, cams, etc.) can create measurable changes in magnetic field. Another typical application of magnetoresistive sensors is current measurement.

Examples where their properties can be put to good effect can be found in automotive applications, e.g. wheel speed sensors for ABS systems and position sensors for chassis position, throttle and pedal position measurement. Other examples include instrumentation and control equipment, which often require position sensors capable of detecting displacements in the region of tenths of a millimetre (or even less) and in electronic ignition systems, which must be able to determine the angular position of an internal combustion engine with great accuracy.

In many of the above mentioned applications it is advantageous to have the required magnet already glued onto the sensor. With the KM110B series Philips Semiconductors offers a number of sensor-magnet combinations which simplify the use of magnetoresistive sensors in many applications.

Finally, because of their high sensitivity, magnetoresistive sensors can measure very weak magnetic fields and are thus ideal for application in electronic compasses.

If the KMZ sensors are to be used to maximum advantage, however, it is important to have a clear understanding of their operating principles and characteristics, and of how their behaviour may be affected by external influences and by their magnetic history.

Table 1 The KMZ10 range of magnetic field sensors

PARAMETER	KMZ10A	KMZ10A1	KMZ10B	KMZ10C	KMZ11B1	UNIT
Measurement range; note 1	±0.5	±0.05	±2.0	±7.5	±2.0	kA/m
Auxiliary field; note 1	0.5	note 2	3.0	3.0	3.0	kA/m
Open circuit sensitivity	16	22.0	4.0	1.5	4.0	$\frac{mV/V}{kA/m}$
Bridge resistance	1.2	1.3	2.2	1.4	2.3	kΩ

Notes

1. In air, 1 kA/m corresponds to approximately 1.25 mT.
2. With switched auxiliary field.

OPERATING PRINCIPLES

The KMZ and KM110B make use of the magnetoresistive effect, the property of a current-carrying magnetic material to change its resistivity in the presence of an external magnetic field. The basic operating principle is shown in Fig.2.

Figure 2 shows a strip of ferromagnetic material, called permalloy (20% Fe, 80% Ni). Assume that, when no external magnetic field is present, the permalloy has an internal magnetization vector which is parallel to the current flow (shown to flow through the permalloy from left to right). If an external magnetic field H, parallel to the plane of the permalloy, but perpendicular to the current flow, is switched on, the internal magnetization vector of the permalloy will rotate around an angle α. As a consequence the resistance R of the permalloy will change as a function of the rotation angle α and is given by:

$$R = R_0 + \Delta R_0 \cos^2\alpha .$$

It can be shown, that:

$$\sin^2\alpha = \frac{H^2}{H_0^2} \qquad \text{for: } H \leq H_0$$

$$\sin^2\alpha = 1 \qquad \text{for: } H > H_0$$

where H_0 can be regarded as a material constant comprising the so called demagnetizing and anisotropic fields.

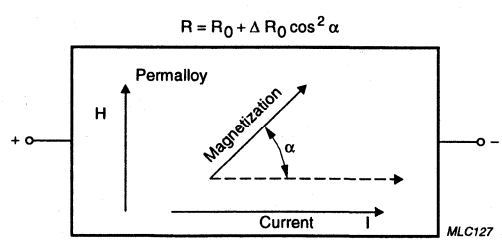
And so:

$$R = R_0 + \Delta R_0\left(1 - \frac{H^2}{H_0^2}\right) \qquad \text{for: } H \leq H_0$$

and:

$$R = R_0 \qquad \text{for: } H > H_0$$

It is obvious from this quadratic expression, that the resistance/magnetic field characteristic is non-linear and, what's more, each value of R is not necessarily associated with a unique value of H (see Fig.3).



The external magnetic field H causes a rotation of the internal magnetization of the permalloy around an angle α, which results in a change in resistance. Note, that H is normal to the current I and parallel to the plane of the permalloy.

Fig.2 The magnetoresistive effect in permalloy.

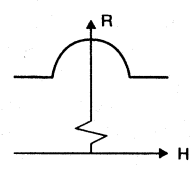


Fig.3 The resistance of the permalloy as a function of the external field H (see Fig.2).

The magnetoresistive effect can be linearized, however, by depositing aluminium stripes (Barber poles), on top of the permalloy strip at an angle of 45° to the strip axis (see Fig.4). As Al has a much higher conductivity than permalloy, the effect of the Barber poles is to rotate the current direction through 45° (the current flow assumes a 'saw-tooth' shape), i.e. to change the rotation angle of the magnetization relative to the current from α to $\alpha - 45°$. The resistance/magnetic field characteristic can easily be derived to:

$$R = R_0 + \frac{\Delta R_0}{2} + \Delta R_0 \left(\frac{H}{H_0}\right)\sqrt{1 - \frac{H^2}{H_0{}^2}}$$

and is shown in Fig.4. The characteristics are now linear around $\frac{H}{H_0} = 0$.

Strong magnetic fields ($H > H_0$), causing a 90° rotation of the magnetization, produce a change in resistance R between 2 and 3%.

When Barber poles are arranged at an angle of –45° to the strip axis the following expression for the sensor characteristic can be applied:

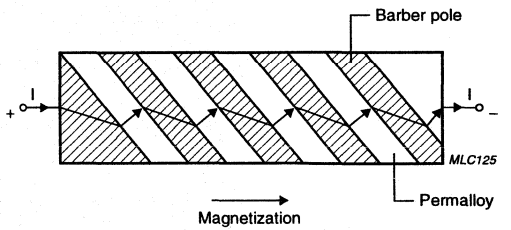
$$R = R_0 + \frac{\Delta R_0}{2} - \Delta R_0 \left(\frac{H}{H_0}\right)\sqrt{1 - \frac{H^2}{H_0{}^2}}.$$

It is the mirror image of the characteristic as shown in Fig.5.

In the sensors of the KMZ series four permalloy strips are arranged in a meander pattern on a silicon substrate (see Fig.7) and connected to form the four arms of a Wheatstone bridge (see Fig.6). In one pair of diagonally opposed elements the Barber poles are at +45° to the strip axis, in the other pair at –45°. A resistance increase in one pair of elements due to an external magnetic field is 'matched' by a decrease of resistance by an equal amount in the other pair. The resulting bridge imbalance is then a linear function of the amplitude of the external magnetic field in the plane of the permalloy strips normal to the strip axis.

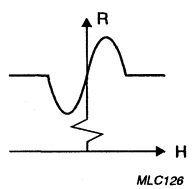
The diagram in Fig.6 contains two further resistors R_T. These are trimming resistors for trimming the sensor offset down to (almost) zero during the production process.

The main characteristics of the KMZ10 and KMZ11 sensors are given in Table 2. The outline of the KMZ10 sensor is shown in Fig.8, the outline of the KMZ11B1 in Fig.9.



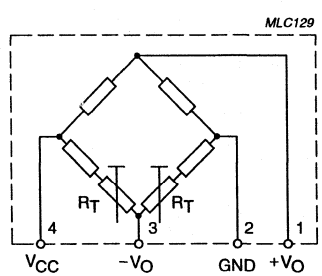
The aluminium Barber poles cause the current to flow in a saw-tooth shape.

Fig.4 Linearization of the magnetoresistive effect.



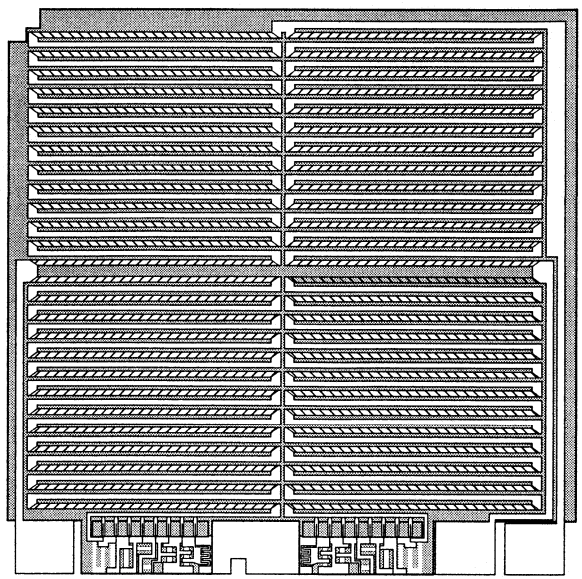
Around H = 0 the magnetoresistive effect has been linearized.

Fig.5 The resistance of the permalloy as a function of the external field H (see Fig.4).



V_{CC} = supply voltage; GND = ground; V_O = output voltage.

Fig.6 KMZ10 and KMZ11 bridge configuration with offset trimmed to zero, by resistors R_T.



The chip incorporates special resistors that are trimmed during manufacture to give zero offset at 25 °C.

Fig.7 KMZ10 chip structure.

Table 2 Main characteristics

SENSOR TYPE[1]	FIELD RANGE (kA/m)[2]	V_{CC} (V)	S $\left(\frac{mV/V}{kA/m}\right)$	R_{bridge} (kΩ)	APPLICATION EXAMPLES
KMZ10A	−0.5 to +0.5	≤9	16.0	1.2	compass, navigation, metal detection, traffic control
KMZ10A1; note 3	−0.05 to +0.05	≤9	22.0	1.3	
KMZ10B	−2.0 to +2.0	≤12	4.0	2.1	wheel speed, angular and linear position, current measurement, reference mark detection
KMZ11B1	−2.0 to +2.0	≤12	4.0	2.1	
KMZ10C	−7.5 to +7.5	≤10	1.5	1.4	
KM110B/1	KMZ10B plus operating FXD100 magnet ($8 \times 8 \times 4.35$ mm^3)				wheel speed, reference mark detection
KM110B/2	KMZ10B plus auxiliary FXD100 magnet ($4 \times 2.3 \times 0.6$ mm^3)				current measurement
KM110B/4	KMZ10B plus operating FXD100 magnet ($5 \times 5 \times 3$ mm^3)				wheel speed, reference mark detection

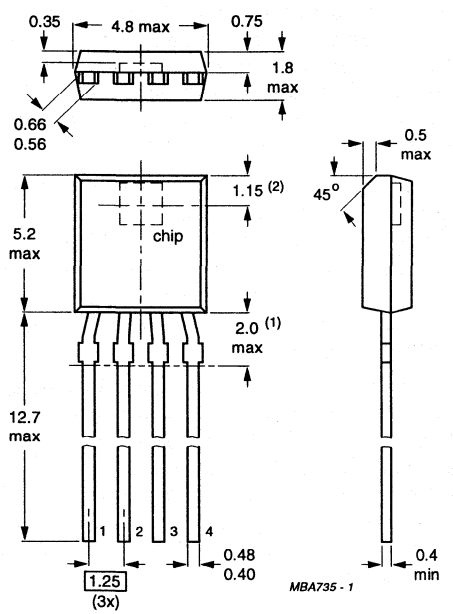
Notes

1. All sensors are supplied in SOT195 package except the KMZ11B1 which is supplied in the surface mounted SO8 (SOT96) package.
2. In air, 1 kA/m corresponds to approximately 1.25 mT.
3. Data given for operation with switched auxiliary field.

PACKAGE OUTLINES

Pinning for the KMZ sensor

PIN	SYMBOL	DESCRIPTION
1	$+V_O$	output voltage
2	GND	ground
3	$-V_O$	output voltage
4	$+V_{CC}$	supply voltage



Dimensions in mm.

Fig.8 Outline of KMZ10 (SOT195).

CHARACTERISTIC BEHAVIOUR

During manufacture, a strong magnetic field is applied parallel to the strip axis. This field imparts a preferred magnetization direction to the permalloy strips. Therefore, even in the absence of an external magnetic field, the magnetization will always tend to align with the strips.

The internal magnetization of the sensor strips, therefore, has two stable positions, so if for any reason the sensor is influenced by a powerful magnetic field opposing the internal aligning field, the magnetization may flip from one position to the other, and the strips become magnetized in the opposite direction (from, for example, the '+x' to the '–x' direction). As demonstrated in Fig.10, this can lead to drastic changes in sensor characteristics.

The field (e.g. '$-H_x$') needed to flip the sensor magnetization, and hence the characteristic, depends on the magnitude of the transverse field 'H_y': the greater the field 'H_y', the smaller the field '$-H_x$'. This is perfectly reasonable, since the greater the field 'H_y', the closer the magnetization's rotation approaches 90°, and hence the easier it will be to flip it into a corresponding stable position in the '–x' direction.

Looking at the curve in Fig.11 where H_y = 0.5 kA/m: for such a low transverse field, the sensor characteristic is stable for all positive values of H_x, and a reverse field of ≈1 kA/m is required before flipping occurs. At H_y = 4 kA/m however, the sensor will flip even at positive values of 'H_x' (at approximately 1 kA/m).

Figure 11 also illustrates that the flipping itself is not instantaneous; this is because not all the permalloy strips flip at the same rate. The hysteresis effect exhibited by the sensor is also shown by Fig.11. Finally, Figs 11 and 12 show that the sensitivity of the sensor falls with increasing 'H_x'. Again, this is perfectly reasonable, since the moment imposed on the magnetization by H_x directly opposes that imposed by 'H_y', thereby reducing the degree of bridge imbalance and hence the output signal for a given value of 'H_y'.

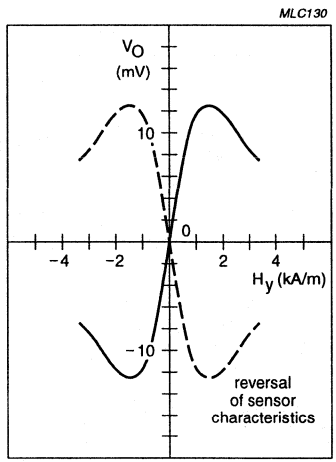
The following general recommendations for operating the KMZ10 can be applied:

- To ensure stable operation, avoid operating the sensor in an environment where it is likely to be subjected to negative external fields ('$-H_x$'). Preferably, apply a positive auxiliary field ('H_x') of sufficient magnitude to prevent any likelihood of flipping within the intended operating range (i.e. the range of 'H_y').
- Use the minimum auxiliary field that will ensure stable operation. Remember, the larger the auxiliary field, the lower the sensitivity. For the KMZ10B sensor, a minimum auxiliary field of approximately 1 kA/m is recommended.
- Finally, before using the sensor for the first time, apply a positive auxiliary field of at least 3 kA/m; this will effectively erase the sensor's history and will ensure that no residual hysteresis remains (see Fig.12). To guarantee stable operation, the sensor should in fact be operated in an auxiliary field of 3 kA/m.

The above mentioned recommendations (particularly the first one) define a kind of safe operating area (SOAR) for the sensors. This can be seen from Fig.13, which is an example (for the KMZ10B sensor) of the SOAR graphs to be found in our data sheets. The graph shows the SOAR of a KMZ10B as a function of auxiliary field 'H_x' and of disturbing field 'H_d' opposing 'H_x'.

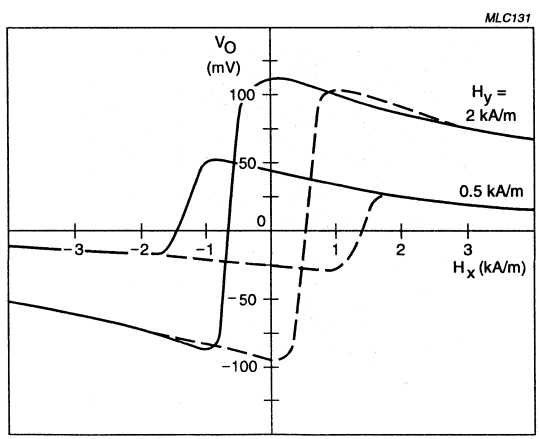
The greater the auxiliary field, the greater the disturbing field that can be tolerated before flipping occurs. For auxiliary fields above 3 kA/m, the SOAR graph shows that the sensor is completely stable, regardless of the magnitude of the disturbing field. It can also be seen from this graph that the SOAR can be extended for low values of 'H_y'. In Fig.13 (for the KMZ10B sensor), the extension for H_y < 1 kA/m is shown.

The KMZ10B sensor with auxiliary magnet is available as KM110B/2.



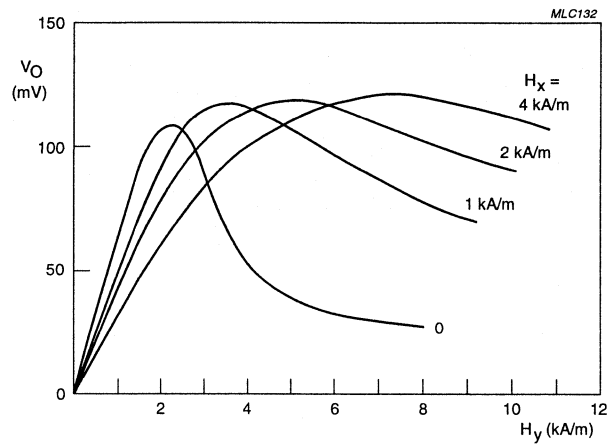
The solid line shows the characteristics of a 'perpendicular' sensor (with the magnetization oriented in the '+x' direction), and the dotted line shows the characteristic of a 'flipped' sensor (with the magnetization oriented in the '–x' direction.

Fig.10 Sensor characteristic.



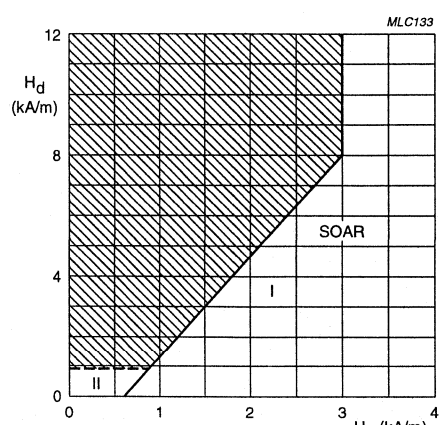
The curves illustrate three characteristics:
The sensor exhibits hysteresis.
The flipping is not instantaneous.
Sensitivity falls with increasing 'H_x'.

Fig.11 Sensor output 'V_O' as a function of auxiliary field 'H_x' for several values of transverse field 'H_y'.



The curves illustrate, more clearly than in Fig.11, the fall in sensitivity (i.e. initial gradient) with increasing 'H_x'.

Fig.12 Output 'V_O' as a function of transverse field 'H_y' for several values of auxiliary field 'H_x'.



The SOAR can be extended slightly (area II) for values of H_y < 1 kA/m.

Fig.13 SOAR of a KMZ10B sensor as a function of auxiliary field 'H_x' and disturbing field 'H_d' opposing 'H_x' (area I).

Effect of temperature on behaviour

Figure 14 shows that the bridge resistance increases linearly with temperature, due to the bridge resistors temperature dependency (i.e. the permalloy strips). Figure 14 shows only the variation for a typical KMZ10B sensor. The data sheets show also the spread in this variation due to manufacturing tolerances, and this should be taken into account when incorporating the sensor in practical circuits.

In addition to the bridge resistance, the sensitivity also varies with temperature. This can be seen from Fig.15, which plots output voltage against transverse field 'H_y' for various temperatures. Figure 15 shows that sensitivity falls with increasing temperature. The reason for this is quite complicated, and is related to the energy-band structure of the permalloy strips.

Figure 16 is similar to Fig.15, but with the sensor powered by a constant current supply. Figure 16 shows that with this constant current supply, the temperature dependency of sensitivity is significantly reduced. This is a direct result of the increase in bridge resistance with temperature (see Fig.14), which partly compensates the fall in sensitivity by increasing the voltage across the bridge and hence the output voltage. Figure 14 adequately demonstrates therefore the advantages of operating with constant current.

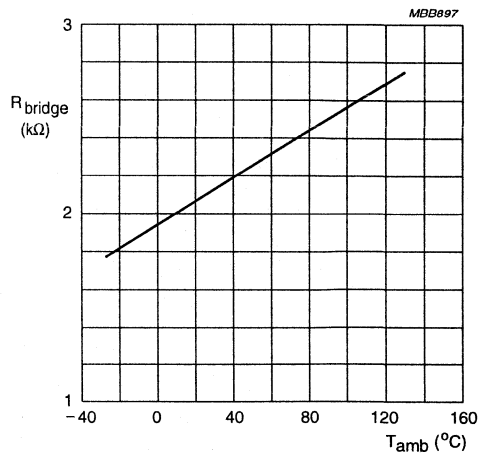
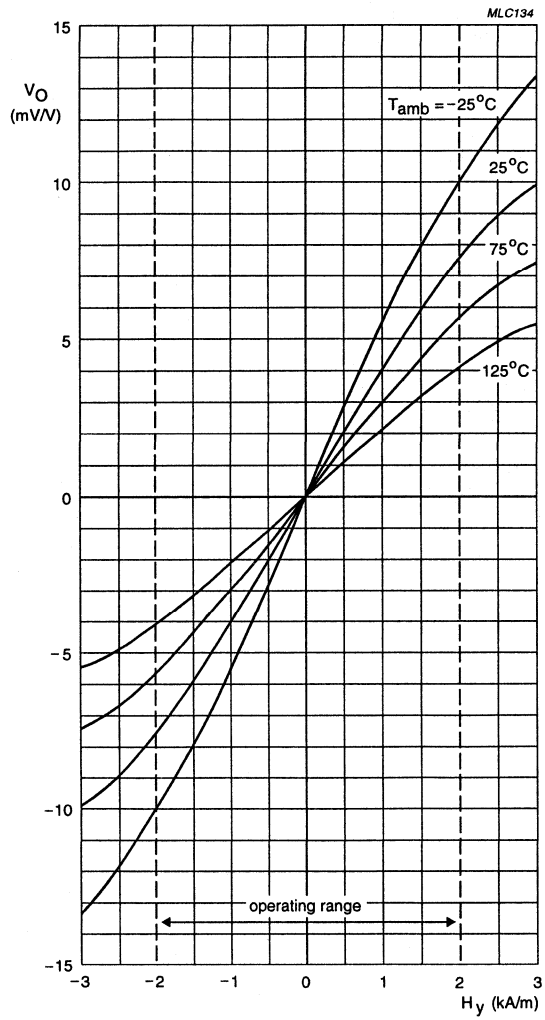
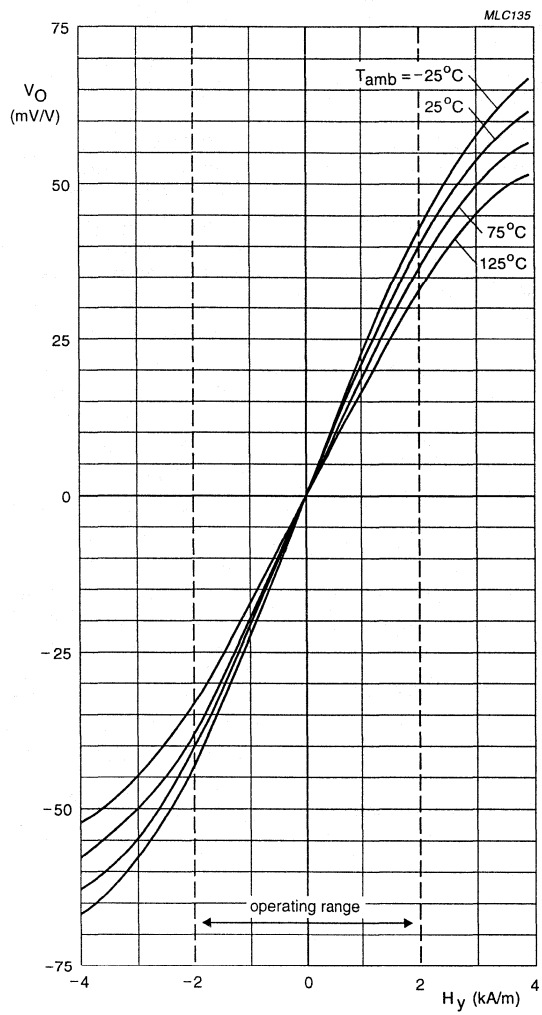


Fig.14 Bridge resistance of a KMZ10B sensor as a function of ambient temperature.



The graph illustrate that sensitivity falls with increasing temperature.

Fig.15 Output voltage 'V_O' as a fraction of the supply voltage of a KMZ10B sensor as a function of transverse field 'H_y' for several temperatures.



The reduction in temperature dependence of sensitivity is a result of the increase in bridge resistance with temperature, which increases the bridge voltage, to partly compensate the fall in sensitivity.

Fig.16 Output voltage 'V_O' of a KMZ10B sensor as a function of transverse field 'H_y' for several temperatures.

USING THE KMZ/KM110B SENSORS

The excellent properties of the KMZ magnetoresistive sensors, like high sensitivity, low and stable offset, wide operating temperature and frequency ranges and robustness, make them highly suitable for use in a wide range of e.g. automotive and industrial applications.

KMZ based products for rotational speed sensing and angular position measurement are extensively discussed in subsequent chapters. In the following sections we will concentrate on several other applications in which our magnetoresistive sensors are currently being used and discuss general application circuitry.

Linear position measurement using permanent magnets

Figures 17 and 18 show one of the simplest arrangements for using a sensor/permanent magnet combination for measuring linear displacement, and illustrates some of the problems likely to be encountered if proper account is not taken of the effects previously described.

When the sensor is placed in the field of a permanent magnet, it is exposed to magnetic fields in both the 'x' and 'y' directions. If the magnet is oriented with its axis parallel to the sensor strips (i.e. in the 'x' direction), as shown in Fig.17a, 'H_x' then provides the auxiliary field and the variation in 'H_y' can be used as a measure of 'x' displacement. Figure 17b shows how both 'H_x' and 'H_y' vary with 'x', and Fig.17c shows the corresponding output signal as a function of 'x'.

In the example shown in Fig.17, 'H_x' never exceeds '$\pm\hat{H}_x$' (the field that can cause flipping of the sensor) and the sensor characteristic remains stable throughout the measuring range.

Consider the example shown in Fig.18. In this example, for certain values of 'x', 'H_x' exceeds '$\pm\hat{H}_x$' (Fig.18b). This could occur if, for example, the magnet were powerful or if the sensor should pass close to the magnet, and as Fig.18c shows, the effects on the output can be drastic.

Assuming the sensor is initially on the transverse axis of the magnet (i.e. x = 0). 'H_y' will be zero and 'H_x' will be at its maximum value ($>\hat{H}_x$) . Therefore, the sensor will be oriented in the '+x' direction and the output voltage 'V_O' will vary as in Fig.17c.

As the sensor moves in the '+x' direction, 'H_y' (and hence 'V_O') increases, and 'H_x' falls to zero and then increases negatively until it exceeds '$-\hat{H}_x$'. At this point, the sensor characteristic flips and the output voltage reverses, moving from 'A' to 'B' in Fig.18c. Any further increase in 'x' causes the sensor voltage to move along 'BE'. However, if the sensor is moved in the opposite direction, 'H_x' increases until it exceeds '$\hat{H}_x$' and 'V_O' moves from 'B' to 'C'. At this point, the sensor characteristic flips again and 'V_O' moves from 'C' to 'D'.

Under these conditions, the sensor characteristic will trace the hysteresis loop 'ABCD', and a similar loop in the '–x' direction. Fig.18c is in fact an idealized situation and the reversals are never as abrupt as shown. It does however illustrate the effects that can occur if the sensor is placed close to a powerful magnet.

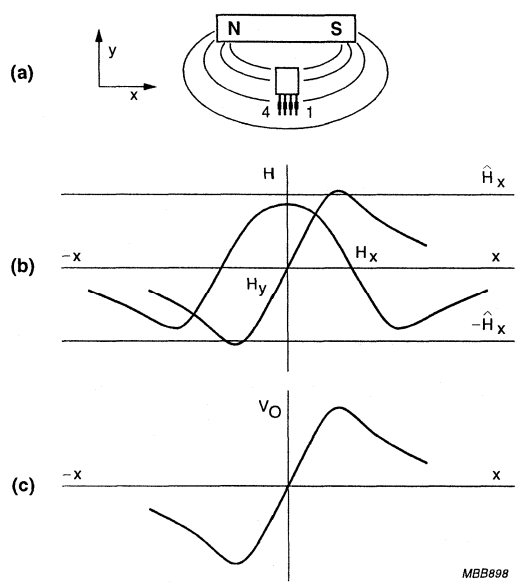
Under certain circumstances, particularly where there are likely to be temporary or fluctuating external fields, it may be advantageous to operate under these conditions, since over the region DD' the field of the permanent magnet will have a stabilizing effect upon the sensor (i.e. it will have to correct any flipping of the sensor due to transient magnetic fields). Note that reversal of the permanent magnet will give rise to the same sensor characteristic as shown in Figs 17c and 18c (i.e. with positive slope), since the sensor will then be forced to operate in its flipped state.

Figure 19 shows the sensor characteristic at distances of 10 mm and 20 mm from a permanent magnet, and amply illustrates the effects shown in Figs 17 and 18.

One-point measurement with the KM110B/1

Figure 20a shows how a KM110B/1 sensor may be used to make position measurements of a metal object, for example a steel plate (alternatively the KM110B/4, with its smaller magnet, may be used). The sensor is located in front of the plate, the magnet's magnetization is perpendicular to the axis of the plate (note that this is a schematic drawing only; in fact the sensor leads are attached on the right-hand side of the sensor package, but are not shown here). A discontinuity in the plate's structure, such as a hole or region of non-magnetic material, will disturb the magnetic field and produce a variation in the output signal from the sensor.

This is shown in Fig.20b, which gives the sensor output signal as a function of hole/sensor offset 'x', for two values of magnet/plate spacing 'd'. The interesting feature of Fig.20 is that the crossover point (i.e. the point where the hole and the sensor precisely coincide) is independent of 'd'. The obvious advantage of this set-up is that precise location of the sensor/magnet combination is unimportant for one-point measurements, so simplifying adjustment procedures. Although not shown in Fig.20b, the crossover point is also independent of the temperature, since it is effectively a null measurement. This is a major advantage of magnetoresistive sensors in this application.



The magnet provides both the auxiliary and transverse fields. In the example shown, the auxiliary field is always less than the field that will cause flipping. Note the pinning arrangement, which indicates that the sensor is viewed from the rear. Reversal of the sensor relative to the permanent magnet will reverse the characteristic.

Fig.17 Sensor output in the field of a permanent magnet as a function of its displacement 'x' parallel to the magnetic axis.

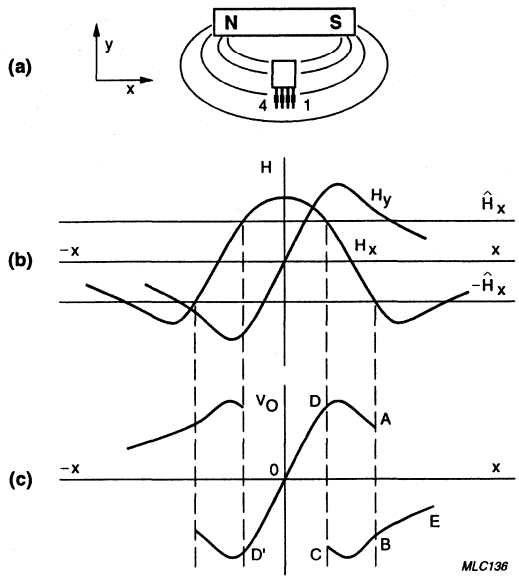
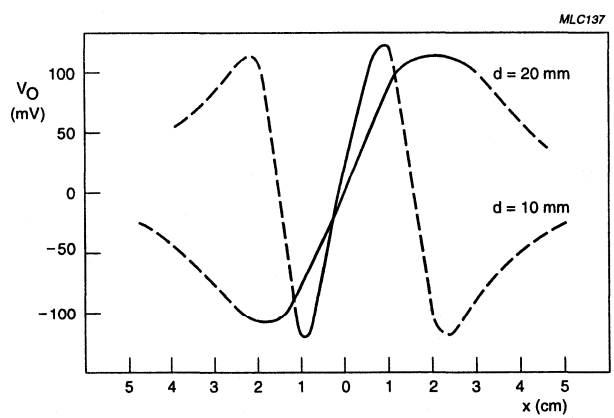


Fig.18 Sensor output in the set-up of Fig.17, but in which the auxiliary field sometimes exceeds '$\hat{H}_x$'.



Sensor distances 'd' of 10 mm and 20 mm from a permanent magnet.

Fig.19 Measured sensor output as a function of displacement 'x' parallel to the magnetic axis.

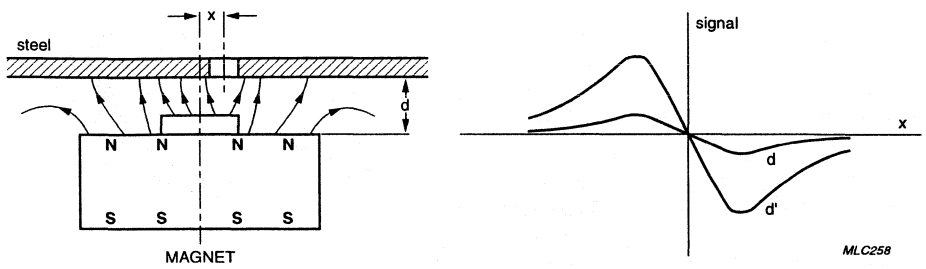


Fig.20 One-point measurement with the KM110B/1.

Current measurement with the KM110B/2

Figures 21 and 22 show two ways in which the KM110B/2 can be used to measure electric current. This could be useful, for example, in headlamp failure systems in automobiles or in clamp-on (non-contacting) meters, as used in the power industry.

Figure 22 is a fairly simple set-up, in which the sensor measures the magnetic field generated by the current-carrying wire. Figure 21 is a more sophisticated arrangement, in which the magnetic field generated by the current-carrying wire is compensated by a secondary circuit wrapped around a ferrite core. At the null-field point (detected by a KM110B/2 sensor located in the air gap between the ends of the core) the magnitude of the current in the secondary circuit is a measure of the current in the main circuit. This arrangement provides a more accurate measurement in precision applications. Note that both examples allow current measurement without any break in or interference with the circuit. In this way, they provide a distinct advantage over thermistor based systems.

Evaluation circuitry for analog signals

For applications in which analog signals are measured, for example in angular position, linear position, one-point and current measurement as shown in Fig.21, a good evaluation circuit should allow for temperature drift compensation and for offset and sensitivity adjustment.

The circuit in Fig.23 fulfils these requirements. In the first stage the sensor signal is pre-amplified, offset is adjusted and temperature drift of the sensitivity is compensated.

For temperature compensation the silicon temperature sensor KTY82/210 in surface mount SOT23 package is used (a leaded alternative is the KTY81/210 sensor in SOT54 package). The grade of compensation can be controlled with the two resistors R7 and R8. Smaller values increase the compensation factor.

In a second stage the final amplification and sensitivity adjustment take place. The output is able to approximately realize a rail to rail output voltage, if the load resistance exceeds 10 kΩ.

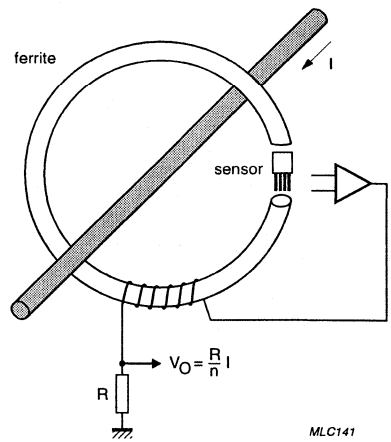
This basic circuit can be extended with additional components to meet specific EMC requirements or can be modified to obtain customized output characteristics (e.g. a different output voltage range or a current output signal).

A more detailed discussion on the subject of temperature compensation in signal conditioning circuitry for magnetoresistive sensors is given in the "*General section for Temperature Sensors*".

Using the magnetoresistive sensor with a compensation coil

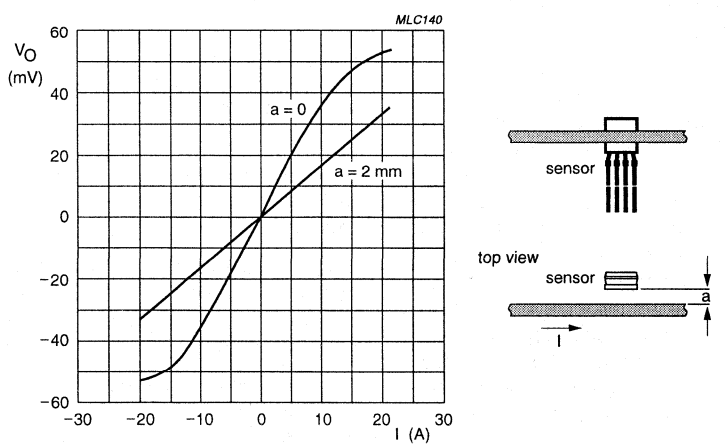
For general magnetic field or current measurements (see Fig.22), it is useful to apply the 'null-field' method, in which an opposite field (generated by a current carrying coil) is compensating the unknown field. The current through the coil is a measure of the magnetic field amplitude. The advantage is that inaccuracies as result of tolerances, temperature drift and slight non-linearities in the sensor characteristics are insignificant.

For the sensor the KM110B/2 is chosen, which includes a small auxiliary magnet. The circuit is shown in Fig.24. With zero external field applied to the sensor bridge the offset is initially set by potentiometer 'R1' to $V_O = 0$. When an external field is applied to the sensor, the resulting output causes the first op-amp to generate a current which passes through 'L1'. As a result a magnetic feedback is produced, in which the unknown magnetic field is almost compensated. The output voltage 'V_O' is thus a direct measure of the magnetic field generated by the coil and hence of the external magnetic field to be measured. The sensitivity can be calibrated by means of 'R4'.



In this set-up, a current-carrying wire is wrapped around a ferrite core, with the KM110B/2 sensor located in the air gap between its ends.

Fig.21 Current measurement with the KM110B/2 sensor.



The sensor measures the magnetic field generated by a current-carrying wire.

Fig.22 Simple set-up for measuring current using the KM110B/2 sensor.

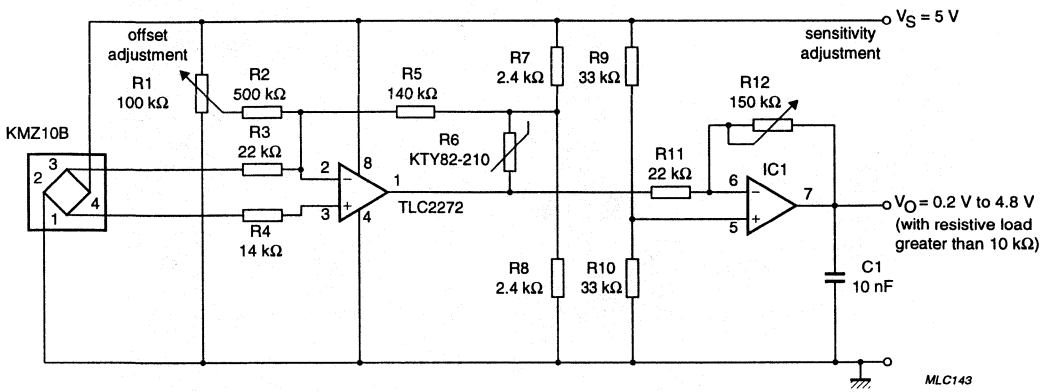
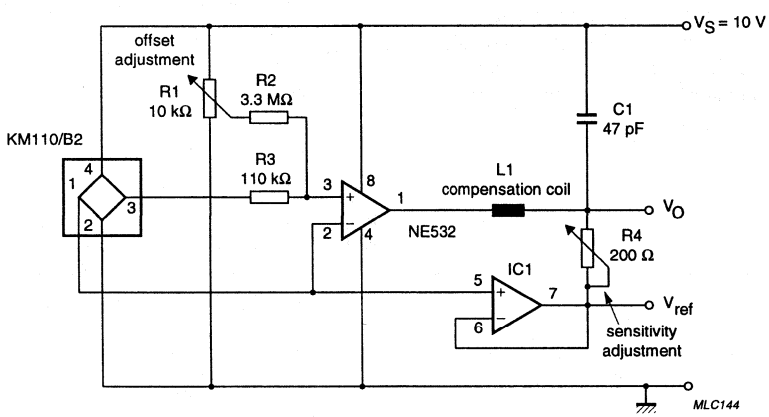


Fig.23 Evaluation circuit for analog signals.



Data for the coil: coil former catalogue number 4322 021 30240,
365 turns, diameter of the Cu wire 0.1 mm.

Fig.24 Signal conditioning circuitry for magnetoresistive sensors in combination with a compensation coil.

Sensor hybrid modules — General part 2

SENSORS FOR CONTACTLESS ANGULAR POSITION MEASUREMENT

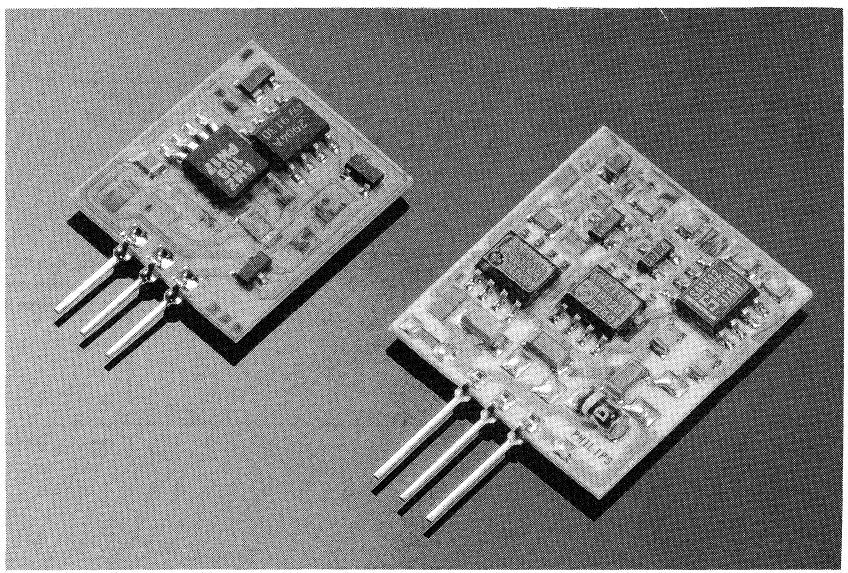


Fig.1 The KM110BH/21 sensor module.

General

Philips Semiconductors has designed a wide range of modules to meet the strong demand for contactless angular measurement systems. In the automotive field alone there are many potential applications, such as electronic control of accelerator pedal, chassis position, steering angle and throttle position.

Magnetoresistive sensors are particular suitable for angular position measurement applications, since they can be operated in such a way, that their output signal is virtually independent of:

- Magnet tolerances and magnet temperature coefficient
- Positioning tolerances and sensor-magnet distance.

Moreover, all modules are pre-calibrated for offset, sensitivity and zero point and contain integrated temperature compensation.

As a consequence, assembly of the (encapsulated) sensor is easy and calibration after assembly becomes superfluous, thus saving considerable costs. More technical details are explained in the next Section "Angular measurement with magnetoresistive sensors".

There are two module series available. The KM110BH/2 family comprises a range of modules in hybrid thick-film technology. The circuits and the magnetic parameters of these modules have been chosen so that they can be used:

- Directly, in a wide range of applications (without further trimming or any adjustments)
- As the basis for customized modules.

The KMA family comprises a range of encapsulated angular position sensors, which are based on the KM110BH/2 hybrid sensors and the encapsulation of which has been developed in cooperation with AB Electronics of Werne, Germany.

Angular measurement with magnetoresistive sensors

With the KMZ magnetoresistive sensor, two different techniques are available for angle measurement. The first, used in most magnetic field sensor angle measurement equipment, entails measuring the **field-strength** of a rotating magnet as a function of the angle. With this technique, the field used is within the normal sensitivity range of the KMZ sensor, and angles of ±90° can be measured.

However, since the magnet's properties influence the sensor output, the measurement equipment must be calibrated after assembly. Only with a very well-defined magnetic system would a pre-calibrated circuit be possible. Defining such a system is both expensive and difficult, due to the tolerances caused by the thermal sensitivity of the magnet.

The second technique, used in our KM110BH/2 modules, requires strong magnetic fields (≥80 kA/m). The KMZ sensor operates in 'saturation mode', detecting only the **field-direction**. In the limiting event of infinite field strength, the field strength and its drift with temperature have no influence on the sensor.

Therefore, using this technique reduces measurement-system tolerances and allows pre-trimming of the sensors; the only requirement is that field directions during trimming correspond with field directions after assembly. The typical angle measurement range is from –45 to +45°, and the sensor output signal is sinusoidal. Because of this, a linear signal can be obtained in the central part of the output characteristic.

In practice, it is not necessary to use very strong and possibly expensive magnets for the sensor to operate in saturation mode. Even with readily available magnets (or field strengths), the influence of tolerances or temperature drift is minimal.

As field strengths decrease, the peak output signal remains more or less constant and the angle range increases from ±45° to a maximum of ±90° (approximately) at very low magnetic fields.

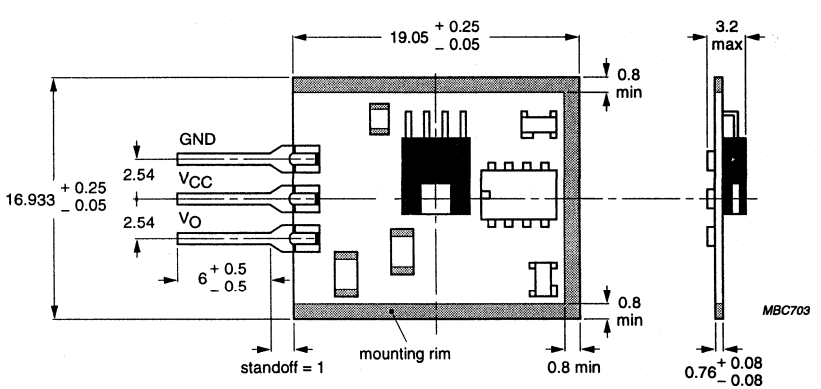
The KM110BH/21 module series

Figure 2 shows the construction of the KM110BH/21 module. It is based on the KMZ10B sensor. There are two types in the range: the KM110BH/2130 and the KM110BH/2190. They are trimmed differently, but both are based on the same circuit (see Fig.3). The KM110BH/2130 is trimmed to a higher amplification and measures angles between –15 and +15°, generating a linear output signal (non-linearity is only ≈1%).

The KM110BH/2190 measures the angle range from approximately –45 to +45°, with a sinusoidal output. Both modules have an analog voltage output signal. Figure 4 shows the output signals 'V_O' of the two modules as a function of measured angle 'α'.

Further data on the KM110BH/21 module series can be found in Table 1.

Although both modules are readily available, it is recommended to use the modules of the KM110BH/23 and/or KM110BH/24 families for new design-ins (see Table 1).



Dimensions in mm.

Fig.2 Construction of a KM110BH/21.

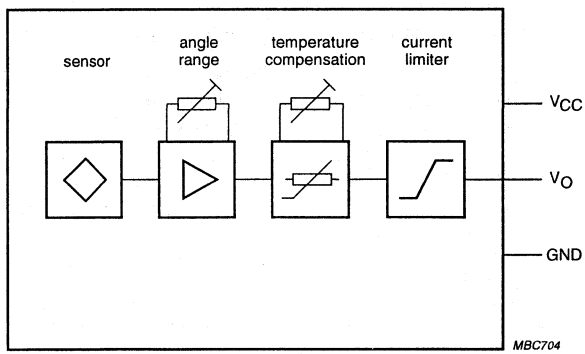
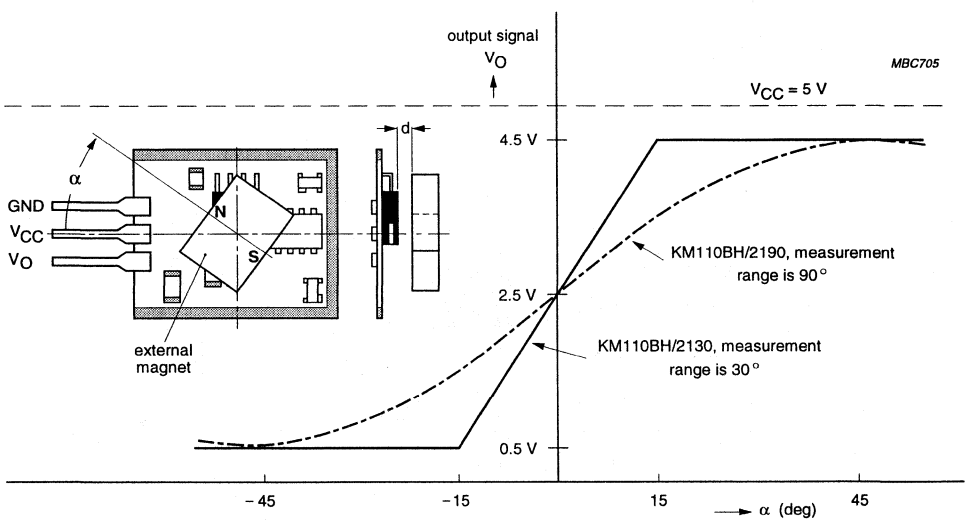


Fig.3 Block diagram of a module circuit.



Dimensions in mm.

Fig.4 Output characteristics of the KM110BH/2130 and KM110BH/2190 modules.

Table 1 Type range of contactless position sensor modules

PARAMETER	KM110BH/						UNIT
	2130[1]	2190[2]	2270	2390	2430	2470	
Angle range	30	90	70	90	30	70	deg
Output voltage[3]	0.5 to 4.5	0.5 to 4.5	–	0.5 to 4.5	0.5 to 4.5	0.5 to 4.5	V
Output current	–	–	4 to 20	–	–	–	mA
Output characteristic	linear	sinusoidal	sinusoidal	linear	linear	sinusoidal	
Supply voltage	5	5	8.5	5	5	5	V
Substrate dimensions	19.1 × 16.9	19.1 × 16.9	23.6 × 20.3	23.6 × 20.3	23.6 × 20.3	23.6 × 20.3	mm^2
Resolution	0.001	0.001	0.001	0.001	0.001	0.001	deg
Temperature range	–40 to +125	–40 to +125	–40 to +125	–40 to +125	–40 to +125	–40 to +125	°C
Production	running	running	running	12/95	8/94	8/94	

Notes

1. For new design-ins the KM110BH/2430 should be used.
2. For new design-ins the KM110BH/2470 or KM110BH/2390 should be used.
3. The output voltage is ratiometric.

The KM110BH/2270 module

The KM110BH/2270 is trimmed to an angle ranging from –35 to +35°. The outline is shown in Fig.5, a block diagram of the circuit in Fig.6. The module is based on the KMZ11B1 sensor. It contains an input voltage stabilization. In contrast to the other modules in the KM110BH/2 range the KM110BH/2270 has an analog **current** output signal (4 to 20 mA). Using a simple resistor this can be converted into a voltage signal. The output characteristic of the KM110BH/2270 is shown in Fig.7. The module contains protection circuitry to make it EMC friendly.

Both resolution and reproducibility are extremely high (better than 0.001° at $\alpha = 0°$). Hysteresis, with a typical value of 0.02° at $\alpha = 0°$, is very low.

When designing an encapsulation for the KM110BH/2270, it may be necessary to have the pins of the hybrid bent in an S-shape in order to avoid force on the solder joints. In this event the KM110BH/2270G should be ordered. Further data is supplied in Table 1.

The KM110BH/2390 module

The KM110BH/2390 module has been designed for linearly measuring angles over ranges of up to 106° (from –53 to +53°). It is based on a modified version of the KMZ11B1, especially designed for linear measurement of wide angle ranges. The outline is shown in Fig.8. The block diagram of the circuit is the same as for the KM110BH/21 module (see Fig.3).

The module has an analog voltage output signal (0.5 to 4.5 V for angles from –45 to +45°). The output characteristic is shown in Fig.9. A summary of module data can be found in Table 1.

The KM110BH/24 module

The outline of the KM110BH/24 module is shown in Fig.10. The module is based on the KMZ11B1. The block diagram of the circuit is shown in Fig.3.

The KM110BH/24 is available in 2 versions. The KM110BH/2430 is trimmed to have an angle range of 30° (–15 to +15°, non-linearity is ≈1%) and has a linear voltage output. The KM110BH/2470 has an angle range of 70° (–35 to +35°) and has a sinusoidal voltage output. The output characteristics are shown in Figs 11 and 12. The modules contain protection circuitry to make them EMC friendly.

Magnets

From a technical viewpoint, the most suitable magnet is a large and strong one; all tolerances are then negligible. However, cost and space must also be considered. The optimum size, therefore, largely depends on individual requirements. In Table 2 three different commercially available SmCo magnets are given, all suitable for angle measurement applications.

For each magnet the dimensions, the recommended measuring distance 'd', the tolerance on 'd', the eccentricity and the temperature range is given.

The magnets described have tolerances of magnetization direction affecting the angle measurement. Deviations of up to 2° are possible. This should be taken into account if no mechanical $\alpha = 0°$ calibration is possible.

The symmetry axis of the module and the rotation axis of the magnet should be identical.

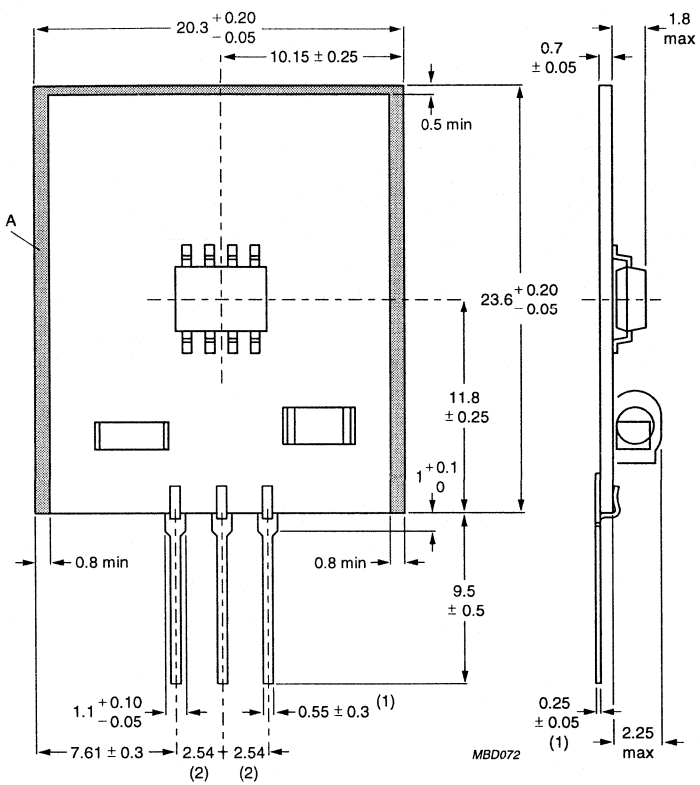
If one of the axis is shifted, the measuring system neglects this tolerance because of the parallel field lines of the magnet. Measurements with magnets 11.2×8 mm^2 faced to the sensor allow for eccentric tolerances of up to 0.5 mm in the event of an accepted V_O tolerance of 1% and up to 0.25 mm for an accepted V_O tolerance of 0.5% (offset, angle range). For smaller magnets, this axis tolerance should be reduced proportionally.

Table 2 Magnets for angle sensor hybrids

MATERIAL	DIMENSIONS[1] (mm)	d[2] (mm)	TOLERANCE d[3] (mm)	ECCENTRICITY[4] (mm)	T_{amb} (°C)
Sm_2Co_{17}	$11.2 \times 5.5 \times 8$	2.1	±0.30	±0.25	−55 to +125
	$6 \times 3 \times 5$	0.7	±0.15	±0.15	
	$8 \times 3 \times 7.5$	0.5	±0.30	±0.20	

Notes

1. The magnetization is always parallel to the latter dimensions given.
2. Distance 'd' between magnet and KMZ sensor front as shown in Fig.4.
3. Maximum deviation of distance 'd' for which the change in sensor output signal is smaller than 0.5% of full scale sensor signal.
4. Maximum deviation of magnet rotational axis to sensor rotational axis for which the change in sensor output signal is smaller than 0.5% of full scale sensor signal.



Dimensions in mm.

Area 'A' (shaded) free of SMD devices.

(1) Dimension before bath soldering; maximum dimension after bath soldering: 0.7 mm.

(2) Pitch tolerance: 0.2 mm.

Fig.5 Outline of the KM110BH/2270.

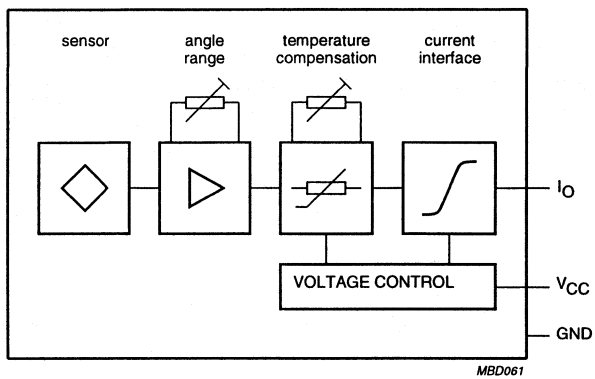


Fig.6 Block diagram of the KM110BH/2270.

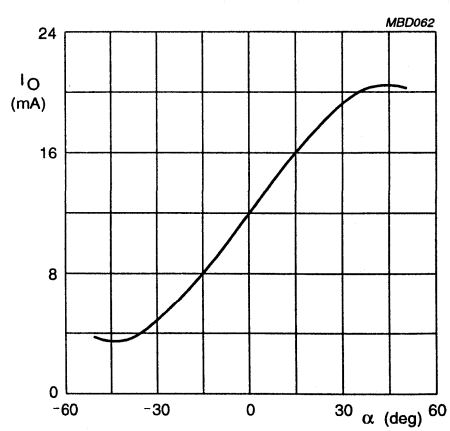
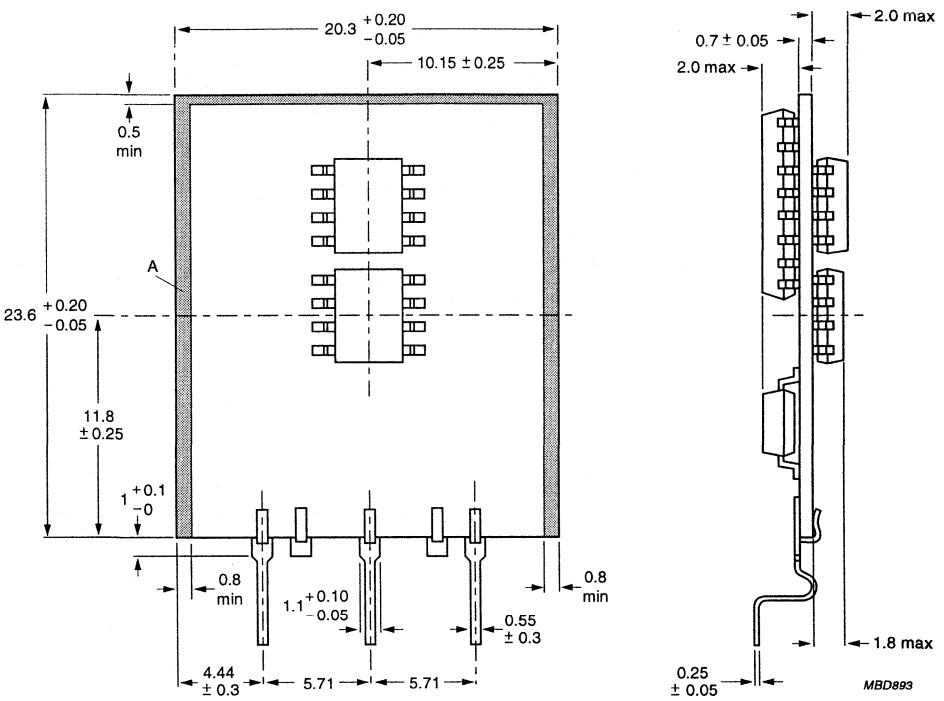


Fig.7 Output current 'I_O' as a function of angular displacement 'α' for the KM110BH/2270.



Dimensions in mm.
Area 'A' (shaded) free of SMD devices.

Fig.8 Outline of the KM110BH/2390.

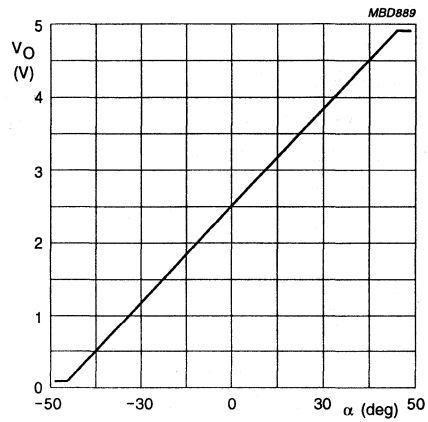
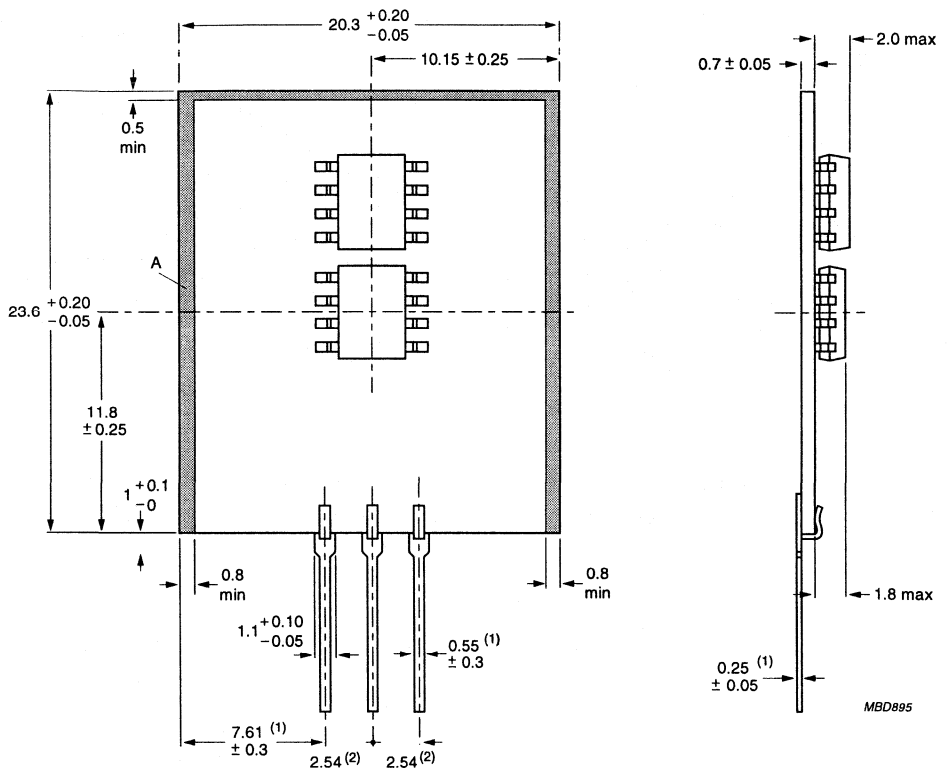


Fig.9 Output voltage 'V_O' as a function of angular displacement 'α' for the KM110BH/2390.



Dimensions in mm.

Area 'A' (shaded) free of SMD devices.

(1) Dimension before bath soldering; maximum dimension after bath soldering: 0.7 mm.

(2) Pitch tolerance: 0.2 mm.

Fig.10 Outline of the KM110BH/2430 and KM110BH/2470.

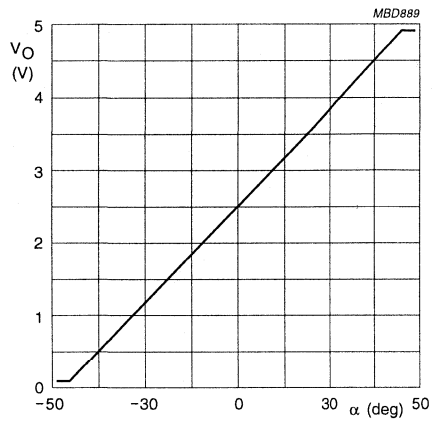


Fig.11 Output voltage 'V_O' as a function of angular displacement 'α' for the KM110BH/2430.

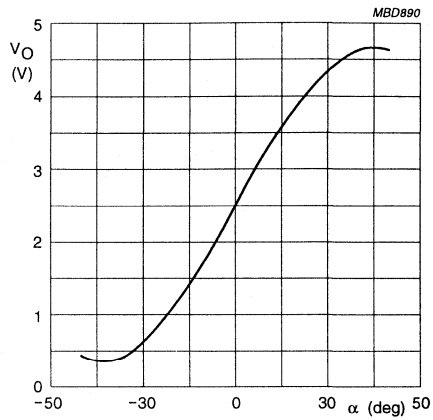


Fig.12 Output voltage 'V_O' as a function of angular displacement 'α' for the KM110BH/2470.

THE KMA10 AND KMA20 ENCAPSULATED SENSORS FOR ANGULAR POSITION MEASUREMENT

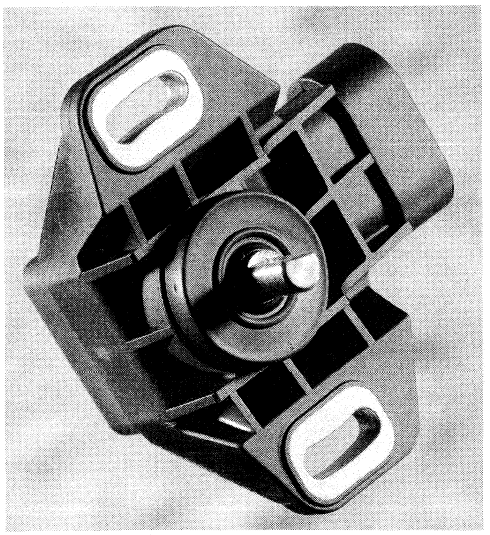


Fig.13 The KMA10 and KMA20 sensors.

The KMA10 and KMA20 are ready-to-use contactless angle sensors, designed to operate in extreme environments. The sensors are based on the KMZ11B1 magnetoresistive sensor element. They contain integrated signal conditioning electronics and are available in a hermetically-sealed, rugged encapsulation. Applications are both automotive and industrial, such as chassis position measurement and angular position measurement of accelerator pedals, control levers, operating handles, shafts, etc.

The KMA10 and KMA20 sensors, jointly developed by Philips Semiconductors and AB Electronics, offer:

- Angle measuring ranges of 30, 70 and 90°
- Contactless operation - wear-free and no microlinearity problems (output is noise-free even for small angle changes)
- Easy/mechanically-adjustable mounting - ready-for-use
- Analog current (KMA10) and voltage (KMA20) output signal
- Operation up to 125 °C
- Protection against aggressive environments
- A rugged mechanical design
- EMC-friendly operation.

The encapsulation

Figure 14 shows the encapsulation of the KMA sensors. The rugged design of the encapsulation, the AMP Superseal connector and the protection cap on the shaft ensure reliable operation under harsh environmental conditions. Thus, the KMA sensors are resistant, for example, to aggressive media and pressurized water (DIN protection class IP65). Moreover they operate at temperatures up to 125 °C and its construction enables easy mounting and connection to an external shaft or spindle.

The sensors are supplied with a 3-pin 'AMP Superseal 1.5 series' socket. For the recommended matching plug, the following AMP components are required:

- A plug connector, part no. 282087-1
- A receptacle contact (strip form, wire size range 1.0 to 1.5 mm^2), part no. 282110-1
- A single wire seal (yellow, insulation diameter 1.8 to 2.4 mm), part no. 281934-2.

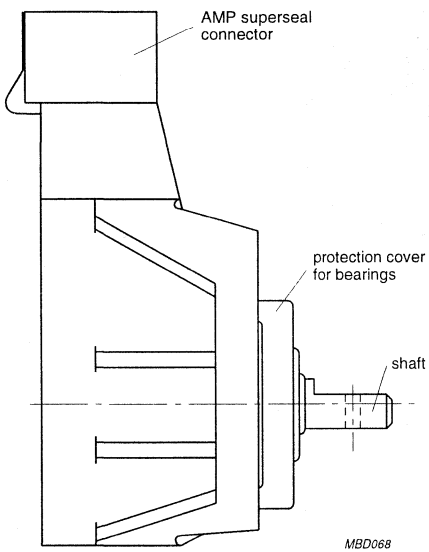


Fig.14 Encapsulation of the KMA sensors.

The KMA10/70

The KMA10 sensor is available in one version, the KMA10/70. It is based on the KM110BH/2270 hybrid and therefore has a 70° measuring range, a sinusoidal current output (see Fig.7) and operates at temperatures up to 100 °C. The maximum absolute angle error (over temperature) is shown in Fig.15.

Remark: the angle error should not be mixed up with the resolution and the reproducibility of the sensor!

The KMA20 family

The KMA20 sensors are available in three versions.

The KMA20/30 is based on the KM110BH/2430 and has a measuring range of 30°. The KMA20/70 is based on the KM110BH/2470 and has a measuring range of 70°. Both sensors have a voltage output. However, the output signal of the KMA20/30 is linear (see Fig.11) and of the KMA20/70 sinusoidal. The maximum absolute angle error (over temperature) is shown in Fig.16.

The last member in the KMA20 family is the KMA20/90, which is based on the KM110BH/2390. It has a linear voltage output signal over its angle measuring range of maximum 106° and a minimum absolute angle error of 1°.

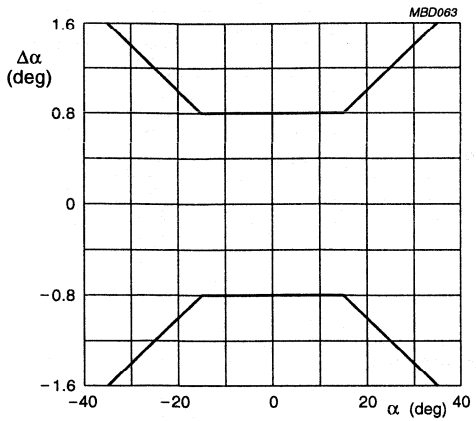
A summary of data of the KMA10 and KMA20 sensors is given in Table 3.

Table 3 Type range encapsulated angle sensors

PARAMETER	KMA10/70	KMA20/30	KMA20/70	KMA20/90	UNIT
Angle range	70	30	70	90	deg
Output voltage[1]	–	0.5 to 4.5	0.5 to 4.5	0.5 to 4.5	V
Output current range	4 to 20	–	–	–	mA
Output characteristic	sinusoidal	linear	sinusoidal	linear	
Supply voltage	8.5	5	5	5	V
Resolution	0.001	0.001	0.001	0.001	deg
Operating life	$>5 \times 10^8$	$>5 \times 10^8$	$>5 \times 10^8$	$>5 \times 10^8$	cycles
Temperature range	–40 to +100	–40 to +125	–40 to +125	–40 to +125	°C
Production	running	8/94	8/94	12/95	

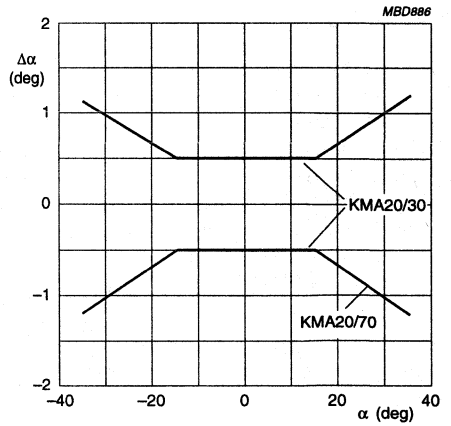
Note

1. The output voltage is ratiometric.



Temperatures between −20 and +85 °C.

Fig.15 Maximum absolute angle error of the KMA10/70.



Temperatures between −20 and +85 °C.

Fig.16 Maximum absolute angle error of the KMA20/30 and KMA20/70.

Angle sensor hybrid KM110BH/2130; KM110BH/2190

DESCRIPTION

Sensor module for contactless measurement of angular displacements of strong magnetic fields. The module is a ready-trimmed (sensitivity and zero point) combination of the magnetoresistive sensor KMZ10B and a signal conditioning circuit in hybrid technology. The KM110BH/2130 delivers a linear output signal that is proportional to the direction of the magnetic field. The KM110BH/2190 delivers a sinusoidal signal.

For new design-ins the KM110BH/23 and KM110BH/24 modules are recommended.

PINNING

PIN	DESCRIPTION
1	ground
2	V_{CC}
3	V_O

PIN CONFIGURATION

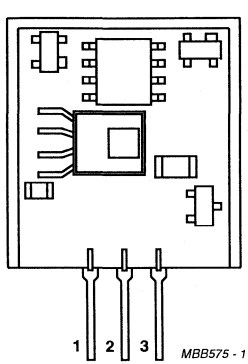


Fig.1 Simplified outline.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage	–	5	–	V
V_O	output voltage range	0.5	–	4.5	V
α	angle range				
	KM110BH/2130	–15	–	15	deg
	KM110BH/2190	–45	–	45	deg
T_{op}	operating temperature range	–40	–	125	°C

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	4.5	5.5	V
I_{CC}	supply current	–	20	mA
T_{stg}	storage temperature range	–40	125	°C
T_{op}	operating temperature range	–40	125	°C
	output short-circuit duration	permanent (see note 1)		

Note

1. If pin 3 is shorted to either pin 1 or pin 2, current may flow permanently, without damage to the device.

CHARACTERISTICS

T_{amb} = 25 °C; V_{CC} = 5 V and a homogeneous magnetic field H_{ext} = 100 kA/m in the sensitive layer of the KMZ sensor unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α	angle range (note 1)					
	KM110BH/2130		–15	–	15	deg
	KM110BH/2190	note 2	–45	–	45	deg
V_O	output voltage range					
	KM110BH/2130	linear, see Fig.4	0.5	–	4.5	V
	KM110BH/2190	sinusoidal, see Fig.5	0.5	–	4.5	V
V_{zero}	zero point voltage	α = 0 deg	–	2.5	–	V
V_{off}	zero point offset voltage					
	KM110BH/2130		–45		+45	mV
	KM110BH/2190		–	±35	–	mV
S	sensitivity (note 3)	α = 0 deg				
	KM110BH/2130		–	139	–	mV/deg
	KM110BH/2190		–	70	–	mV/deg
FL	deviation of linearity (note 4)					
	KM110BH/2130		–	–	±1	%/FS
	KM110BH/2190		–	–	–	%/FS
SP_{max}	maximum angular speed					
	KM110BH/2130		–	10	–	deg/ms
	KM110BH/2190		–	30	–	deg/ms
R_L	load resistance		10	–	–	kΩ
Temperature coefficients (–40 to +85 °C)						
TCV_{zero}	temperature coefficient of zero point voltage					
	KM110BH/2130		–	0.6	–	mV/K
	KM110BH/2190		–	0.3	–	mV/K
TCS	temperature coefficient of sensitivity		–	±200	–	ppm/K

Notes

1. Refer to Fig.3. The magnetic field can be achieved using the first magnet listed in Table 1. Other magnets, along with their required distances from the front of the KMZ sensor, are given in this table.
2. Valid for $H_{ext} = \infty$. The real field strength of 100 kA/m gives a slightly higher operating angle range of ±46.5 deg.
3. The sensitivity will change slightly with +0.33% per 10% magnetic field increase if H_{ext} deviates from 100 kA/m.
4. Deviation from best straight line in angle range.

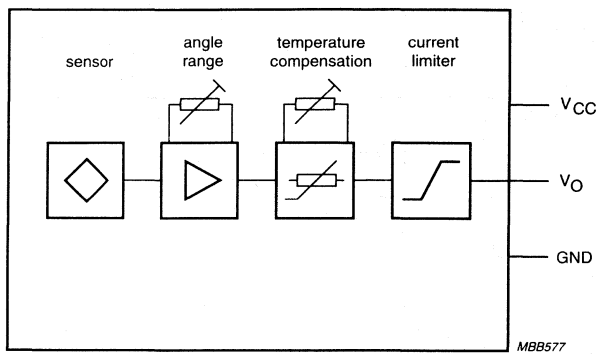


Fig.2 Circuit diagram.

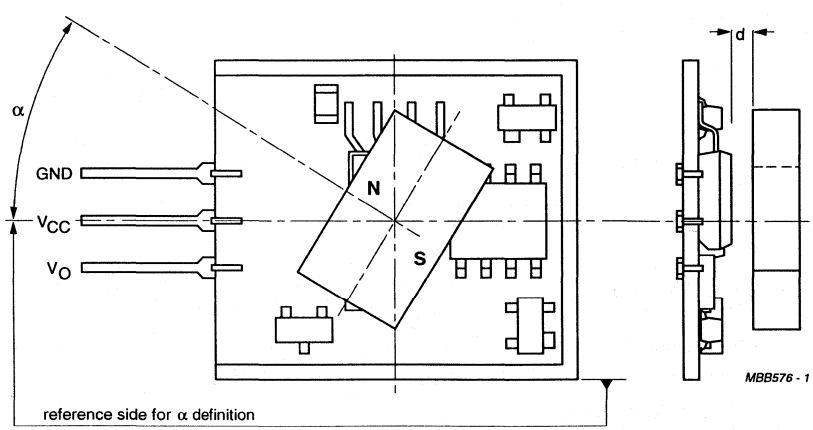


Fig.3 Optimum magnet position relative to the sensor module.

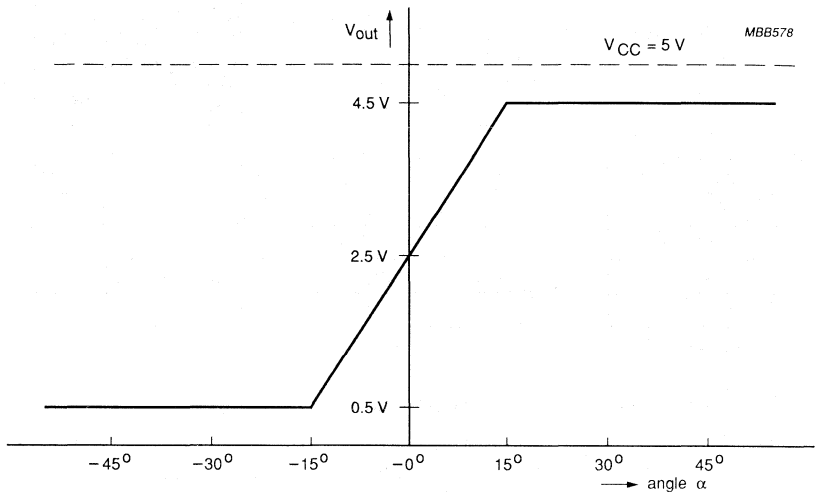


Fig.4 Output signal of KM110BH/2130.

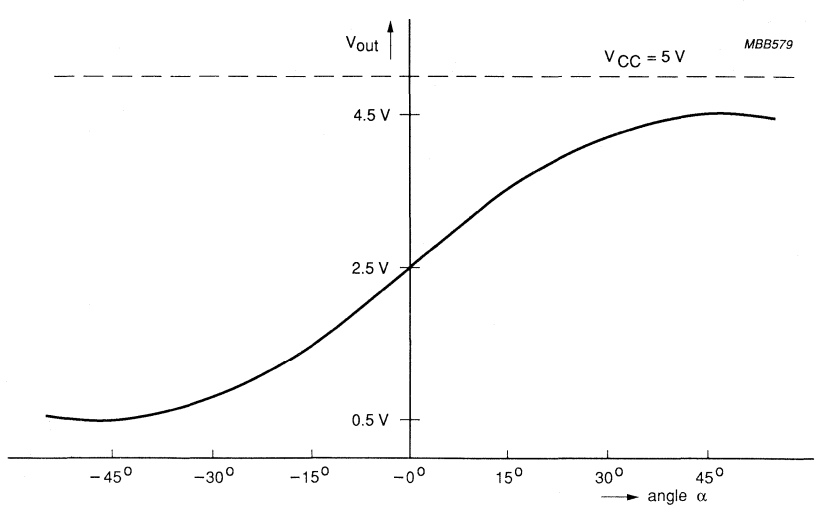


Fig.5 Output signal of KM110BH/2190.

Table 1 Magnets for angle sensor hybrids

MAGNETS			HYBRID ANGLE SENSORS			
MATERIAL	DIMENSIONS (note 1) (mm)	TEMP. RANGE (°C)	DISTANCE d (note 2) (mm)	ANGLE RANGE CORRESPONDING TO V_O = 0.5 to 4.5 V		TEMP. RANGE (°C)
				/2130	/2190	
NdFeB (note 3)	11.2 x 5.5 x 8	−55 to +110	2.5	30	93	−40 to +125
NdFeB (note 3)	6 x 3 x 5		0.8			
SmCo	11.2 x 5.5 x 8	−55 to +125	2.0	30	93	
SmCo	6 x 3 x 5		0.6			
FXD 330	10 x 7 x 8	−55 to +125	0.5	30.5	94.5	
FXD 330	7 x 5 x 4		0.2	30	93	

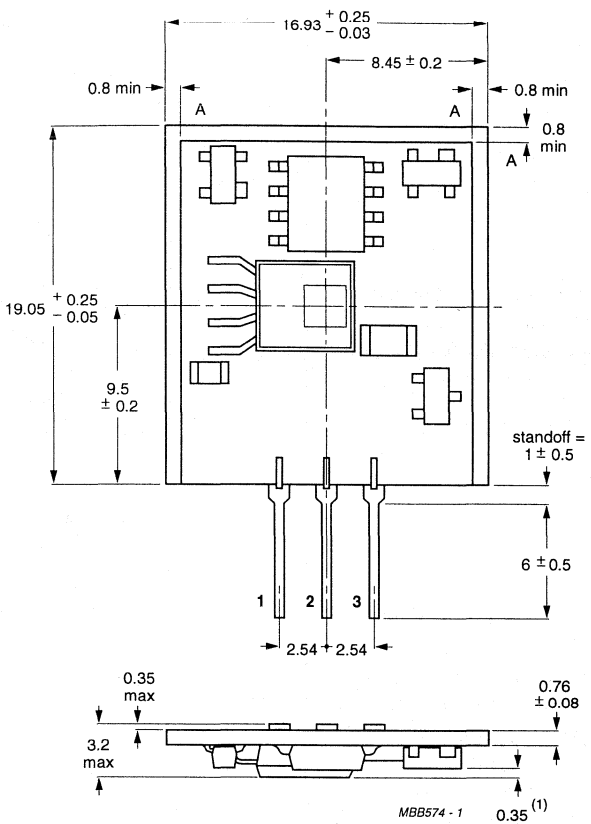
Notes

1. The magnetization is always parallel to the latter dimension given.
2. Between magnet and KMZ sensor front as shown in Fig.3.
3. Special care must be taken to avoid exposure of NdFeB magnets to moisture or vapour.

APPLICATION

In life-support systems, the behaviour of electronic components throughout their working life can be unpredictable. The use of these devices in support systems can only be permitted when there is no danger to life caused by devices failing unexpectedly.

PACKAGE OUTLINE



Dimensions in mm.

Area 'A' free of SMD devices.

(1) Sensitive layer below KMZ front.

Fig.6 KM110BH/2130; KM110BH/2190.

Angle sensor hybrid circuit KM110BH/2270

FEATURES

- Angle measuring range 70°
- Contactless, therefore wear-free and no micro-linearity problems
- Easy to mount, ready for use
- Analog current output signal
- Operating temperatures up to 100 °C
- EMC resistant
- Sample kit with magnet available.

DESCRIPTION

Sensor module for contactless measurement of angular displacements of strong magnetic fields between –35° and +35°. The module is a ready-trimmed (sensitivity and zero point) combination of the magnetoresistive sensor KMZ10B and a signal conditioning circuit in hybrid technology. The KMZ110BH/2270 delivers a sinusoidal current output signal which is a function of the direction of the magnetic field. The module can be used for contactless angle measurement.

PIN OPTIONS

The KMZ110BH/2270 sensor hybrid is available with different electrical contacts.

- Stretched pins with a pitch of 2.54 mm. These pins are recommended for connector and/or cable connections.
- Double 's' bent pins (see Fig. 6) with a pitch of 5.71 mm. Bent pins are recommended for rigid soldered connections to compensate for mechanical stress. This hybrid circuit is available under type number KM110BH/2270G.

PINNING

PIN	DESCRIPTION
1	ground
2	V_{CC}
3	I_o

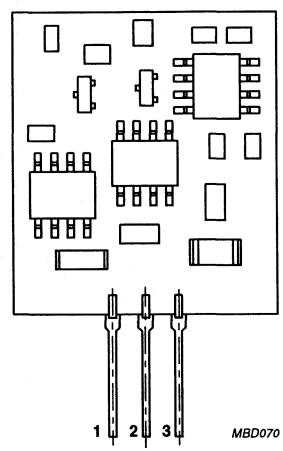


Fig.1 Simplified outline.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage	–	8.5	–	V
I_o	output current range	–	4 to 20	–	mA
α	angle range	–	–35 to +35	–	deg
T_{op}	operating temperature	–40	–	+100	°C

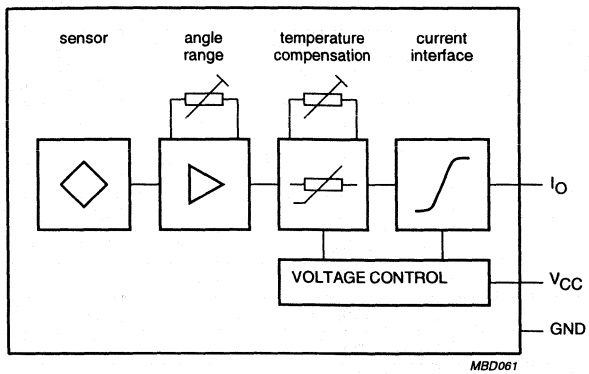


Fig.2 Circuit diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage	8.1	11	V
I_{CC}	supply current	–	40	mA
T_{stg}	storage temperature	–40	+125	°C
T_{op}	operating temperature	–40	+100	°C
	output short-circuit duration	permanent; note 1		

Note

1. If pin 3 is shorted to either pin 1 or pin 2, current may flow permanently, without damage to the device.

CHARACTERISTICS

T_{amb} = 25 °C; V_{CC} = 8.5 V and a homogeneous magnetic field H_{ext} = 100 kA/m in the sensitive layer of the KMZ10B sensor, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α	angle range	note 1	–	–35 to +35	–46.5 to +46.5	deg
I_o	output current range	note 2; sinusoidal, see Fig.4	–	4 to 20	3.2 to 20.8	mA
I_{zero}	zero point current	α = 0°	–	12	–	mA
I_{offset}	zero point offset current		–	±120	–	µA
S	sensitivity	α = 0°; note 3	0.289	0.292	0.295	mA/deg
Rp	reproducibility	α = 0°; note 4	–	<0.001	–	deg
Rs	resolution	α = 0°; note 5	–	<0.001	–	deg
Rhy	hysteresis	α = 0°; note 6	–	<0.05	–	deg
SP_{max}	maximum angular speed		–	20	–	deg/ms
R_L	load resistance		–	200	220	Ω
Temperature coefficients (–40 to +85 °C)						
TCI_{zero}	temperature coefficient of zero point current		–	±1.5	–	µA/K
TCS	temperature coefficient of sensitivity		–	±100	–	ppm/K

Note

1. Refer to Fig.3. The magnetic field H_{ext} = 100 kA/m can be achieved using the magnets listed in Table 1.
2. Maximum values refer to ±46.5° including offset and sensitivity tolerances.
3. The sensitivity will change slightly with +0.33% per 10% magnetic field increase if H_{ext} deviates from 100 kA/m.
4. Difference in output signal (expressed in degrees) between two zero point (α = 0) measurements, in which the zero point is approached from the same side of the measuring range (e.g. cycle: +35° → 0° → +35° → 0°).
5. The smallest detectable change of angle $\Delta\alpha$ for α = 0° (cycle: 0° → $\Delta\alpha$).
6. As note 4, but with the zero point being approached from the upper end and lower end of the measuring range respectively (cycle: +35° → 0° → –35° → 0°).

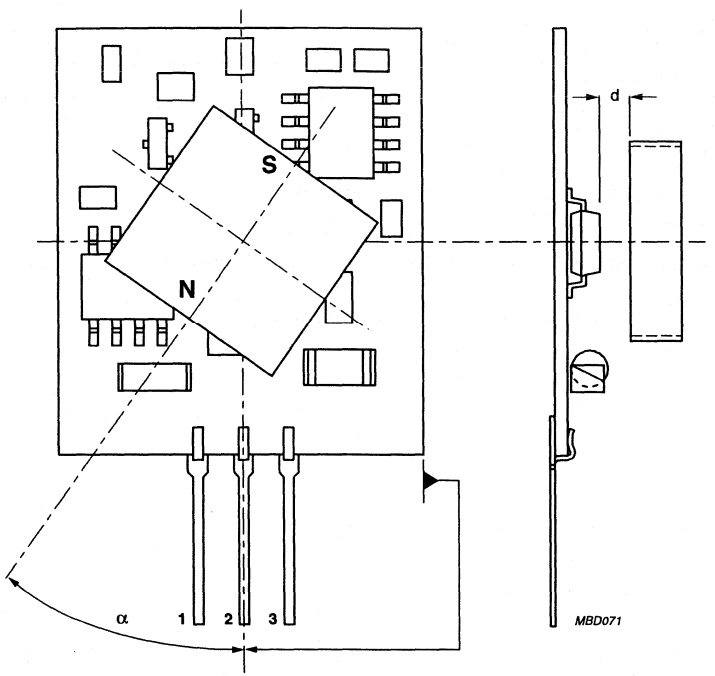


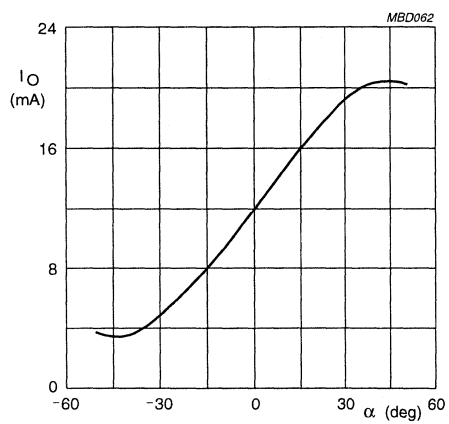
Fig.3 Optimum magnet position relative to the sensor module.

Table 1 Magnets for angle sensor hybrid.

MATERIAL	DIMENSIONS (note 1) (mm)	DISTANCE 'd' (note 2) (mm)	TOLERANCE OF 'd' (note 3) (mm)	EXCENTRICITY (note 4) (mm)	TEMPERATURE RANGE (°C)
Sm_2Co_{17}	11.2 x 5.5 x 8	2.1	±0.30	±0.25	−55 to +125
	6 x 3 x 5	0.7	±0.15	±0.15	
	8 x 3 x 7.5	0.5	±0.30	±0.20	

Notes

1. The magnetization is always parallel to the latter given dimensions.
2. Between magnet and KMZ11B1 sensor front as shown in Fig.3.
3. Maximum deviation of distance 'd' for which the change in sensor output signal is smaller than 0.5% of full scale sensor signal.
4. Maximum deviation of magnet rotational axis to sensor rotational axis for which the change in sensor output signal is smaller than 0.5% of full scale sensor signal.



$I_{o(nom)} = 12 + 8.644 \times \sin(1.935 \times \alpha)$ in the range $-46.5° \leq \alpha \leq +46.5°$.
$T_{amb} = 25$ °C; $V_{CC} = 8.5$ V; $H_{ext} = 100$ kA/m.

Fig.4 Output current as a function of angular displacement.

APPLICATION INFORMATION

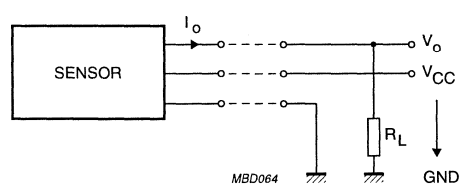
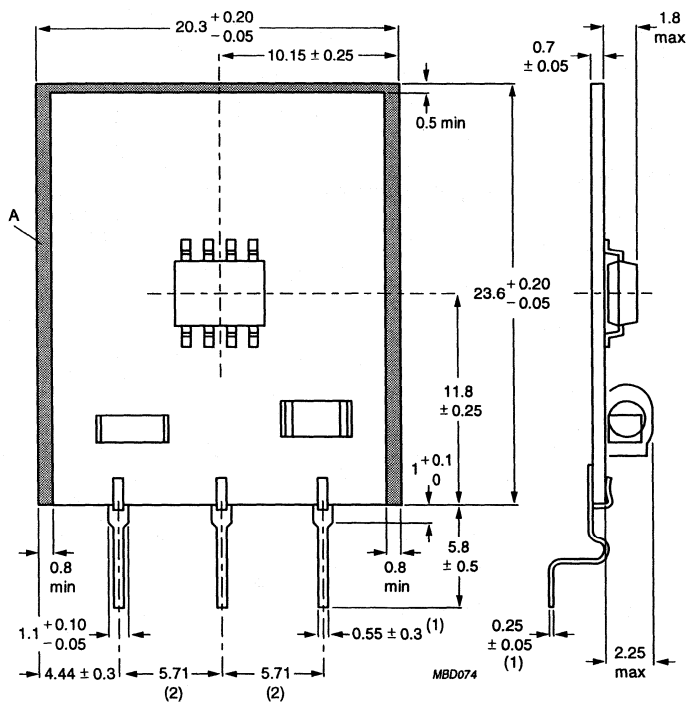


Fig.5 Application example.

PACKAGE OUTLINE - BENT PIN OPTION



Dimensions in mm.

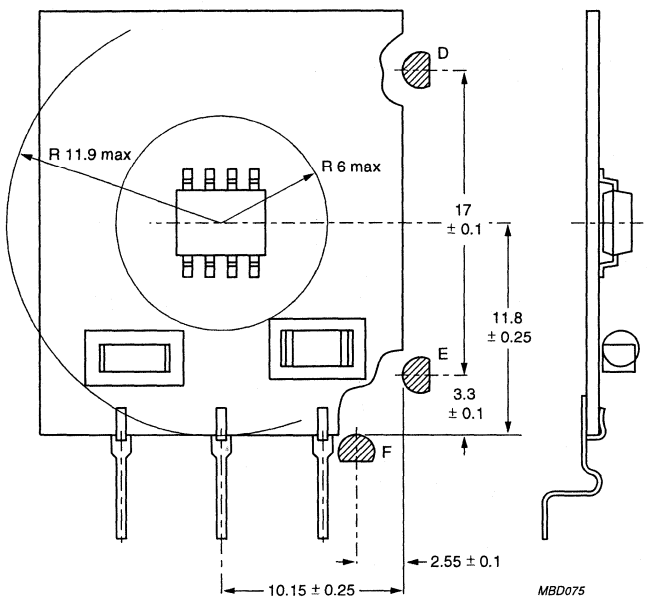
Area 'A' (shaded) free of SMD devices.

(1) Dimension before bath soldering; maximum dimension after bath soldering: 0.7 mm.

(2) Pitch tolerance: 0.2 mm.

Fig.6 KM110BH/2270G.

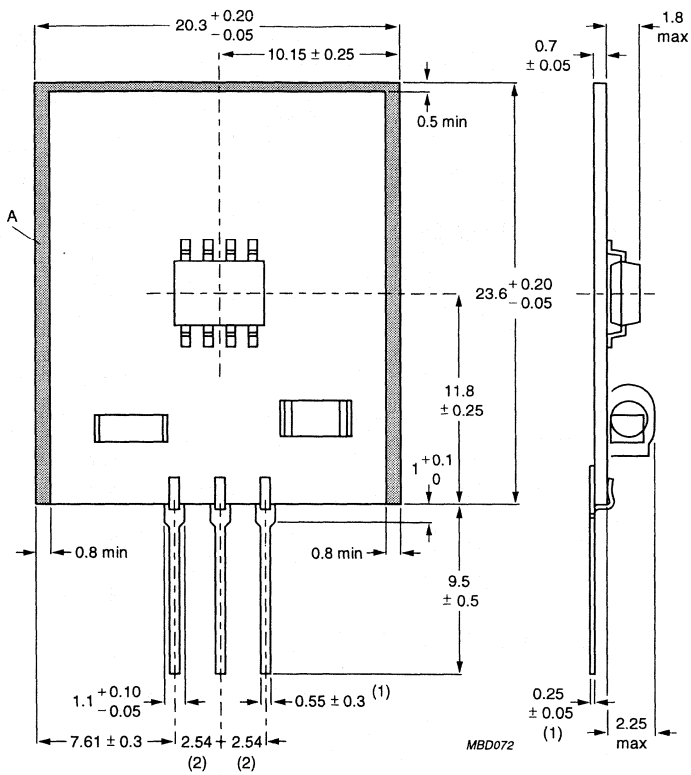
REFERENCE DATA FOR THE ASSEMBLY AND MAGNET POSITIONING - BENT PIN OPTION



Dimensions in mm.
D,E: Definition of reference side for angle α.
D,E,F: Reference points for sensor assembly.
Radii for free rotation of magnets due to height of the components on the hybrid circuit.

Fig.7 KM110BH/2270G.

PACKAGE OUTLINE - STRETCHED PIN OPTION



Dimensions in mm.

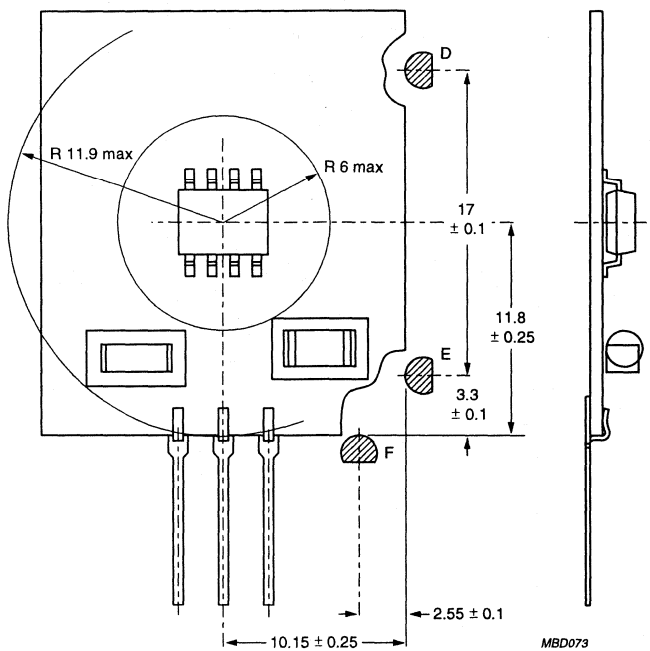
Area 'A' (shaded) free of SMD devices.

(1) Dimension before bath soldering; maximum dimension after bath soldering: 0.7 mm.

(2) Pitch tolerance: 0.2 mm.

Fig.8 KM110BH/2270.

REFERENCE DATA FOR THE ASSEMBLY AND MAGNET POSITIONING - STRETCHED PIN OPTION



Dimensions in mm.
D,E: Definition of reference side for angle α.
D,E,F: Reference points for sensor assembly.
Radii for free rotation of magnets due to height of the components on the hybrid circuit.

Fig.9 KM110BH/2270.

Contactless angle sensor KMA10/70

FEATURES

- Angle measuring range 70°
- Contactless, therefore wear-free and no micro-linearity problems
- Easy to mount, ready for use
- Mechanically adjustable
- Analog current output signal
- Operating temperatures up to 100 °C
- Rugged mechanical design
- Resistant against aggressive media, pressurized water, etc.
- EMC resistant
- Sample kit with connector available.

PINNING

PIN	DESCRIPTION
1	ground
2	V_{CC}
3	I_o

DESCRIPTION

Sensor module for contactless measurement of angular displacements of strong magnetic fields between –35° and +35°. The sensor is based on the magnetoresistive sensor KMZ11B1 and contains a signal conditioning circuit in hybrid technology. The KMA10/70 delivers a sinusoidal current output signal which is a function of the angular displacement. The sensor can be used for contactless angle measurement or as a contactless potentiometer and can be directly mounted into equipment.

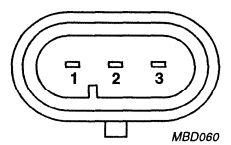


Fig.1 Simplified connector outline.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage	–	8.5	–	V
I_o	output current range	–	4 to 20	–	mA
α	angle range	–	–35 to +35	–	deg
T_{op}	operating temperature	–40	–	+100	°C

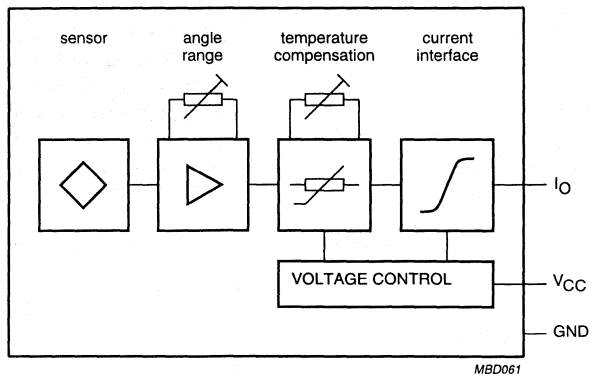


Fig.2 Functional diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage	8.1	11	V
I_{CC}	supply current	–	40	mA
T_{stg}	storage temperature	−40	+125	°C
T_{op}	operating temperature	−40	+100	°C
	output short-circuit duration	permanent; note 1		

Note

1. If pin 3 is shorted to either pin 1 or pin 2, current may flow permanently without damage to the device.

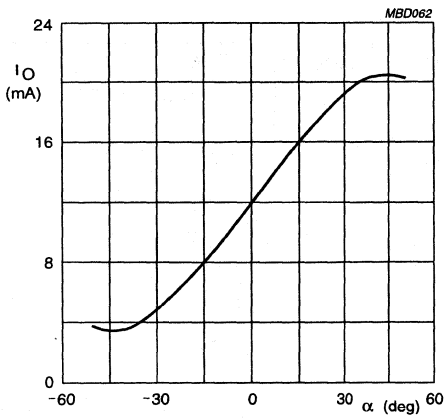
CHARACTERISTICS

T_{amb} = 25 °C; V_{CC} = 8.5 V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α	angle range	see Fig.6	–	–35 to +35	–46.5 to +46.5	deg
I_o	output current range	sinusoidal; note 1 see Fig.3	–	4 to 20	3.2 to 20.8	mA
I_{zero}	zero point current	α = 0°	–	12	–	mA
I_{offset}	zero point offset current		–	±120	–	µA
S	sensitivity	α = 0°	0.289	0.292	0.295	mA/deg
Rp	reproducibility	α = 0°; note 2	–	<0.001	–	deg
Rs	resolution	α = 0°; note 3	–	<0.001	–	deg
Rhy	hysteresis	α = 0°; note 4	–	<0.05	–	deg
SP_{max}	maximum angular speed		–	20	–	deg/ms
R_L	load resistance		–	200	220	Ω
Temperature coefficients (–40 to +85 °C)						
TCI_{zero}	temperature coefficient of zero point current		–	±1.5	–	µA/K
TCS	temperature coefficient of sensitivity		–	±100	–	ppm/K
Mechanical						
total mechanical travel			–	–75 to +75	–	deg
allowed torque to mechanical stop			–	–	0.2	Nm
maximum torque perpendicular to rotation axis			–	–	30	Nmm
maximum screw torque for fixing with washer (washer diameter ∅10 mm)			2	2.5	3	Nm
number of cycles (70°)			–	1×10^8	–	
number of dither cycles			–	8×10^8	–	
protection class according to DIN 40050			IP65	–	–	

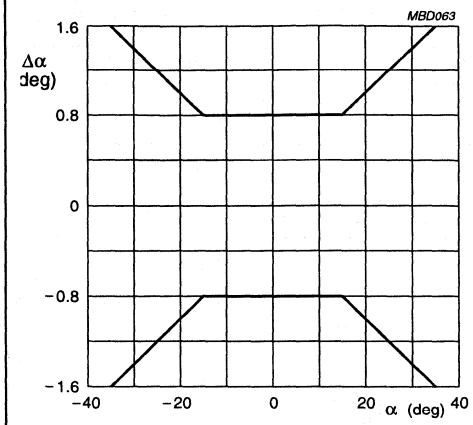
Notes

1. Maximum values refer to ±46.5° including offset and sensitivity tolerances.
2. Difference in output signal (expressed in degrees) between two zero point (α = 0) measurements, in which the zero point is approached from the same side of the measuring range (e.g. cycle: +35° → 0° → +35° → 0°).
3. The smallest detectable change of angle $\Delta\alpha$ for α = 0° (cycle: 0° → $\Delta\alpha$).
4. As note 2, but with the zero point being approached from the upper end and lower end of the measuring range respectively (cycle: +35° → 0° → 35° → 0°).



$I_{o\ (nom)} = 12 + 8.644 \times \sin(1.935 \times \alpha)$ in the range $-46.5° \leq \alpha \leq +46.5°$.
$T_{amb} = 25$ °C; $V_{CC} = 8.5$ V.

Fig.3 Output current as a function of angular displacement.



The zero point $\alpha = 0$ is defined for $I_o = 12$ mA.
$T_{amb} = -20$ to +85 °C.
$\Delta\alpha$ increases by a factor of 2 for $T_{amb} = -40$ to −20 °C and +85 °C to +100 °C.

Fig.4 Maximum absolute angle error $\Delta\alpha$.

APPLICATION INFORMATION

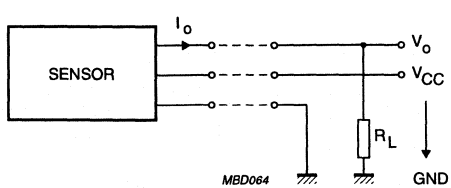


Fig.5 Application example.

MECHANICAL DATA

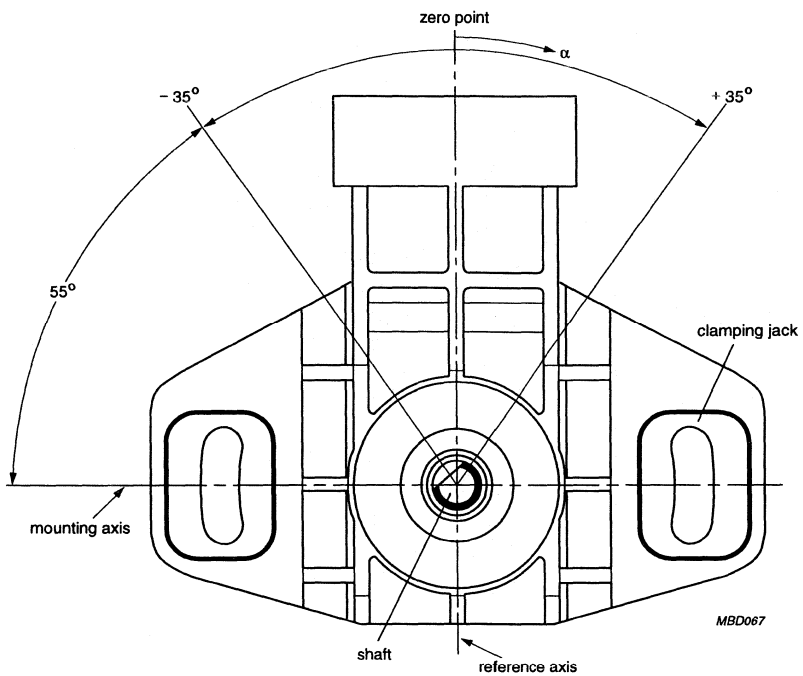


Fig.6 Front view.

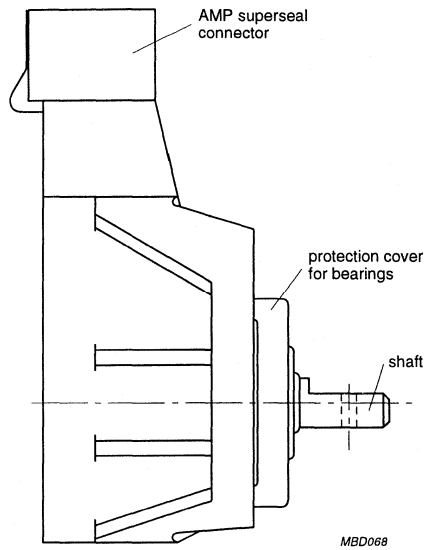
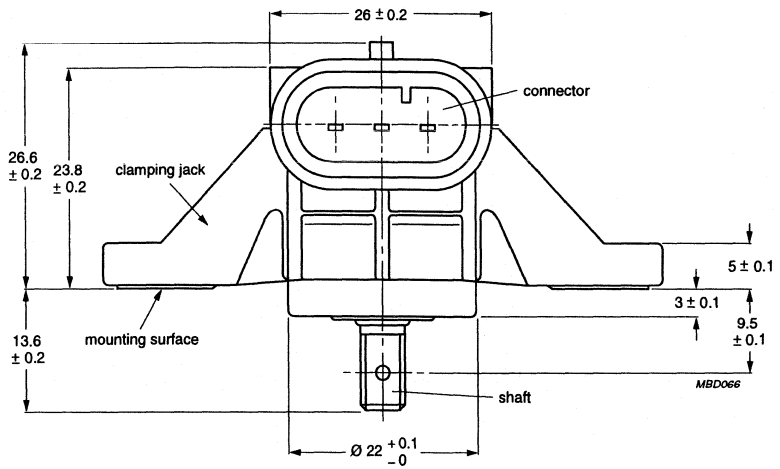
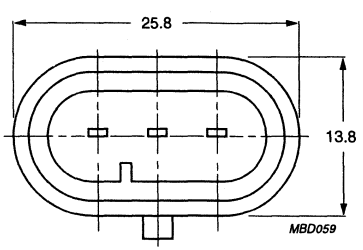


Fig.7 Side view.



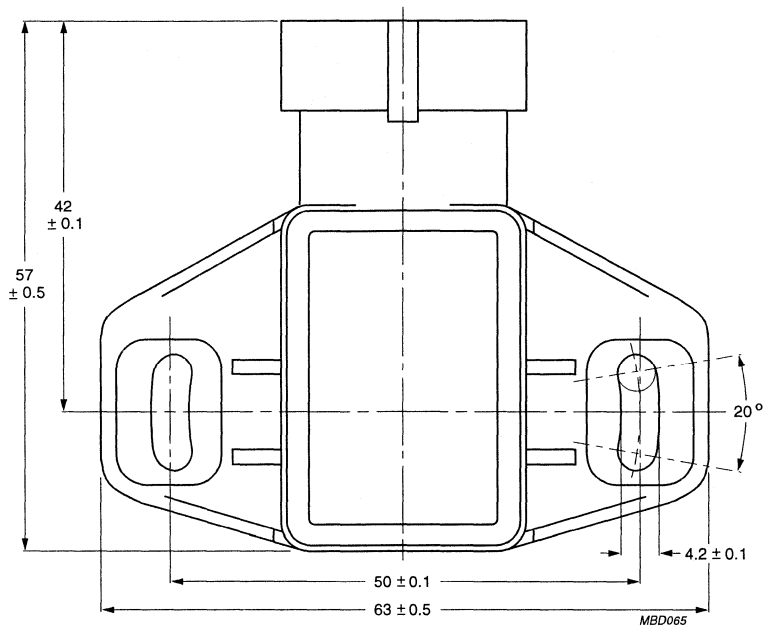
Dimensions in mm.

Fig.8 Top view and dimensions.



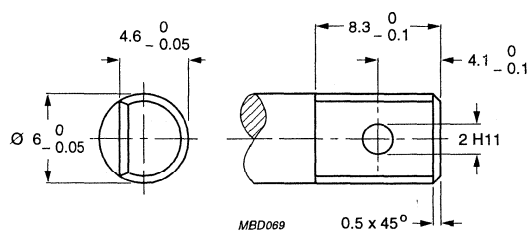
Dimensions in mm.

Fig.9 Connector detail.



Dimensions in mm.

Fig.10 Back view and dimensions.



Dimensions in mm.

Fig.11 Shaft detail.

MOUNTING

When sensor is mounted into equipment, pressure should only be exerted on the clamping jacks. The mounting area should correspond to the washer diameter (maximum mounting pressure 100 N). Pressure should be perpendicular to the clamping surface.

The screw torque for fixing with a washer (washer diameter Ø10 mm) is min. 2, typ. 2.5 and max. 3 Nm.

CONNECTOR

The sensor has a 3 pin AMP SUPERSEAL 1.5 series connector. For the recommended matching plug connector the following AMP part numbers are valid:

- plug connector part number 282087-1
- receptacle contact (strip form, wire size range 1.0 to 1.5 mm^2) part number 282110-1
- single wire seal (yellow, insulation diameter 1.8 to 2.4 mm) part number 281934-2.

Contactless angle sensors KMA20/30; KMA20/70

FEATURES

- Angle measuring range 30° or 70°
- Contactless, therefore wearfree and no microlinearity problems
- Easy to mount, ready for use
- Mechanically adjustable
- 5 V supply; ratiometric voltage output signal
- Operating temperatures up to 125 °C
- Rugged mechanical design
- Resistant against aggressive media, pressurized water, etc.
- EMC resistant
- Sample kit with connector available.

PINNING

PIN	DESCRIPTION
1	GND (ground)
2	V_{CC}
3	V_O

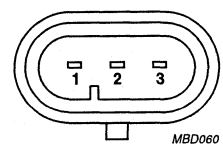


Fig.1 Pin configuration.

DESCRIPTION

Encapsulated angle sensors for contactless measurement of angular displacements. The sensor is based on the magnetoresistive Sensor KMZ and contains a signal conditioning circuit in hybrid technology.

The KMA20/30 delivers a linear and the KMA20/70 a sinusoidal voltage output signal which are a function of the angular displacement. These sensors can be used for contactless angle measurement or as contactless potentiometers and can be directly mounted into equipment.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage	–	5	–	V
T_{oper}	operating temperature	–40	–	+125	°C
α	angle range:				
	KMA20/30	–	–15 to +15	–	deg
	KMA20/70	–	–35 to +35	–	deg
V_O	output voltage range	–	0.5 to 4.5	–	V

EMC RESISTIVITY

The EMC compatibility is dependent on the assembly of the sensors. The EMC resistivity has to be tested in the final application.

BLOCK DIAGRAM

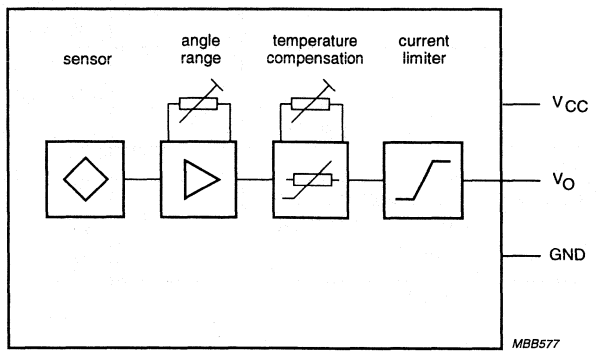


Fig.2 Block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage	4.5	16	V
I_{CC}	supply current	–	15	mA
T_{stg}	storage temperature	–40	+125	°C
T_{oper}	operating temperature; note 1	–40	+125	°C
	output short-circuit duration to GND	permanent, note 2		

Note

1. For operations above T_{oper} = 100 °C, maximum V_{CC} derates linearly from 16 V to 5 V at T_{oper} = 125 °C.
2. If pin 3 is shorted to either pin 1 or pin 2, current may flow permanently, without damaging the sensors.

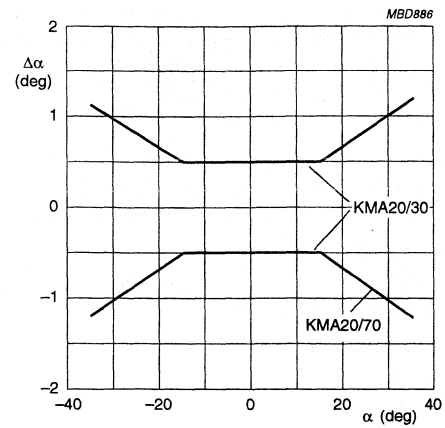
CHARACTERISTICS

T_{amb} = 25 °C; V_{CC} = 5 V; R_L = 1.7 kΩ, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α	angle range:	see Fig.12				
	KMA20/30		–	–15 to +15	–	deg
	KMA20/70		–	–35 to +35	–	deg
V_O	output voltage range:					
	KMA20/30	linear; see Fig.5	–	0.5 to 4.5	–	V
	KMA20/70	sinusoidal; see Fig.4	–	0.5 to 4.5	–	V
V_{zero}	zero point voltage	α = 0°	–	2.5	–	V
V_{off}	zero point offset voltage:	related to sinusoidal sensor characteristic; see Fig.4				
	KMA20/30		–	±25	–	mV
	KMA20/70		–	±15	–	mV
S	sensitivity:	α = 0°				
	KMA20/30		137	140	143	mV/deg
	KMA20/70		73	74.5	76	mV/deg
R_p	reproducibility	α = 0°; note 1	–	<0.001	–	deg
R_s	resolution	α = 0°; note 2	–	<0.001	–	deg
FH	hysteresis	α = 0°; note 3	–	<0.05	–	deg
SP_{max}	maximum angular speed:					
	KMA20/30		–	60	–	deg/ms
	KMA20/70		–	150	–	deg/ms
R_L	load resistance		1.7	–	–	kΩ
C_L	load capacitor		–	–	10	nF
Temperature coefficients (–40 to +100 °C)						
TCV_{zero}	temperature coefficient of zero point voltage:					
	KMA20/30		–	0.25	0.6	mV/K
	KMA20/70		–	0.1	0.3	mV/K
TCS	temperature coefficient of sensitivity		–	100×10^{-6}	–	K^{-1}

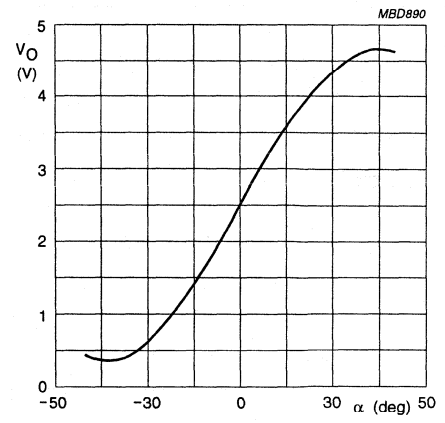
Notes

1. Difference in output signal (expressed in degrees) between two zero point (α = 0°) measurements, in which the zero point is approached from the same side of the measuring range (e.g. cycle: +15° ⇒ 0° ⇒ +15° ⇒ 0°).
2. The smallest detectable change of angle Δα for α = 0° (cycle: 0° ⇒ Δα).
3. As note 1, but with the zero point being approached from the upper end and lower end of the measuring range respectively (e.g. cycle: +15° ⇒ 0° ⇒ –15° ⇒ 0°).



T_{amb} = −25 to +85 °C.
α = 0° for T_{amb} = 25 °C and V_O = 2.5 V.
Δα increases by a factor 2 in the temperature range:
T_{amb} = −40 to −20 °C and +85 to +125 °C.

Fig.3 Maximum angle error Δα as a function of angle position.



$V_O = 2.5 + 2.128 \times \sin(2\alpha)$ for $-36.5° \leq \alpha \leq +36.5°$.
T_{amb} = 25 °C; V_{CC} = 5 V.

Fig.4 KMA20/70 output signal as a function of angle position.

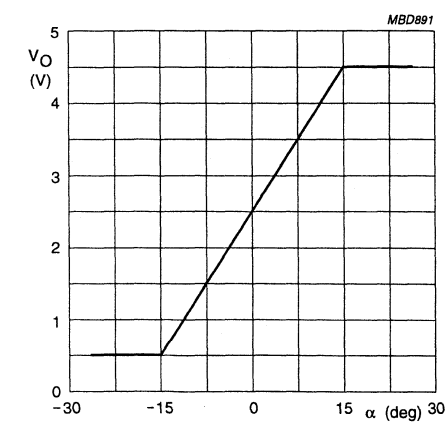


Fig.5 KMA20/30 output signal as a function of angle position.

APPLICATION INFORMATION

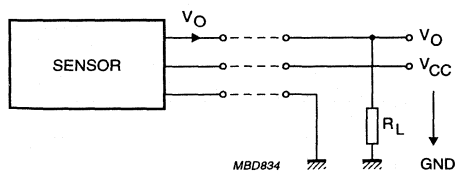


Fig.6 Application circuit.

MOUNTING INSTRUCTIONS

When the sensors are mounted into equipment pressure should be exerted on clamping jacks only. The mounting area should correspond to the washer diameter (maximum mounting pressure is 100 N). Pressure should be perpendicular to clamping surface.

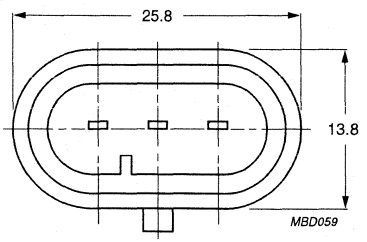
The sensors provides a 3-pin AMP SUPERSEAL 1.5 series connector. For the recommended matching plug connector the following AMP part numbers are valid:

- Plug connector part no. 282087-1
- Receptable contact (strip form, wire size 1.0 to 1.5 mm^2) part no. 282110-1
- Single wire seal (yellow, insulation diameter 1.8 to 2.4 mm) part no. 281934-2.

Mounting data

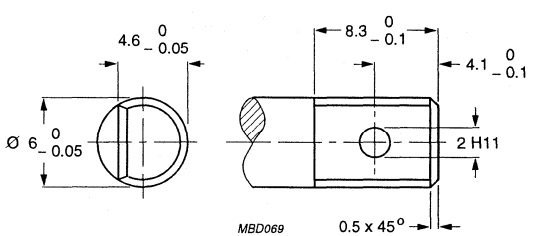
DESCRIPTION	MIN.	TYP.	MAX.	UNIT
Total mechanical travel	–	–75 to +75	–	deg
Allowed torque to mechanical stop	–	–	0.2	Nm
Maximum torque perpendicular to rotation axis	–	–	30	Nmm
Maximum screw torque for fixing with washer (washer diameter ∅ 10 mm)	2	2.5	3	Nm
Number of cycles (70°)	–	1×10^8	–	
Protection class according to DIN	IP65	–	–	

CONNECTOR AND SHAFT DIMENSIONS



Dimensions in mm.

Fig.7 Connector dimensions.



Dimensions in mm.

Fig.8 Shaft dimensions.

PACKAGE OUTLINE

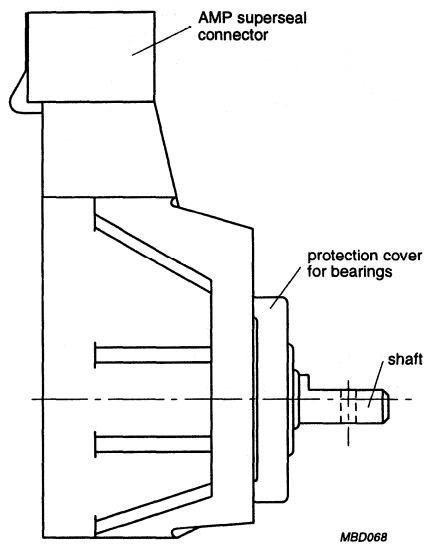
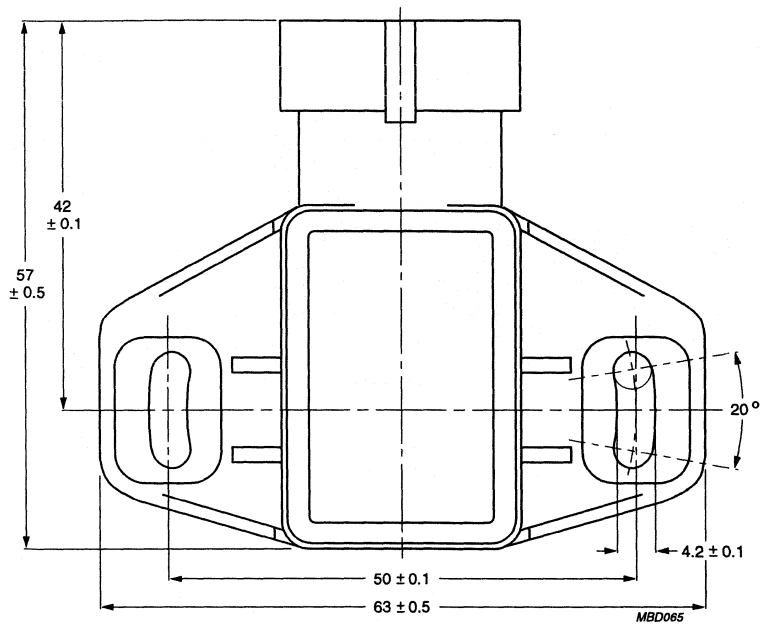
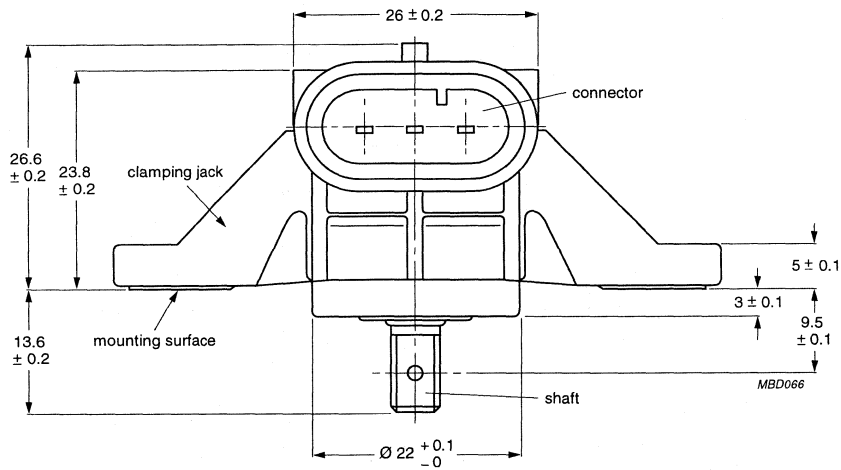


Fig.9 Side view.



Dimensions in mm.

Fig.10 Back view.



Dimensions in mm.

Fig.11 Top view.

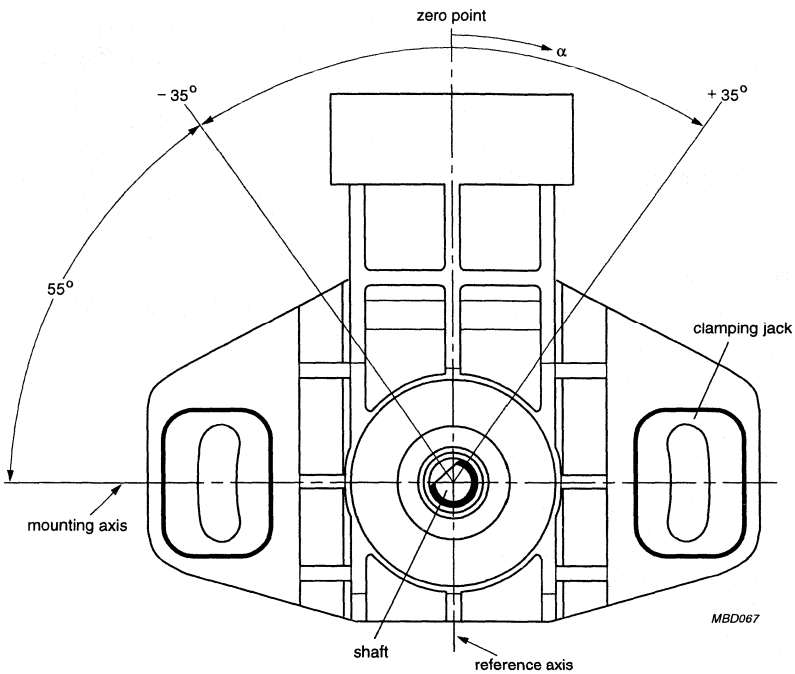


Fig.12 Front view.

Contactless angle sensor KMA20/90

FEATURES

- Linear angle measuring range >90°
- Contactless, therefore wearfree
- Easy to mount, ready for use
- Mechanically adjustable
- 5 V supply; ratiometric voltage output signal
- Operating temperatures up to 125 °C
- Rugged mechanical design
- Resistant against aggressive media, pressurized water, etc.
- EMC resistant
- Sample kit with connector available.

PINNING

PIN	DESCRIPTION
1	GND (ground)
2	V_{CC}
3	V_O

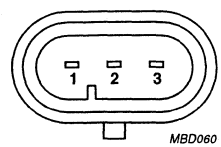


Fig.1 Pin configuration.

DESCRIPTION

Encapsulated angle sensor for contactless measurement of angular displacements. The sensor is based on the magnetoresistive Sensor KMZ and contains a signal conditioning circuit in hybrid technology.

The KMA20/90 delivers a linear voltage output signal which is a function of the angular displacement. The sensor can be used for contactless angle measurement or as a contactless potentiometer and can be directly mounted into equipment.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage	–	5	–	V
T_{oper}	operating temperature	–40	–	+125	°C
α	angle range	–	–45 to +45	–	deg
V_O	output voltage range	–	0.5 to 4.5	–	V

EMC RESISTIVITY

The EMC compatibility is dependent on the assembly of the sensor. The EMC resistivity has to be tested in the final application.

BLOCK DIAGRAM

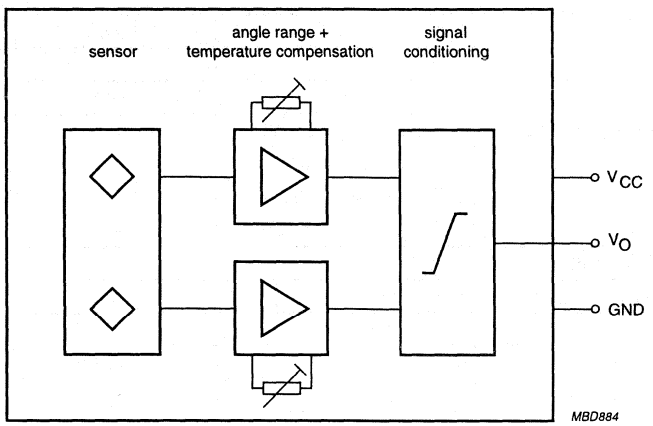


Fig.2 Block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage	4.5	16	V
I_{CC}	supply current	–	25	mA
T_{stg}	storage temperature	−40	+125	°C
T_{oper}	operating temperature; note 1	−40	+125	°C
	output short-circuit duration to GND	permanent; note 2		

Notes

1. For operations above T_{oper} = 100 °C, maximum V_{CC} derates linearly from 16 V to 5 V at T_{oper} = 125 °C.
2. If pin 3 is shorted to either pin 1 or pin 2, current may flow permanently, without damaging the sensor.

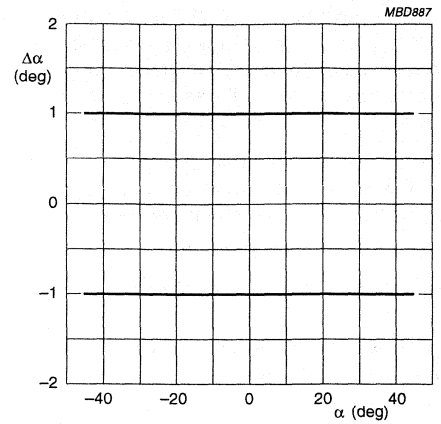
CHARACTERISTICS

T_{amb} = 25 °C; V_{CC} = 5 V; R_L = 25 kΩ, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α	angle range	see Fig.11	–	–45 to +45	–53 to +53	deg
V_O	output voltage range	linear; see Fig.4	–	0.5 to 4.5	0.15 to 4.85	V
V_{zero}	zero point voltage	α = 0°	–	2.5	–	V
S	sensitivity	α = 0°	43.5	44.5	45.5	mV/deg
$\Delta\alpha$	maximum expected angle error	related to V_{ref} = 2.5 V:				
		T_{amb} = –20 to +85 °C	–	–	1	deg
		T_{amb} = –40 to –20 °C	–	–	1.5	deg
		T_{amb} = +85 to +125 °C	–	–	1.5	deg
FL	deviation of linearity	note 1	–	1	2	%·FS
R_p	reproducibility	α = 0°; note 2	–	<0.001	–	deg
R_s	resolution	α = 0°; note 3	–	<0.001	–	deg
FH	hysteresis	α = 0°; note 4	–	<0.05	–	deg
SP_{max}	maximum angular speed		–	50	–	deg/ms
R_L	load resistance		10	–	–	kΩ
C_L	load capacitor		–	–	10	nF
Temperature coefficients (–40 to +100 °C)						
TCV_{zero}	temperature coefficient of zero point voltage		–	0.2	0.6	mV/K
TCS	temperature coefficient of sensitivity		–	$\pm 100 \times 10^{-6}$	–	K^{-1}

Notes

1. Deviation of best straight line in angle range.
2. Difference in output signal (expressed in degrees) between two zero point (α = 0°) measurements, in which the zero point is approached from the same side of the measuring range (e.g. cycle: +45° ⇒ 0° ⇒ +45° ⇒ 0°).
3. The smallest detectable change of angle $\Delta\alpha$ for α = 0° (cycle: 0° ⇒ $\Delta\alpha$).
4. As note 2, but with the zero point being approached from the upper end and lower end of the measuring range respectively (e.g. cycle: +45° ⇒ 0° ⇒ –45° ⇒0°).



T_{amb} = −25 to +85 °C.
α = 0° for T_{amb} = 25 °C and V_O = 2.5 V.
Δα increases by a factor 2 in the temperature range:
T_{amb} = −40 to −85 °C and +85 to +125 °C.

Fig.3 Maximum angle error Δα as a function of angle position.

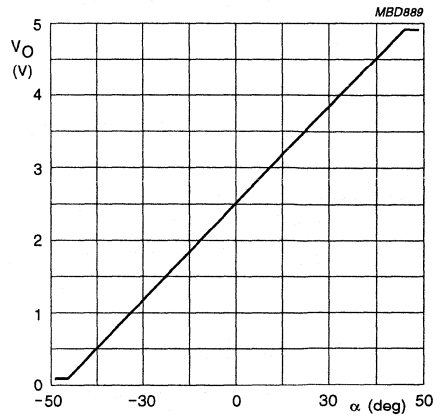


Fig.4 Output signal as a function of angle position.

APPLICATION INFORMATION

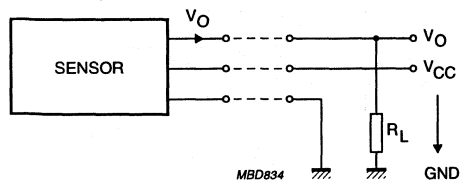


Fig.5 Application circuit.

MOUNTING INSTRUCTIONS

When sensor is mounted into equipment pressure should be exerted on clamping jacks only. The mounting area should correspond to the washer diameter (maximum mounting pressure is 100 N). Pressure should be perpendicular to clamping surface.

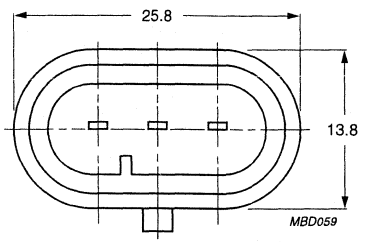
The sensor provides a 3-pin AMP SUPERSEAL 1.5 series connector. For the recommended matching plug connector the following AMP part numbers are valid:

- Plug connector part no. 282087-1
- Receptable contact (strip form, wire size 1.0 to 1.5 mm^2) part no. 282110-1
- Single wire seal (yellow, insulation diameter 1.8 to 2.4 mm) part no. 281934-2.

Mounting data

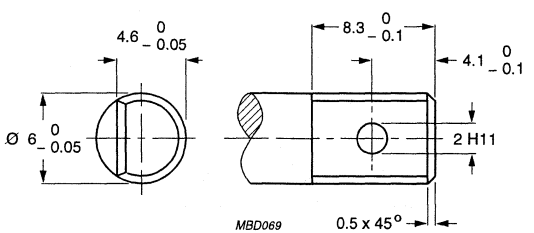
DESCRIPTION	MIN.	TYP.	MAX.	UNIT
Total mechanical travel	–	–75 to +75	–	deg
Allowed torque to mechanical stop	–	–	0.2	Nm
Maximum torque perpendicular to rotation axis	–	–	30	Nmm
Maximum screw torque for fixing with washer (washer diameter Ø 10 mm)	2	2.5	3	Nm
Number of cycles (90°)	–	1×10^8	–	
Protection class according to DIN	IP65	–	–	

CONNECTOR AND SHAFT DIMENSIONS



Dimensions in mm.

Fig.6 Connector dimensions.



Dimensions in mm.

Fig.7 Shaft dimensions.

PACKAGE OUTLINE

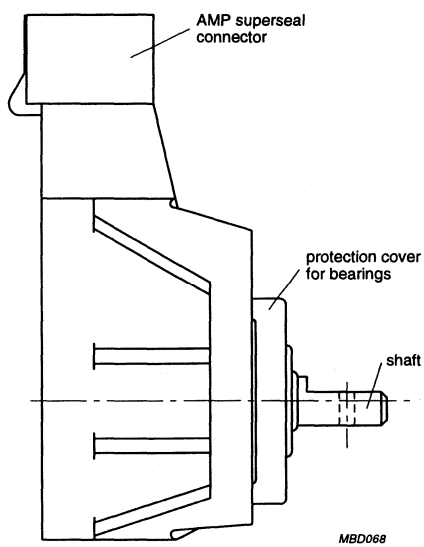
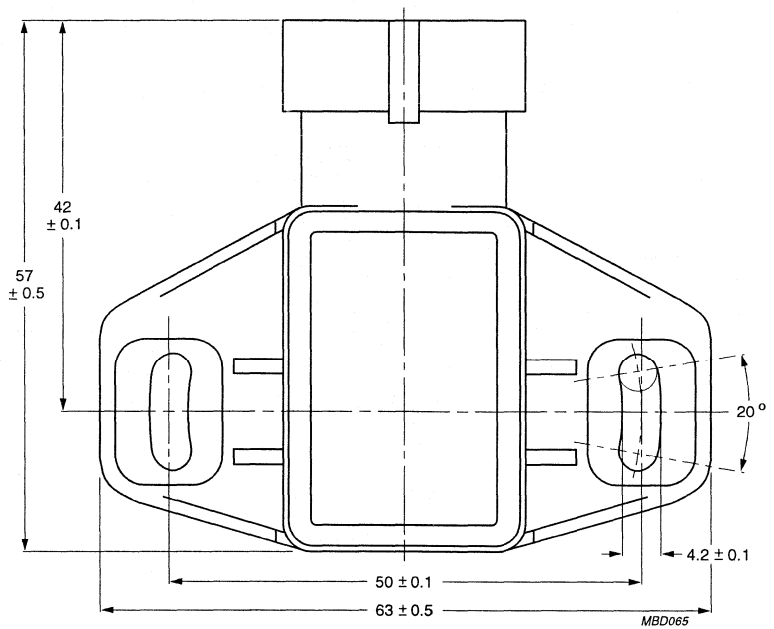
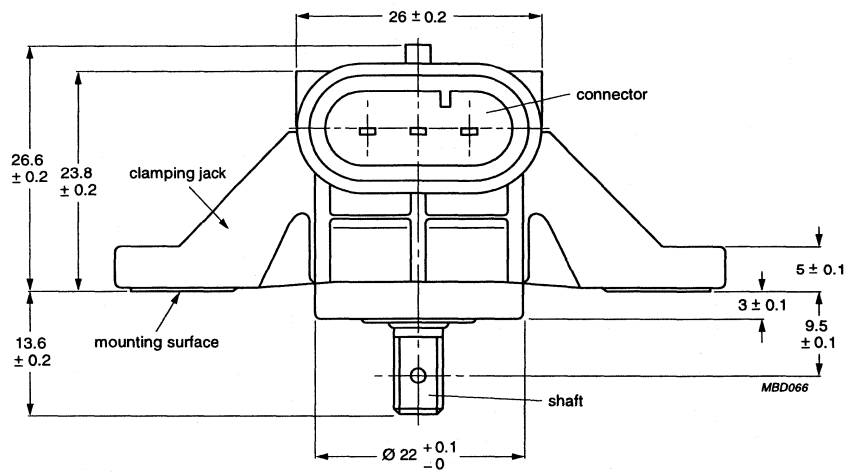


Fig.8 Side view.



Dimensions in mm.

Fig.9 Back view.



Dimensions in mm.

Fig.10 Top view.

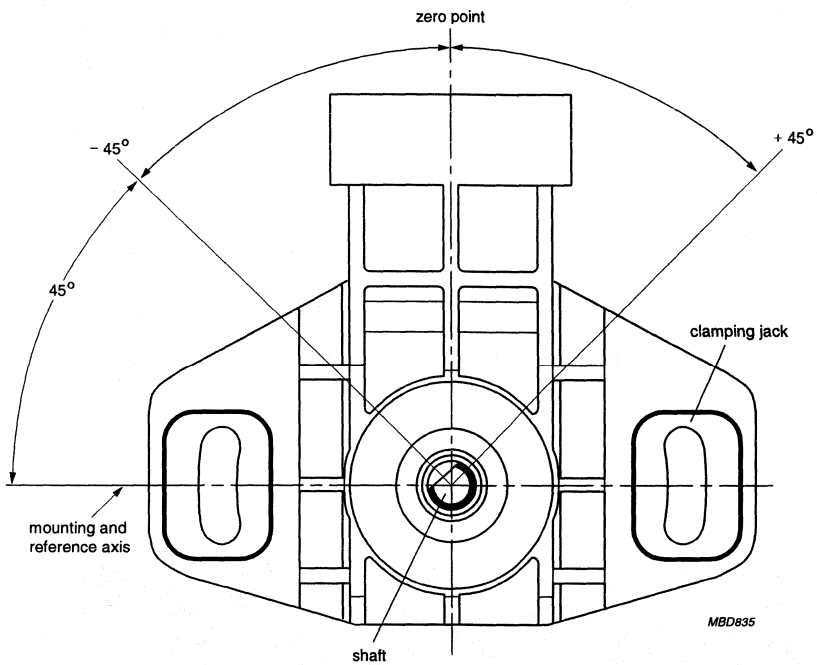


Fig.11 Front view.

Sensor hybrid modules — General part 1

GENERAL

The KMZ10 and KMZ11 series of magnetoresistive sensors are successfully used in a wide range of applications, due to their excellent characteristics:

- High sensitivity
- Wide operating frequency range (0 Hz (DC) to >1 MHz)
- Wide operating temperature range (–40 to +150 °C; 190 °C peak)
- Linear characteristics
- Long life
- Insensitivity to mechanical stress.

In order to assist the designer in applying KMZ sensors, Philips Semiconductors has developed a number of sensor modules for rotational speed measurement and reference mark detection in both IC and hybrid thick-film technology, containing a KMZ sensor in addition to signal conditioning circuitry. These sensor modules offer many important advantages e.g.:

- Contactless measurement, making them wear-free with a long life and high reliability
- Ready for use: all modules are trimmed; no further adjustment or trimming is required
- Shorter system-development times.

All sensor modules are offered as standard products. However, they may also serve as a starting point for the development of customized products.

The following three series of modules are described:

- KMI10 series of integrated sensors for contactless rotational speed measurement
- KM110BH/1 series of hybrid modules for contactless rotational speed measurement
- KM110BH/3 series of hybrid modules for contactless measurement of rotational speed and direction.

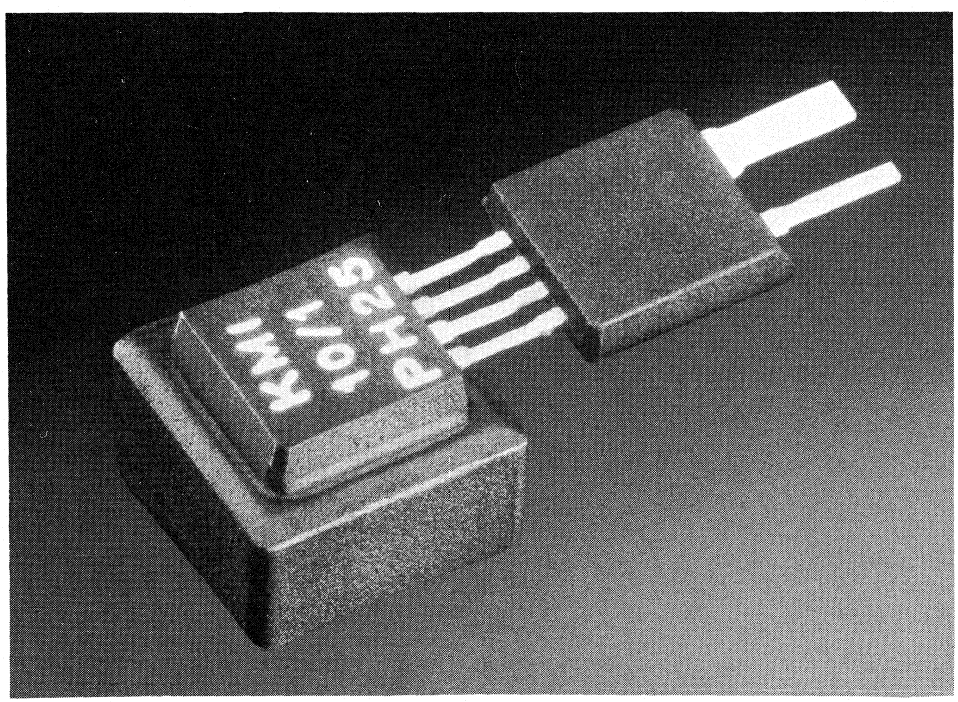


Fig.1 The KMI10/1 sensor.

THE KMI10/X INTEGRATED ROTATIONAL SPEED SENSORS

The KMI10/X sensors are designed for measuring wheel-speeds and are also suitable for reference mark, proximity switch and current detection. They comprise a KMZ10B1 magnetoresistive sensor (an adapted version of the KMZ10B sensor), a ferrite magnet and an advanced bipolar signal-conditioning IC, mounted on a single leadframe. Major features of the KMI10/X sensors are:

- Calibrated sensor, small package
- Measuring range from 0 Hz (zero speed)
- Large measuring distance (>2.5 mm)
- Digital current output signal
  - Two-lead output
- Operating temperature range up to 190 °C
- Vibration insensitive
- Wide range of gear-tooth structures possible
- EMC resistant
- Can be injection-moulded.

The data given below was measured on production-line KMI10 sensors. Both typical data and that measured beyond the allowed maximum ratings, show the sensor's excellent performance even in the most extreme environments.

Operation of the KMI10 sensors

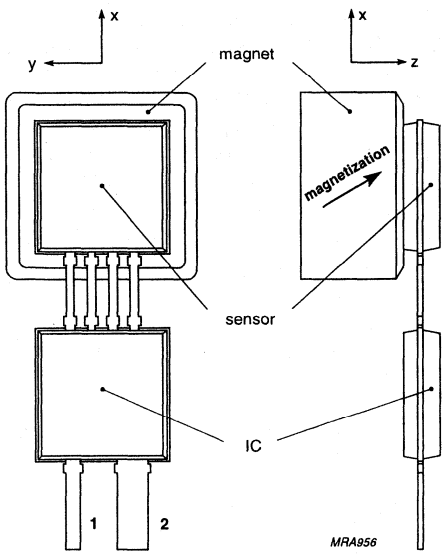
Figures 2 and 3 show the outline of the KMI10/1 and KMI10/4 sensors. The magnets are specially designed to apply a symmetrical magnetic field in the y-z plane of the sensors and a field at 30° relative to the z-axis in the x-z plane. The resulting component in the x-direction of the sensor plane stabilizes the magnetoresistive element and the symmetrical field in the y-z plane is used to detect rotational speed.

Figure 4 shows the speed detection operation. The teeth of a ferromagnetic wheel moving in the y-direction, cause a bending of the field lines which generates an output signal from the magnetoresistive sensor if the teeth have a non-symmetric position relative to the sensor. The output is always zero for symmetric positions of the teeth (i.e. either a tooth or a valley is directly in front of the sensor) and for non-symmetric positions its amplitude depends on the distance between the sensor and the wheel.

In the signal-conditioning circuit (Figs 5 and 6), the magnetoresistive sensor's output signal goes through an EMC filter and is amplified. This amplified voltage is then digitized by a comparator which contains a built-in switching hysteresis: this is realized using a Schmitt-trigger (see Section "Switching hysteresis"). A voltage-control circuit powers the sensor, the amplifier and the comparator with a stabilized 5 V supply. This circuit is in turn stabilized by a pre-stabilized bandgap-reference (GAP) diode.

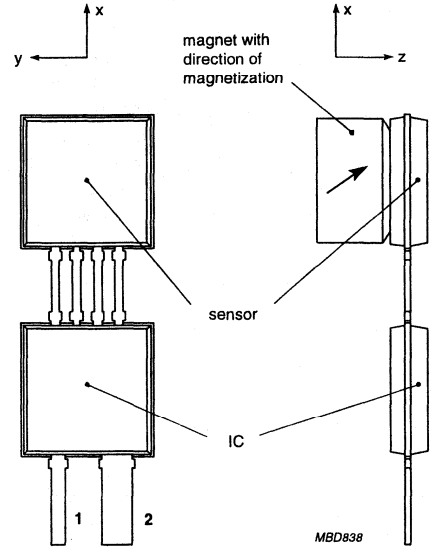
To enable The KMI10's output signal to be safely carried to a detecting circuit, the output signal is transmitted as the current (I_{CC}) in the simple two-wire supply cable. This is done using two current sources, integrated in the signal-conditioning IC. One constant current source supplies a base output current of 7 mA (which is partly used for the 5 V supply). A second, switchable, 7 mA current source is added to this when triggered by the amplified and digitized output signal of the magnetoresistive sensor. Thus, during operation, I_{CC} switches back and forth between 7 and 14 mA (see Fig.7).

The IC and magnetoresistive sensor are deliberately in separate encapsulations to optimize the KMI10's performance at high temperatures. The magnetoresistive sensor can then be exposed to higher temperatures than the IC and the IC's power dissipation will not cause inhomogeneous heating of the sensor element.



Pin 1: V_{CC} (supply voltage).
Pin 2: V– (ground).

Fig.2 Simplified outline of KMI10/1.



Pin 1: V_{CC} (supply voltage).
Pin 2: V– (ground).

Fig.3 Simplified outline of KMI10/4.

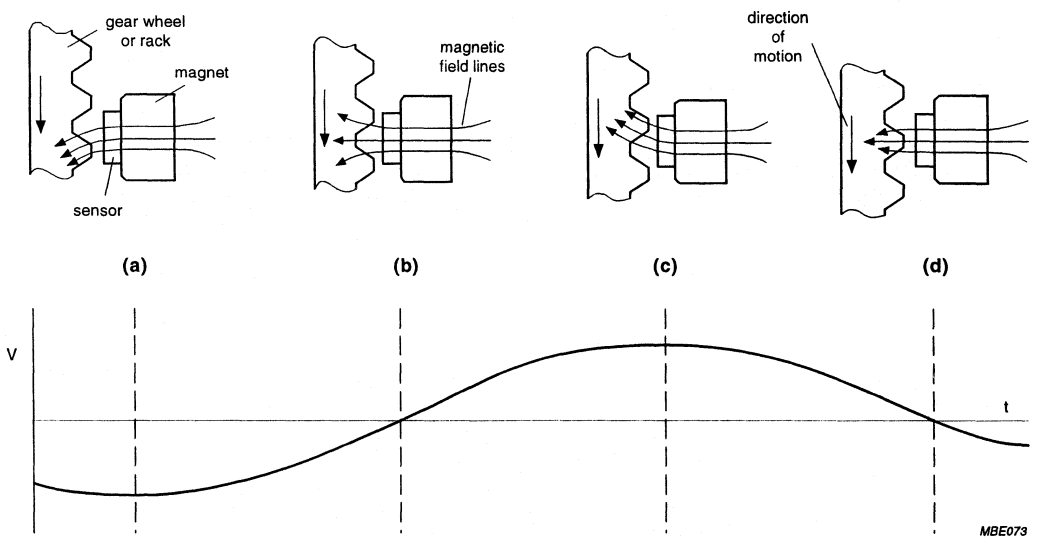


Fig.4 Speed detection using a magnetoresistive sensor.

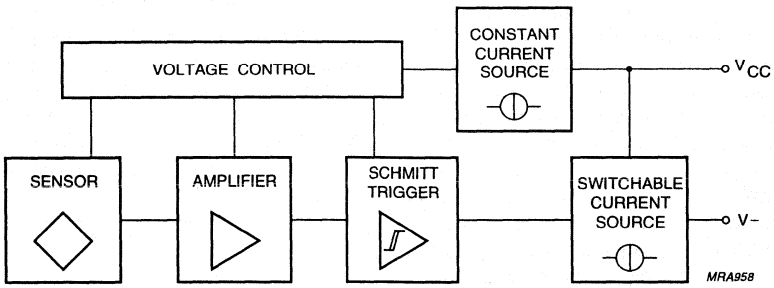


Fig.5 Block diagram of sensor and signal-conditioning circuitry.

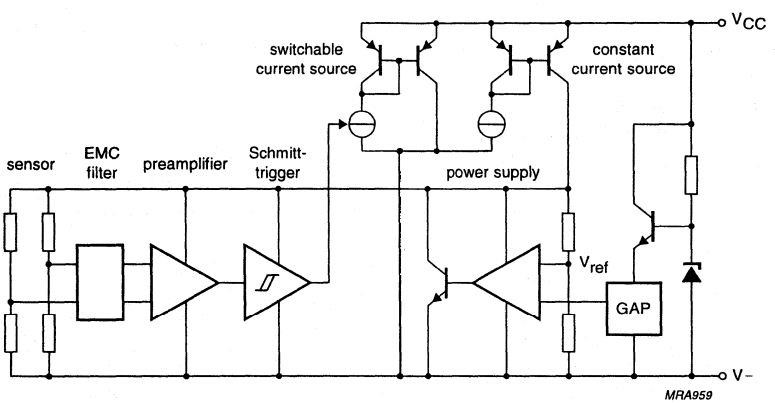


Fig.6 Sensor signal-conditioning circuit diagram.

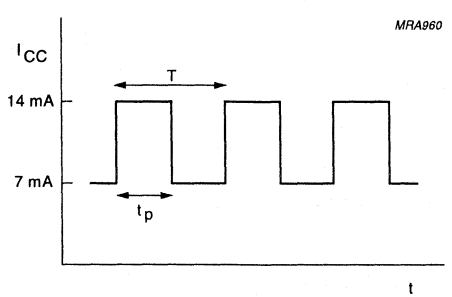


Fig.7 Current output signal.

Sensing distance

In measuring a gear wheel's rotational speed, the sensing distance is defined as the distance between the front of the magnetoresistive sensor and the tips of the teeth as measured on the central axis of the magnet (see Fig.8). The KMI10's output signal depends on the magnetic field variations at the sensor chip, generated by the rotating wheel. Beyond a certain distance 'd', I_{CC} ceases to vary between 7 and 14 mA and remains at a constant value of 7 mA. The KMI10 is optimized to deliver a stable digital output signal within a large sensing distance range and to have a sufficiently large switching hysteresis to avoid unwanted signals due to vibrations (see Section "Switching hysteresis").

The magnetoresistive effect is temperature dependent but the signal-conditioning IC largely compensates this. The residual effect on the maximum distance 'd' is shown in Fig.9.

The movement of the ferromagnetic gear wheel in the magnetic field induces eddy currents in the magnetoresistive sensor. These generate an offset voltage in the KMI10's output which linearly increases with the rotational speed. For the digital output signal to be unaffected, the maximum sensing distance is slightly shorter at higher frequencies (see Fig.9).

The magnetic field variation caused by the movement of the wheel's teeth depends on the structure of the teeth themselves. While normal and large teeth will be 'seen' very clearly by the KMI10 a smooth wheel will generate no field modulations. The variation of the maximum distance 'd' versus gear wheel module is shown in Fig.10.

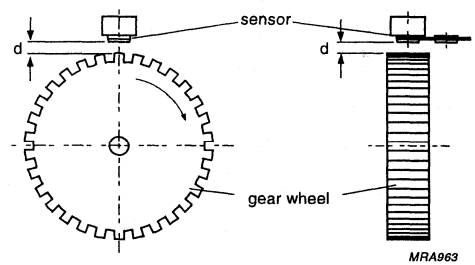
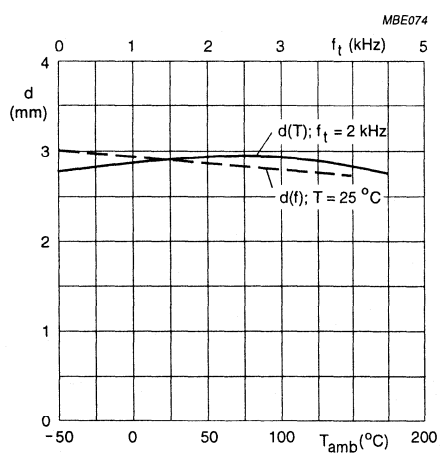


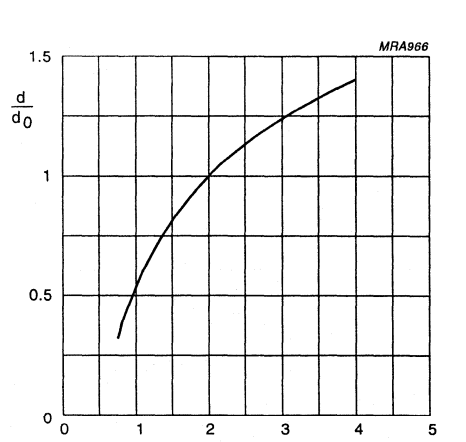
Fig.8 Sensor positioning.



The wheel's module m (in mm) = the pitch diameter of the wheel (in mm) divided by the number of the teeth: the wheel's tooth pitch (in mm) = $\pi \times m$.

V_{CC} = 12 V; m = 2 mm.

Fig.9 Maximum sensing distance of the KM10/1 as a function of temperature and tooth wheel frequency.



d_0 = distance at m = 2 mm.

Fig.10 Normalized maximum sensing distance as a function of gear wheel module.

Switching hysteresis

To prevent unexpected and/or unwanted switching behaviour of the KMI10 due to mechanical vibrations (of the sensor or the gear wheel) or circuit oscillations at low rotational speeds, the signal-conditioning circuitry contains a switching hysteresis. This has a significant influence on the measuring properties of the sensor and a trade-off has been made between hysteresis and sensing distance. A large switching hysteresis ensures insensitivity to vibrations but limits the distance 'd' to short values. On the other hand, a small switching hysteresis enables a longer distance but implies a higher sensitivity to vibrations. As the switching hysteresis is very sensitive to gear wheel structure and sensing distance, these have to be carefully defined. For the KMI10/1 the maximum distance 'd' is always >2.5 mm and is typically 2.9 mm. For the KMI10/4 the maximum distance 'd' is >2.0 mm and is typically 2.3 mm (m = 2 mm).

Figure 12 shows how the switching hysteresis was measured mechanically and gives the test results as a function of sensing distance. In terms of linear movement of a gear tooth, hysteresis can be restated as follows: for a gear wheel with m = 2 mm and a sensor with d = 1.5 mm the hysteresis corresponds to a linear gear tooth movement of 0.3 mm. If the gear wheel diameter is 100 mm this hysteresis is equivalent to 0.32° of rotational distance. For other gear wheels the mechanical effects stemming from the switching hysteresis will be correspondingly different.

Temperature effects on the switching hysteresis due to changes in sensitivity or magnetic field strength are compensated in the IC. Thus the switching behaviour of the KMI10 is consistently stable across the whole temperature range.

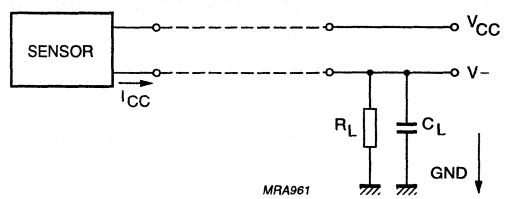


Fig.11 Test/application circuit for the KMI10.

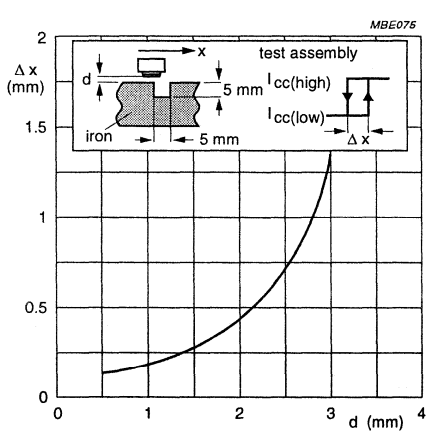


Fig.12 Mechanically measured hysteresis 'Δx' of the KMI10 as a function of sensing distance 'd' for the test assembly shown.

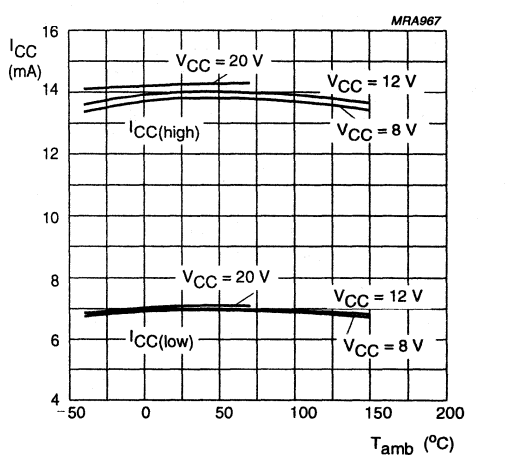
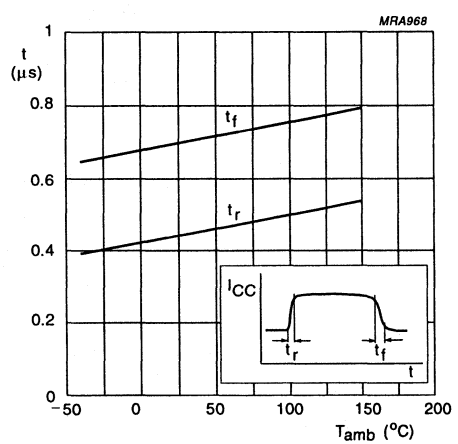


Fig.13 Output current 'I_{CC}' as a function of ambient temperature 'T_{amb}' for various supply voltages 'V_{CC}'.

Output signal

Figure 11 shows a test/application circuit for the KMI10 (an alternative circuit is shown in Fig.15). The load resistor R_L has a specified value of 115 Ω but this can be varied provided the influence on the minimum supply voltage V_{CC} is taken into account. The output voltage V– corresponding to I_{CC} = 7 or 14 mA is about 0.8 to 1.6 V. Figure 13 shows the typical influence of supply voltage, V_{CC} and ambient temperature T_{amb}, on the current levels. The output signal's switching times (10 to 90 % definition) depend on the value of C_L introduced for noise and interference reduction. Its capacitance should be adapted to specific application requirements. Figure 14 shows the rise and fall times of the output signal for C_L = 100 pF as a function of ambient temperature.



V_{CC} = 12 V; C_L = 100 pF; R_L = 115 Ω.

Fig.14 Switching times 't_r and t_f' as functions of ambient temperature 'T_{amb}'.

EMC

Figure 15 shows a recommended application circuit for automotive applications (wheel sensing f_t < 5 kHz). It provides a protection interface to meet Electromagnetic Compatibility (EMC) standards and safeguard against voltage spikes. Table 1 lists the tests which are applicable to this circuit.

Tests for electrostatic discharge (ESD) were conducted in line with *"IEC 801-2"* to demonstrate the KMI10/1's handling capabilities. The *"IEC 801-2"* test conditions were: C = 150 pF, R = 150 Ω, V = 2 kV.

Electromagnetic disturbances with fields up to 150 V/m and f = 1 GHz (ref. *"DIN 40839"*) have no influence on performance.

Table 1 EMC test results

EMC REF. DIN 40839	SYMBOL	MIN. (V)	MAX. (V)	REMARKS
Test pulse 1	V_{LD}	−100	–	t_d = 2 ms
Test pulse 2	V_{LD}	–	100	t_d = 0.2 ms
Test pulse 3a	V_{LD}	−150	–	t_d = 0.1 µs
Test pulse 3b	V_{LD}	–	100	t_d = 0.1 µs
Test pulse 4	V_{LD}	−7	–	t_d = 130 ms
Test pulse 5	V_{LD}	–	120	t_d = 400 ms

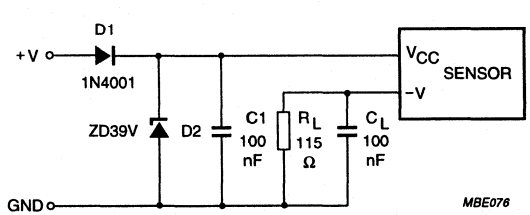


Fig.15 Test/application circuit for the KMI10.

Mounting

Figure 8 shows how the KMI10 should be mounted for measuring the rotational speed of a ferrous gear wheel. The sensor position is important since the speed sensing takes place in one direction only (along the y-axis, in both directions).

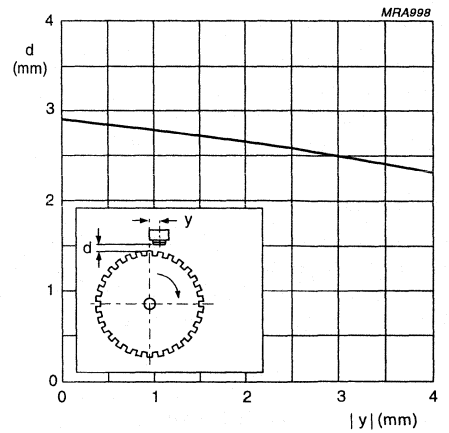
When mounting the KMI10 there are two factors shown in Figs 16 and 17 that may affect performance:

- The angle Θ between the symmetry axes of sensor and the wheel (in the y-z plane)
- The horizontal shift 'y' relative to the optimum sensor position.

These must be minimized. Recommended tolerances for optimum conditions are $|\Theta| \leq 1°$ and $|y| \leq 0.5$ mm.

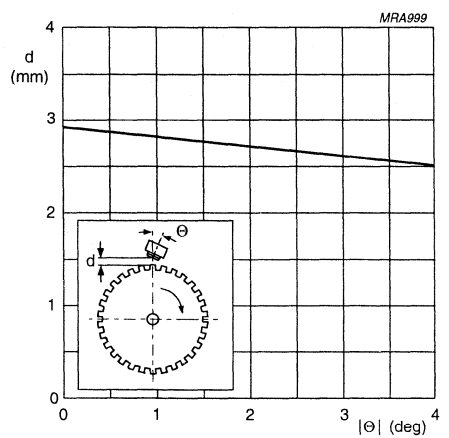
A shift in position in the x-direction is not critical to the KMI10's performance. The magnet's field component in the x-direction means that an x-shift has a non-symmetrical behaviour (see Fig.18).

A tilt in the x-z plane has a negligible influence on the optimum sensing distance for angles <4°.



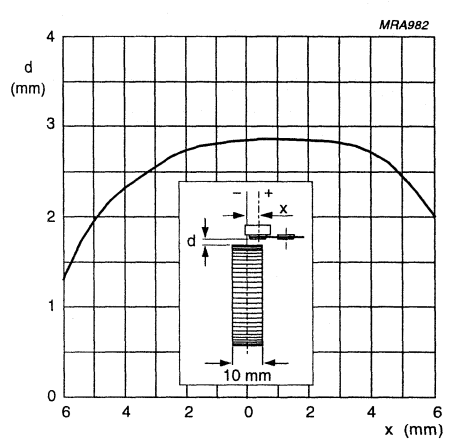
V_{CC} = 12 V; f = 2 kHz; m = 2 mm; pitch diameter = 100 mm.

Fig.16 Influence of position tolerance '|y|' on maximum sensing distance 'd'.



V_{CC} = 12 V; f = 2 kHz; m = 2 mm.

Fig.17 Influence of angular tolerance '|Θ|' on maximum sensing distance 'd'.



V_{CC} = 12 V; f = 2 kHz; m = 2 mm.

Fig.18 Influence of position tolerance 'x' on maximum sensing distance 'd'.

Encapsulation

When designing an encapsulation for the KMI10 sensors, the following should be noted:

- Both the KMI10/1 and KMI10/4 can be injection moulded. Contacting and intermittent problems, as are occasionally observed with inductive sensors, do not occur.
- The encapsulated material should be non-magnetic.
- The part of the encapsulation directly in front of the magnetoresistive sensor element should be as thin as possible to operate the KMI10/X at the longest possible distance from the object to be measured.

Applications and specifications

Although the KMI10/X was developed for wheel speed measurement, it can also be used for detecting reference marks, currents and proximity switching. Information on these applications is available on request.

The main characteristics for the KMI10/1 and KMI10/4 are given in Table 2.

Table 2 Main characteristics

SYMBOL	DESCRIPTION	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage:					
	KMI10/1	$T_{amb} \leq 60°$ C	7.5	–	20	V
	KMI10/4	$T_{amb} \leq 150°$ C	7.5	–	16	V
d	sensing distance:	m = 2 for wheel module				
	KMI10/1		0	–	2.9	mm
	KMI10/4		0	–	2.3	mm
f_t	tooth wheel frequency		0	–	25000	Hz
$I_{CC(high)}$	output current high		–	14	–	mA
$I_{CC(low)}$	output current low		–	7	–	mA
T_{amb}	operating ambient temperature		–40	–	150	°C
T_{peak}	peak temperature		–	–	190	°C

KM110BH/1 MODULE SERIES FOR MAGNETORESISTIVE SENSING OF ROTATION AND REFERENCE MARK DETECTION

The KM110BH/1 series consists of four hybrid modules for measuring rotational speed or detecting reference marks. In contrast to the KMI10 series, the KM110BH/1X modules have a digital voltage output. They can operate:

- Quasi-statically (0 Hz frequency)
- At large distance from the objects to be measured
- From –40 to +125 °C (190 °C peak)
- Without external magnets.

For new design-ins it is recommended to consider the integrated sensors KMI10/1 and KMI10/4 instead of the KM110BH/11 and KM110BH/13 modules. When very large measuring distances are required (up to 3.5. mm) the KM110 BH /12 and KM110BH/14 are the obvious choices.

Sensor module

The module is based on thick-film technology using a ceramic substrate. Two versions are available, with circuitry optimized for specific application areas:

- A quasi-static module for slow movement sensing (i.e. speed measurements down to zero)
- A module with a high-pass filter for use at large measuring distances and speeds above zero.

The position of the sensor can also be selected, as the module is supplied with the sensor either radially or tangentially arranged. Figure 20 shows both mechanical arrangements, set to measure the rotation of a toothed wheel. The data for this set-up and the type range are given in Table 3. Table 4 gives the main characteristics of the module.

The circuit and sensor position options enable the module to be used in many applications, e.g.:

- Incremental measurement can be performed easily and at low cost
- The module can be used as the first stage when customizing speed sensing equipment.

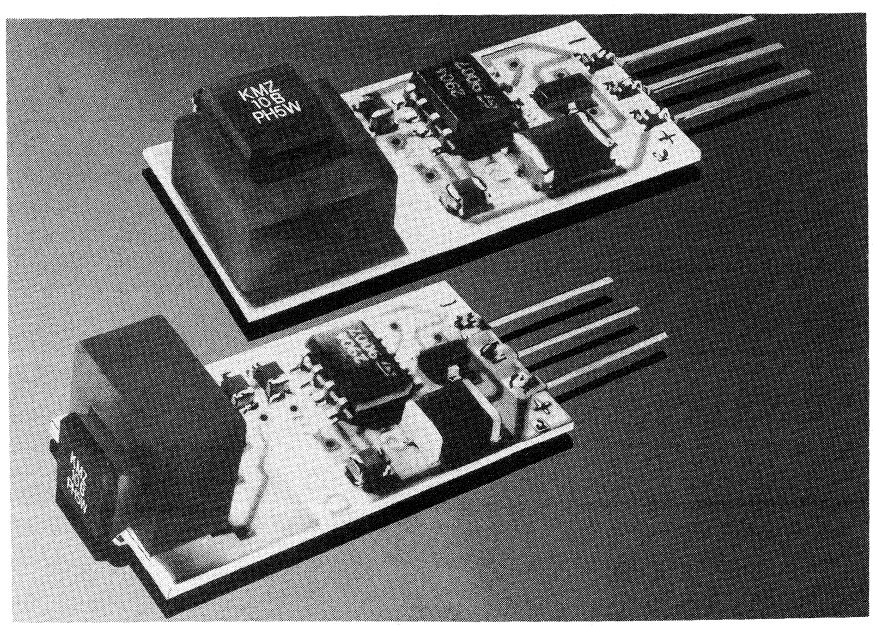


Fig.19 The KM110BH/1 series.

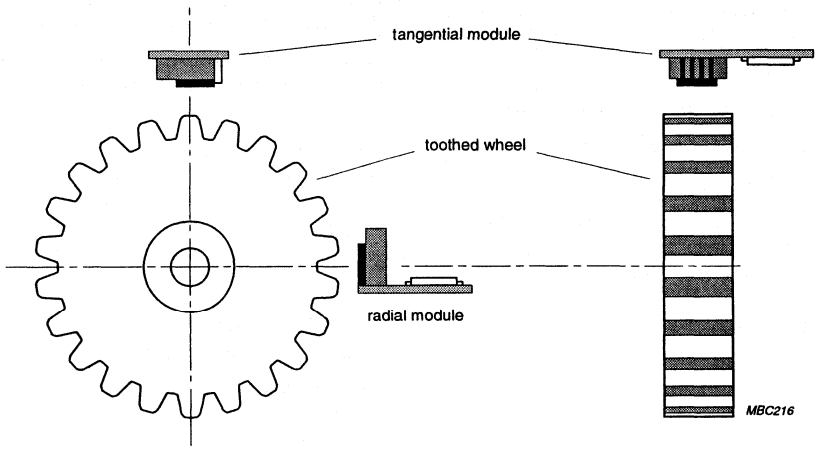


Fig.20 Radial and tangential versions of the module, arranged for rotation measurement of a toothed wheel.

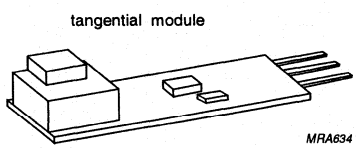


Fig.21 Tangential module (KM110BH/11 and KM110BH/12).

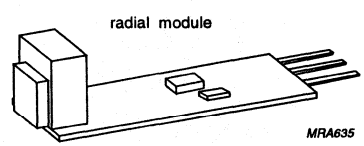


Fig.22 Radial module (KM110BH/13 and KM110BH/14).

Table 3 Philips' magnetoresistive sensor modules

SYMBOL	PARAMETER	KM110BH/11[1][3]	KM110BH/12[2][3]	KM110BH/13[1][4]	KM110BH/14[2][4]	UNIT
f_t	tooth wheel frequency	0 to 3000	1 to 3000	0 to 3000	1 to 3000	Hz
d	maximum sensing distance to tooth wheel	2.5	3.5	2.5	3.5	mm

Notes

1. Without filter.
2. With filter.
3. See Fig.21.
4. See Fig.22.

Table 4 Main characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	note 1	4	5	10	V
$V_{O(rel)}$	relative digital output signal		0	–	5	V
T_{oper}	operating temperature		–40	–	+125[2]	°C
d	measuring distance	without filter; note 3	0	–	2.5	mm
		with filter; note 3	0	–	3.5	mm
f_t	tooth wheel frequency	without filter	0	–	3000	Hz
		with filter	1	–	3000	Hz

Notes

1. Maximum ripple for filter version is 50 mV.
2. During 500 hours maximum 150 °C.
3. Gear wheel dimensions: diameter = 104 mm; width = 10 mm; 50 teeth; m = 2.05; material: 9SMnPb28k.

Module circuit

Figure 23 shows the sensor module circuit. The circuit amplifies the sensor signal (IC1) and then digitizes it using a comparator (IC2) to provide the digital output signal (V_O). For good switching performance (especially at low frequencies) and to suppress small noise signals, the comparator has a built-in switching hysteresis. The hysteresis has a defined temperature drift to compensate the temperature dependent sensor signal.

In the module for quasi-static operation, the bridge connectors BR1 and BR2 are open. In the version that uses the filter, these connectors are closed.

The recommended supply is 5 V, but values in the range of ≈4 to ≈10 V are also possible. If the filter versions of the modules are used (KM110BH/12 or KM110BH/14), the ripple on the supply voltage should not exceed 50 mV; this prevents unwanted switching of the comparator. The output can withstand short-circuiting to the two supply levels. Normally, the external load should be ≥100 kΩ, but with an additional external pull-up resistor, a lower value may be used. The values of internal resistors R18 and R19 are 10 kΩ and 100 Ω respectively. Since a protection diode is not provided on the substrate, care should be taken to ensure the correct supply polarity.

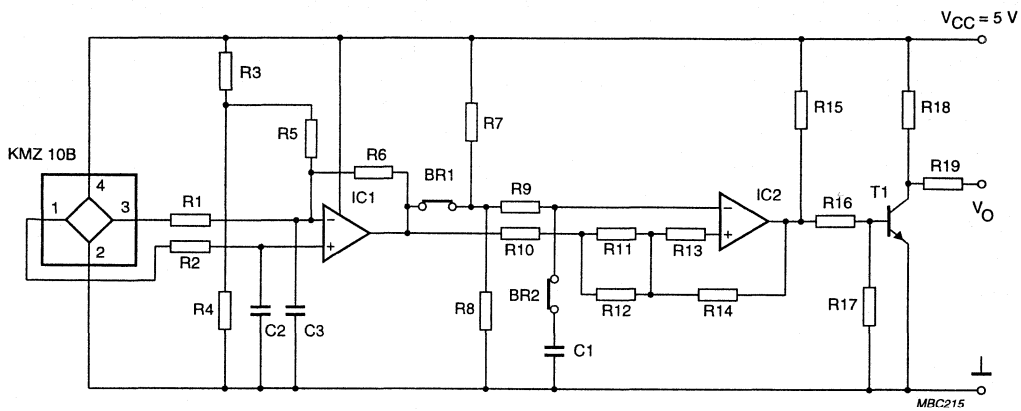


Fig.23 Sensor module circuit.

Mounting

The module's magnetoresistive sensor operates as a magnetic Wheatstone bridge, measuring non-symmetrical magnetic conditions such as metal teeth or pins in front of the sensor. Figure 20 shows how the module should be mounted for measuring the rotation of a ferrous pulse wheel. The sensor position is important, since sensing is not symmetrical around the module's symmetrical axis.

When mounting the module, there are two factors, shown in Fig.24, that may affect the performance of the module:

- The angle 'γ' between the symmetry axes of the sensor module and the wheel
- The vertical shift 'y' relative to the optimum sensor position.

These two factors must be minimized, especially when using the modules without filter (types KM110BH/11 and KM110BH/13). Recommended tolerances for normal conditions are: $\gamma < 1°$, $y < 0.5$ mm.

The sensor's symmetry axis corresponds to that of the module's magnet (the crystal is not mounted in the centre of the sensor encapsulation).

Module encapsulation

When designing a module encapsulation, the following considerations should be borne in mind:

- The encapsulation material should be non-magnetic
- To operate the module at large distance from the object to be measured, the part of the encapsulation directly in front of the sensor element should be as thin as possible
- No components should be located near the sides of the module; 0.8 mm of substrate edge is available to allow the module to be securely mounted into grooves (see Figs 25 and 26)

When potting hybrid modules, it is strongly recommended to do this in two steps.

During the first step the module should be covered by an elastic layer This absorbs mechanical stress caused by varying expansion coefficients of the different materials used, as well as thermally generated stress. The following materials are suggested:

Dow Corning, silicone coating, type HIPEC Q1-9224

Dexter-Hysol, semiconductor encapsulant, type 4323.

During the second step a potting material has to be used, that supplies the necessary mechanical stability needed for successful mounting; for example:

Grace-Emerson, Stycast 2651-40.

Temperature range

The front of the module (sensor and magnet) can withstand temperatures up to 190 °C provided the duration is limited to a few hours over the module's lifetime. The integrated circuit, however, should not operate in environments above 125 °C.

Performance

The maximum measuring distance depends upon the structure of the wheel and, for modules without filter, also on the accuracy of mounting. If the wheel structures differ greatly from the example shown, the range has to be found by measurement.

With high rotational speeds, eddy current signals are generated that reduce the performance of the modules without filter.

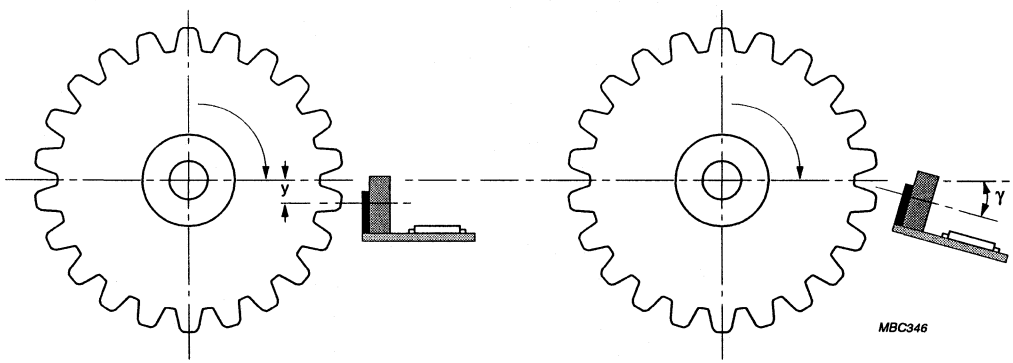
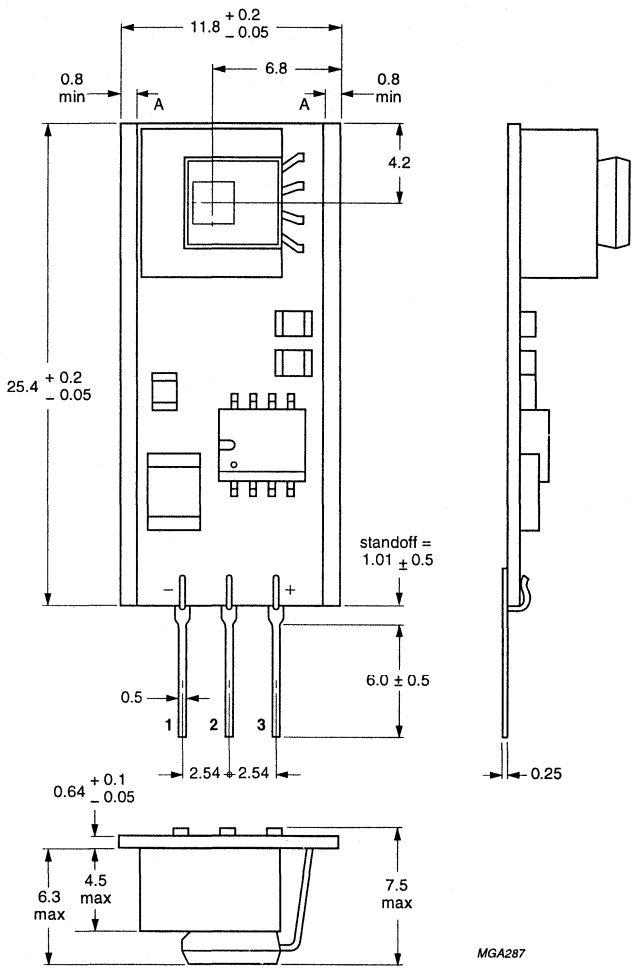
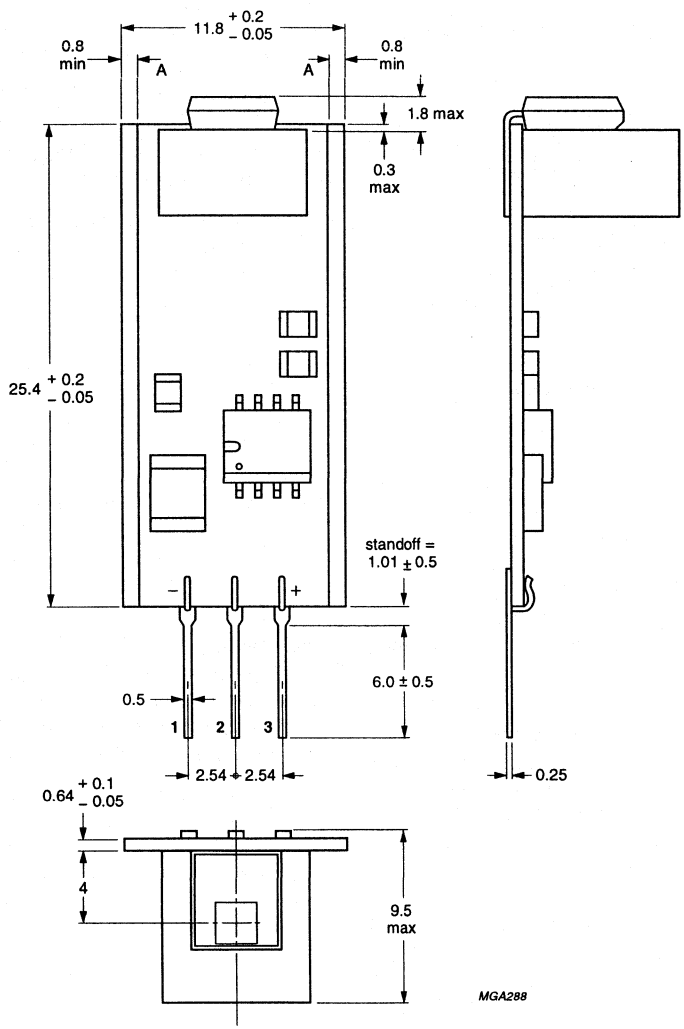


Fig.24 Sensor position tolerances.



Pin 1: ground
Pin 2: V_O
Pin 3: V_{CC}
Dimensions in mm.

Fig.25 Module dimensions: KM110BH/11 and KM110BH/12.



Pin 1: ground
Pin 2: V_O
Pin 3: V_{CC}
Dimensions in mm.

Fig.26 Module dimensions: KM110BH/13 and KM110BH/14.

THE KM110BH/31 MODULE FOR MAGNETORESISTIVE SENSING OF ROTATIONAL SPEED AND DIRECTION

Based around the KMZ10B magnetoresistive sensor, the KM110BH/3 series extends the successful KMI10 and KM110BH/1 families of sensor modules for contactless rotational speed sensing. In addition, the KM110BH/3 series uses a circuit which enables it to indicate **rotational direction**, as well as accurately measure rotational speeds. The KM110BH/3X sensors can operate:

From 2 Hz (10 Hz for the KM110BH/32) to 20 kHz at a large distance from the object to be measured.

From –40 to +125 °C (150 °C peak).

With a wide range of toothed wheels.

The sensors are available in two versions. The KM110BH/31 has a digital **voltage** output and the KM110BH/32 has a digital **current** output.

Direction indication with magnetoresistive sensors

Until recently, two magnetic sensors were needed to indicate the rotational direction of a toothed wheel. The technique required placing the sensors around the wheel with a specific distance between one another to ensure that the two sensor output signals were optimally phase-shifted by 90°. The distance, of course, varied with the module (m)[1] of the specific toothed wheel used. However, with filters to suppress offset signals, it was possible to vary the distance between the sensors and thus use different wheels.

The single-sensor technique used in the KM110BH/3X sensor is based on separate signal-processing for the sensor's two half-bridge signals. As the bridge geometry is fixed within the sensor chip, there is an optimum wheel module (of e.g. m = 0.8 mm for the KM110BH/31). Nevertheless it operates successfully using toothed wheels with a wide range of pitches. Although the stability of the two half bridges is reduced with non-optimal pitches, filtering compensates for this and allows the KM110BH/3X sensors to operate at long distances from the wheel. Without filtering, the circuit could indicate zero speed, and be capable of incremental counting, but the operating range would be limited.

Mounting

The sensor operates like a magnetic Wheatstone bridge, measuring non-symmetric magnetic conditions, as when teeth or pins move in front of the sensor. The KM110BH/31 can sense this movement in two possible directions (shown in Fig.27). The mounting position, therefore, is very important for accurate measurements. Two types of mounting error affect the KM110BH/31's performance:

- Allowing an angle between the sensor's symmetry axis (the centre line in Fig.27), and that of the toothed wheel
- Vertical shifting of the sensor away from the optimum position shown in Fig.27.

The sensor's symmetry axis corresponds with that of the built-in magnet: the chip is not mounted in the centre of the sensor encapsulation.

Circuit

Figure 28 shows a block diagram of the KM110BH/31 circuit with separate signal processing for each half of the bridge. The digital output signals (V_{O1} and V_{O2}) are connected directly to the output pins. The circuit design enables evaluation of the output signals by a microcontroller. Figures 30 and 31 show that both output signals vary with rotational direction. If desired, the two output signals may be connected to a flip-flop for a direct indication of rotation (see Fig.29).

Since a protection diode is not included in the KM110BH/31, care should be taken to ensure the correct supply polarity (V_{CC}). The recommended supply is 5 V, but operation is possible with supplies from 4 to 10 V. The supply ripple should not exceed 40 mV to prevent unwanted switching of the comparator.

Both output pins can withstand short-circuiting to the supply lead (V_{CC}). Normally the external load should be ≥100 kΩ, but with an additional external pull-up resistor, this value can be reduced. The output resistance is 100 Ω when the signal is LOW and 10 kΩ when HIGH.

(1) $m = \frac{\text{pitch diameter}}{\text{number of teeth}}$; pitch $= m \times \pi$

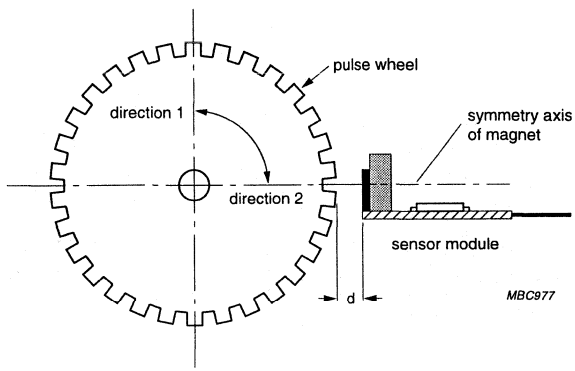


Fig.27 Optimum operating position.

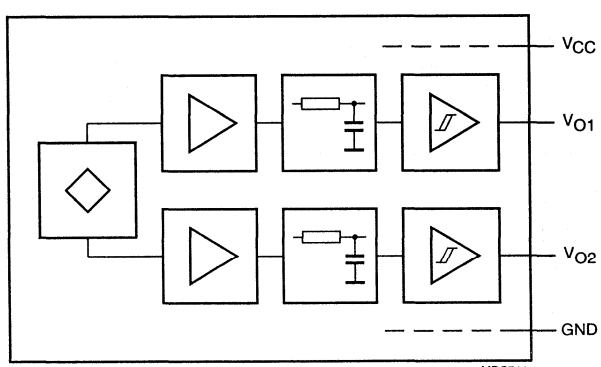


Fig.28 Block diagram of module circuit.

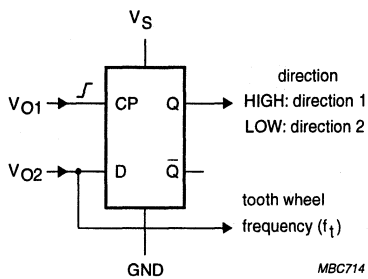


Fig.29 Circuit for rotation indication.

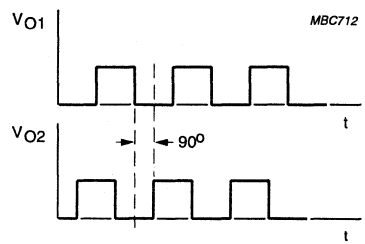


Fig.30 Output signals (direction 1).

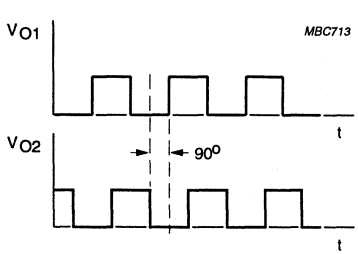


Fig.31 Output signals (direction 2).

Encapsulation

When designing a module encapsulation, the following considerations should be borne in mind:

- The encapsulation material should be non-magnetic
- To operate the module at large distance from the object to be measured, the part of the encapsulation directly in front of the sensor element should be as thin as possible
- No components should be located near the sides of the module; 0.8 mm of substrate edge is available to allow the module to be securely mounted into grooves (see Figs 32 and 33).

When potting hybrid modules, it is strongly recommended to do this in two steps.

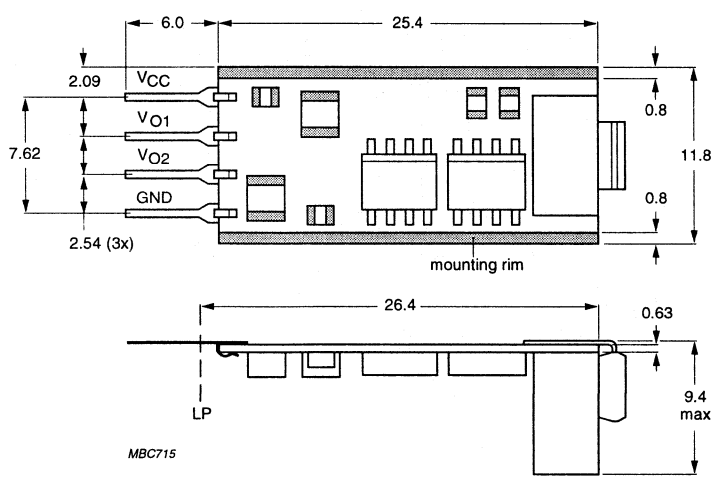
During the first step the module should be covered by an elastic layer. This absorbs mechanical stress caused by varying expansion coefficients of the different materials used, as well as thermally generated stress. The following materials are suggested:

Dow Corning, silicone coating, type HIPEC Q1-9224

Dexter-Hysol, semiconductor encapsulant, type 4323.

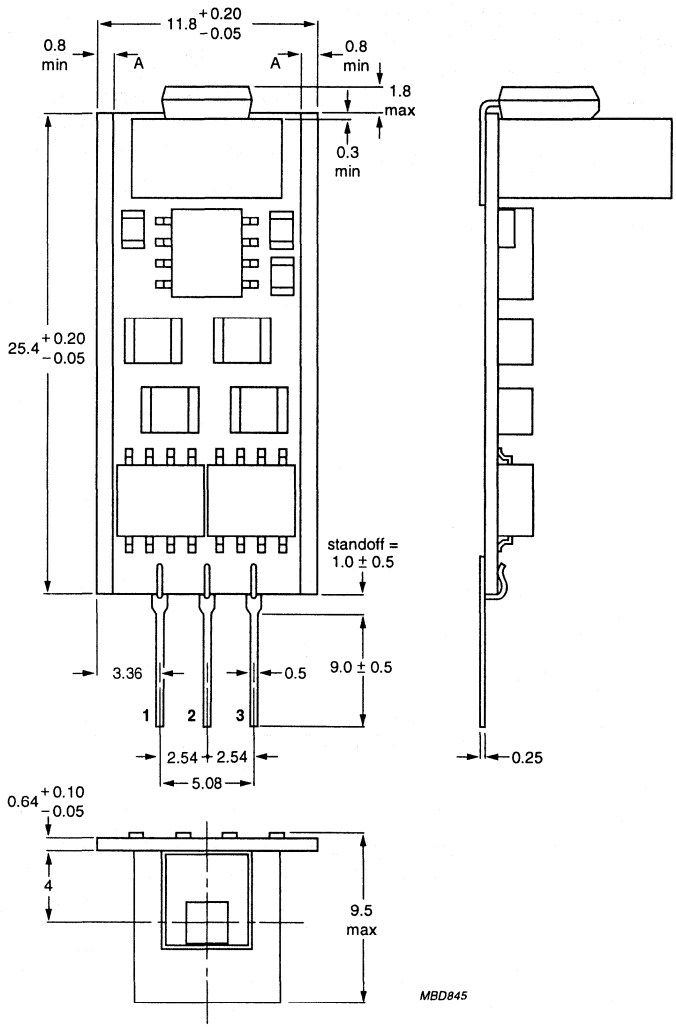
During the second step a potting material has to be used that supplies the necessary mechanical stability needed for successful mounting; for example:

Grace-Emerson, Stycast 2651-40.



Dimensions in mm.

Fig.32 Module dimensions: KM110BH/31.



Pin 1: ground
Pin 2: V_{CC1}
Pin 3: V_{CC2}
Dimensions in mm.

Fig.33 Module dimensions: KM110BH/32.

Temperature range

The front of the KM110BH/3X sensors (i.e. sensor and magnet) can withstand temperatures up to 150 °C provided the duration is limited to a few hours over the module's lifetime. The integrated circuits, however, should not operate in environments above 125 °C.

Performance

The distance range depends on the structure of the toothed wheel and also on the accuracy of mounting. The latter may influence the output signal form and cause an effective phase shift if the measuring distance is very small.

If different wheel modules (m) are used form the range given in Fig.34, the measuring distance range has to be found by measurement.

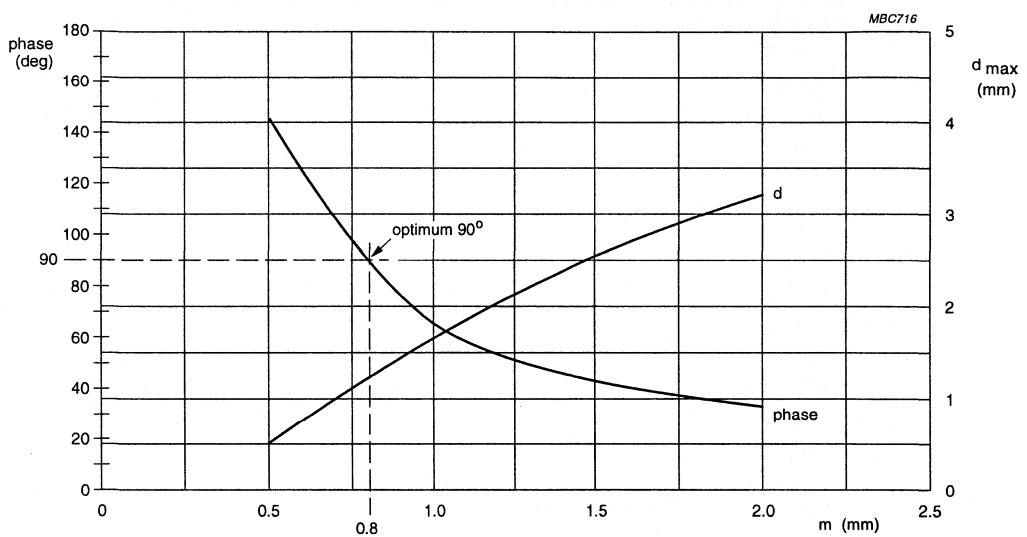


Fig.34 Effect of different toothed wheel structures on the KM110BH/31.

Table 5 Characteristics of the KM110BH/31 and KM110BH/32

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage (note 1):				
	KM110BH/31	4	5	10	V
	KM110BH/32	7.5	–	16	V
V_{O1}; V_{O2}	digital output signals (note 2):				
	KM110BH/31 (low)	–	–	0.4	V
	KM110BH/31 (high)	4.3	–	–	V
I_{O1}; I_{O2}	output signals:				
	KM110BH/32 (low)	–	7	–	mA
	KM110BH/32 (high)	–	14	–	mA
T_{oper}	operating temperature:				
	KM110BH/31	–40	–	+125	°C
	KM110BH/32	–40	–	+125	°C
T_{peak}	peak temperature:				
	KM110BH/31	–	150	–	°C
	KM110BH/32	–	150	–	°C
d	measuring distance (see Fig.34):				
	KM110BH/31	0	–	3	mm
	KM110BH/32	0	–	3	mm
f_t	tooth wheel frequency:				
	KM110BH/31	2	–	20000	Hz
	KM110BH/32	10	–	20000	Hz
R_L	external load resistor:				
	KM110BH/31	100	–	–	kΩ
	KM110BH/32	–	120	–	Ω

Notes

1. Maximum ripple is 40 mV.
2. The peak voltage is relative to V_{CC}.

Integrated rotational speed sensor KMI10/1

FEATURES

- Digital current output signal
- Zero speed capability
- Wide air gap
- Wide temperature range
- Insensitive to vibration
- EMC resistant.

DESCRIPTION

The KMI10/1 sensor detects rotational speed of ferrous gear wheels and reference marks (note 1). The sensor consists of a magnetoresistive sensor element, a signal conditioning IC in bipolar technology and a magnetized ferrite magnet. The frequency of the digital current output signal is proportional to the rotational speed of a gear wheel.

Note 1

The sensor contains a customized IC. Passenger car Anti Blocking Systems (ABS) applications restricted, other applications free.

Caution

Do not press two or more products together against their magnetic forces.

PINNING

PIN	DESCRIPTION
1	V_{CC}
2	V–

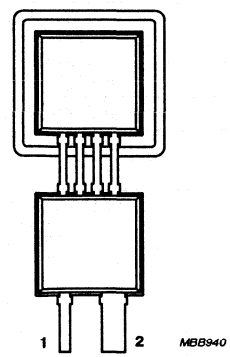


Fig.1 Simplified outline.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage	–	12	–	V
$I_{CC\ low}$	current output signal low	–	7	–	mA
$I_{CC\ high}$	current output signal high	–	14	–	mA
d	sensing distance	0 to 2.5	0 to 2.9	–	mm
f	operating frequency	0	–	25 000	Hz
T_{amb}	ambient operating temperature	–40	–	150	°C

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage	T_{amb} = –40 to 60 °C T_{amb} = –40 to 150 °C	7.5 7.5	20 16	V V
T_{stg}	storage temperature		–40	150	°C
T_{amb}	ambient operating temperature	note 1	–40	150	°C
T_{peak}	peak temperature	sensor front only, 3 x 1 h over lifetime	–	190	°C
T_{sld}	soldering temperature	t ≤ 10 s	–	260	°C
	output short-circuit duration to GND		continuous, (note 2)		

Notes

1. The ambient operating temperature of the module can be extended up to +175 °C for a limited time. This will be monitored by environmental quality tests up to 100 h of operation at +175 °C under characteristic conditions.
2. With R_L = 115 Ω the device is continuously protected against wrong polarity of DC supply voltage (V_{CC}) to GND (see Fig.7).

CHARACTERISTICS

T_{amb} = 25 °C; V_{CC} = 12 V; d = 2.1 mm; f = 2 kHz; test circuit: see Fig.7; R_L = 115 Ω; sensor position: see Fig.9; gear wheel: module 2 mm; material 1.0715; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CC\ low}$	current output signal low	see Figs 6 and 16	5.6	7	8.4	mA
$I_{CC\ high}$	current output signal high	see Figs 6 and 16	11.2	14	16.8	mA
t_r	output signal rise time	see Fig.17; C_L = 100 pF; 10% to 90% value	–	0.5	–	µs
t_f	output signal fall time	see Fig.17; C_L = 100 pF; 10% to 90% value	–	0.7	–	µs
t_D	switching delay time	between stimulation pulse (generated by a coil) and output signal	–	1	–	µs
f	operating frequency	for both rotation directions	0	–	25 000	Hz
d	sensing distance	see Fig.9 and note 1	0 to 2.5	0 to 2.9	–	mm
t_1/T	duty cycle	see Fig.6	30	50	70	%

Note

1. High rotational speeds of wheels reduce the sensing distance due to eddy current effects (see Fig.14).

FUNCTIONAL DESCRIPTION

The KMI10/1 sensor is sensitive to the motion of ferrous gear wheels or reference marks. The functional principle is shown in Fig.3. Due to the effect of flux bending, the different directions of magnetic field lines in the magnetoresistive sensor element will cause an electrical signal. Because of the chosen sensor orientation and the direction of ferrite magnetization, the KMI10/1 is sensitive to movement in 'y' direction in front of the sensor only (see Fig.2). The magnetoresistive sensor element signal is amplified, temperature compensated and given to a Schmitt trigger in the conditioning IC (Figs 4 and 5). The digital output signal level (Fig.6) is within the measuring range independent of the sensing distance (Fig.8). A current (2-wire) output signal enables safe sensor signal transport to the detecting circuit (Fig.7). The IC housing is deliberately separated from the sensor element housing to optimize the sensor behaviour at high temperatures.

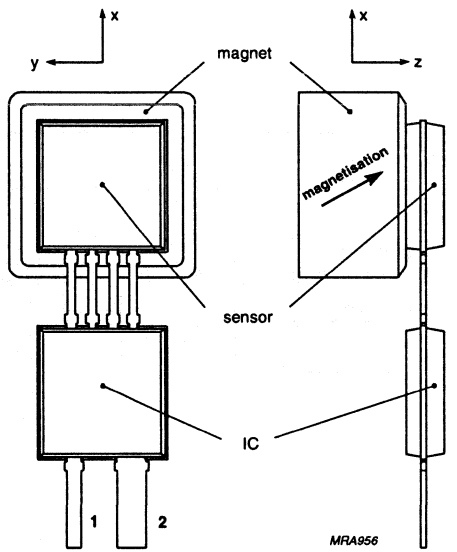


Fig.2 Component detail of the KMI10/1.

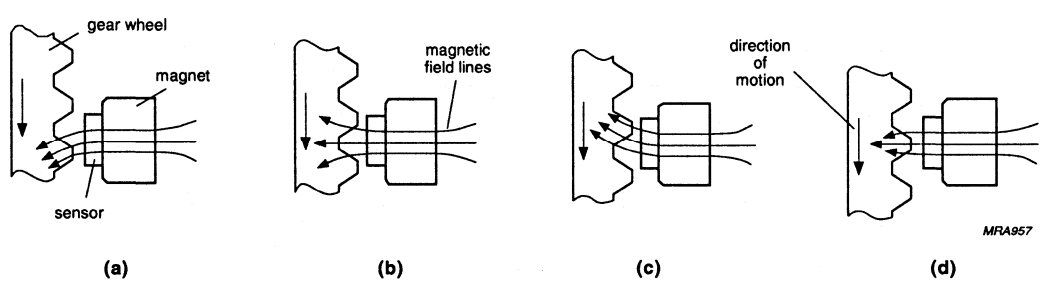


Fig.3 Functional principle of KMI10/1.

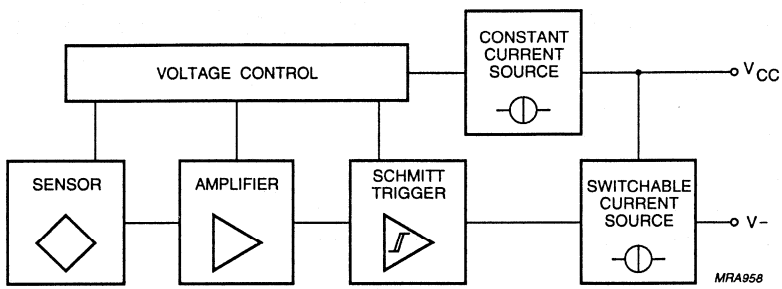


Fig.4 Block diagram 1.

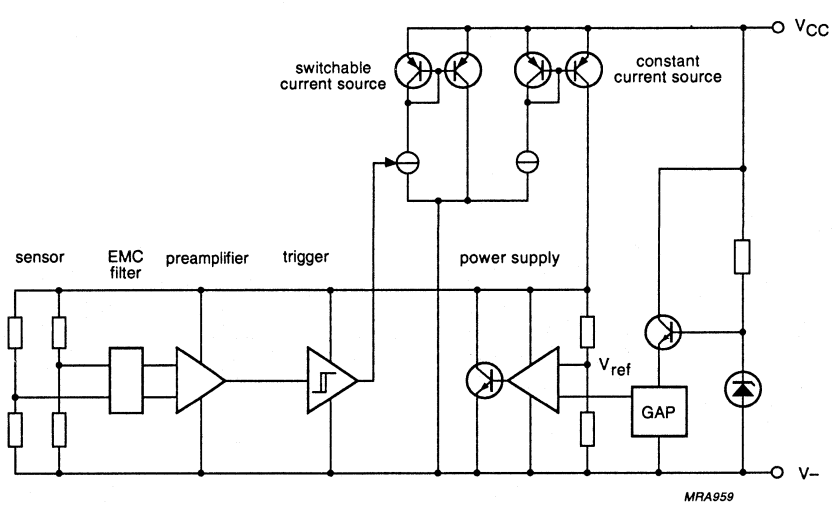


Fig.5 Block diagram 2.

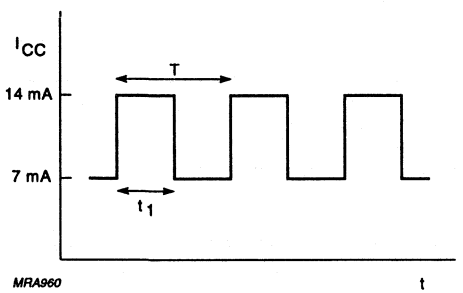


Fig.6 Output signal of KMI10/1.

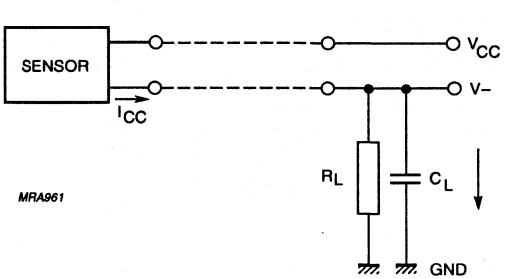
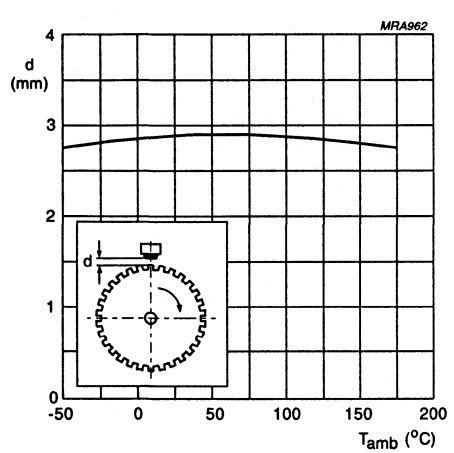


Fig.7 Test and application circuit.



V_{CC} = 12 V; f = 2 kHz; module = 2 mm.

Fig.8 Typical sensing distance.

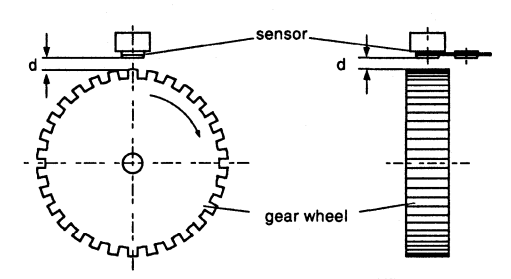


Fig.9 Sensor position.

Mounting conditions

The recommended sensor position in front of a gear wheel is shown in Fig.9. The distance 'd' is measured between the sensor front and the tip of a gear wheel tooth. The KMI10/1 senses ferrous indicators like gear wheels in ±'y' direction (Fig.2) only (no rotational symmetry of the sensor). The effect of incorrect mounting positions on sensing distance is shown in Figs 11, 12 and 13. The symmetrical reference axis of the sensor corresponds to the axis of the ferrite magnet.

Environmental conditions

Due to eddy current effects the sensing distance depends on the tooth frequency (Fig.14). The influence of gear wheel module on the sensing distance is shown in Fig.15.

Gear Wheel Dimensions

SYMBOL	DESCRIPTION	UNIT
German DIN		
z	number of teeth	
d	diameter	mm
m	module m = d/z	mm
p	pitch p = π x m	mm
ASA (note 1)		
PD	pitch diameter (d in inch)	inch
DP	diametric pitch DP = z/PD	$inch^{-1}$
CP	circular pitch CP = π/DP	inch

Note

1. For conversion from ASA to DIN: m = 25.4 mm/DP; p = 25.4 mm x CP.

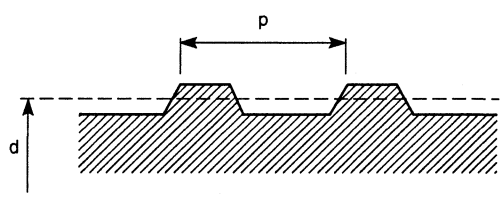
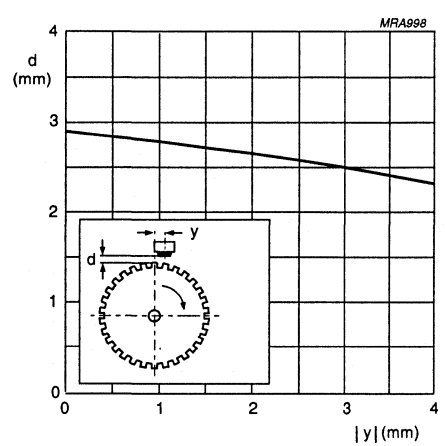
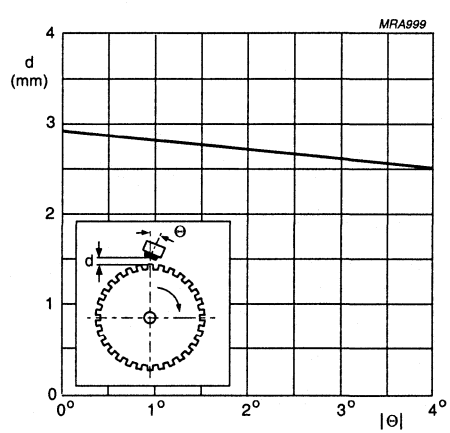


Fig.10 Gear wheel dimensions.



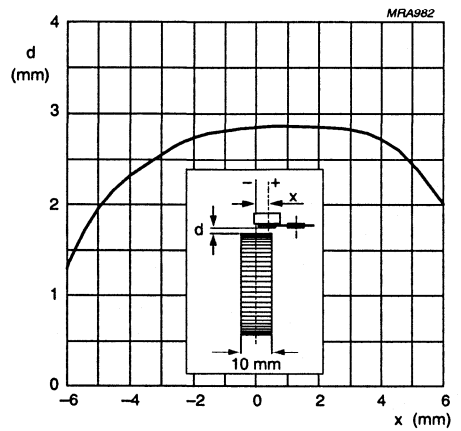
V_{CC} = 12 V; f = 2 kHz; module = 2 mm; pitch diameter = 100 mm.

Fig.11 Position tolerance 'y'.



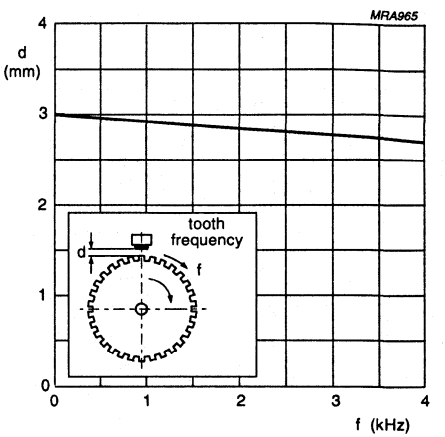
V_{CC} = 12 V; f = 2 kHz; module = 2 mm.

Fig.12 Position tolerance θ.



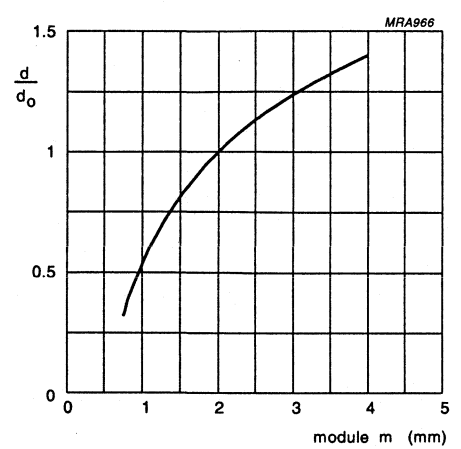
V_{CC} = 12 V; f = 2 kHz; module = 2 mm.

Fig.13 Position tolerance x.



V_{CC} = 12 V; module = 2 mm.

Fig.14 Tooth frequency dependence.



d_o = measuring distance for a gear wheel with module m = 2 mm.

Fig.15 Normalized maximum sensing distance as a function of gear wheel module.

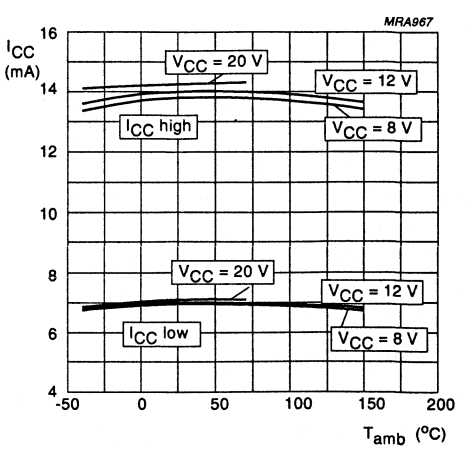
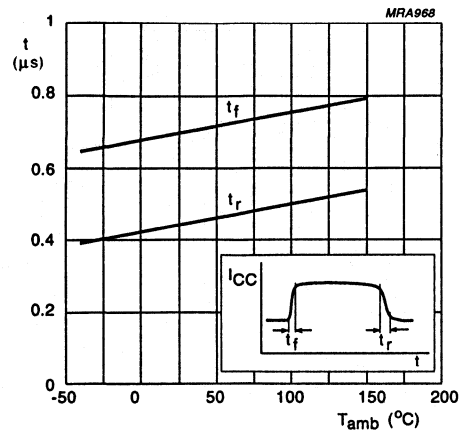


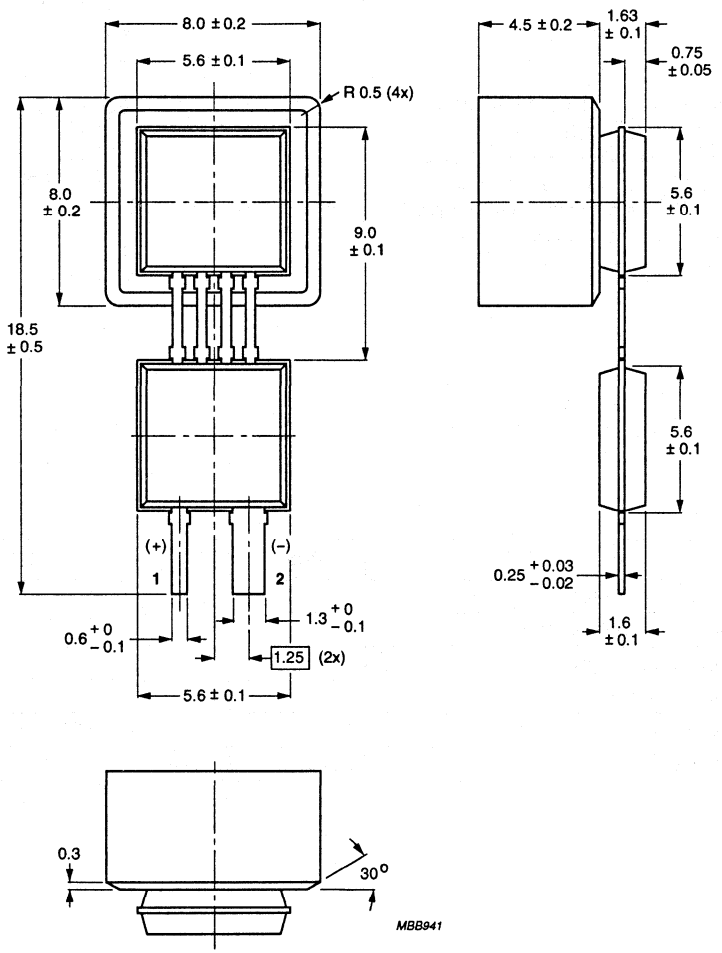
Fig.16 Output current levels.



V_{CC} = 12 V; C_L = 100 pF; R_L = 115 Ω.

Fig.17 Switching time.

PACKAGE OUTLINE



Dimensions in mm.

Fig.18 KMI10/1.

Rotational speed sensor KMI10/4

FEATURES

- Digital current output signal
- Zero speed capability
- Wide air gap
- Wide temperature range
- Vibration insensitive
- EMC resistant.

DESCRIPTION

The KMI10/4 sensor detects rotational speed of ferrous gear wheels and reference marks(1). The sensor comprises a magnetoresistive sensor element, a signal conditioning circuit in bipolar technology and a ferrite magnet. The frequency of the digital current output signal is proportional to the rotational speed of a gear wheel.

(1) The sensor contains a customized integrated circuit. Automotive Anti Blocking Systems (ABS) applications are restricted, other applications are free.

PINNING

PIN	DESCRIPTION
1	V_{CC}
2	V–

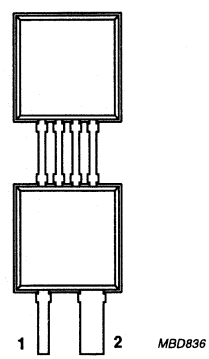


Fig.1 Simplified outline.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage	–	12	–	V
T_{amb}	operating ambient temperature	–40	–	+150	°C
$I_{CC(low)}$	output current low	–	7	–	mA
$I_{CC(high)}$	output current high	–	14	–	mA
$f_{t(oper)}$	operating tooth frequency	0	–	25000	Hz
d	sensing distance	0 to 2.0	0 to 2.3	–	mm

FUNCTIONAL DESCRIPTION

The KMI10/4 sensor is sensitive to the motion of ferrous gear wheels or reference marks. The functional principle is shown in Fig.3. Due to the effect of flux bending, the different directions of magnetic field lines in the magnetoresistive sensor element will cause an electrical signal. Because of the chosen sensor orientation and the direction of ferrite magnetization, the KMI10/4 is sensitive to movement in 'y' direction in front of the sensor only (see Fig.2). The magnetoresistive sensor element signal is amplified, temperature compensated and passed to a Schmitt-trigger in the conditioning IC (see Figs 4 and 5). The digital output signal (see Fig.6) is at a fixed level independent of the sensing distance. A (2-wire) output current ensures safe sensor signal transport to the detecting circuit (see Fig.7). The IC housing is deliberately separated from the sensor element housing to optimize the sensor behaviour at high temperatures.

The strength of the magnetic field caused by the Ferroxdure 100 magnet in the different sensor directions, measured at the centre of the magnetoresistive bridge, is typically: H_x = 7 kA/m (auxiliary field) and H_z = 17 kA/m (perpendicular to the sensor surface). H_y is zero due to the trimming process.

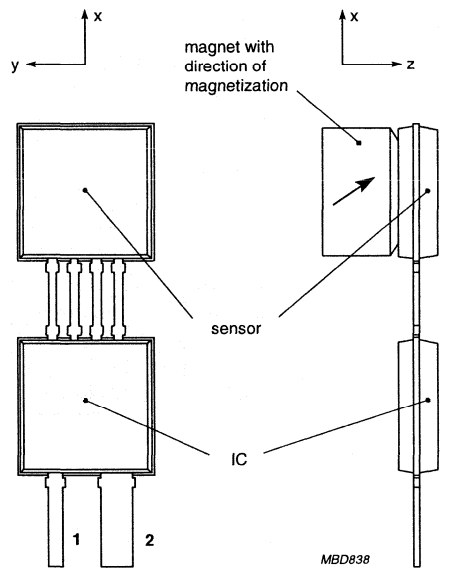


Fig.2 Component detail of the KMI10/4.

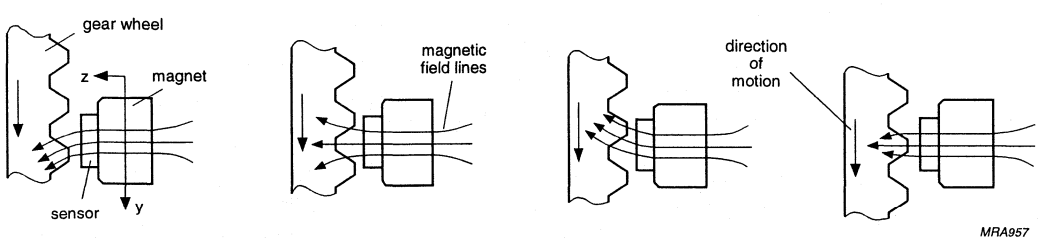


Fig.3 Functional principle.

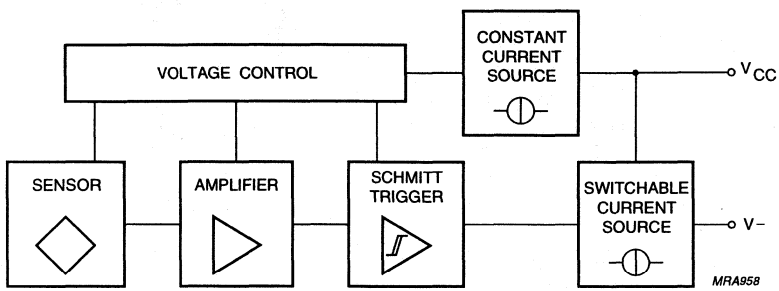


Fig.4 Block diagram.

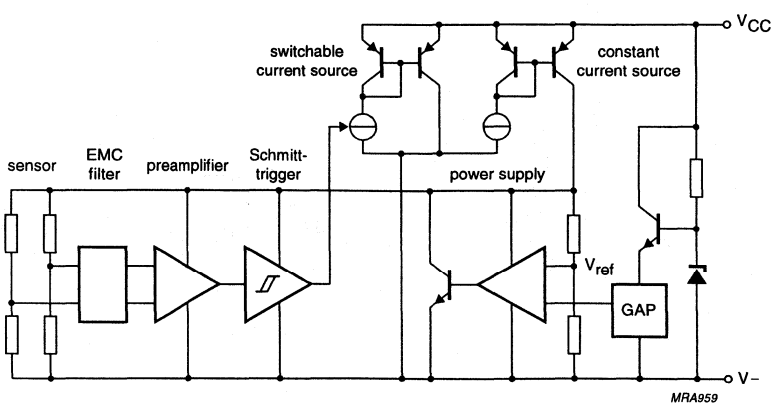


Fig.5 Simplified circuit diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage	T_{amb} = −40 to +60 °C	7.5	20	V
		T_{amb} = −40 to +150 °C	7.5	16	V
T_{stg}	storage temperature		−40	+150	°C
T_{amb}	operating ambient temperature		−40	+150(1)	°C
T_{peak}	peak temperature	sensor front only, 3 × 1 h over lifetime	–	190	°C
T_{sld}	soldering temperature	t ≤ 10 s	–	260	°C
	output short-circuit duration to GND		continuous, note 2		

Notes

1. The ambient operating temperature range of the module can be extended up to +175 °C for a limited time.
2. With R_L = 115 Ω, the device is continuously protected against wrong polarity of DC supply voltage V_{CC} to GND (see Fig.7).

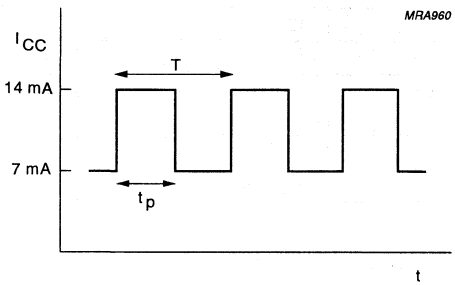
CHARACTERISTICS

T_{amb} = 25 °C; V_{CC} = 12 V; d = 1.5 mm; f = 2 kHz; test circuit: see Fig.7; R_L = 115 W; test arrangement: see Fig.15; gear wheel: module 2 mm; material 1.0715; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CC(low)}$	output current low	see Figs 6 and 8	5.6	7	8.4	mA
$I_{CC(high)}$	output current high	see Figs 6 and 8	11.2	14	16.8	mA
t_r	output current rise time	C_L = 100 pF; see Fig.9; 10% to 90% value	–	0.5	–	µs
t_f	output current fall time	C_L = 100 pF; see Fig.9; 10% to 90% value	–	0.7	–	µs
t_d	switching delay time	between stimulation pulse (generated by a coil) and output signal	–	1	–	µs
$f_{t(oper)}$	operating tooth frequency	for both rotation directions	0	–	25000	Hz
δ	duty cycle	see Fig.6	20	50	80	%
d	sensing distance	see Fig.15; note 1	0 to 2.0	0 to 2.3	–	mm

Note

1. High rotational speeds of wheels reduce the sensing distance due to eddy current effects (see Fig.17).



$$\delta = \frac{t_p}{T} \times 100\%$$

Fig.6 Output signal as a function of time.

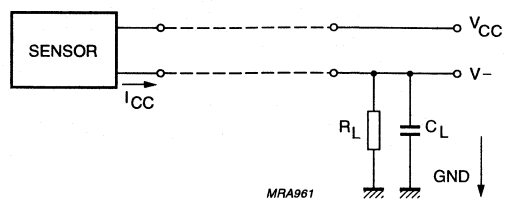


Fig.7 Test and application circuit.

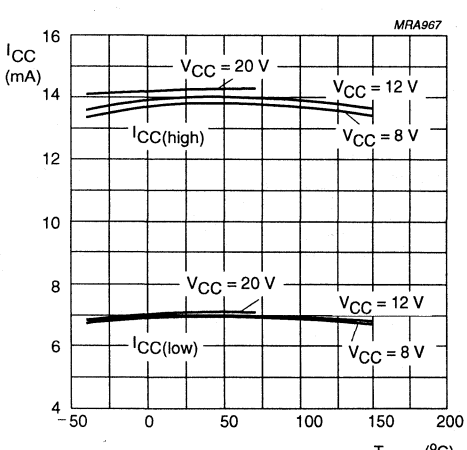


Fig.8 Output current levels as functions of ambient temperature.

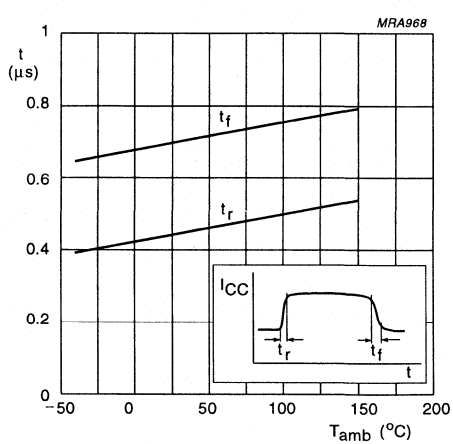


Fig.9 Output current switching times as functions of ambient temperature.

APPLICATION INFORMATION

Mounting conditions

The recommended sensor position in front of a gear wheel is shown in Fig.15. Distance 'd' is measured between the sensor front and the tip of a gear wheel tooth. The KMI10/4 senses ferrous indicators like gear wheels in ± y-direction only (no rotational symmetry of the sensor); see Fig.2. The effect of incorrect mounting positions on sensing distance is shown in Figs 11, 12 and 13. The symmetrical reference axis of the sensor corresponds to the axis of the ferrite magnet.

Environmental conditions

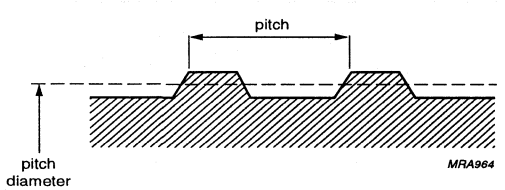
Due to eddy current effects the sensing distance depends on the tooth frequency (see Fig.17). The influence of gear wheel module on the sensing distance is shown in Fig.16.

Gear wheel dimensions

SYMBOL	DESCRIPTION	UNIT
German DIN		
z	number of teeth	
d	diameter	mm
m	module m = d/z	mm
p	pitch = $\pi \times m$	mm
ASA(1)		
PD	pitch diameter (d in inch)	inch
DP	diameter pitch DP = z/PD	$inch^{-1}$
CP	circular pitch CP = π/DP	inch

Note

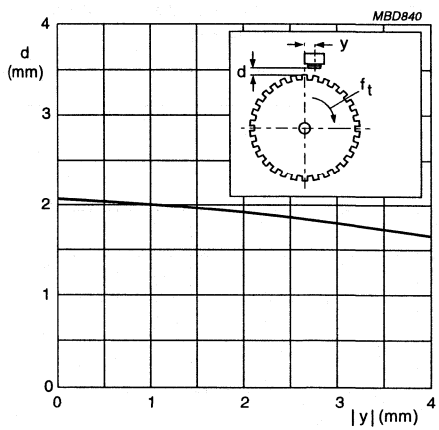
1. For conversion from ASA to DIN: m = 25.4 mm/DP; p = 25.4 mm × CP.



$$\text{module} = \frac{\text{pitch diameter}}{\text{number of teeth}}$$

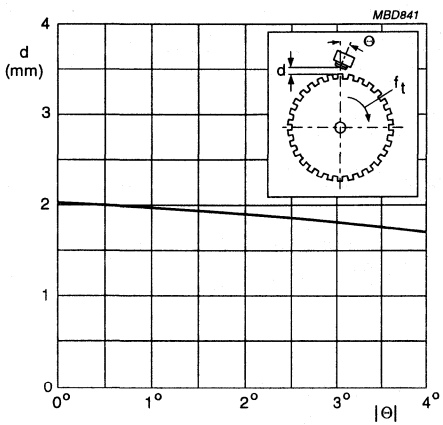
$$\text{pitch} = \text{module} \times \pi$$

Fig.10 Gear wheel definitions.



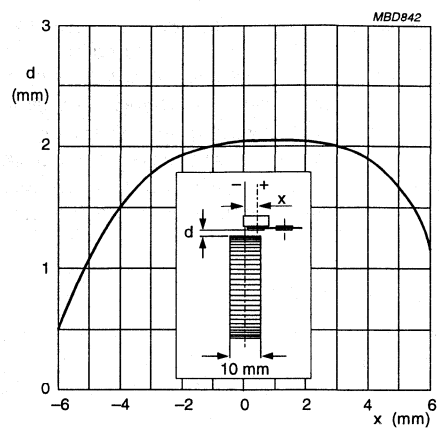
V_{CC} = 12 V; f_t = 2 kHz; module = 2 mm; pitch diameter = 100 mm.

Fig.11 Sensing distance as a function of positional tolerance in the y-axis.



V_{CC} = 12 V; f_t = 2 kHz; module = 2 mm.

Fig.12 Sensing distance as a function of positional tolerance.



V_{CC} = 12 V; f_t = 2 kHz; module = 2 mm.

Fig.13 Sensing distance as a function of positional tolerance in the x-axis.

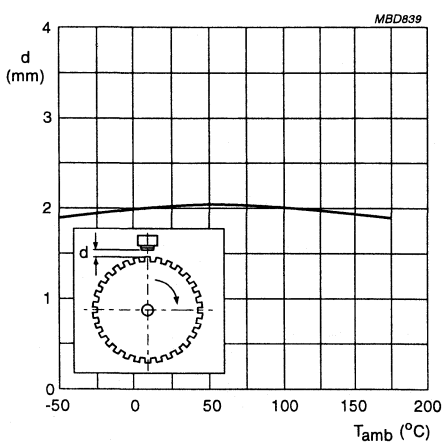


Fig.14 Typical sensing distance as a function of ambient temperature.

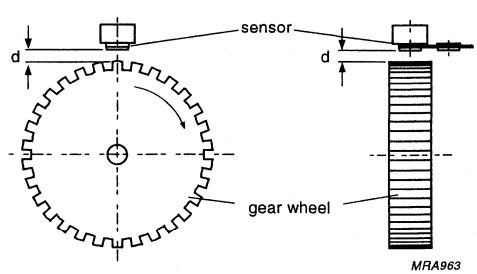
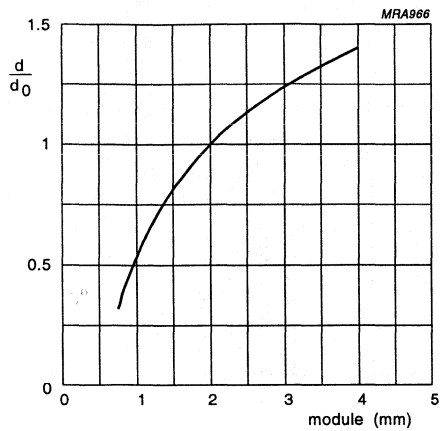
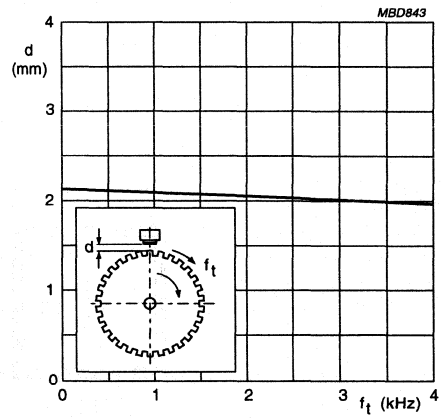


Fig.15 Sensor positioning.



d_0 = sensing distance for gear wheel with module = 2 mm.

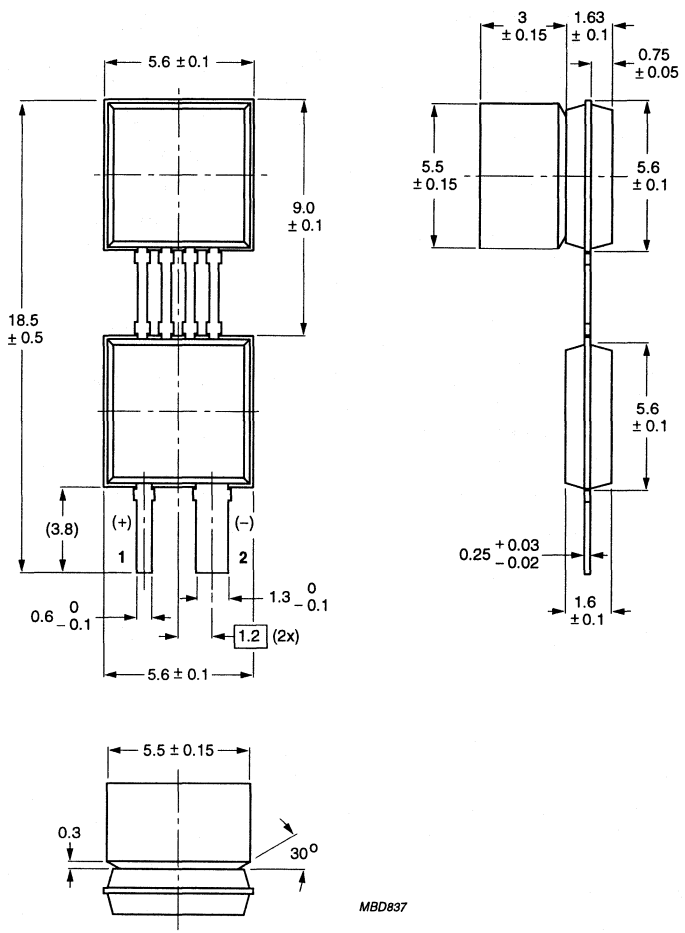
Fig.16 Normalized maximum sensing distance as a function of a gear wheel module.



V_{CC} = 12 V; module = 2 mm.

Fig.17 Sensing distance as a function of tooth frequency.

PACKAGE OUTLINE



Dimensions in mm.

Fig.18 Outline of KMI10/4.

DESCRIPTION

Sensor modules used for the detection of rotation and markings. The module is a combination of a magnetoresistive sensor, a permanent magnet and a signal conditioning circuit in hybrid technology. The module delivers a ratiometric digital output signal with short-circuit protection.

The KM110BH/11 is the DC coupled version, which allows revolution sensing beginning at 0 Hz. It is not intended for new design-ins; use KMI10/1 or KMI10/4 instead.

The AC coupled KM110BH/12 starts at 1 Hz for increased sensing distance.

PINNING

PIN	DESCRIPTION
1	ground
2	V_{OUT}
3	V_{CC}

PIN CONFIGURATION

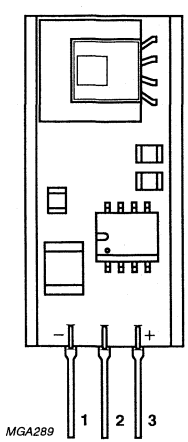


Fig.1 Simplified outline.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage	–	5	–	V
V_{OL}	output signal LOW	–	–	0.4	V
V_{OH}	output signal HIGH	4.3	–	–	V
d	sensing distance	–	–	3.5	mm
f	operating frequency range	0	–	3000	Hz
T_{op}	operating temperature range	–40	–	125	°C

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		4	10	V
V_{ripple}	ripple voltage supply	KM110BH/12 only	–	50	mV
I	supply current		–	14	mA
T_{stg}	storage temperature range		–40	125	°C
T_{op}	operating temperature range	note 1	–40	125	°C
$T_{op\ sens}$	peak temperature	note 2	–	190	°C
	output short-circuit duration to ground	permanent (note 3)			

Notes

1. The operating temperature range of the module can be extended up to +150 °C for a limited time. This will be monitored by environmental quality tests up to 500 hours of operation at +150 °C under characteristic conditions.
2. This value applies to the sensor only, for a period not exceeding 1 hour.
3. If pin 3 is shorted to either pin 1 or pin 2, current may flow permanently, without damage to the device.

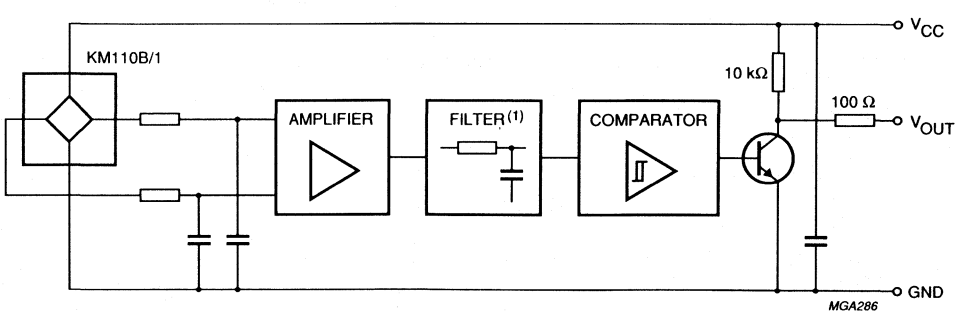
CHARACTERISTICS

T_{amb} = 25 °C; f = 2 kHz; V_{CC} = 5 V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{OL}	output signal LOW		–	0.4	V
V_{OH}	output signal HIGH		4.3	–	V
t_r	output signal rise time	$C_L \leq 50$ pF	–	10	µs
t_f	output signal fall time	$C_L \leq 50$ pF	–	10	µs
f	operating frequency range	for both directions of rotation			
	KM110BH/11 (note 1)		0	3000	Hz
	KM110BH/12		1	3000	Hz
R_L	load resistance	note 2	100	–	kΩ
d	sensing distance	note 3			
	KM110BH/11	see Fig.3	–	2.5	mm
	KM110BH/12		–	3.5	mm
y	linear position error	see Fig.4	–	0.5	mm
θ	angle error	see Fig.4	–	1	deg

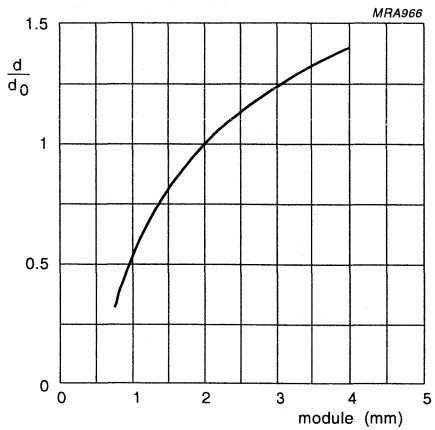
Notes

1. High rotation speeds of wheels reduce the range of the KMB110H/11, due to eddy currents. This causes a reduction in sensing distance.
2. $R_L \leq 100$ kΩ possible with external pull-up resistor.
3. Gear wheel dimensions: diameter = 104 mm; width = 10 mm; 50 teeth; module 2.08; material 9SMnPb28k.



(1) KM110BH/12 only.

Fig.2 Circuit diagram.



d_0 = measuring distance for a gear wheel with module m = 2 mm.

Fig.3 Normalized measuring distance as a function of gear wheel module.

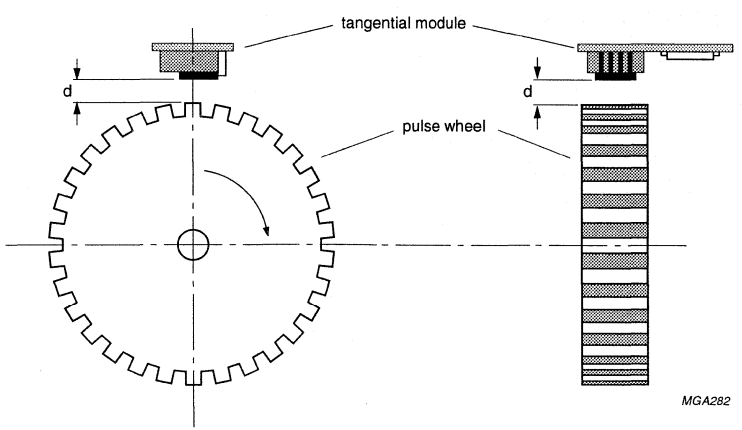


Fig.4 Optimal sensor position.

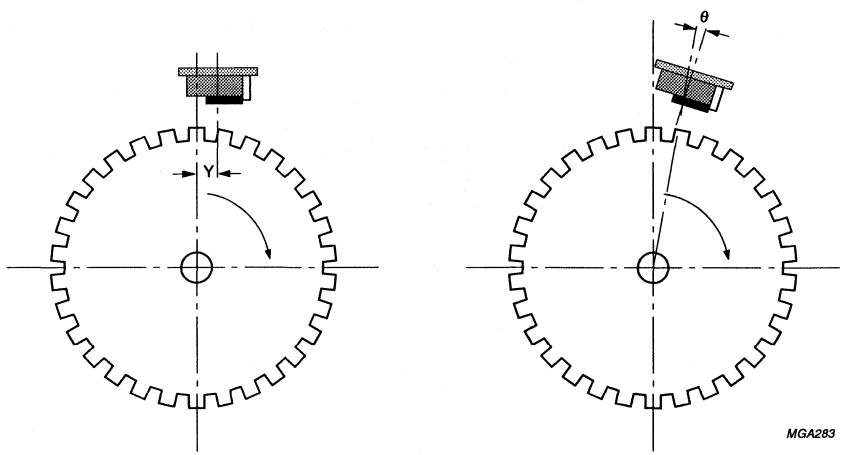


Fig.5 Sensor position with tolerances.

Gear wheel dimensions

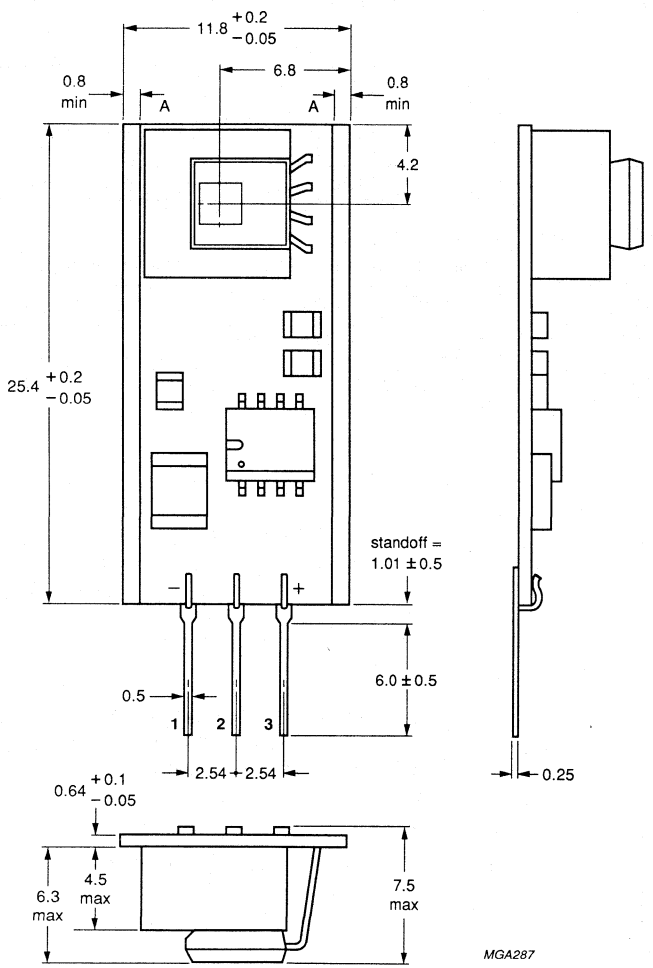
The gear wheel dimensions are specified in accordance with the German DIN standard, where:

d = pitch diameter (mm); z = number of teeth; m = module
m = d/z (mm); t = pitch = $\pi \times$ m (mm).

Mounting conditions

Refer to Fig.4. The module senses ferrous indicators like wheels in one direction only (no rotational symmetry). The symmetrical axis of the sensor corresponds to the axis of the ferrite magnet. The crystal is not mounted in the centre of the housing.

PACKAGE OUTLINE



Dimensions in mm.

Area 'A' free of SMD devices.

Fig.5 KM110BH/11; KM110BH/12.

Revolution sensors KM110BH/13; KM110BH/14

DESCRIPTION

Sensor modules used for the detection of rotation and markings. The module is a combination of a magnetoresistive sensor, a permanent magnet and a signal conditioning circuit in hybrid technology. The module delivers a ratiometric digital output signal with short-circuit protection.

The KM110BH/13 is the DC coupled version, which allows revolution sensing beginning at 0 Hz. It is not intended for new design-ins; use KMI10/1 or KMI10/4 instead.

The AC coupled KM110BH/14 starts at 1 Hz for increased sensing distance.

PINNING

PIN	DESCRIPTION
1	ground
2	V_{OUT}
3	V_{CC}

PIN CONFIGURATION

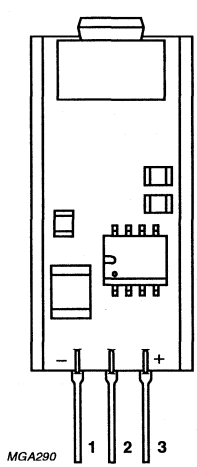


Fig.1 Simplified outline.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage	–	5	–	V
V_{OL}	output signal LOW	–	–	0.4	V
V_{OH}	output signal HIGH	4.3	–	–	V
d	sensing distance	–	–	3.5	mm
f	operating frequency range	0	–	3000	Hz
T_{op}	operating temperature range	–40	–	125	°C

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		4	10	V
V_{ripple}	ripple voltage supply	KM110BH/14 only	–	50	mV
I	supply current		–	14	mA
T_{stg}	storage temperature range		–40	125	°C
T_{op}	operating temperature range	note 1	–40	125	°C
$T_{op\ sens}$	peak temperature	note 2	–	190	°C
	output short-circuit duration to ground	permanent (see note 3)			

Notes

1. The operating temperature range of the module can be extended up to +150 °C for a limited time. This will be monitored by environmental quality tests up to 500 hours of operation at +150 °C under characteristic conditions.
2. This value applies to the sensor only, for a period not exceeding 1 hour.
3. If pin 3 is shorted to either pin 1 or pin 2, current may flow permanently, without damage to the device.

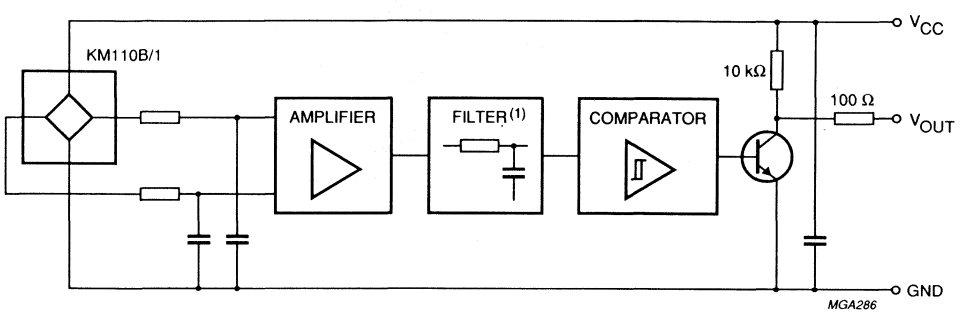
CHARACTERISTICS

T_{amb} = 25 °C; f = 2 kHz; V_{CC} = 5 V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{OL}	output signal LOW		–	0.4	V
V_{OH}	output signal HIGH		4.3	–	V
t_r	output signal rise time	$C_L \leq 50$ pF	–	10	µs
t_f	output signal fall time	$C_L \leq 50$ pF	–	10	µs
f	operating frequency range	for both directions of rotation			
	KM110BH/13 (note 1)		0	3000	Hz
	KM110BH/14		1	3000	Hz
R_L	load resistance	note 2	100	–	kΩ
d	sensing distance	note 3			
	KM110BH/13	see Fig.3	–	2.5	mm
	KM110BH/14		–	3.5	mm
y	linear position error	see Fig.4	–	0.5	mm
θ	angle error	see Fig.4	–	1	deg

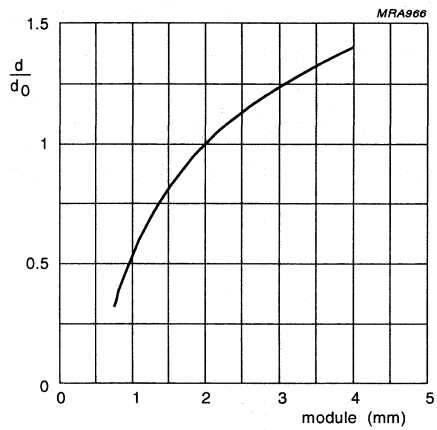
Notes

1. High rotation speeds of wheels reduce the range of the KMB110H/11, due to eddy currents. This causes a reduction in sensing distance.
2. $R_L \leq 100$ kΩ possible with external pull-up resistor.
3. Gear wheel dimensions: diameter = 104 mm; width = 10 mm; 50 teeth; module 2.08; material 9SMnPb28k.



(1) KM110BH/14 only.

Fig.2 Circuit diagram.



d_0 = measuring distance for a gear wheel with module m = 2 mm.

Fig.3 Normalized measuring distance as a function of gear wheel module.

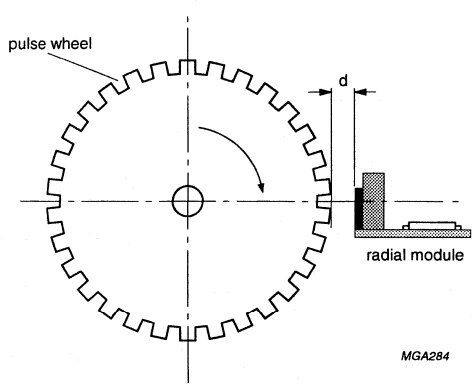


Fig.4 Optimal sensor position.

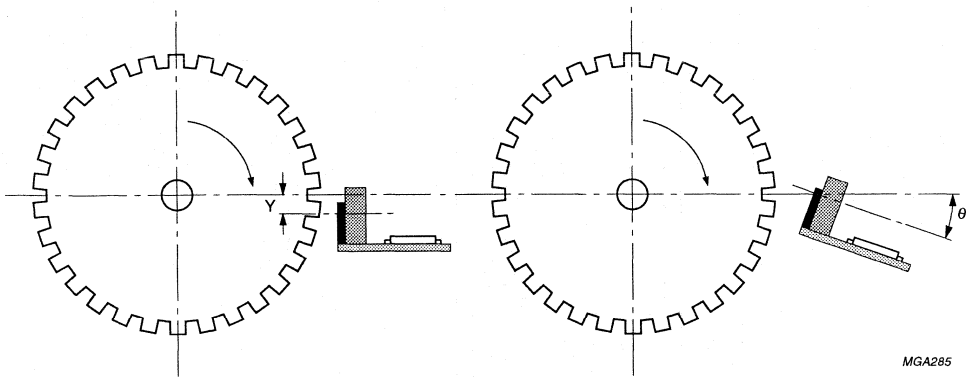


Fig.5 Sensor position with tolerances.

Gear wheel dimensions

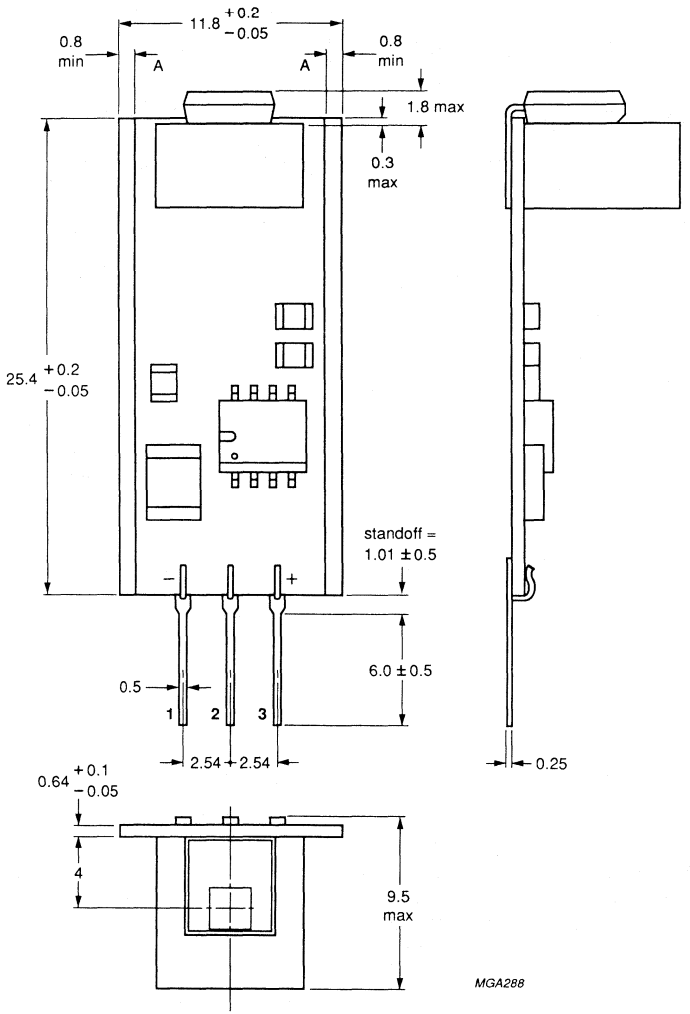
The gear wheel dimensions are specified in accordance with the German DIN standard, where:

d = pitch diameter (mm); z = number of teeth; m = module m = d/z (mm); t = pitch = $\pi \times$ m (mm).

Mounting conditions

Refer to Fig.4. The module senses ferrous indicators like wheels in one direction only (no rotational symmetry). The symmetrical axis of the sensor corresponds to the axis of the ferrite magnet. The crystal is not mounted in the centre of the housing.

PACKAGE OUTLINE



Dimensions in mm.

Area 'A' free of SMD devices.

Fig.5 KM110BH/13; KM110BH/14.

Rotational speed sensor with direction recognition

KM110BH/31

DESCRIPTION

Sensor module for the detection of rotational speed and its direction. The module consists of the magnetoresistive sensor KMZ10B, a permanent magnet and a signal conditioning circuit in hybrid technology. The module delivers a digital output signal with short-circuit protection.

PINNING

PIN	DESCRIPTION
1	V_{CC}
2	V_{O1}
3	V_{O2}
4	ground

PIN CONFIGURATION

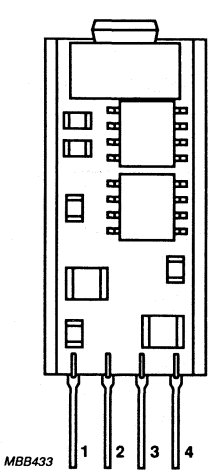


Fig.1 Simplified outline.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage	–	5	–	V
V_{O1L}, V_{O2L}	output signal LOW	–	–	0.4	V
V_{O1H}, V_{O2H}	output signal HIGH	4.3	–	–	V
d	sensing distance	–	–	3	mm
f	operating frequency range	2	–	50000	Hz
T_{op}	operating temperature range	–40	–	125	°C

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		4	10	V
V_{ripple}	ripple voltage supply		–	40	mV
I_{CC}	supply current		–	14	mA
T_{stg}	storage temperature range		–40	125	°C
T_{op}	operating temperature range	note 1	–40	125	°C
$T_{op\ sens}$	peak temperature	sensor only	–	150	°C
	output short-circuit duration to ground	continuous			

Note

1. The operating temperature range of the module can be extended up to +150 °C for a limited time. This will be monitored by environmental quality tests up to 500 hours of operation at +150 °C under characteristic conditions.

CHARACTERISTICS

T_{amb} = 25 °C; f = 2 kHz; V_{CC} = 5 V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{O1L}, V_{O2L}	output signal LOW	note 1	–	0.4	V
V_{O1H}, V_{O2H}	output signal HIGH	note 2	4.3	–	V
t_r	output signal rise time	$C_L \leq 50$ pF	–	10	µs
t_f	output signal fall time	$C_L \leq 50$ pF	–	10	µs
f	operating frequency range	for both directions of rotation	2	50 000	Hz
R_L	load resistance	note 3	100	–	kΩ
d	sensing distance	note 4 see Fig.3		3	mm
y	linear position error	see Fig.4	–	0.5	mm
θ	angle error	see Fig.4	–	1	deg

Notes

1. Refer to Figs 2, 5 and 6. The KM110BH/31 sensor is based on separated signal conditioning for two half-bridge signals. As the average distance between the two bridge-halves is fixed by the magnetoresistive sensor dimensions, the optimum structure pitch of a gear wheel should be 2.8 mm. Figures 5 and 6 show the dependence of both output signals on the direction of movement.
2. V_{O1H} and V_{O2H} are relative to V_{CC}.
3. $R_L \leq 100$ kΩ possible with external pull-up resistor.
4. Gear wheel dimensions: diameter = 104 mm; width = 10 mm; 50 teeth; module 2.08; material 9SMnPb28k.

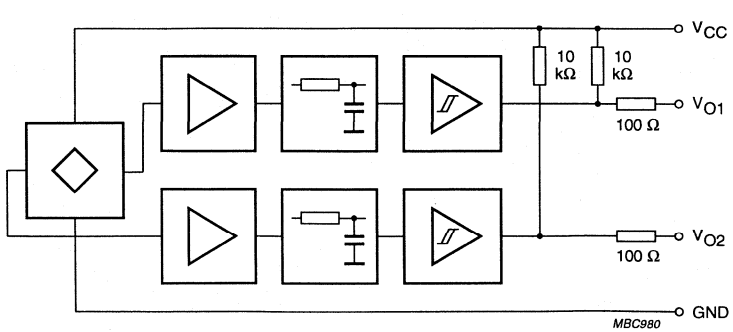


Fig.2 Circuit diagram.

Gear wheel dimensions

The gear wheel dimensions are specified in accordance with the German DIN 780 standard, where:

d = pitch diameter (mm); z = number of teeth; m = module m = d/z (mm); t = pitch = π x m (mm).

Mounting conditions

Refer to Fig.3 for the correct mounting position. The module senses ferrous indicators like wheels in one plane only (no rotational symmetry). The measuring axis of the sensor corresponds to the symmetry axis of the ferrite magnet - the crystal is not mounted in the centre of the housing.

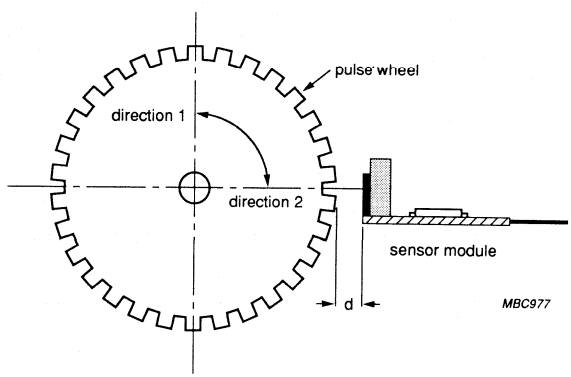


Fig.3 Optimal sensor position.

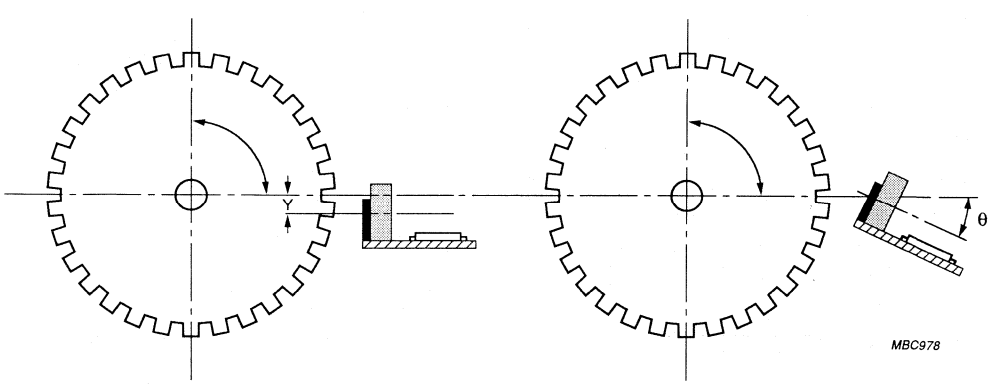


Fig.4 Sensor position with tolerances.

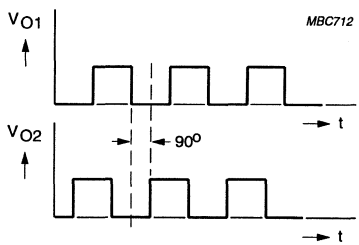


Fig.5 Output signals with gear wheel rotation in direction 1.

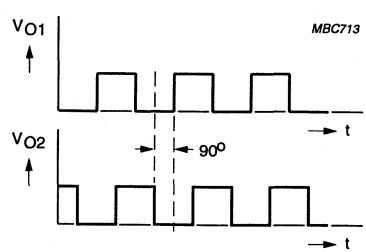


Fig.6 Output signals with gear wheel rotation in direction 2.

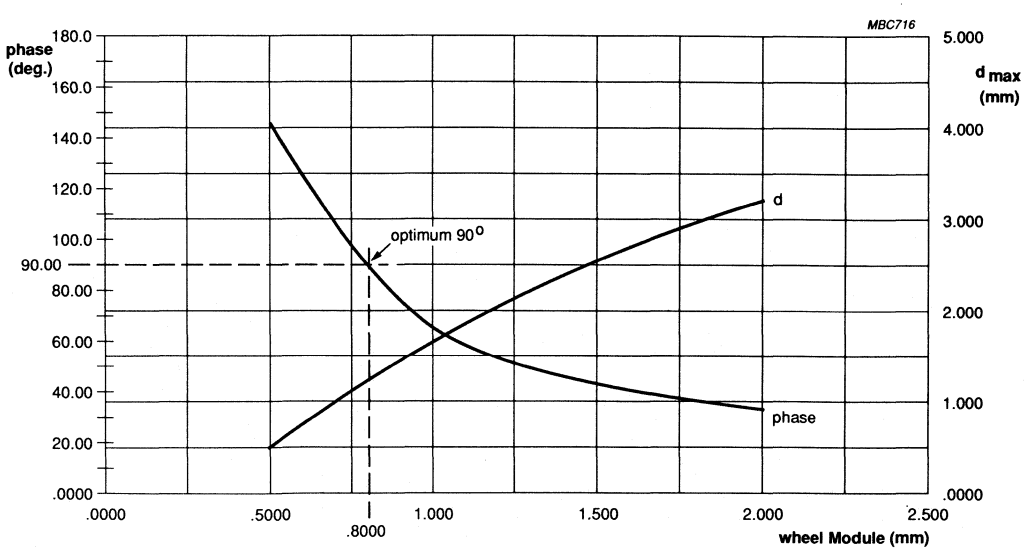


Fig.7 Phase and distance relationship for different gear wheel modules.

APPLICATION INFORMATION

Direction recognition can be achieved with a microprocessor or with a simple flip-flop circuit, see Fig.8.

In life-support systems, the behaviour of electronic components throughout their working life can be unpredictable. The use of these devices in support systems can only be permitted when there is no danger to life caused by devices failing unexpectedly.

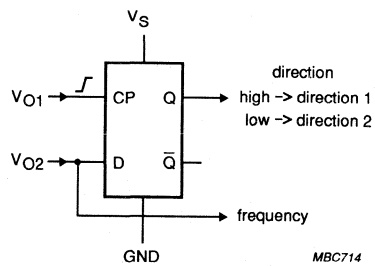
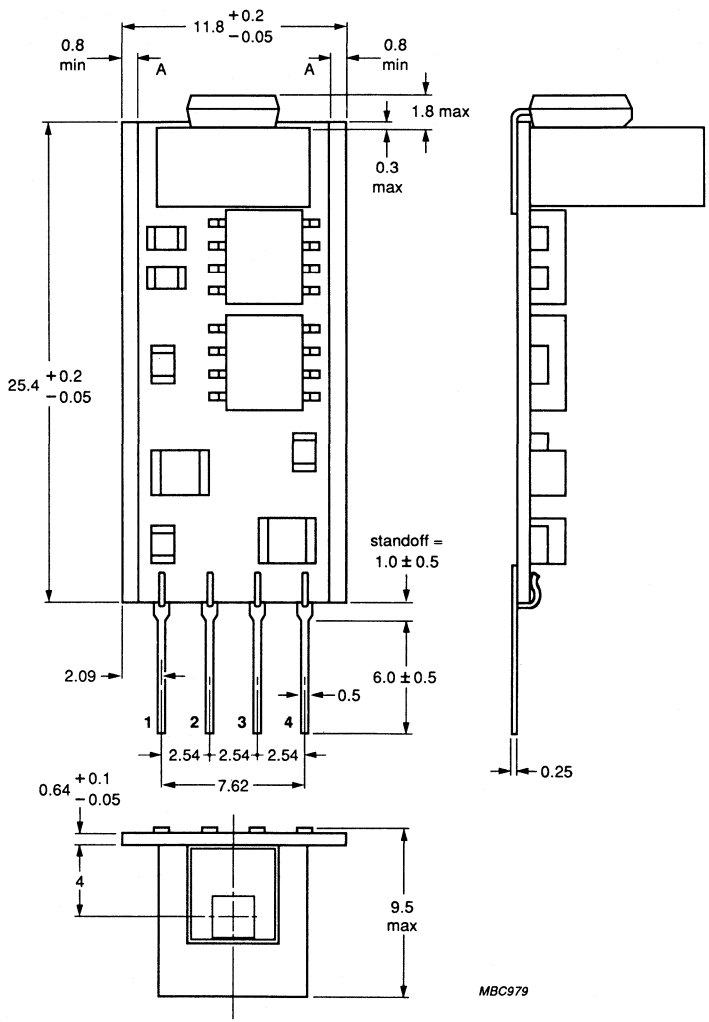


Fig.8 Interface for direction rotation.

PACKAGE OUTLINE



Dimensions in mm.

Area 'A' free of SMD devices.

Fig.9 KM110BH/31.

Rotational speed sensor with direction recognition

KM110BH/32

FEATURES

- Contactless rotational speed sensing
- Direction recognition capability
- Easy to mount, ready for use
- Digital output current signal
- Operating temperatures up to 125 °C
- EMC resistant.

DESCRIPTION

The KM110BH/32 sensor detects rotational speed and direction. The sensor comprises a magnetoresistive sensor element, KMZ10B, a signal conditioning circuit in hybrid technology and a permanent magnet. The KM110BH/32 delivers a digital current output signal with short-circuit protection.

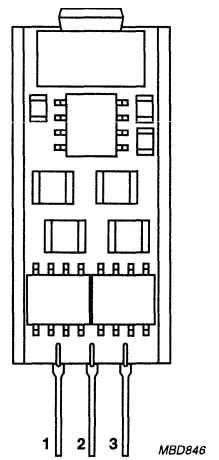


Fig.1 Simplified outline.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1	ground
V_{CC1}	2	DC supply 1 voltage
V_{CC2}	3	DC supply 2 voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC1}	DC supply 1 voltage	–	12	–	V
V_{CC2}	DC supply 2 voltage	–	12	–	V
$I_{CC1(low)}$	output 1 current low	–	7	–	mA
$I_{CC2(low)}$	output 2 current low	–	7	–	mA
$I_{CC1(high)}$	output 1 current high	–	14	–	mA
$I_{CC2(high)}$	output 2 current high	–	14	–	mA
$f_{t(oper)}$	operating tooth frequency	10	–	20000	Hz
d	sensing distance	–	0 to 4	–	mm
T_{amb}	operating ambient temperature	–40	–	+125	°C

BLOCK DIAGRAM

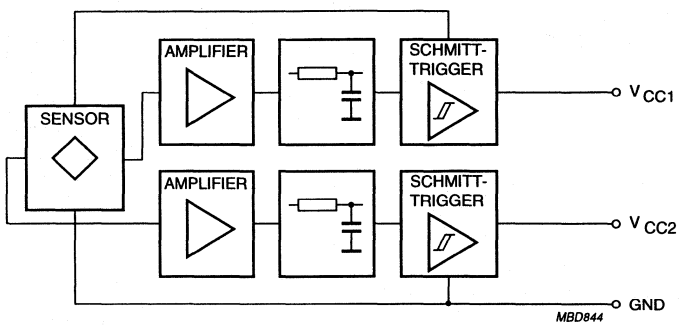


Fig.2 Block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC1}	DC supply 1 voltage		7.5	16	V
V_{CC2}	DC supply 2 voltage		7.5	16	V
T_{stg}	storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–40	+125(1)	°C
T_{peak}	peak temperature	sensor element only	–	150	°C

Note

1. The operating temperature range of the module can be extended up to +150 °C for a limited time.

Rotational speed sensor with direction recognition

KM110BH/32

CHARACTERISTICS

T_{amb} = 25 °C; $V_{CC1} = V_{CC2}$ = 12 V; f = 2 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CC1(low)}$	output 1 current low	note 1	5.6	–	8.4	mA
$I_{CC2(low)}$	output 2 current low	note 1	5.6	–	8.4	mA
$I_{CC1(high)}$	output 1 current high		11.2	–	16.8	mA
$I_{CC2(high)}$	output 2 current high		11.2	–	16.8	mA
t_r	output current rise time	$C_L \leq 50$ pF	–	–	10	µs
t_f	output current fall time	$C_L \leq 50$ pF	–	–	10	µs
$f_{t(oper)}$	operating tooth frequency	for both rotation directions	10	–	20000	Hz
R_L	load resistance		–	–	120	Ω
d	sensing distance	see Fig.5	–	0 to 4	–	mm
y	linear position error	see Fig.6	–	–	0.5	mm
θ	angular error	see Fig.6	–	–	1	deg

Note

1. The KM110BH/32 sensor is based on separated signal conditioning for two half-bridge signals (see Fig.2). As the average distance between the two bridge-halves is fixed by the magnetoresistive sensor dimensions, the optimum pitch of the pulse wheel should be 2.8 mm. Figures 3 and 4 show the dependency of the direction movement.

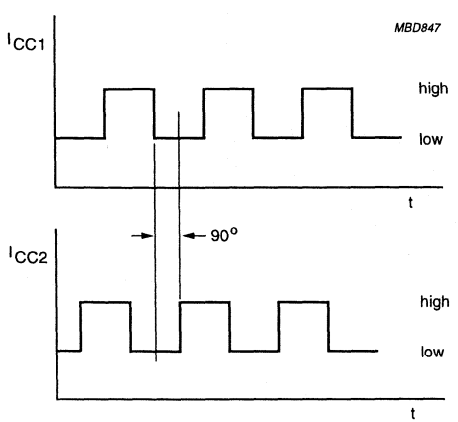


Fig.3 Output signals with pulse wheel rotation in direction 1.

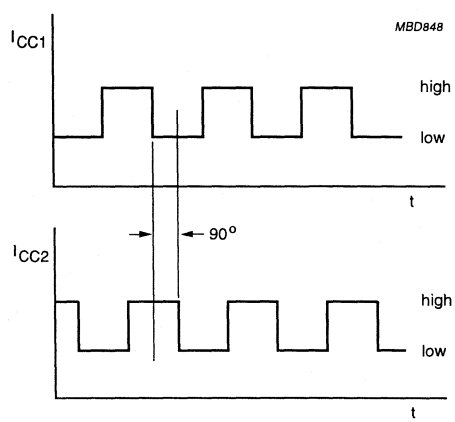


Fig.4 Output signals with pulse wheel rotation in direction 2.

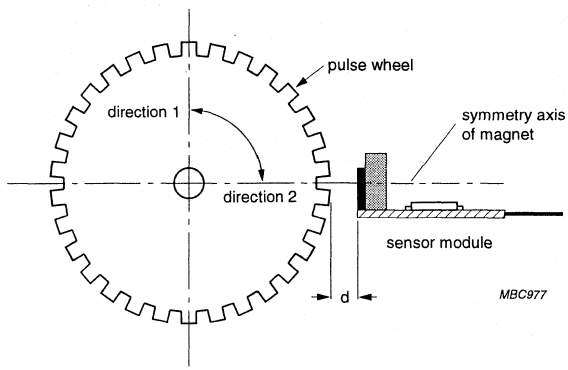


Fig.5 Sensor positioning.

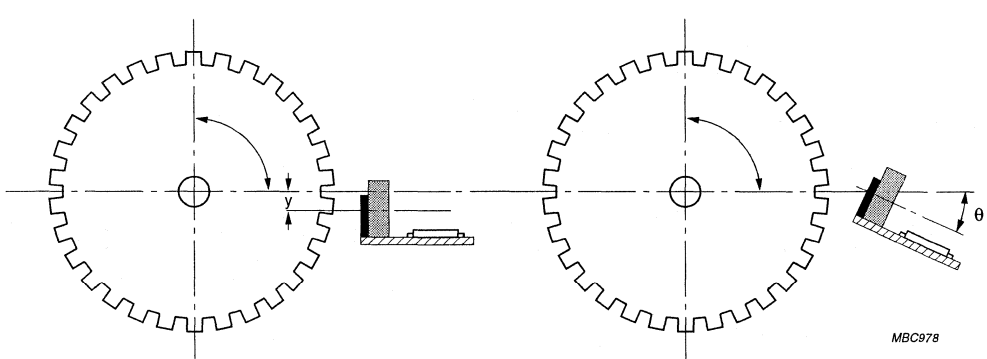


Fig.6 Sensor positional errors.

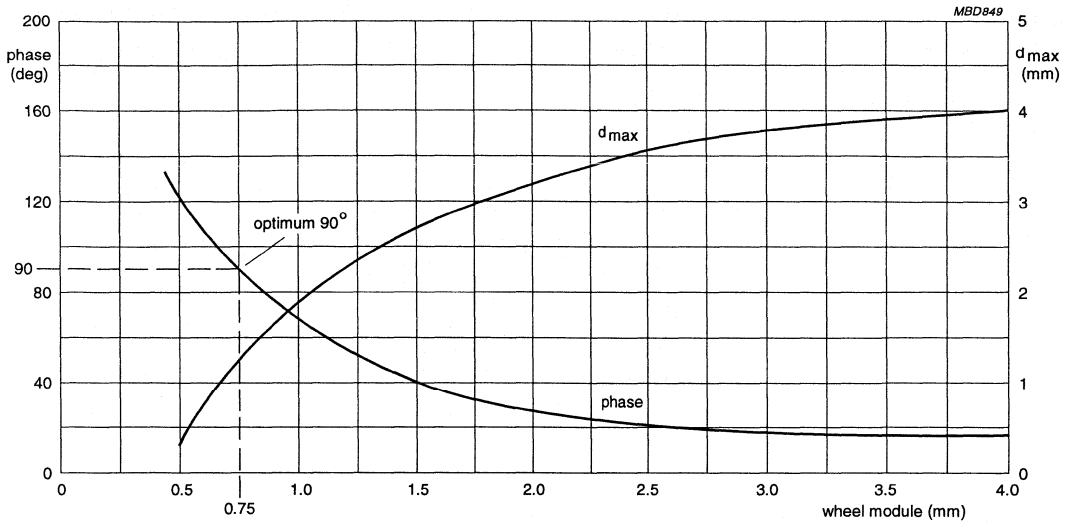


Fig.7 Phase and distance relationship for different pulse wheel modules.

APPLICATION INFORMATION

Mounting conditions

Refer to Fig.5 for the correct mounting position. The module senses ferrous indicators like pulse wheels in one plane only (no rotational symmetry). The measuring axis of the sensor corresponds to the symmetry axis of the ferrite magnet. The crystal is not mounted in the centre of the housing.

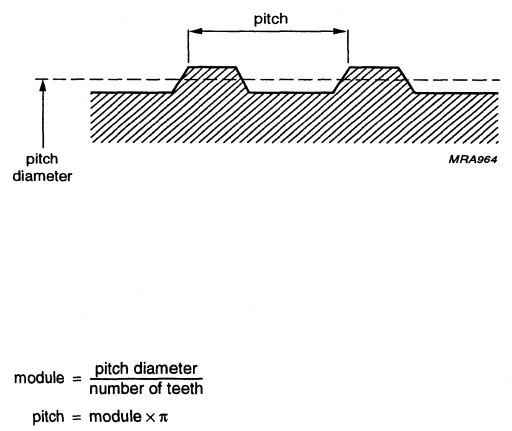


Fig.8 Gear wheel definitions.

Signal evaluation

The two output signals from the sensor are constant current symmetrical pulses with a lead/lag difference of 90°. Ground is common to both channels. A simple two-channel current to voltage conversion is shown in Fig.9. Operation is similar for both channels. The voltage developed across a measuring resistor in the positive supply line is applied to buffer IC1. The voltage output pulse V_{O1} (V_{O2}) is referred to ground and is at a level suitable for input to subsequent digital processing circuitry.

Direction recognition can be achieved with a microcontroller or with a simple flip-flop circuit (see Fig.10).

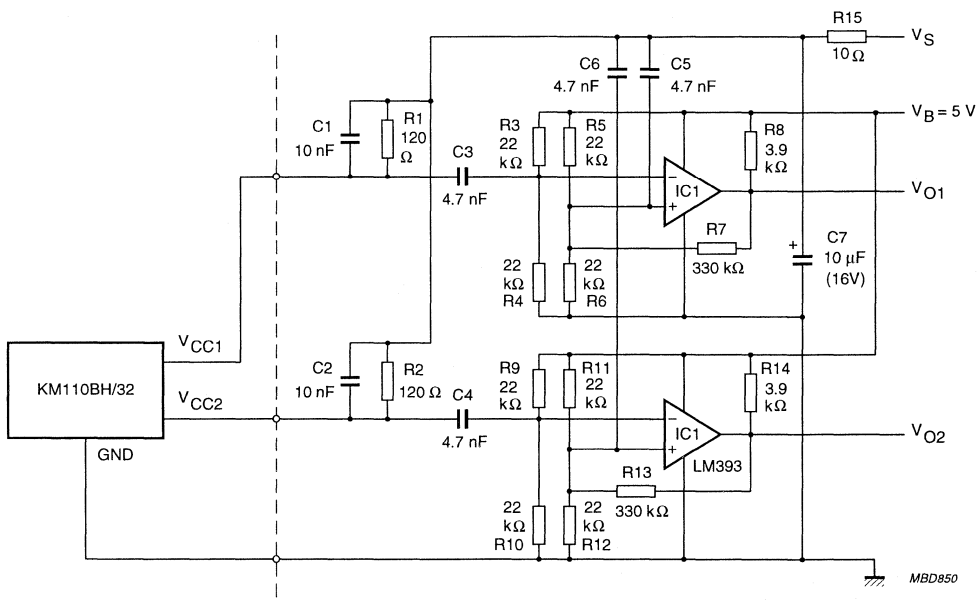


Fig.9 Output signal conversion circuit.

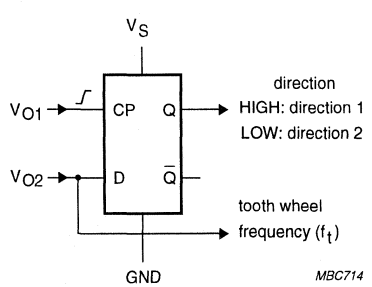
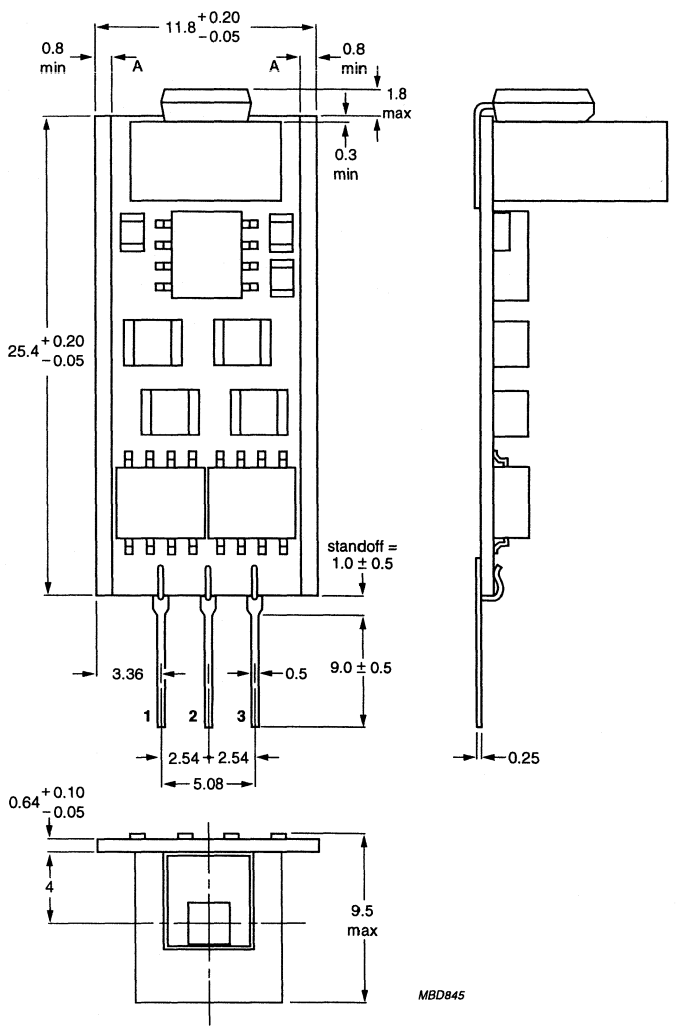


Fig.10 Interface for direction recognition.

PACKAGE OUTLINE



Dimensions in mm.
Area 'A' free of SMD devices.

Fig.11 Outline of KM110BH/32.

POWER SWITCHES

Automotive motor control with Philips MOSFETs

Application report

The trend for comfort and convenience features in today's cars means that more electric motors are required than ever - a glance at Table 1 will show that up to 30 motors may be used in top of the range models, and the next generation of cars will require most of these features as standard in middle of the range models.

All these motors need to be activated and deactivated, usually from the dashboard; that requires a lot of copper cable in the wiring harnesses - up to 4km in overall length, weighing about 20 kg. Such a harness might contain over 1000 wires, each requiring connectors at either end and taking up to six hours to build. Not only does this represent a cost and weight penalty, it can also create major 'bottlenecks' at locations such as door hinges, where it becomes almost impossible to physically accommodate the 70-80 wires required. Now, if the motor switching, reversing or speed control were to be done at the load by semiconductor switches, these in turn can be driven via much thinner, lighter wiring thus alleviating the bottlenecks. Even greater savings - approaching the weight of a passenger - can be achieved by incorporating multiplex wiring controlled by a serial bus.

Types of motors used in automobiles

Motor design for automotive applications represents an attempt at achieving the optimum compromise between conflicting requirements. The torque/speed characteristic demanded by the application must be satisfied while taking account of the constraints of the materials, of space and of cost.

There are four main families of DC motors which are, or which have the potential to be used in automobiles.

Wound field DC Commutator Motors

Traditionally motors with wound stator fields, a rotor supply fed via brushes and a multi-segment commutator - see Fig. 1 - have been widely used. Recently, however, they have been largely replaced by permanent magnet motors. Characteristically they are found with square frames. They may be Series wound (with high torque at start up but tend to 'run away' on no-load), Shunt wound (with relatively flat speed/torque characteristics) or (rarely) Compound wound.

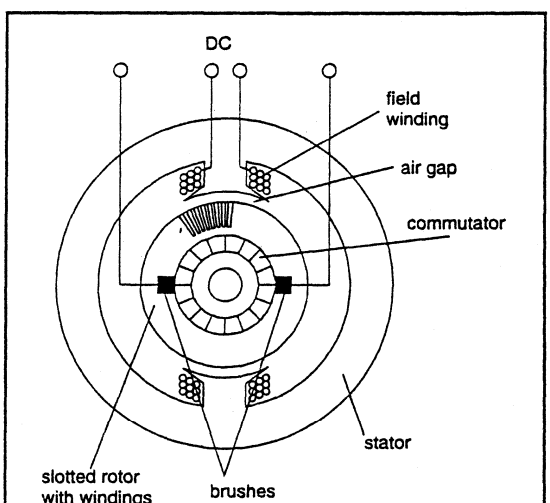
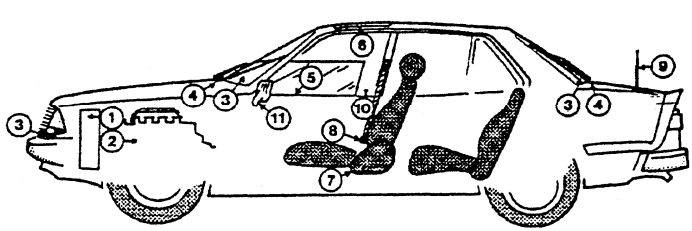


Fig. 1 Wound Field DC Commutator Motor



MOSFETs control motors for:

1. radiator fans
2. fuel pumps
3. front, rear and headlamp wipers
4. front and rear washer units
5. window lifters
6. sun-roofs
7. seat adjustments
8. seat belts
9. radio aerials
10. door locks
11. mirror adjustment

motor application	typical power (W)	nominal current (A)	typical number of such motors	type of drive	typical number of switches per motor	proposed standard BUK-	MOSFET * L²FET BUK-	comments
air-conditioning	300	25	1	unidirectional, variable speed	1	456	556	Active suspension may also require such high power motors
radiator fan	120-240	10-20	1	unidirectional, variable speed	1	455	555	These motors may go brushless, requiring 3 to 6 lower rated switches
fuel pump	100	8	1	unidirectional	1	453	553	
wipers:				unidirectional, variable speed				Reversing action is at present mechanical. This could be done electronically using 2 or 4 switches
front			1-2					
rear	60-100	5-8	1		1	452/453	552/553	
headlamp			2					
washers:								
front			1-2					
	30-60	2.5-5		undirectional	1	452	552	
rear			1-2					
window lifter	25-120	2-10	2-4	reversible	4	452/455	552/555	
sun-roof	40-100	3.5-8	1	reversible	4	452/453	552/553	
seat adjustment (slide, recline, lift, lumbar)	50	4	4-16	reversible	4	453	553	
seat belt	50	4	2-4	reversible	4	453	553	
pop-up headlamp	50	4	2	reversible	4	453	553	
radio aerial	25	2	1	reversible	4	452	552	
door lock	12-36	1-3	6-9	reversible	4	451/452	551/552	
mirror adjustment	12	1	2	reversible	4	451	551	

* These are meant for guidance only. Specific applications should be checked against individual users requirements. In addition to standard and L²FETs, FredFETs and low and high side TOPFETs might be considered. Also a variety of isolated, non-isolated and surface mount package options are available

Table 1 Typical motor and switch requirements in top of range car.

Permanent Magnet (PM) DC Commutator Motors

These are now the most commonly used motors in modern cars. The permanent magnet forms the stator, the rotor consists of slotted iron containing the copper windings - see Fig. 2. They have a lighter rotor and a smaller frame size than wound field machines. Typical weight ratios between a PM and a wound field motor are:

Copper	1:10
Magnets	1:7
Rotor	1:2.5
Case	1:1

PM motors have a linear torque/speed characteristic - see Fig. 3 for typical curves relating torque, speed, current and efficiency. (Philips 4322 010 76130). They are generally used below 5000 rpm. Their inductance (typically 100 - 500 μH) is much lower than wound field machines. New materials (e.g. neodymium iron boron compounds) offer even more powerful fields in smaller volumes.

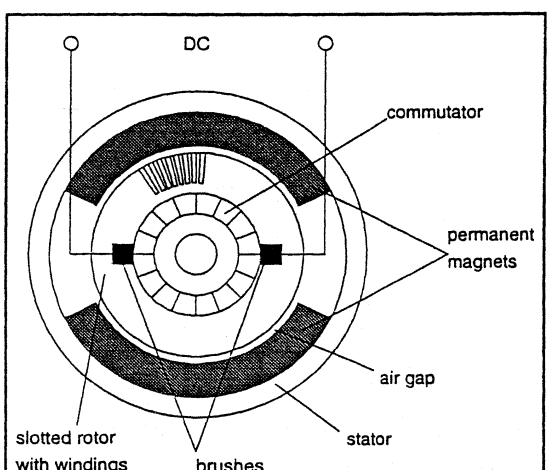


Fig. 2 Permanent Magnet Commutator Motor

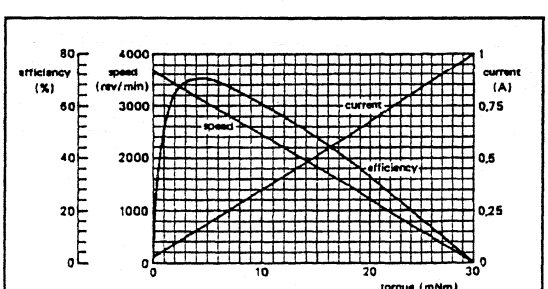


Fig. 3 Performance Curves for PM Commutator Motor

PM Brushless DC Motors

Although common in EDP systems, brushless DC motors are not yet used extensively in cars. They are under consideration for certain specialised functions, e.g. fuel pump where their 'arc free' operation makes them attractive. They have a wound stator field and a permanent magnet rotor - Fig. 4. As their name suggests they have neither mechanical commutator nor brushes, thus eliminating brush noise/wear and associated maintenance. Instead they depend on electronic commutation and they require a rotor position monitor, which may incorporate Hall effect sensors, magneto resistors or induced signals in the non energised winding. Thanks to their lightweight, low inertia rotor they offer high efficiency, high power density, high speed operation and high acceleration. They can be used as servos.

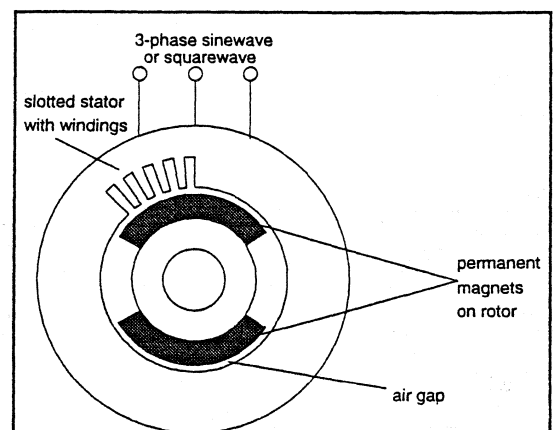


Fig. 4 Permanent Magnet Brushless Motor

Switched Reluctance Motors

These motors - see Fig. 5 - are the wound field equivalent to the PM brushless DC machine, with similar advantages and limitations. Again, not yet widely used, they have been proposed for some of the larger motor applications such as radiator and air conditioning fans, where their high power/weight ratio makes them attractive. They can also be used as stepper motors in such applications as ABS and throttle control.

Motor drive configurations

The type of motor has a considerable influence on the configuration of the drive circuit. The two families of DC motors, commutator and brushless need different drive circuits. However suitably chosen MOSFETs can be used to advantage with both.

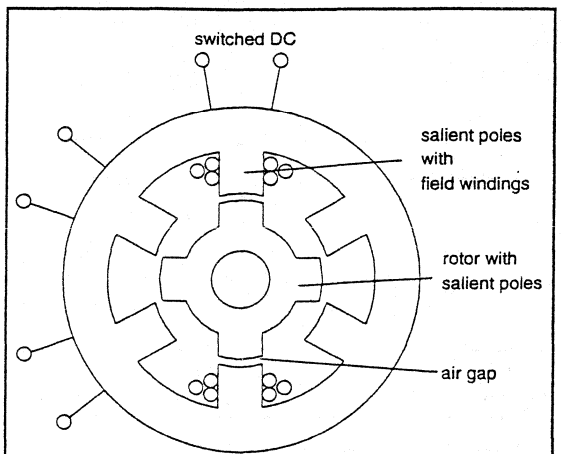


Fig. 5 Switch Reluctance Motor

Commutator Motors

Both permanent magnet and wound field commutator motors can be controlled by a switch in series with the DC supply - Fig. 6. Traditionally relays have been used, but they are not considered to be very reliable, particularly in high vibration environments. Semiconductors offer an attractive alternative, providing:

- low on-state voltage drop.
- low drive power requirements.
- immunity from vibration.

The Power MOSFET scores on all counts, offering ON resistances measured in mΩ and requiring only a few volts (at almost zero current) at the gate, to achieve this.

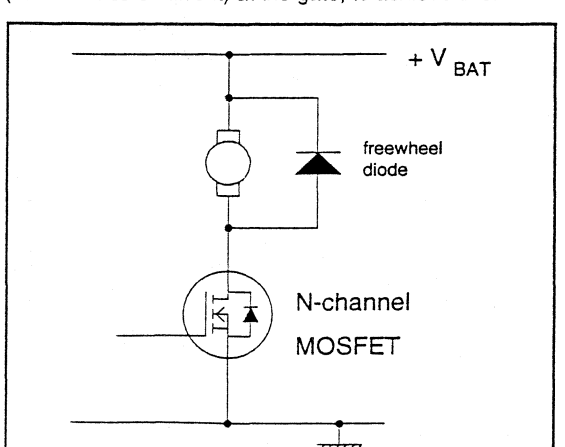


Fig. 6 Commutating Motor Switch

When a motor is switched off, it may or may not be running. If it is, then the motor acts as a voltage source and the rotating mechanical energy must be dissipated either by friction or by being transformed into electrical energy and returned to the supply via the inherent anti-parallel diode of the MOSFET. If it is not turning, then the motor appears as purely an inductance and for a low side switch the voltage transient developed will take the MOSFET into avalanche. Now, depending on the magnitude of the energy stored in the field and the avalanche capability of the MOSFETs, a diode in parallel with the motor may or may not be required.

As a first approximation, if

$$\frac{1}{2} \cdot L_m I_m^2 < W_{DSS}$$

then a diode may not be needed.

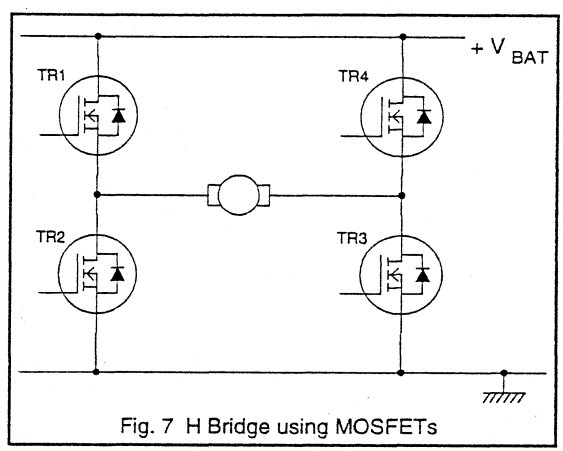


Fig. 7 H Bridge using MOSFETs

Reversing the polarity of the supply, to a commutator motor, reverses the direction of rotation. This usually requires an H bridge of semiconductors, see Fig. 7. In this case the built in diodes, inherent in MOSFETs, mean that no extra diodes are necessary. It should be noted that there are now two devices in series with the motor. So, to maintain the same low level of on-state voltage drop, each MOSFET must be doubled in area. With four devices in all, this means a reversing H bridge requires 8 x the crystal area needed by a unidirectional drive.

Chopping the supply, controls the mean voltage applied to the motor, and hence its speed. In the case of the H bridge TR1 and TR4 might be used to control direction, while a chopping signal (typically 20kHz) is applied to TR3 or TR2. When reversing the direction of rotation, it is preferable to arrange the gating logic so that the system goes through a condition where TR1, TR2, TR3 and TR4 are all off.

Switched Field Motors

PM brushless motors typically require 6 switches to generate the rotating field, see Fig. 8. Although there are motors, which operate at lower power density, which can be driven from 3 switches. The circuit in Fig. 9 shows a low side switch version of such a drive. A similar arrangement with high side switches would be possible.

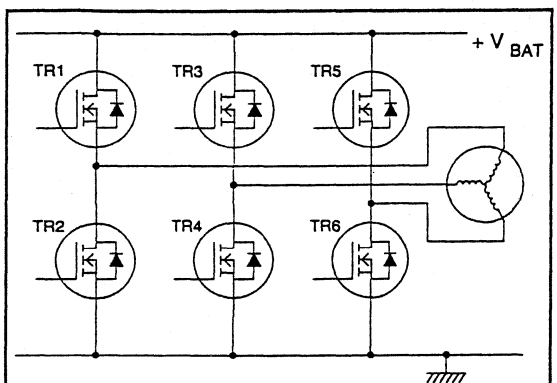


Fig. 8 MOSFET Brushless Motor Drive

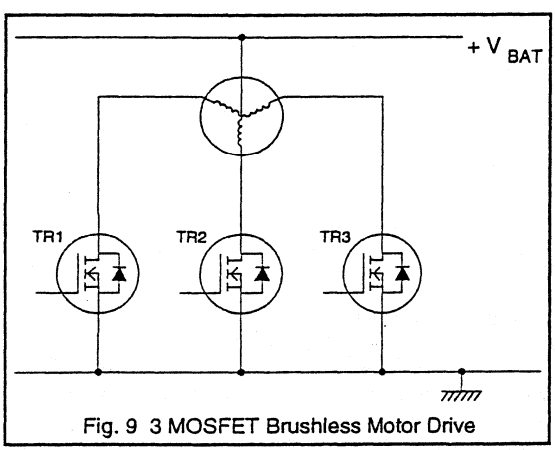


Fig. 9 3 MOSFET Brushless Motor Drive

Switched reluctance motors may use as few as 4 or as many as 12 switches to generate the rotating field, a 4 switch version is shown in Fig. 10.

The speed and direction of all switched field motors is controlled by the timing of the field pulses. In the case of brushless DC machines these timing pulses can be derived from a dedicated IC such as the Philips NE5570. Rotor position sensing is required - using, for example, magnetoresistive sensors - to determine which windings should be energised. Compared with a DC commutator motor, the power switches for a brushless motor have to be fast, because they must switch at every commutation.

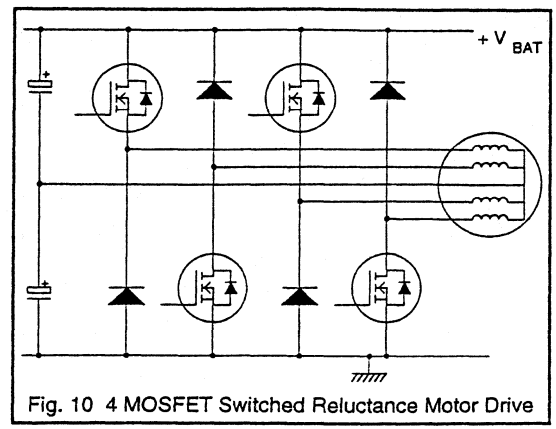


Fig. 10 4 MOSFET Switched Reluctance Motor Drive

PWM speed control pushes up the required switching speed even further. Philips MOSFETs are designed so that both switch and inbuilt diode are capable of efficient switching at the highest frequencies and voltages encountered in automotive applications.

High side drivers

Often, in automobiles, there is a requirement for the switch to be connected to the positive battery terminal with the load connected via the common chassis to negative. Negative earth reduces corrosion and low side load is safer when loads are being worked on or replaced. Also, when H bridges are considered the upper arms are of course high side switches.

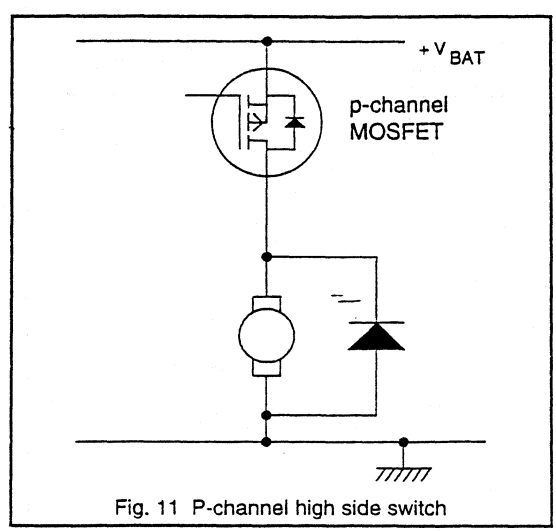


Fig. 11 P-channel high side switch

There are two MOSFET possibilities for high side switches:

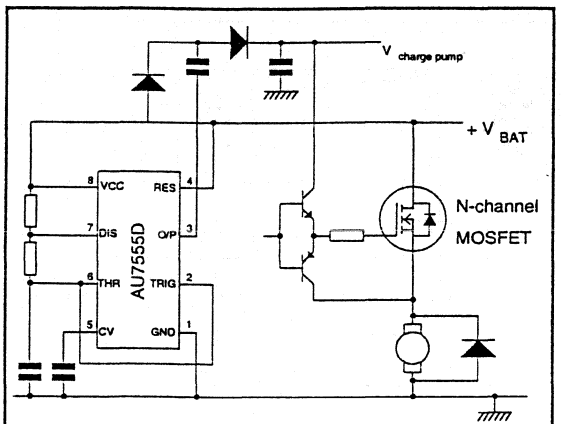


Fig. 12 N-channel high side switch with charge pump

- **P-channel switches.** These simplify the drive circuit which only needs referencing to the positive supply, see Fig. 11. Unfortunately p-channel devices require almost three times the silicon area to achieve the same on resistance as n-channel MOSFETs, which increases cost. Also P-channel devices that can be operated from logic level signals are not readily available.

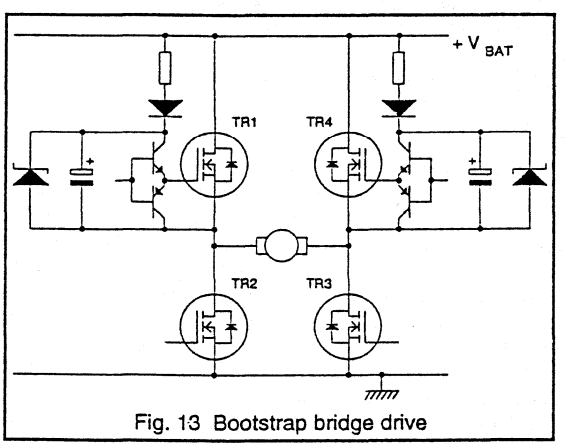


Fig. 13 Bootstrap bridge drive

- **N-channel switches.** To ensure that these are fully turned on, the gate must be driven 10 V higher than the positive supply for conventional MOSFETs or 5 V higher for Logic Level types. This higher voltage might be derived from an auxiliary supply, but the cost of 'bussing' this around the vehicle is considerable.

The additional drive can be obtained locally from a charge pump, an example in shown in Fig. 12. An oscillator (e.g Philips AU7555D) free runs to generate a rectangular 12 V waveform, typically at around 100kHz. A voltage doubler then raises this to around twice the battery voltage. This arrangement is equally suitable for 'DC' or chopper drives.

An alternative approach for H bridge choppers is to use the MOSFETs themselves to generate the drive voltage with a bootstrap circuit as shown in Fig. 13. This circuit works well over a range of mark-space ratios from 5% to 95%. Zener diodes should be used in this circuit to limit the transients that may be introduced onto the auxiliary line.

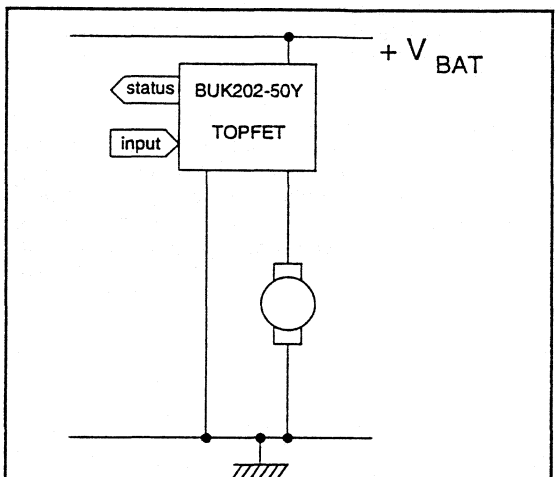


Fig. 14 High Side TOPFET

High Side TOPFET

The ideal high side switch to drive motor loads would be one which could be switched on and off by a ground referenced logic signal, is fully self-protected against short circuit motors and over temperatures and is capable of reporting on the load status to a central controller.

The Philips response to these requirements is a range of high side TOPFETs. The range contains devices with $R_{DS(ON)}$ from 38 to 220 mΩ, with and without internal ground resistors. All the devices feature on board charge pump and level shifting, short circuit and thermal protection and status reporting of such conditions as open or short circuit load. As can be seen in Fig. 14, the use of a TOPFET makes the circuit for a protected high side drive for a motor very simple.

Currents in motor circuits

There are 5 classes of current that can flow in a motor circuit:-

- **nominal** - this is the maximum steady state current that will flow when the motor is performing its function under normal conditions. It is characterised by its relatively low level and its long duration.

- **overload** - this is the current which flows when the motor is driving a load greater than it is capable of driving continuously, but is still performing its function i.e not stalled. This is not necessarily a fault condition - some applications where the motor is used infrequently and for only a short time, use a smaller motor, than would be needed for continuous operation, and over-run it. In these cases the nominal current is often the overload current. Overload currents tend to be about twice the nominal current and have a duration between 5 and 60 seconds.

- **inrush** - or starting currents are typical 5 to 8 times the nominal current and have a duration of around 100 ms, see Fig. 15. The starting torque of a motor is governed by this current so if high torque is required then the control circuit must not restrict the current. Conversely if starting torque is not critical, then current limiting techniques can be employed which will allow smaller devices to be used and permit sensitive fault thresholds to be used.

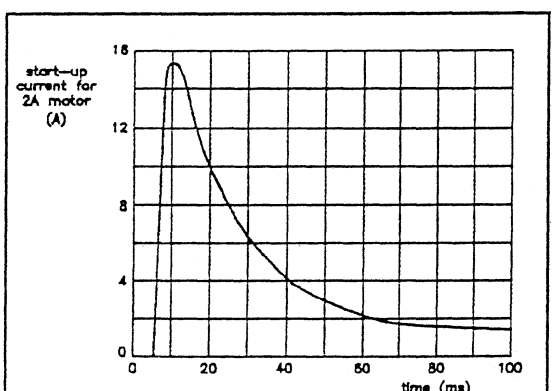


Fig. 15 Start-up Current in 2 A Motor

- **stall** - if the motor cannot turn then the current is limited only by the series resistance of the motor windings and the switch. In this case, a current of 5-8 times the running current can flow through the combination. Fig. 16 shows the current that flows through a stalled 2 A motor - the current gradually falls as the temperature, and consequently the resistance, of the motor and the MOSFET rises.

- **short circuit** - if the motor is shorted out then the current is limited only by the resistance of the switch and the wiring. The normal protection method, in this case, is a fuse. Unless other current control methods are used then it is the I^2t rating of the fuse which determines how long the current will flow.

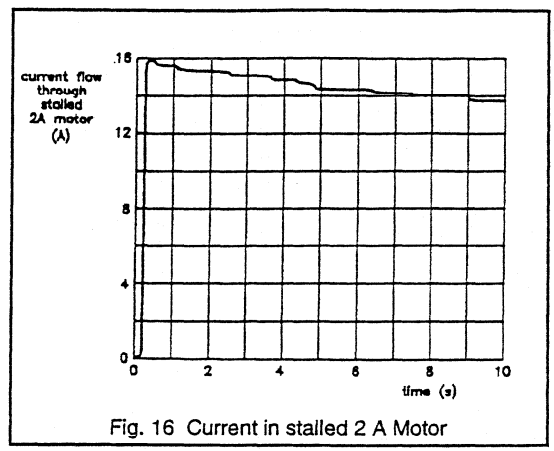


Fig. 16 Current in stalled 2 A Motor

It is important that the devices, selected for the control circuit, can operate reliably with all of these currents. With some types of switching device, it is necessary to select on the basis of the absolute maximum current alone. Often this results in a large and expensive device being used. The characteristics of MOSFETs, in particular their thermally limited SOAR (no second breakdown), allows the designer to specify a much smaller device whose performance more closely matches the needs of the circuit.

Device requirements

Voltage

The highest voltage encountered under normal operation is 16 V, under jump start this can rise to 22 V. In the case where the battery becomes disconnected with the alternator running the voltage can rise to 50 V (assuming external protection is present) or 60 V in the case of 24 V vehicles see Table 2. Thus the normal voltage requirement is 50/60v, however the power supply rail in a vehicle is particularly noisy. The switching of the numerous inductive loads generates local voltage spikes and surges of both polarities. These can occur singly or in bursts, have magnitudes of 100 V or more and durations of the order of 1ms.

It is important to chose MOSFETs capable of withstanding these stresses, either by ensuring V_{DS} exceeds the value of the transients or by selecting 50/60 V devices with sufficient avalanche energy capability to absorb the pulse. For transients in excess of these values it is necessary to provide external protection.

However, the TOPFET range of devices, both low and high side, have overvoltage protection on chip. As a consequence they are rated to withstand very much higher transient energies.

Voltage Range	Cause
>50 (60)*	coupling of spurious spikes
30 to 50	clamped load dump
22 to 30	voltage surge on cut-off of inductive loads
16 to 22 (32 to 40)*	jump start or regulator degraded
10.5 to 16 (20 to 32)*	normal operating condition
8 to 10.5	alternator degraded
6 to 8 (9 to 12)*	starting a petrol engine
0 to 6 (0 to 6)*	starting a diesel engine
negative	negative peaks or reverse connected battery

* 24 V supply

Table 2 Conditions Affecting Abnormal Supply Voltages

Temperature

The ambient temperature requirement in the passenger compartment is -40 to +85°C , and -40 to +125°C under the bonnet. All Philips MOSFETs shown in Table 1 have T_{jmax} = 175°C.

The TOPFETs have a maximum operating T_j of 150°C because above this temperature the on chip protection circuits may react and turn the device off. This prevents the device from damage that could result from over dissipation. This protection eases the problems of the thermal design by reducing the need for large safety margins.

L²FETs

The supply voltage in an automobile derived from the battery is only 12 V (nominal). This can vary from 10.5 V to 16 V under normal operation. It is important that the MOSFET switches be fully turned on under these conditions, not forgetting that for high side switches it may be necessary to derive the gate drive from a charge pump or bootstrap.

Whilst a gate source voltage of 6 V is usually sufficient to turn a conventional MOSFET on, to achieve the lowest on resistance, 10 V is required. Thus the margin between available and required gate drive voltage may be quite tight in automotive drive applications.

One way to ease the problem is to use Logic Level MOSFETs (L²FET), such as the BUK553-60A or BUK555-60A, which achieve a very low on resistance state with only 5 V gate-source.

Conclusions

There is an increasing demand for low cost, reliable electronic switching of motors in automobiles. Despite the wide variety of motor types and drive configurations there is a Philips Power MOSFET solution to all of these demands. The broad range of types includes standard and logic level FETs, FredFETs, high and low side TOPFETs. The combination of low on-state resistance, ease of drive and ruggedness makes them an attractive choice in the arduous automotive environment.

Automotive lamp control with Philips MOSFETs

Application report

The modern motor vehicle, with its many features, is a complex electrical system. The safe and efficient operation of this system calls for sophisticated electronic control. A significant part of any control system is the device which switches the power to the load. It is important that the right type of device is chosen for this job because it can have a major influence on the overall system cost and effectiveness. This choice should be influenced by the nature of the load. This article will discuss the features of the various types of switching device - both mechanical and solid state. These factors will be put into the context of the needs of a device for the control of resistive loads like lamps and heaters. It will be shown that solid state devices allow the designer a greater degree of control than mechanical switches and that the features of Power MOSFETs make them well suited to use in automotive applications.

Choice of switch type

Mechanical or solid-state

Designers of automotive systems now have the choice of either mechanical or solid-state switches. Although mechanical switches can prove be a cheap solution they do have their limitations. Solid-state switches overcome these limitations and provide the designer with several useful additional features.

Areas where the limitations of relays become apparent include:-

- **Reliability** - to achieve the required levels of sensitivity and efficiency means that relay coils have to be wound with many turns of very fine wire. This wire is susceptible to damage under conditions of high mechanical stress - vibration and shock.
- **Mounting** - special assembly techniques are needed when dealing with automotive relays. Their outlines are not compatible with the common methods of automated assembly like auto insertion and surface mounting.
- **Dissipation** - the power loss in the coil of a relay is not negligible - the resulting temperature rise makes it unwise to mount other components in close proximity. In some multiple relay applications it is necessary to provide cooling by ventilation.
- **Temperature** - the maximum operating temperature of relays is typically in the range 70°C - 85°C.
- **Corrosion** - the unsealed mechanism of relays are vulnerable in contaminating and corrosive environments.
- **Overloads** - relays can also prove to be unreliable under high transient load conditions. The arcing which occurs when switching high currents and voltages causes contact wear leading eventually to high resistance or even the contacts welding together.
- **Hazardous Materials** - to achieve the prefered switching performance, relays need to use materials like cadmium. The use of such materials is becoming restricted by legislation on health and safety grounds.
- **Noise** - the operation of a relay is not silent. This is proving to be unacceptably intrusive when relays are sited in the passenger compartment.

Solid-state switches can overcome these limitations but can also give the designer the option of introducing the following useful features:-

- **Current limiting** - a relay has two states - on or off so the current which flows depends only on the load. There is no mechanism which allows a relay to regulate the current which flows through it. The best that a relay can do is to try and turn off, when a high current is detected, but because they are so slow, very large currents may be flowing before the relay can react and damage may have already been caused. However the characteristics of solid state devices like MOSFETs and bipolar transistors allow them to control the current. This allows designers the chance to introduce systems which can handle faults in a safe and controlled manner.
- **Control of switching rate** - the lack control that a relay has over the current proves to be a limitation not only during fault conditions but also during normal switching. Without control, the rate at which current changes, dI/dt, depends only on the external circuit and extremely high rates can result. The combination of high dI/dt and the contact bounce that relays are prone to, creates an 'electrically' noisy environment for surrounding systems. The control available with solid-state switches permits the designer to restrain the current and produce 'soft' switching eliminating any possible EMC problems.

Power MOSFET or Bipolar Transistor

All solid-state switches have significant advantages over relays but there are different types of solid-state switch and their particular characteristics need to be taken into account if an optimum choice is to be made. There are two major types of solid-state switches which are suitable for use in automotive applications - power MOSFETs and bipolar transistors - and several factors need to be considered if the optimum choice is to be made.

- **Overload** - The choice of device type can be influenced by the magnitude and duration of overload currents associated with the application - for example the inrush current of lamps. This factor is particularly important because the maximum current that can be safely conducted by a bipolar transistor is independent of its duration. Whereas the safe operating area of a MOSFET allows it to handle short duration currents very much greater than its DC rating.
- **Drive power** - There can be a significant difference between the total power needed to drive bipolar and MOS transistors. A MOSFET's oxide insulation makes it a voltage controlled device whereas a bipolar needs current drive. However, most control circuits are voltage rather than current orientated and the conversion to current operation often involves the used of loss inducing resistors.
- **Reverse protection** - If the switching device is required to survive reverse conduction conditions then it is necessary to have a diode, connected in anti parallel, around it. If the device is a bipolar transistor then an extra component will be needed. However the device is a MOSFET then it has an inherent body / drain diode which will perform this function without the additional expenditure in components or board space.

Logic level and standard mosfets

The battery voltage in a car is a nominal 12 V. This can vary from 10.5 V to 16 V under normal operation and can fall as low as 6 V during starting. It is important that MOSFET switches be fully turned on at these voltages, bearing in mind that for a high-side switches it may be necessary to derive the gate voltage from a charge pump circuit. While a V_{GS} of 6 V is usually sufficient to turn a standard MOSFET on, 10 V is required to achieve the lowest on-state resistance, $R_{DS(ON)}$. Thus the margin between available and required gate drive voltage may be quite tight in automotive drive applications. One way to overcome this problem is to use L^2FETs such as the BUK553-60A or BUK555-60A, which achieve a very low $R_{DS(ON)}$ with a V_{GS} of only 5 V.

Switch configuration

A load's control circuit can be sited in either its positive or negative feeds. These are referred to as high side and low side switching respectively. Which configuration is chosen often depends on the location of the load/switch and the wiring scheme of the vehicle but other factors like safety can be overriding. The use of semiconductor switches introduces another element into the decision process because of the need to ensure that they are being driven correctly.

Low Side Switch

In this arrangement the load is permanently connected (perhaps via a fuse and the ignition switch) to the positive supply. The switching device is connected between the negative terminal of the load and the vehicle ground. This, together with the almost universal practice of referencing control signals to the vehicle ground, makes the implementation of a low side switch with MOSFETs extremely simple. The circuit shown in Fig. 1 shows a MOSFET connected as a low side switch to a lamp load. The Source terminal of the MOSFET is connected to ground so the control signal, which is also referenced to ground, can be connected to the Gate.

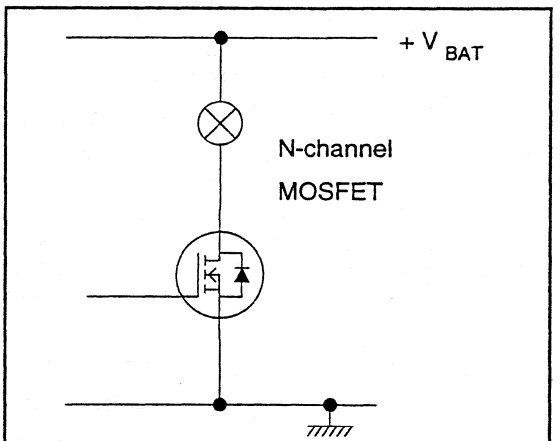


Fig. 1 Low side switch with N-channel MOSFET

High Side Drivers

Often, however, there is a requirement for the switch to be connected to the positive battery terminal with the load connected via the common chassis to the negative. This arrangement reduces electrochemical corrosion and the risk of accidentally activating the device during maintenance.

One method of creating such a high side switch is to use P-channel rather than N-channel MOSFETs. A typical arrangement is shown in Fig. 2. In this the source is connected to the +ve feed and the drain to the load. The MOSFET can be turned ON by taking the control line to zero and it will be OFF when the gate is at +ve supply voltage. Unfortunately P-channel MOSFETs require almost three times the silicon area to achieve the same low on-state resistance as N-channel types and so are much more expensive. An additional problem is the difficulty of obtaining P-channel devices with low enough gate threshold voltage to operate reliably at low battery voltages.

Automotive lamp control with Philips MOSFETs

Application report

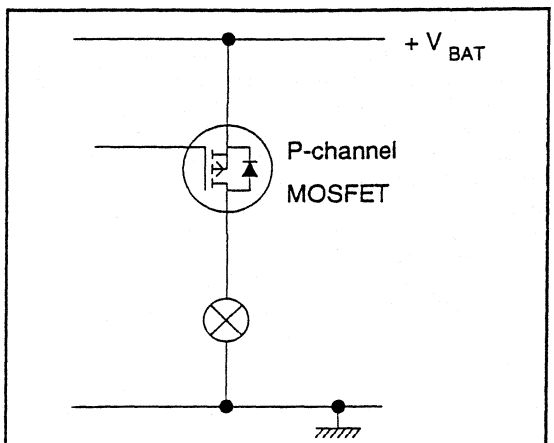


Fig. 2 P-channel high side switch.

Using N-channel devices overcomes these problems but involves a more complicated drive circuit.

To ensure that a n-channel MOSFET is fully turned on, the gate must be driven 10 V higher than its source, for conventional MOSFETs, or 5 V higher for Logic Level (L^2) FETs. With the source connected to the load and with most of the supply being dropped across the it, the gate has to taken to a voltage higher than the supply voltage. This higher voltage might be derived from an auxiliary supply, but the cost of 'bussing' this around the vehicle would be high. Figure 3 shows how this auxiliary supply could be produced locally. It consists of an oscillator - based around the Philips AU7555D - running at approximately 100 kHz which is driving a charge pump which nearly doubles the supply voltage.

An alternative approach, which can be used when the device doesn't have to be continuously ON, for example PWM lamp dimming or lamp flashing, is shown in Fig. 4. In this bootstrap arrangement capacitor C is charged to the supply voltage when the MOSFET is OFF. When the MOSFET is turned ON, its source terminal, and the negative end of C, rises to the supply voltage. The potential of the positive end of C is now higher than the +ve supply and diode D is reverse biased preventing C from being discharged. C can now act as the high voltage supply for the gate. The inevitable leakages will tend to discharge C and hence reduce the gate/source voltage, but with good components it is easy to ensure that a voltage high enough to keep the MOSFET fully ON is available for several seconds.

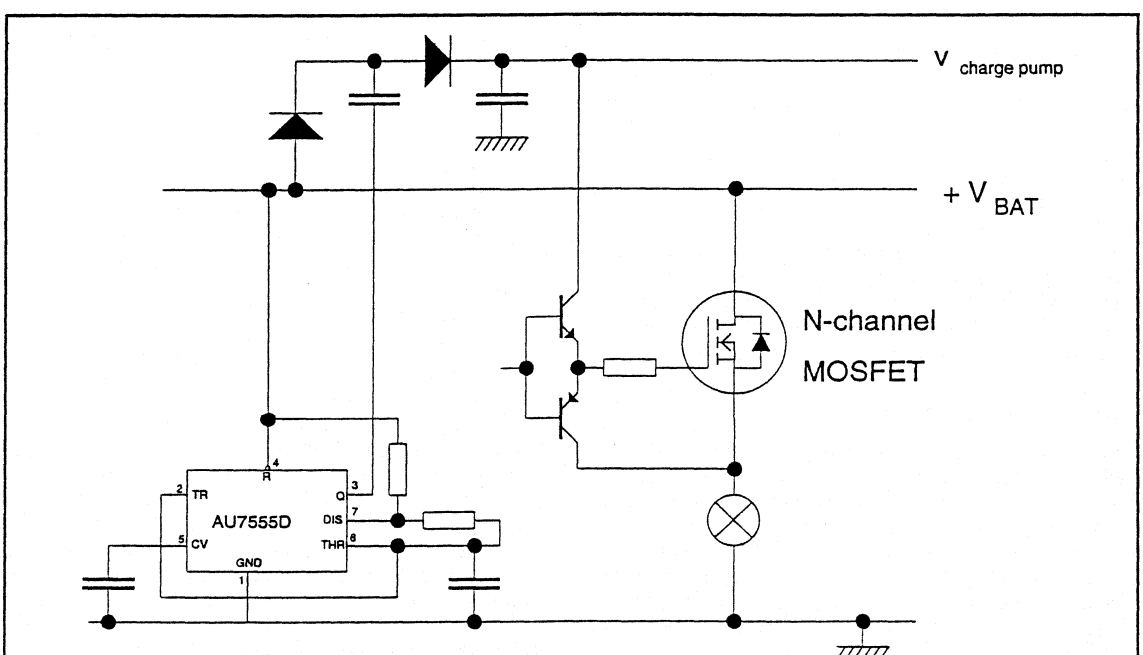


Fig. 3 N-channel High-side switch with charge pump

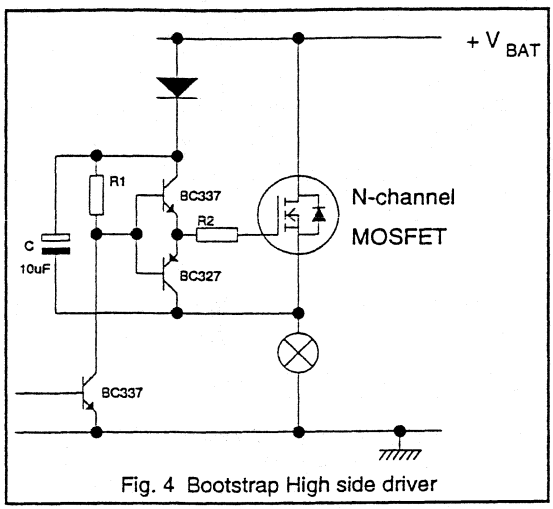


Fig. 4 Bootstrap High side driver

Inrush current

Any circuit or device which is intended to drive either a lamp or a heater must be able to handle not only the normal running current but also the inrush current at start up. All lamps and many heaters are essentially resistors made from metal conductors whose resistivity will increase with temperature.

In the case of lamps, the extremely high operating temperature (3000 K) means that the hot to cold resistance ratio is large. Typical values for a 60 W headlamp bulb are:-

	filament resistance	current
cold (-40°C)	0.17 Ω	70 A
hot	2.4 Ω	5 A

The figures given for the currents assume that there is 12 V across the lamp, in practice wiring and switch resistance will reduce the cold current somewhat, but the ratio will still be large. The actual ratio depends upon the size and construction of the lamp but figures between 10 and 14 are common. For safety, the higher figure should be used.

The low thermal mass and the high power dissipation (850 W peak in 60W lamp) means that the lamp heats up very quickly. This means that the current falls from its peak value equally quickly. The time it takes for the current to fall back to its normal value depends on the size and construction of the lamp - the larger the lamp the longer it will take to heat up. Typically the current will have an exponentially decay with a time constant of 1 - 10 ms. The waveforms in Fig. 5 show the typical inrush current for a 60 W lamp being switched on by a MOSFET. The initial temperature of the lamp filament was 25°C.

The normal operating temperature of a heater is not as high as that of a lamp, so the inrush current is rarely greater than twice the nominal current and often less. The duration of the 'inrush' can, however, last for many minutes and it may be this current which is used to define the 'normal' operating condition.

Being essentially resistive, lamps and heaters have very low inductance. This means that the current in the load will rise as quickly as the rest of the wiring will let it. This can lead to serious interference problems.

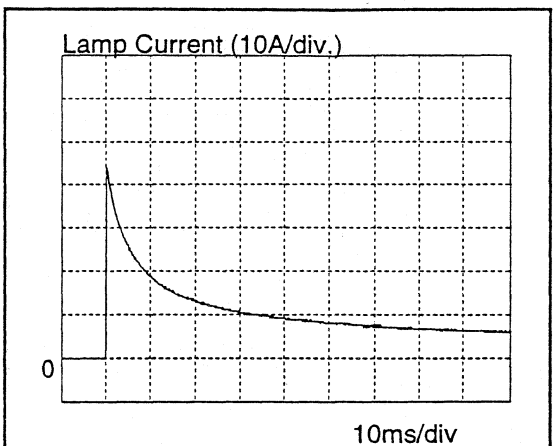


Fig. 5 Current in 60 W lamp during start up

Switch rate

The inductance associated with the supply wires in a car, is not negligible - a figure of 5µH is often quoted. This inductance, combined with the high rates of change of current associated with the switching of resistive loads and lamps, results in transient voltage appearing on the supply leads. The magnitude of the transient is given by:-

$$V_{transient} = -L.\frac{dI}{dt}$$

For example a current which rises as slowly as 2 A/µs will cause a 10 V dip in the supply to the switching circuit. This effect can be clearly seen in the waveforms of Fig. 6a. Such a perturbation can have an effect in two ways. In the first case the control circuit may be upset by having its supply reduced to only 2 V and may, if not specifically designed to cope with it, fail to function correctly. In the second case, it is easy for a transient as large as this, with its significant high frequency content, to be transmitted into adjacent conductors in the wiring loom. If some of the conductors are signal wires then false triggering of other functions could result.

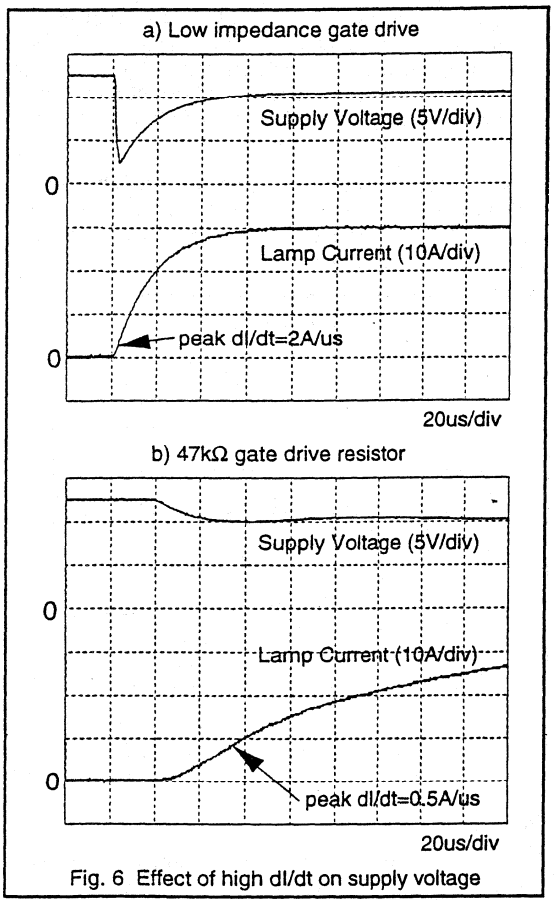


Fig. 6 Effect of high dI/dt on supply voltage

The dip will be reduced to manageable proportions if the dI/dt can be held to 0.5 A/µs. Since the loads are resistive, achieving this means reducing the rate that the voltage is applied to the load. This type of 'soft' starting is relatively easy to implement when the controlling device is a Power MOSFET. All that is needed is to put resistance in series with the gate drive.

The plots shown in Fig. 6b illustrate the effect inserting 47 kΩ in series with the gate supply of a BUK455-60A. The load for these tests was a 60W lamp being supplied from a battery via a 5 µH inductor. The dip in voltage due to dI/dt is now lost in the voltage drop from the wiring resistance.

The rate at which current falls at turn off is also important. High negative dI/dt will result in a large positive spike on the supply rails. As with the negative dip, this spike could cause interference in adjacent wires but it could also cause overvoltage damage. Unlike the turn on dip which can never be greater than 12 V, the magnitude of the turn off spike is potentially unlimited. In practice, however, it is extremely

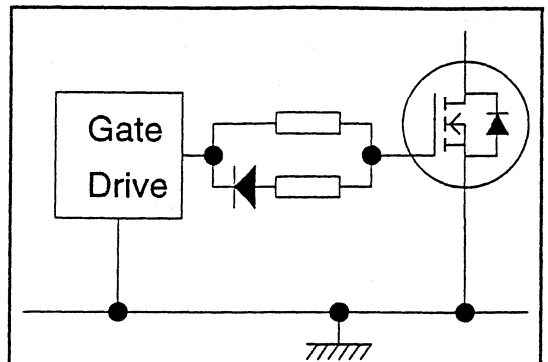


Fig. 7 Gate supply networks for switching rate control

unlikely that the voltage would exceed 30 V. Transient voltages of this magnitude are relatively common in the automotive environment and all circuits should be able to withstand them. It is still worthwhile keeping the turn off transient under control by ensuring that the dI/dt is low enough - a figure of <1 A/µs is standard.

Soft turn off, like soft turn on, is easy to implement if the controlling device is a Power MOSFET. In fact the same series resistor can be used to limit both the turn on and turn off rates. With a lamp load, however, this method will give a much slower turn off than is really necessary because of the large difference between the current at turn on and turn off. If this is a problem then an additional resistor and diode put in parallel with the first resistor - see Fig. 7 - will speed up the turn off.

MOSFET selection

The type of device chosen for a particular application depends upon the features that the control circuit needs to have. Table 3 lists the available MOSFET types and some of their features that would be useful in automotive applications.

Having chosen the type of MOSFET it becomes necessary to decided on the size of device. With MOSFETs this decision is made easier because, in its on-state, a MOSFET can be treated as a resistance and because its safe operating area (SOAR) is set by thermal considerations only (no second breakdown effects). The first stage of the selection process is to chose a device on the basis of the nominal current requirement. The next stage is to check that the inrush current, of the particular application and the drive method used, does not result in the MOSFET exceeding the transient thermal ratings. Having selected a device that is capable of switching the load the designer can then use the quoted values for the on-state resistance ($R_{DS(ON)}$) to check that any on-state voltage drop

requirements are being met. Tables 3 and 4 lists many of the different of lamps and resistive loads found in cars and suggests MOSFET types that can be used to control them.

MOSFET Type	Features
Standard	Wide range of current ratings from 5 to >100 A. Wide range of package styles Fast recovery anti-parallel diode (60 / 100 V types) Extremely fast switching.
L^2FET	as standard + Fully operational with low voltage supply
Low side TOPFET	as L^2FET + overvoltage protection overload protection over temperature protection 3 and 5 pin versions linear and switching control
High side TOPFET	Single component providing:- high side switch (on chip charge pump and level shifting) device protection load protection status reporting CMOS compatible input

TABLE 1 MOSFET Types and Features

The automotive environment

The environment that circuits and devices can be subjected to in automotive applications can prove to be extremely severe. Knowledge of the conditions that can exist is necessary to ensure that suitable devices and circuits are chosen. The two most stressful aspects of the environment are the temperature and voltage.

Temperature

The lowest temperature that is likely to be reached is -40°C. This is related to the minimum outside temperature and may be lower under some special circumstances. The maximum temperature depends to a great extent upon the siting of circuits. The general ambient temperature in the engine compartment can be quite high and it is reasonable to assume that devices will see temperatures of 125°C. Within the passenger area, conditions are somewhat more benign, but in areas where heat is generated and air flow is restricted, the temperature will be higher than might be expected. For this reason it is necessary to assume that the circuits and devices will have to work in an ambient temperature of 85°C.

Voltage

It is possible to split the voltage conditions that can occur into two groups - Normal and Abnormal. 'Normal' conditions are essentially those which can be present for very long periods of time. Under such conditions it is reasonable to expect devices and circuits to be completely operational and to suffer no ill effects. 'Abnormal' conditions are characterised by their temporary nature. They are not expected to persist for long periods and during them, some loss in device / circuit performance can be expected and, in some cases, is allowable.

Normal voltages

When considering the 'Normal' environment it is important to included both the typical and extreme cases. The crucial condition for most devices and circuits is when the engine is running. At this time the supply voltage can be anywhere between 10.5 and 16 V in '12 V' systems or between 20 and 32 V in '24 V' systems.

The other significant 'normal' operating mode is when engine not running. In this state the supply voltage could be very low but voltages below some level must be considered as a fault condition. However some circuits will have to operate with voltages as low as 6 V.

Voltage Level		Cause
12 V systems	24 V systems	
40 V - 50 V	60 V - 75 V	external spikes
30 V - 40 V	50 V - 60 V	clamped load dump
22 V - 30 V	22 V - 30 V	inductive load switch off
16 V - 22 V	32 V - 40 V	jump start
16 V - 22 V	32 V - 40 V	faulty regulator
8 V - 10.5 V	12 V - 20 V	faulty alternator
6 V - 8 V	9 V - 12 V	starting a petrol engine
0 V - 6 V	0 V - 6 V	starting a diesel engine

Table 2 Abnormal Supply Voltages

Abnormal voltages

It is possible to envisage a situation in which nearly any voltage could appear on the supply wires of a vehicle. How extreme the voltages get depends to a great extent upon the protection, both deliberate and incidental, built into the system. The actual voltage that appears at the terminals of a circuit is also influenced strongly by its location and the location of the protection. Analysis of the automotive environment has produced a list of expected abnormal conditions. The values of voltage that these conditions can be expected to produce are shown in Table 2.

Load	Typical Power	Nominal Current	Peak Inrush Current	Number of lamps /car	Recommended MOSFET[1] Standard FET SOT186	Standard FET TO220	Logic Level FET SOT186	Logic Level FET TO220
headlamp	60 W 55 W 45 W 40 W	5 A 4.6 A 3.8 A 3.3 A	70 A 64 A 53 A 47 A	2	BUK445-60A	BUK455-60A	BUK545-60A	BUK555-60A
spotlight	55 W	4.6 A	64 A	2	BUK445-60A	BUK455-60A	BUK545-60A	BUK555-60A
front fog light	55 W	4.6 A	64 A	2	BUK445-60A	BUK455-60A	BUK545-60A	BUK555-60A
rear fog light	21 W	1.8 A	25 A	2	BUK442-60A BUK443-60A[2]	BUK452-60A BUK453-60A[2]	BUK542-60A BUK543-60A[2]	BUK552-60A BUK553-60A[2]
front sidelight	5 W	0.4 A	6 A	2	BUK441-60A	BUK451-60A	BUK541-60A	BUK551-60A
rear sidelight	5 W 10 W	0.42 A 0.83 A	5.8 A 12 A	2 2	BUK441-60A	BUK451-60A	BUK541-60A	BUK551-60A
brake light	21 W	1.8 A	25 A	2	BUK442-60A BUK443-60A[2]	BUK452-60A BUK453-60A[2]	BUK542-60A BUK543-60A[2]	BUK552-60A BUK553-60A[2]
direction indicator light	21 W	1.8 A	25 A	4	BUK442-60A BUK443-60A[2]	BUK452-60A BUK453-60A[2]	BUK542-60A BUK543-60A[2]	BUK552-60A BUK553-60A[2]
side marker light	3 W 4 W 5 W	0.25 A 0.33 A 0.42 A	3.5 A 4.7 A 5.8 A	4 4 4	BUK441-60A	BUK451-60A	BUK541-60A	BUK551-60A
license plate light	3 W 5 W	0.25 A 0.42 A	3.5 A 5.8 A	2 1	BUK441-60A	BUK451-60A	BUK541-60A	BUK551-60A
reversing / backup light	21 W	1.8 A	25 A	2	BUK442-60A BUK443-60A[2]	BUK452-60A BUK453-60A[2]	BUK542-60A BUK543-60A[2]	BUK552-60A BUK553-60A[2]
instrument panel light	2.2 W	0.18 A	2.5 A	5	BUK441-60A	BUK451-60A	BUK541-60A	BUK551-60A
courtesy light	2.2 W	0.18 A	2.5 A	4	BUK441-60A	BUK451-60A	BUK541-60A	BUK551-60A
door light	2.2 W	0.18 A	2.5 A	4	BUK441-60A	BUK451-60A	BUK541-60A	BUK551-60A
boot / bonnet light	2.2 W	0.18 A	2.5 A	4	BUK441-60A	BUK451-60A	BUK541-60A	BUK551-60A

Notes

[1] These are meant for general guidance only. Specific applications should be checked against individual users' requirements. In addition to standard and logic level MOSFETs, high and low side TOPFETs might also be considered.

[2] This device can be used to control two bulbs simultaneously.

TABLE 3 Automotive lamps - characteristics and recommended MOSFET drivers

Load	Typical Power	Nominal Current	Number /car	Recommended MOSFET[1] TO220	SOT186(A) F-pack	Comments
screen heater	300-600 W	25-50 A	1	2 x BUK556-60H		Devices connected in parallel
seat heater	100-120 W	8-10 A	2	BUK452-60A[2]	BUK442-60A[2]	

Notes

[1] These are meant for general guidance only. Specific applications should be checked against individual users' requirements. In addition to standard MOSFETs, L²FETs, low and high side TOPFETs might also be considered.

[2] To achieve an on-state voltage drop of <1 V the BUKxx3-60A device should be used.

TABLE 4 Automotive Resistive Loads - characteristics and recommended MOSFET drivers

An introduction to the 3-pin TOPFET

Application report

The TOPFET (Temperature and Overload Protected MOSFET) concept has been developed by Philips Semiconductors and is achieved by the addition of a series of dedicated on-chip protection circuits to a low voltage power MOSFET. The resulting device has all the advantages of a conventional power MOSFET (low $R_{DS(on)}$, logic level or standard gate voltage drive) with the additional benefit of integrated protection from hazardous overstress conditions.

TOPFETs are designed for operation in low voltage power applications, particularly automotive electronic systems. The operation and protection features of the TOPFET range of devices also make them suitable for other low voltage power systems. TOPFETs can be used for all common load types currently controlled by conventional power MOSFETs.

The first generation of TOPFET devices are summarised in Table 1.

Protection strategy

A functional block diagram and the circuit symbol of the first generation 3-pin TOPFETs are shown in Fig. 1. The functional block diagram indicates that the logic and protection circuits are supplied directly from the input pin. This places a requirement on the user that the input voltage must be sufficiently high to ensure that the protection circuits are being correctly driven.

The TOPFET includes an internal resistance between the input pin and the power MOSFET gate. This is required to ensure that the protection circuits are supplied even under conditions when the circuits have been activated to turn off the power MOSFET stage. The value of this resistance has been chosen to be a suitable compromise between the requirements of switching speed and drive capability.

Variants of this configuration with differing input resistor values (higher or lower) will be produced to suit different application requirements.

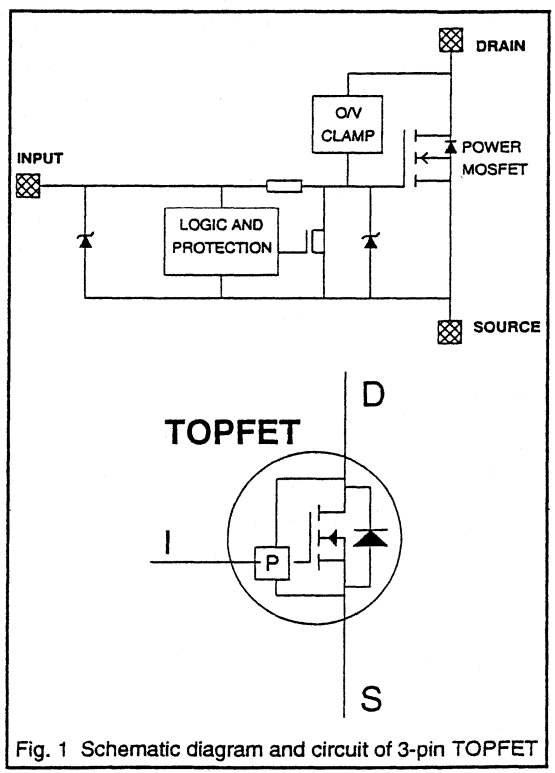


Fig. 1 Schematic diagram and circuit of 3-pin TOPFET

TOPFET	Package	V_{DS} (V)	$R_{DS(ON)}$ (mΩ)	at V_{IS} = (V)
BUK100-50GL	TO220	50	125	5
BUK100-50GS	TO220	50	100	10
BUK101-50GL	TO220	50	60	5
BUK101-50GS	TO220	50	50	10
BUK102-50GL	TO220	50	35	5
BUK102-50GS	TO220	50	28	10

Table 1. 3-pin TOPFET type range

Overtemperature protection

TOPFETs include an on-chip protection circuit which measures the absolute temperature of the device. If the chip temperature rises to a dangerous level then the overtemperature protection circuit operates to turn off the power MOSFET stage. Once tripped, the device remains protected until it is reset via the input pin. In the tripped condition the gate of the power MOSFET stage is pulled down by the control logic and so some current is drawn by the input pin of the TOPFET. If the overtemperature condition persists after the gate has been reset then the protection circuit is reactivated.

Short circuit protection

In the case of short circuit faults the rate of rise of temperature in a MOSFET switch can be very rapid. Guaranteed protection under this type of condition is best achieved using the on-chip protection strategy which is implemented in the TOPFET range of devices. The short circuit protection circuit acts rapidly to protect the device if the temperature of the TOPFET rises excessively.

The TOPFET does not limit the current in the power circuit under normal operation. This ensures that the TOPFET does not affect the operation of circuits where large inrush currents are required. As with the overtemperature protection circuit, the short circuit protection circuit turns off the power MOSFET gate via the control logic and is reset by taking the input pin low.

Overvoltage protection

Transient overvoltage protection is an additional feature of the TOPFET range. This is achieved by a combination of a rugged avalanche breakdown characteristic in the PowerMOS stage and an internal dynamic clamp circuit. Operation is guaranteed by an overvoltage clamping energy rating for the TOPFET. Overvoltage protection gives guarantees against fault conditions in the system as well as the ability for unclamped inductive load turn-off.

ESD protection

The input pin of the TOPFET is protected with an ESD protection zener. This device protects the PowerMOS gate and the TOPFET circuit from ESD transients. The energy in the ESD pulse is dissipated in the ESD source rather than in the TOPFET itself. This input zener diode cannot be used in the continuous breakdown mode and so is the determining factor in setting the maximum allowable TOPFET input voltage.

One feature of the implementation of the protection circuits used in the first generation TOPFET devices is that the input cannot be reverse biased with respect to the source. This must be adhered to at all times. When the TOPFET is in reverse conduction the protection circuits are not active.

Driving TOPFETs

Application report

The output of a TOPFET is similar to that of a Power MOSFET. However, the TOPFET's protection features make the input characteristics significantly different. As a consequence, TOPFETs have different drive requirements. This fact sheet describes these requirements and suggests suitable drivers for the different TOPFET versions.

3-Pin TOPFET

Input requirements

3-pin TOPFETs can replace ordinary MOSFETs in many circuits if the driver can meet certain conditions. The first of these conditions is the need to keep within the TOPFET's V_{IS} ratings and in particular to keep the input positive with respect to the source. The second is the need to provide an adequate supply to the protection circuits even when the TOPFET has tripped and the input current is significantly higher.

Table 1 summarises these requirements. It gives the limiting values of V_{IS}, the minimum input voltage for valid protection in normal and latched mode and the normal and latched input currents for each 3-pin TOPFET.

Drivers

The complementary drive arrangement shown in Fig. 1 is well suited to the input requirements of 3-pin TOPFETs. The transistors shown are the output of a cmos IC gate, which for some TOPFETs may have sufficient drive. If not, a push pull drive with discrete devices should be used. Suitable cmos families are given in Table 1.

The BUK101-50DL has a very low input current requirement, achieved by increasing the value of the internal input resistor - at the expense of a significant increase in switching times. This means that this device can be driven from the output port of an 80C51 micro controller as shown in Fig. 2. Designers should be aware that other high resistance / low current TOPFETs could be produced if they are requested.

5-Pin TOPFET

Input Requirements

The requirements of a 5-pin TOPFET are somewhat different to that of a 3-pin device. The first major difference is that both the input and the protection pins need to be supplied. The second difference is that the input resistance is external and is selected by the designer. One requirement which remains is the need to keep both the input-source and protection-source voltages within the range 0 to 11 V.

The protection pin driver must be able to keep the voltage above V_{PSP} when supplying the protection current, I_{PS}. With the 5-pin device the protection supply is independent, so the current drawn when TOPFET trips does not change.

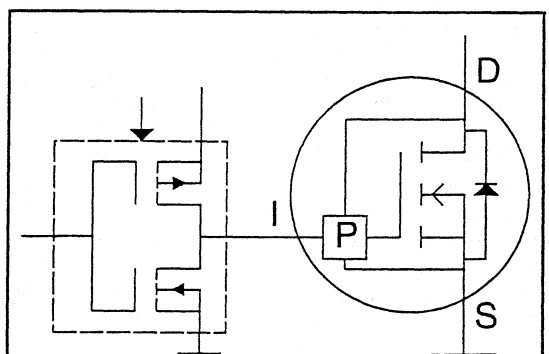


Fig. 1 Complementary driver for 3-pin TOPFET

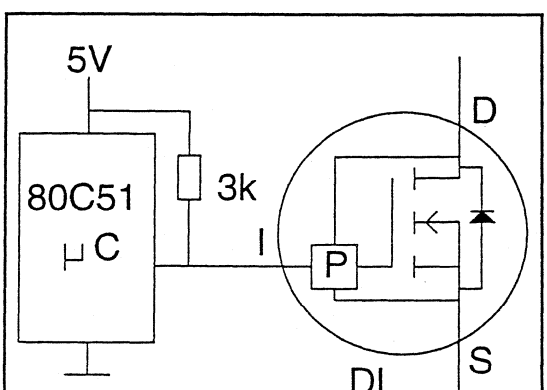


Fig. 2 Micro controller drive for 3-pin TOPFET

Type	Input voltage (V)				Input Current (mA)		Driver
	limiting value		for valid protection				
	min.	max.	normal	latched	normal	latched	
BUK100-50GS	0	11	5	3.5	1.0	5.0	HEF / Discrete
BUK101-50GS	0	11	5	3.5	1.0	4.0	HEF / Discrete
BUK102-50GS	0	11	5	3.5	1.0	20	Discrete
BUK100-50GL	0	6	4	3.5	0.35	2.0	HC/HCT
BUK101-50GL	0	6	4	3.5	0.35	2.0	HC/HCT
BUK102-50GL	0	6	4	3.5	0.35	10	Discrete
BUK101-50DL	0	6	4	3.5	0.35	0.65	Micro

Table 1 Input parameters of 3-pin TOPFETs

The input pin requirements depend on the mode of operation chosen by the designer. If the TOPFET is expected to turn itself off, in overtemperature or shorted load situations, then the output impedance of the drive needs to be > 2 kΩ. This will allow the TOPFET's internal turn-off transistor to pull the input pin low. If, however, the circuit uses the TOPFET flag to signal to the driver to turn off, then driver resistance can be very much lower.

Independent of which method is used for overload turn-off, there is a separate requirement to ensure adequate overvoltage clamping. If this feature is needed then the input to source resistance of the driver - when it is pulling the input low - needs to be > 100 Ω. If it is lower, then the TOPFET's internal clamping drive will be unable to raise the gate voltage high enough to turn the MOSFET on.

Drives

The drive for the protection pin can, most conveniently, be supplied by a cmos IC gate. A 74HC or HCT for L type devices or a HEF4000 series device for the S type. Care is needed however to ensure that the minimum protection voltage, V_{PSP}, requirements are still met when the input voltage, V_{IS} is high and the load is shorted.

A typical high impedance drive arrangement, which lets TOPFET protect itself against shorted load, overtemperature and overvoltage, is shown in Fig. 3.

One method of creating a fast drive is shown in Fig. 4. In this arrangement a NOR gate with a low impedance output stage drives the input via a 100 Ω resistor. One input of the NOR gate is connected to the flag pin and will be pulled high by the 10 kΩ pull-up resistor if the TOPFET indicates a fault. With one input high, the output of the gate will be low turning the TOPFET off. The 100 Ω resistor ensures that the overvoltage clamp is still operational.

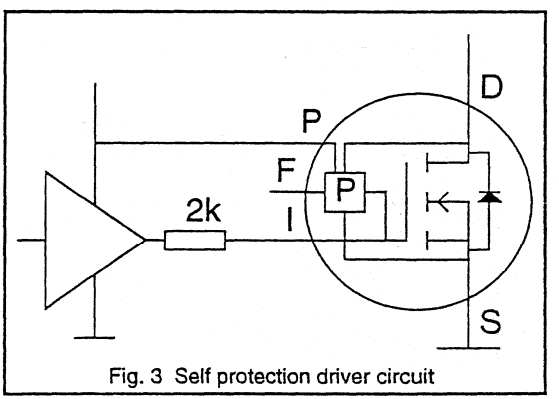


Fig. 3 Self protection driver circuit

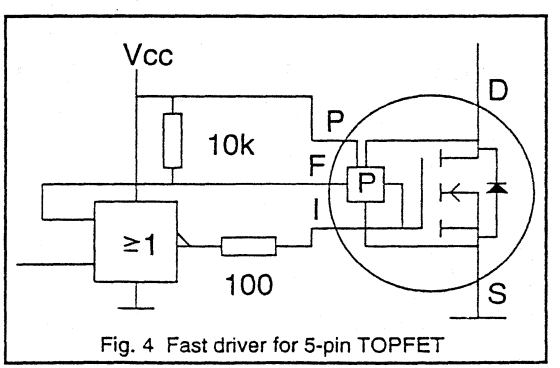


Fig. 4 Fast driver for 5-pin TOPFET

PowerMOS transistor
Logic level TOPFET

BUK100-50DL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Lower operating input current permits direct drive by micro-controller
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MAX.	UNIT
V_{DS}	Continuous drain source voltage		50	V
I_D	Continuous drain current		13.5	A
P_D	Total power dissipation		40	W
T_j	Continuous junction temperature		150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		125	mΩ
I_{ISL}	Input supply current	V_{IS} = 5 V	650	µA

FUNCTIONAL BLOCK DIAGRAM

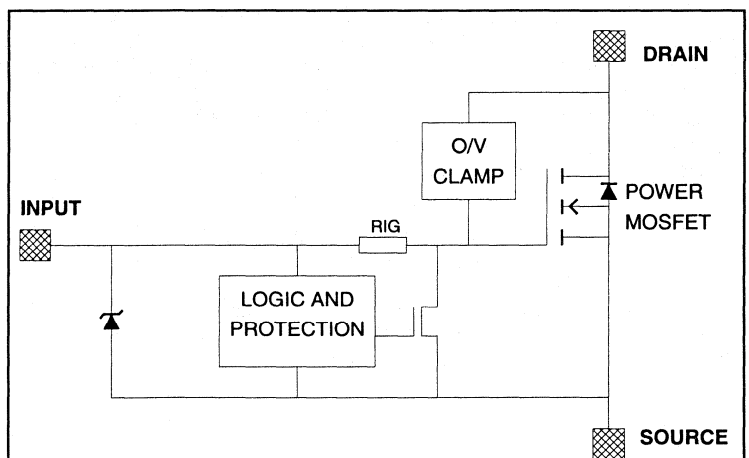
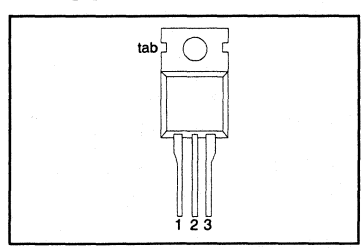


Fig.1. Elements of the TOPFET.

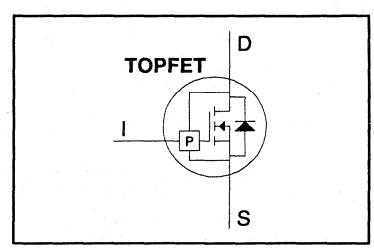
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	13.5	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; $V_{IS} = 5$ V	-	8.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	54	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	40	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 5$ V	-	50	V
	Short circuit load protection[4]				
$V_{DDP(P)}$	Protected drain source supply voltage[5]	$V_{IS} = 5$ V	-	24	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25$ °C	-	0.6	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0$ V	-	15	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; $I_{DM} = 15$ A; $V_{DD} \leq 20$ V; inductive load	-	200	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; $I_{DM} = 8$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

5 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than $V_{DDP(P)}$ maximum.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[1]	V_{IS} = 5 V; I_{DM} = 7.5 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	85	125	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[2]	T_{mb} = 25 °C; L ≤ 10 µH; R_L = 10 mΩ				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.2	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
$I_{D(SC)}$	Drain current[3]	V_{DD} = 13 V; V_{IS} = 5 V	-	25	-	A
$I_{DM(SC)}$	Peak drain current[4]	V_{IS} = 5 V; V_{DD} = 13 V	-	60	-	A
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 1$ A[5]	150	-	-	°C

TRANSFER CHARACTERISTIC

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 7.5 A $t_p \leq 300$ µs; $\delta \leq 0.01$	5	9	-	S

1 Continuous input voltage. The specified pulse width is for the drain current.

2 Refer to OVERLOAD PROTECTION LIMITING VALUES.

3 Continuous drain-source supply voltage. Pulsed input voltage.

4 Continuous input voltage. Momentary short circuit load connection. (The higher peak current is due to the effect of capacitance Cgd).

5 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	100	200	350	µA
			V_{IS} = 4 V	-	160	270	µA
V_{ISR}	Protection reset voltage[1]		T_j = 25 °C	2.0	2.6	3.5	V
			T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	330	650	µA
			V_{IS} = 3.5 V	-	240	430	µA
$V_{(BR)IS}$	Input breakdown voltage	I_I = 10 mA		6	-	-	V
R_{IG}	Input series resistance		T_j = 25 °C	-	33	-	kΩ
	to gate of power MOSFET		T_j = 150 °C	-	50	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	8	-	µs
t_r	Rise time	resistive load R_L = 4 Ω	-	40	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	40	-	µs
t_f	Fall time	resistive load R_L = 4 Ω	-	35	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	15	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDO}	Forward voltage	I_S = 15 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

1 The input voltage below which the overload protection circuits will be reset.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

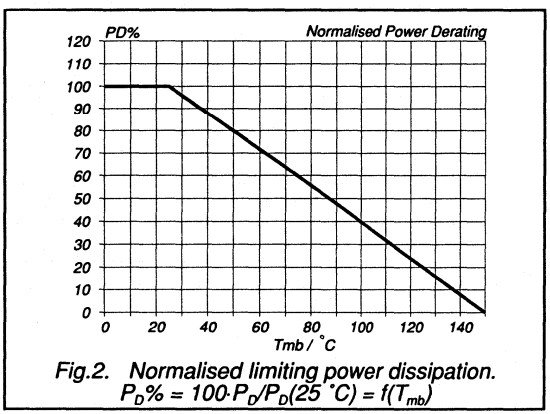


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

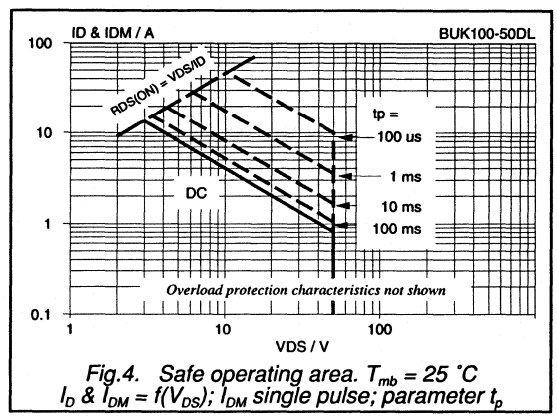


Fig.4. Safe operating area. T_{mb} = 25 °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

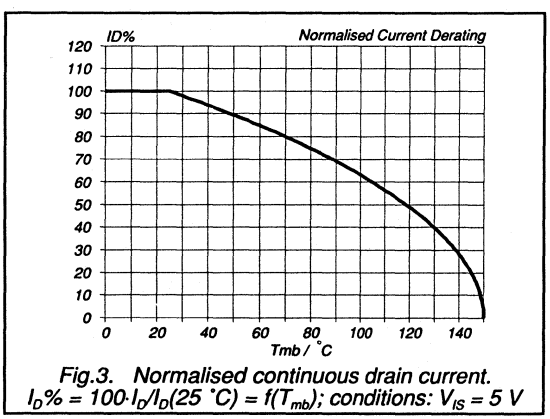


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: V_{IS} = 5 V

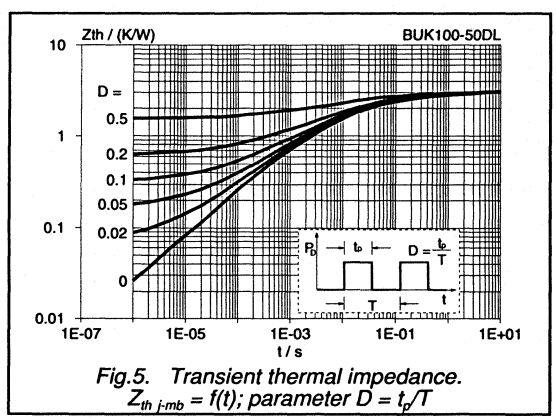


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

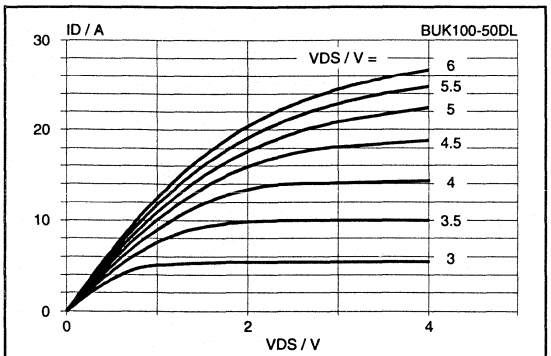


Fig.6. Typical on-state characteristics, T_j = 25 °C. ID = f(V_{DS}); parameter V_{IS}; t_p = 2 ms

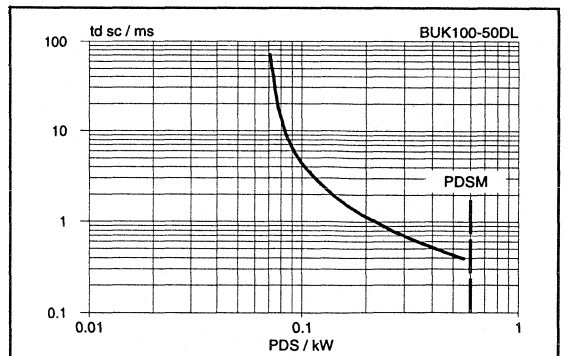


Fig.9. Typical overload protection characteristics. $t_{d\,sc}$ = f(P_{DS}); conditions: $V_{IS} \geq$ 4 V; T_j = 25 °C.

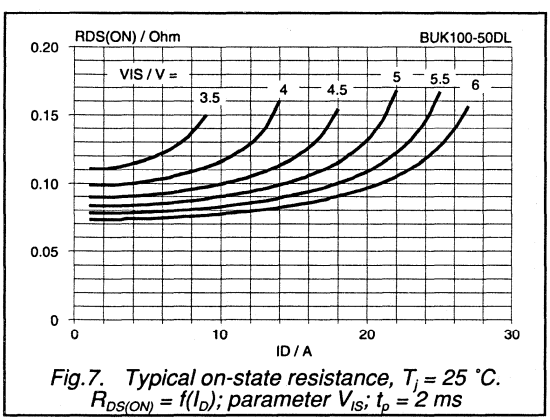


Fig.7. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)}$ = f(I_D); parameter V_{IS}; t_p = 2 ms

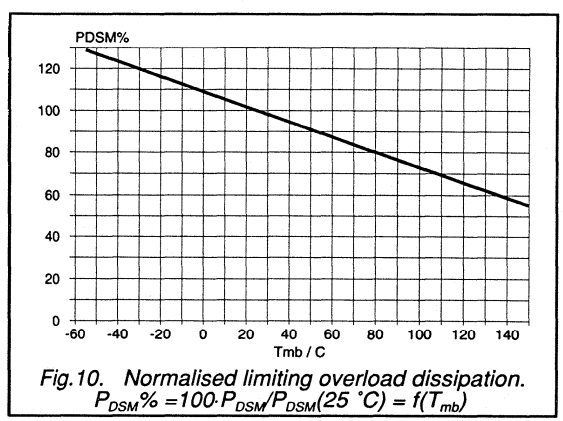


Fig.10. Normalised limiting overload dissipation. P_{DSM}% =100·P_{DSM}/P_{DSM}(25 °C) = f(T_{mb})

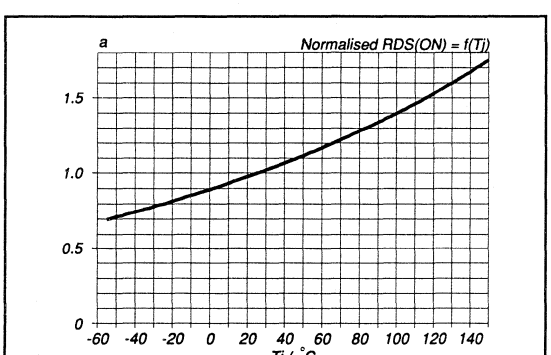


Fig.8. Normalised drain-source on-state resistance. a = $R_{DS(ON)}$/$R_{DS(ON)}$25 °C = f(T_j); I_D = 13 A; V_{IS} = 5 V

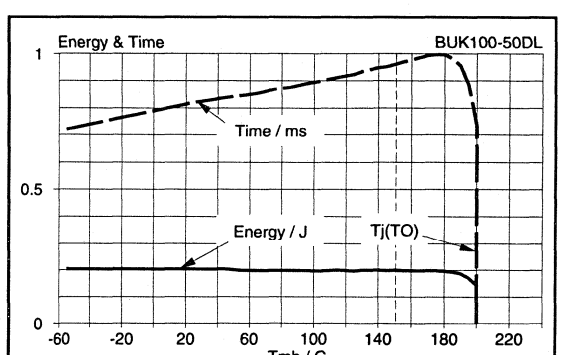


Fig.11. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

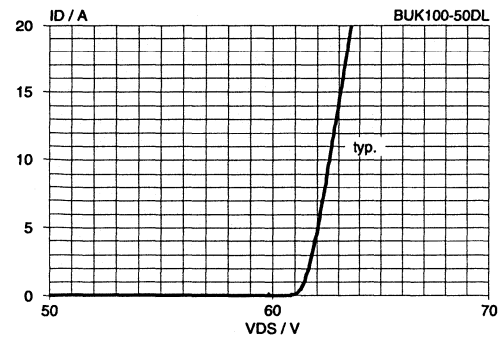


Fig.12. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50$ µs

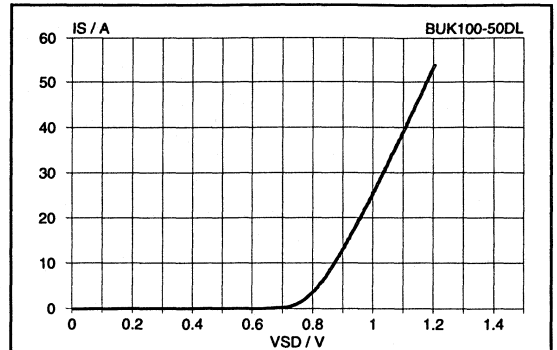


Fig.15. Typical reverse diode current, $T_j = 25$ °C. $I_S = f(V_{SDS})$; conditions: $V_{IS} = 0$ V; $t_p = 250$ µs

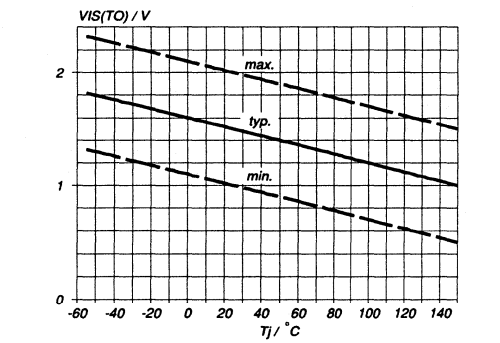


Fig.13. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

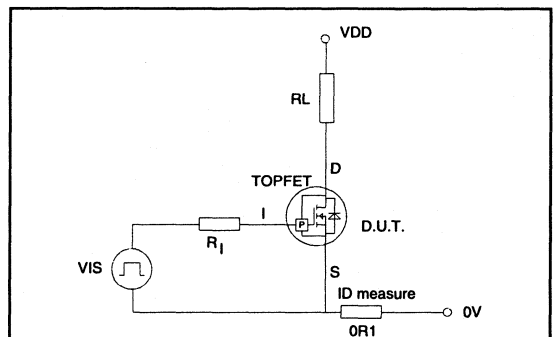


Fig.16. Test circuit for resistive load switching times.

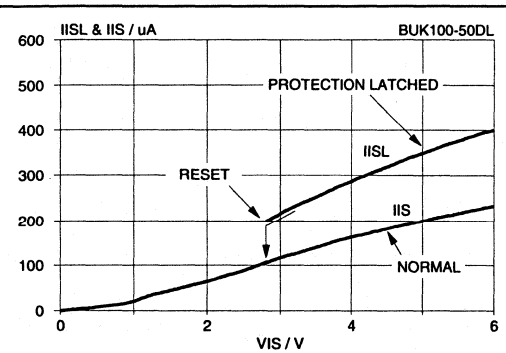


Fig.14. Typical DC input characteristics, $T_j = 25$ °C. I_{ISL} & $I_{IS} = f(V_{IS})$; protection latched & normal operation

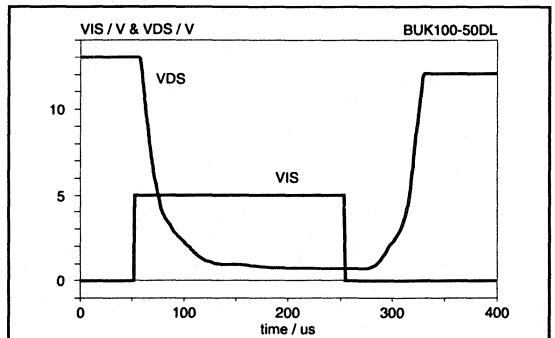


Fig.17. Typical switching waveforms, resistive load. $V_{DD} = 13$ V; $R_L = 4\ \Omega$; $R_I = 50\ \Omega$, $T_j = 25$ °C.

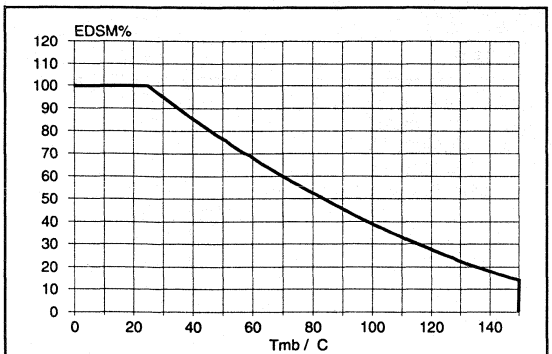


Fig.18. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 15 A; V_{IS} = 5 V

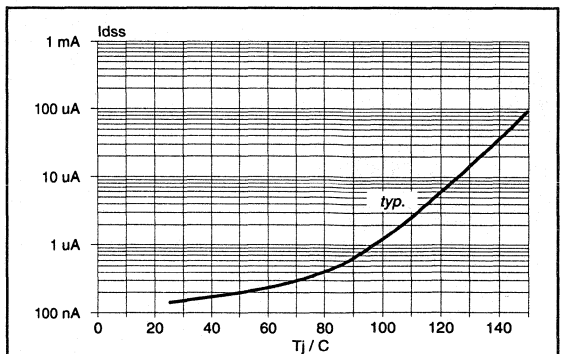


Fig.20. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

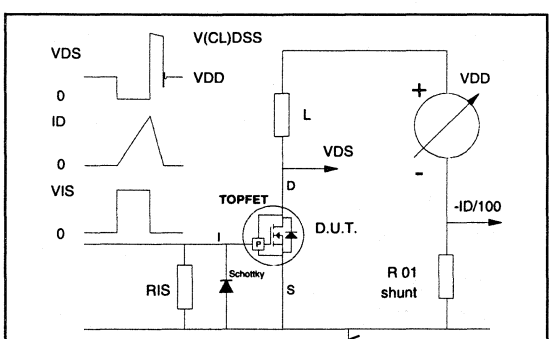


Fig.19. Clamping energy test circuit, R_{IS} = 50 Ω.
$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

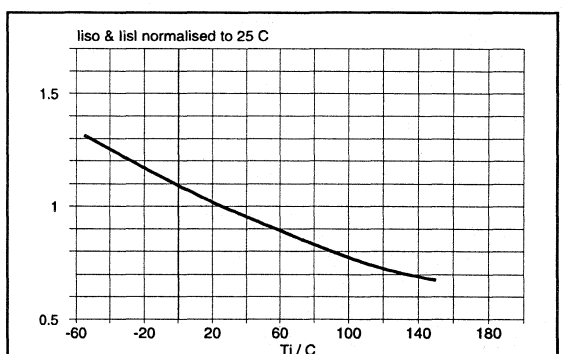


Fig.21. Normalised input currents (normal & latched). $I_{ISO}/I_{ISO}25°C$ & $I_{ISL}/I_{ISL}25°C = f(T_j)$; V_{IS} = 5 V

PowerMOS transistor Logic level TOPFET

BUK100-50GL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	13.5	A
P_D	Total power dissipation	40	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 5 V	125	mΩ

FUNCTIONAL BLOCK DIAGRAM

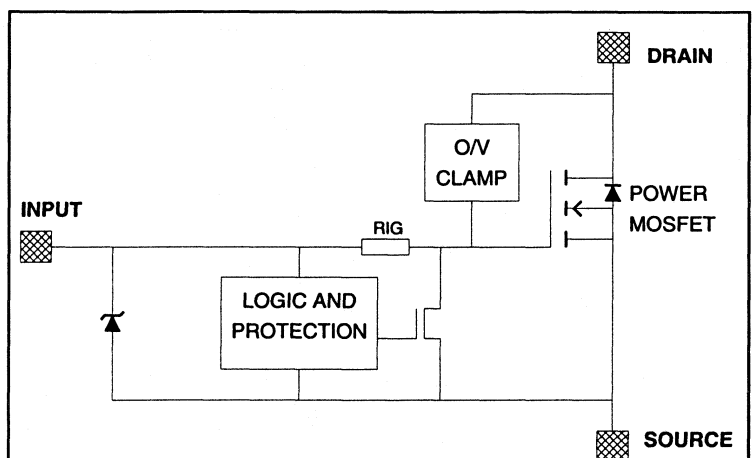
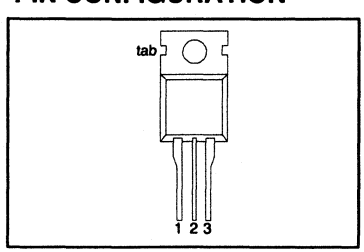


Fig.1. Elements of the TOPFET.

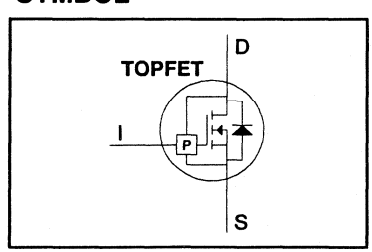
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	13.5	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 5 V	-	8.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	54	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	40	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 5 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 5 V	-	35	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	0.6	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	15	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 15 A; $V_{DD} \leq 20$ V; inductive load	-	200	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; I_{DM} = 4 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{IS} = 5 V; I_{DM} = 7.5 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	85	125	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.2	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 1$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 5 V; normal operation	-	0.2	0.35	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 5 V; protection latched	0.5	1.2	2.0	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	6	-	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	4	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 7.5 A $t_p \leq 300$ µs; $\delta \leq 0.01$	5	9	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 5 V	-	25	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	1.5	-	µs
t_r	Rise time	resistive load R_L = 4 Ω	-	8	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	6	-	µs
t_f	Fall time	resistive load R_L = 4 Ω	-	4.5	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	1.5	-	µs
t_r	Rise time	inductive load I_{DM} = 3 A	-	1	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	10	-	µs
t_f	Fall time	inductive load I_{DM} = 3 A	-	0.5	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	13.5	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 15 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

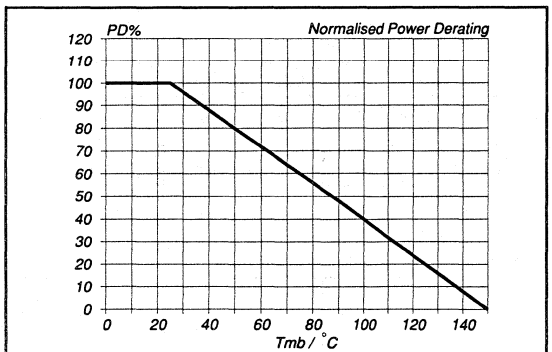


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D / P_D(25\ ^\circ C) = f(T_{mb})$

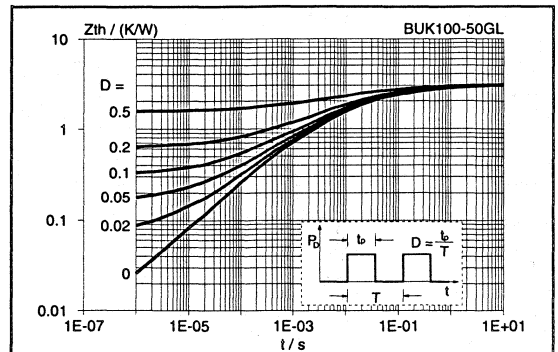


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

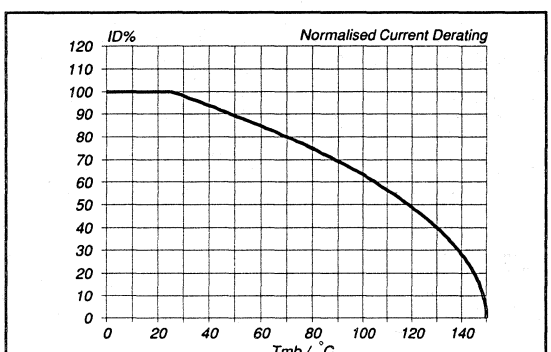


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D / I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

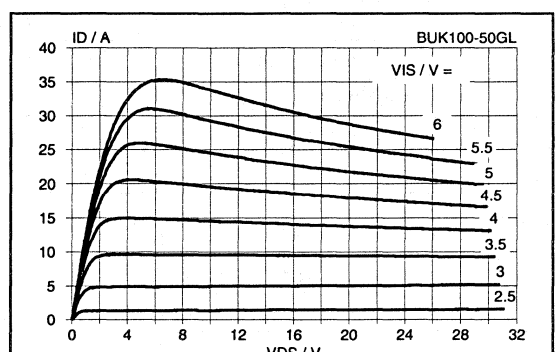


Fig.6. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

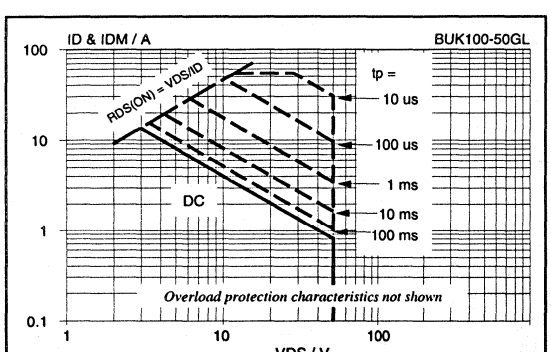


Fig.4. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

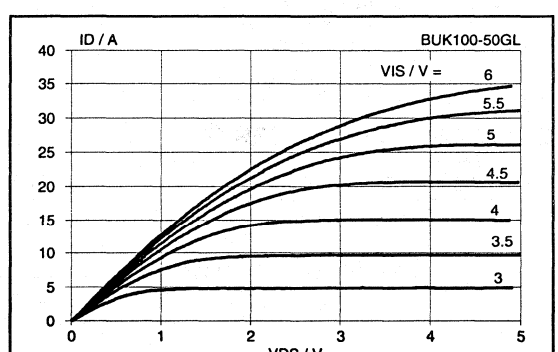


Fig.7. Typical on-state characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

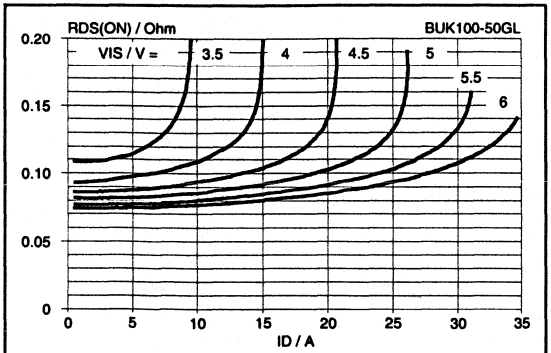


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

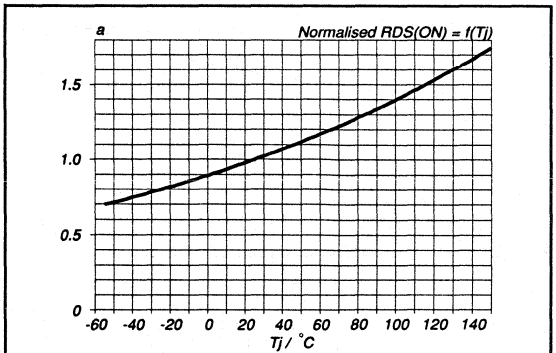


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ °C = f(T_j)$; I_D = 13 A; V_{IS} = 5 V

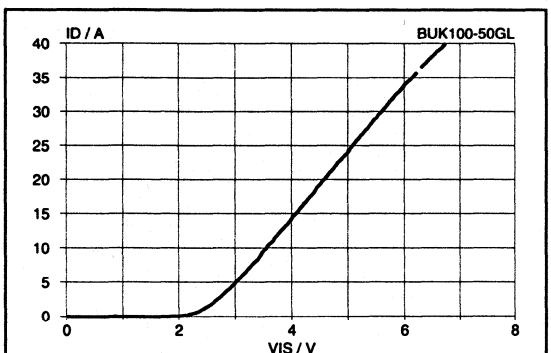


Fig.9. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

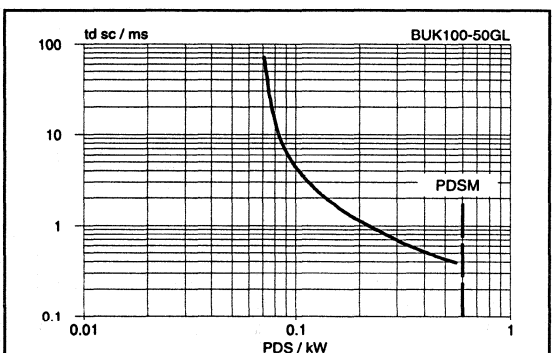


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; T_j = 25 °C.

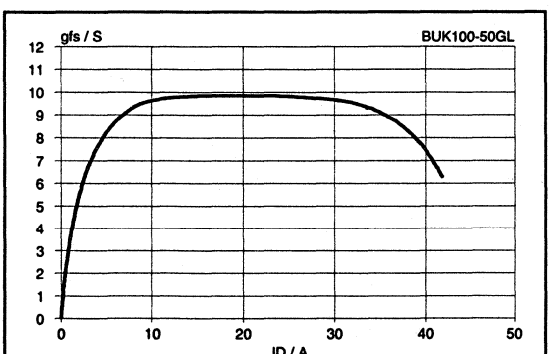


Fig.10. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

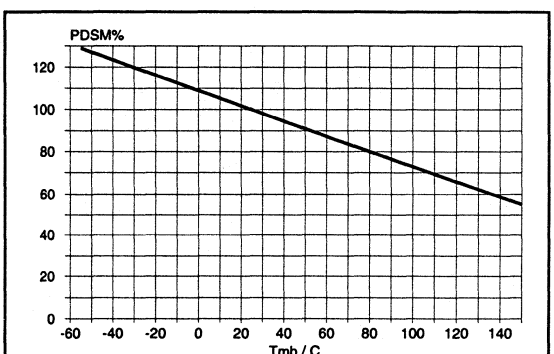


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

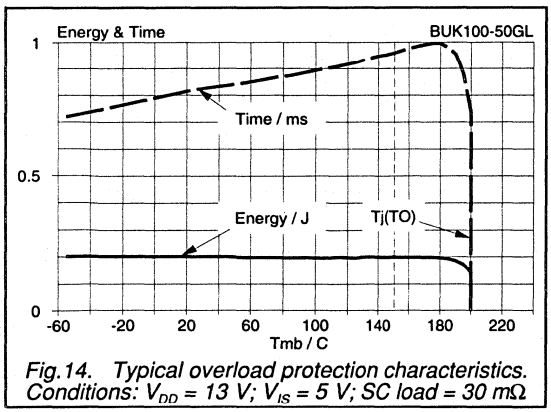


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

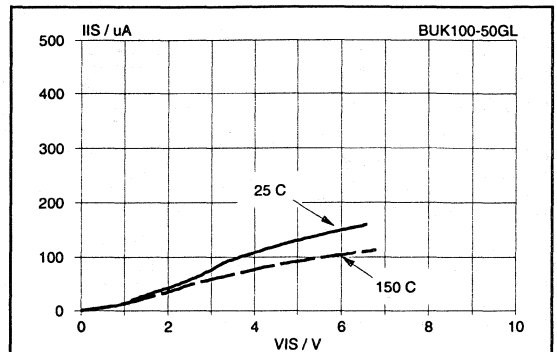


Fig.17. Typical DC input characteristics. $I_{IS} = f(V_{IS})$; normal operation, parameter: T_j

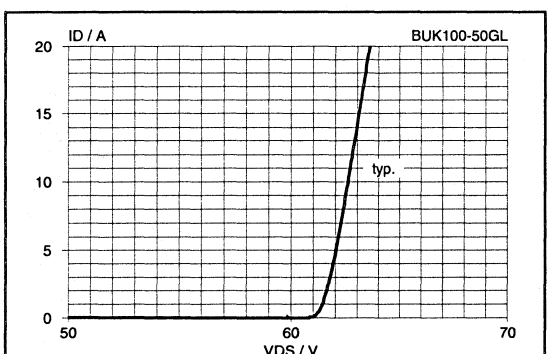


Fig.15. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

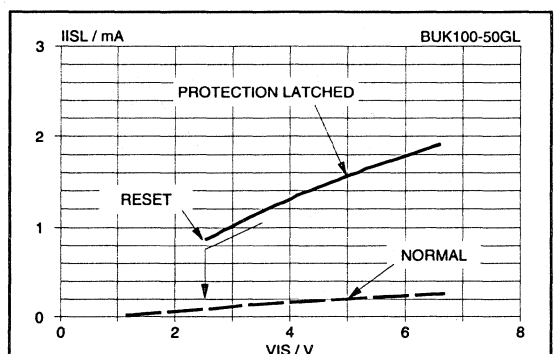


Fig.18. Typical DC input characteristics, T_j = 25 °C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

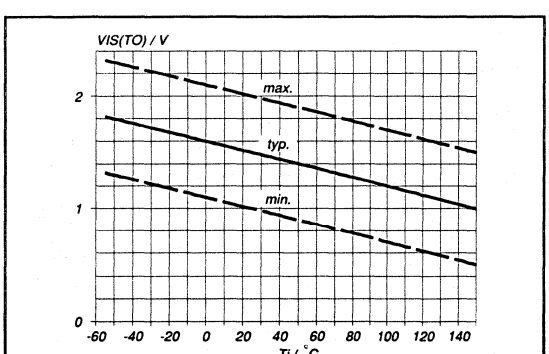


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

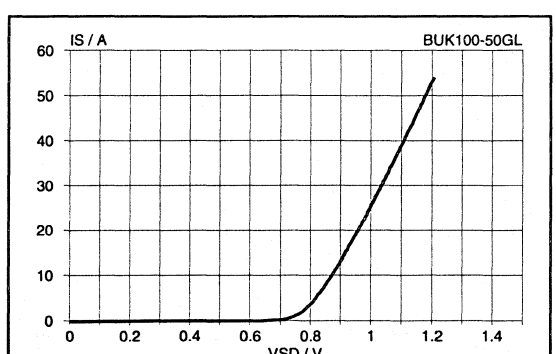


Fig.19. Typical reverse diode current, T_j = 25 °C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

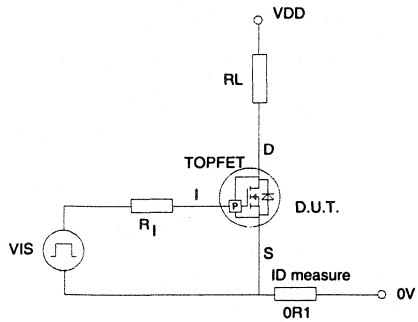


Fig.20. Test circuit for resistive load switching times.

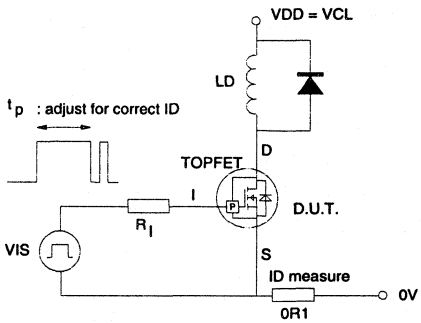


Fig.23. Test circuit for inductive load switching times.

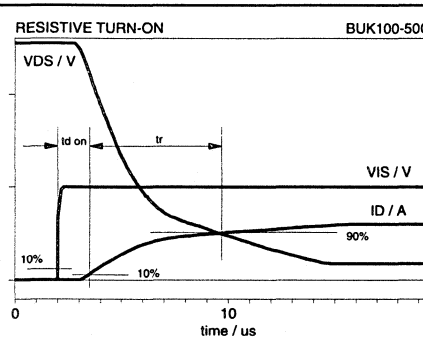


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 °C.

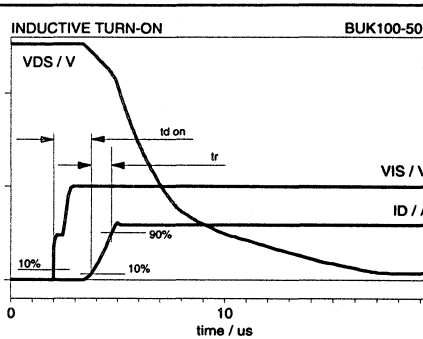


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 °C.

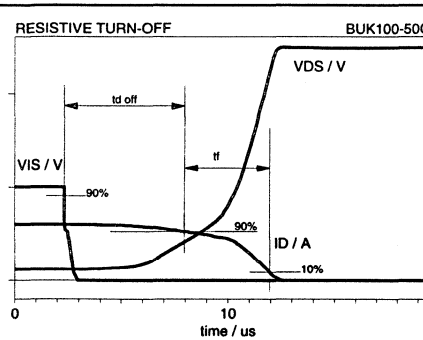


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 °C.

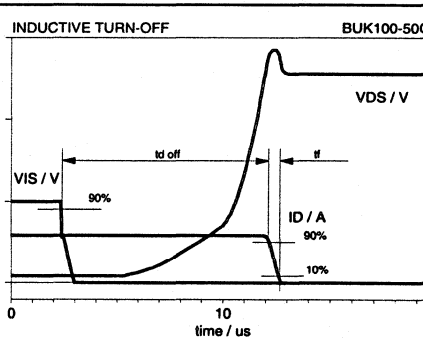


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 °C.

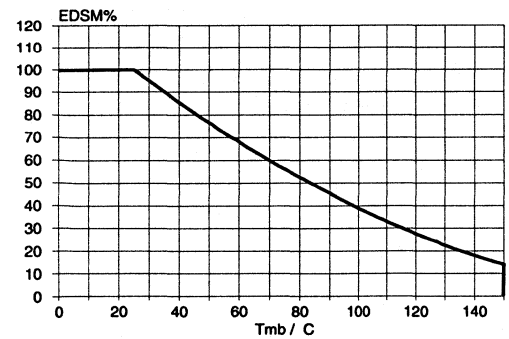


Fig.26. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 15 A; V_{IS} = 5 V

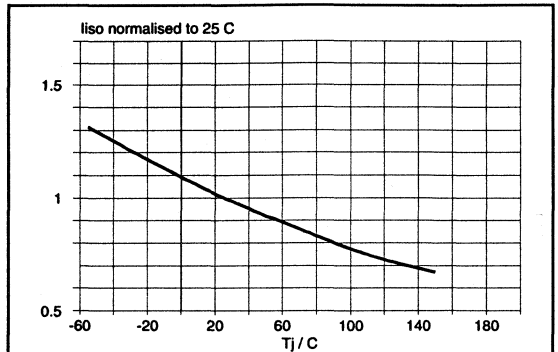


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^\circ C = f(T_j)$; V_{IS} = 5 V

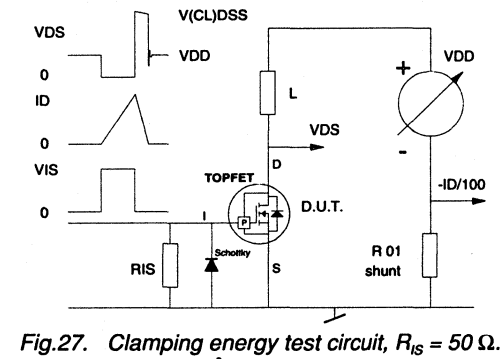


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.
$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$

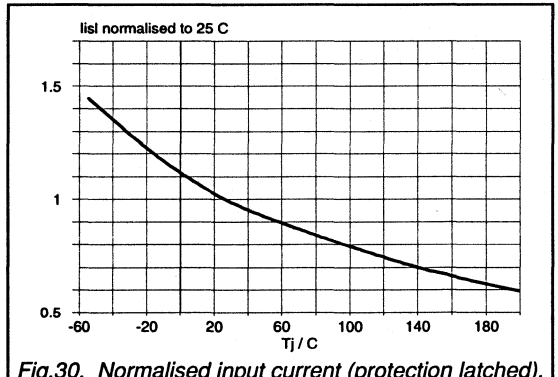


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^\circ C = f(T_j)$; V_{IS} = 5 V

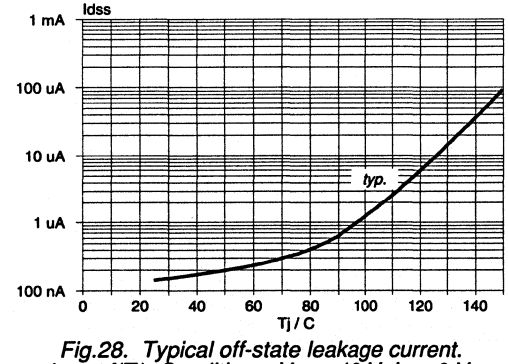


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

PowerMOS transistor TOPFET

BUK100-50GS

DESCRIPTION

Monolithic temperature and overload protected power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 10 V input level
- Low threshold voltage also allows 5 V control
- Control of power MOSFET and supply of overload protection circuits derived from input
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	15	A
P_D	Total power dissipation	40	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 10 V	100	mΩ

FUNCTIONAL BLOCK DIAGRAM

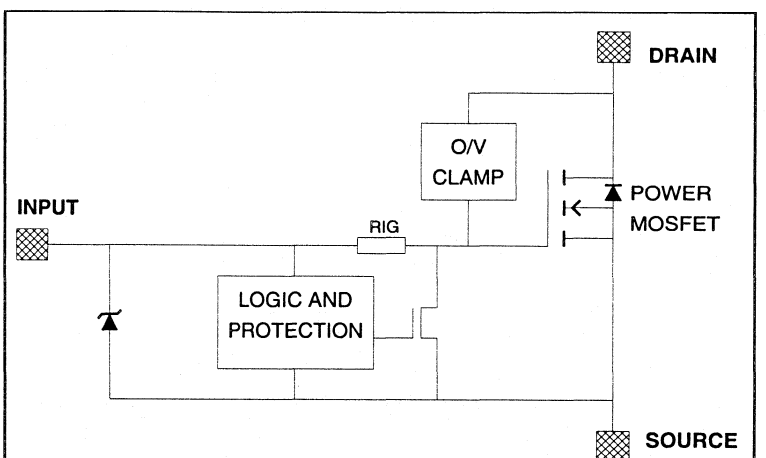
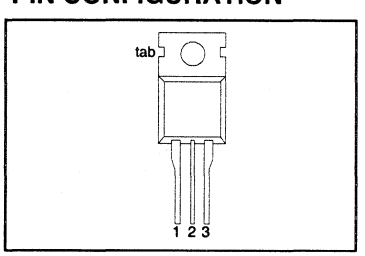


Fig.1. Elements of the TOPFET.

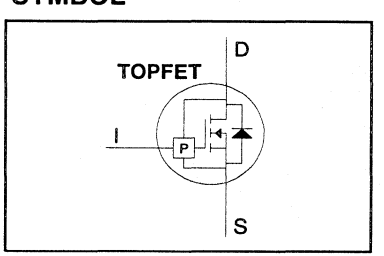
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	11	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	15	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 10 V	-	9.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	60	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	40	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	5	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V	-	20	V
		V_{IS} = 5 V	-	35	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	0.6	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	15	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 15 A; $V_{DD} \leq 20$ V; inductive load	-	200	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; I_{DM} = 4 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA		50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \le 300\ \mu s$; $\delta \le 0.01$		-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V		-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V		-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	I_{DM} = 7.5 A; $t_p \le 300\ \mu s$; $\delta \le 0.01$	V_{IS} = 10 V	-	65	100	mΩ
			V_{IS} = 5 V	-	85	125	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 10 V	-	0.2	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 10 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 10 V; from $I_D \ge 1$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 10 V; normal operation	-	0.4	1.0	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 10 V; protection latched	1.0	2.5	5.0	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	11	13	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	4	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 7.5 A $t_p \leq 300$ µs; $\delta \leq 0.01$	5	9	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 10 V	-	40	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 10 V	-	1	-	µs
t_r	Rise time	resistive load R_L = 4 Ω	-	4	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	10	-	µs
t_f	Fall time	resistive load R_L = 4 Ω	-	5	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 10 V	-	1	-	µs
t_r	Rise time	inductive load I_{DM} = 3 A	-	0.5	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	15	-	µs
t_f	Fall time	inductive load I_{DM} = 3 A	-	0.5	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	15	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 15 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

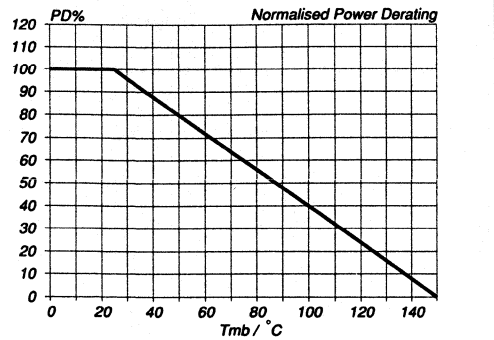


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

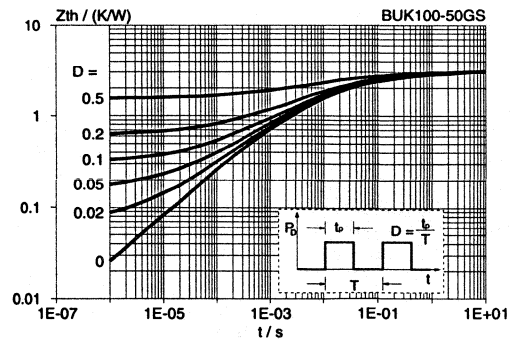


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

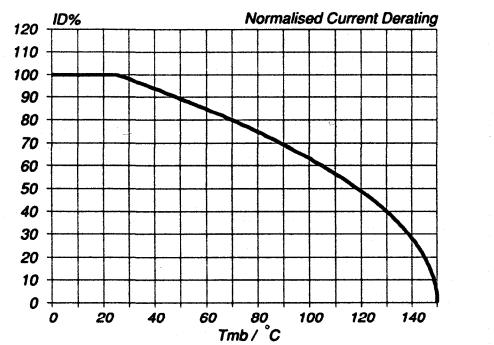


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

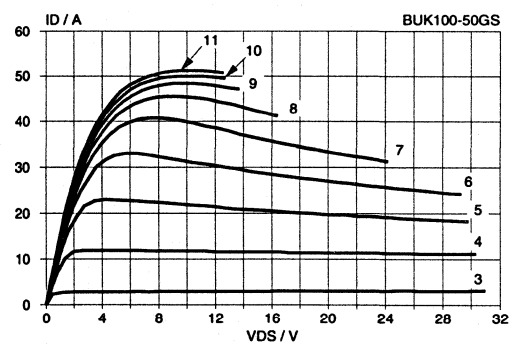


Fig.6. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

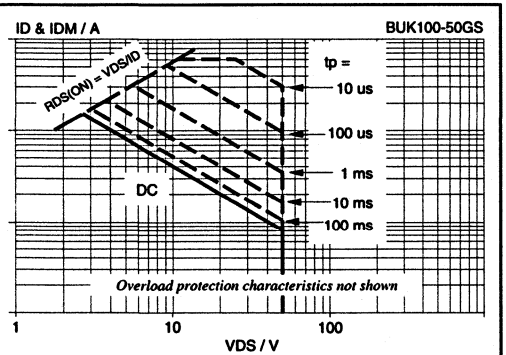


Fig.4. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

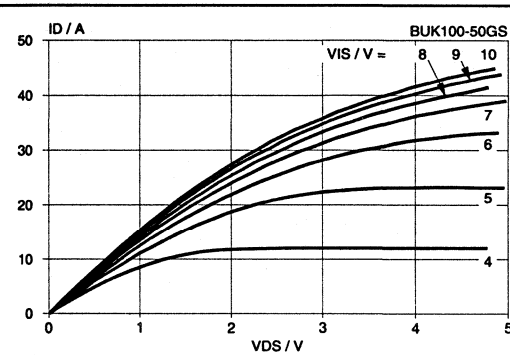


Fig.7. Typical on-state characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

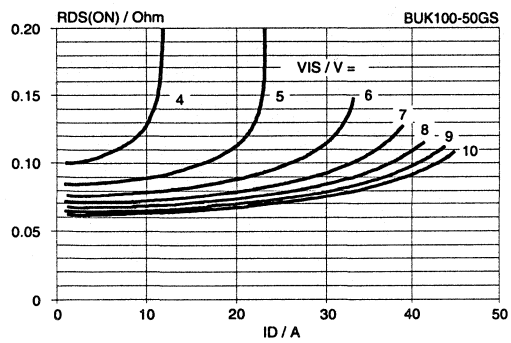


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

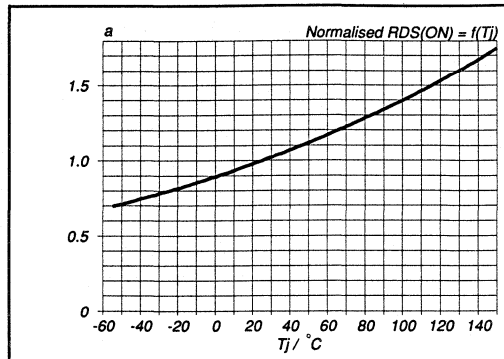


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ °C = f(T_j)$; I_D = 13 A; V_{IS} = 5 V

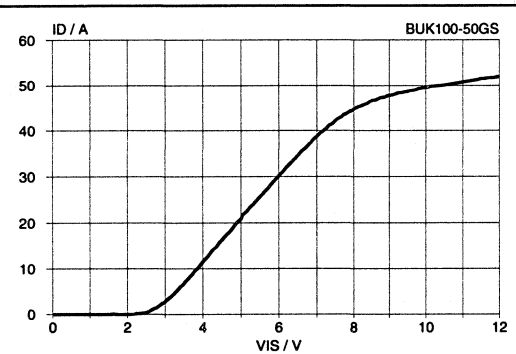


Fig.9. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

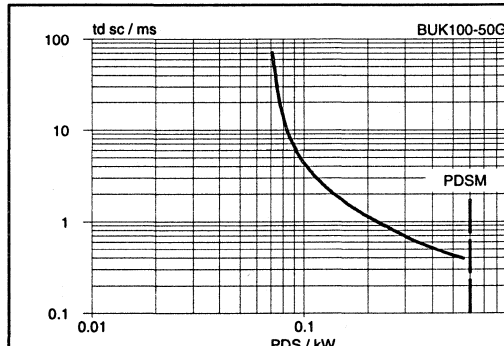


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 5$ V; T_j = 25 °C.

Fig.10. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

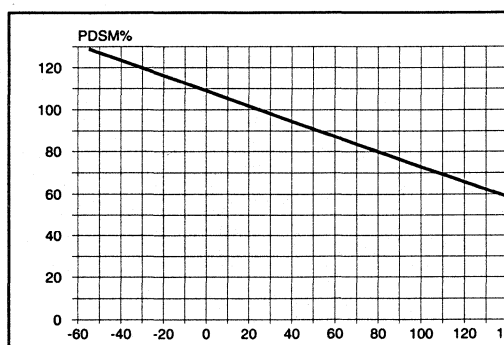


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

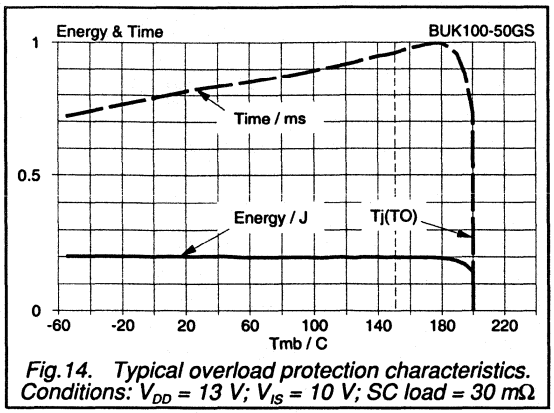


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 10 V; SC load = 30 mΩ

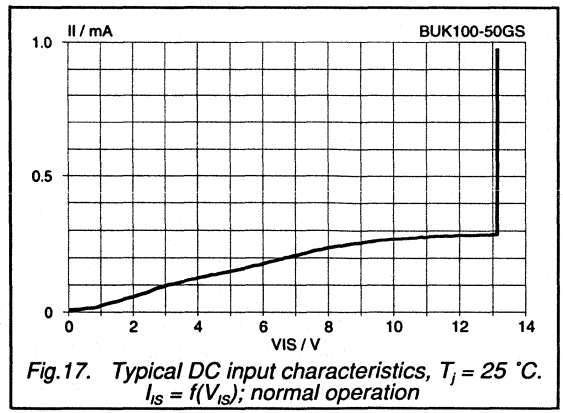


Fig.17. Typical DC input characteristics, T_j = 25 °C. $I_{IS} = f(V_{IS})$; normal operation

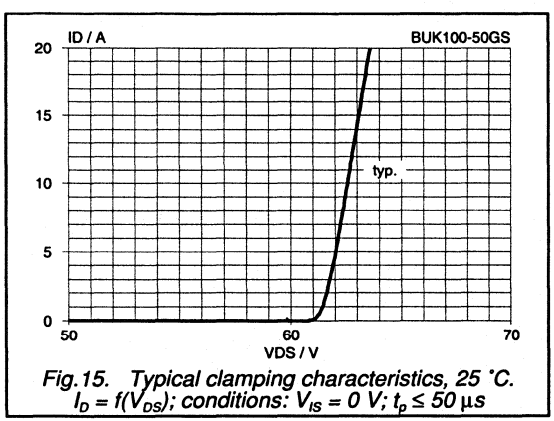


Fig.15. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

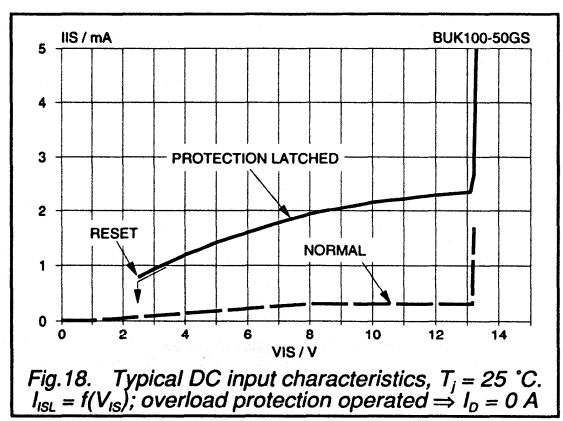


Fig.18. Typical DC input characteristics, T_j = 25 °C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

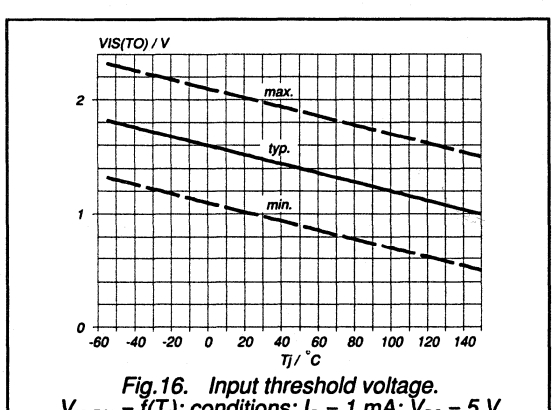


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

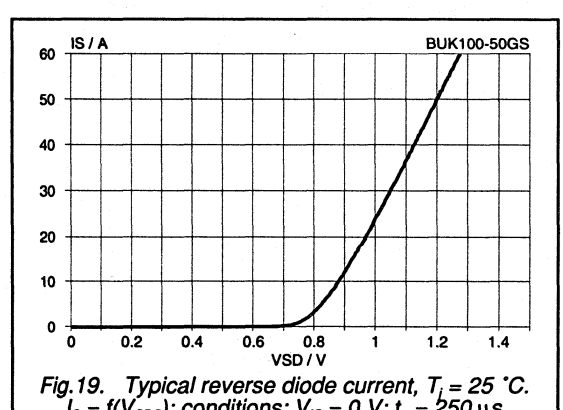


Fig.19. Typical reverse diode current, T_j = 25 °C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

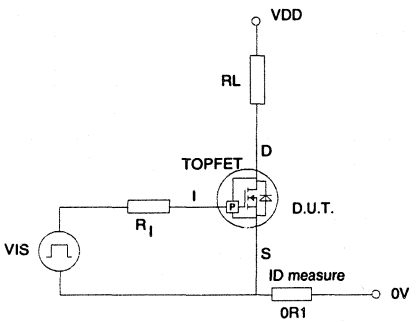


Fig.20. Test circuit for resistive load switching times.

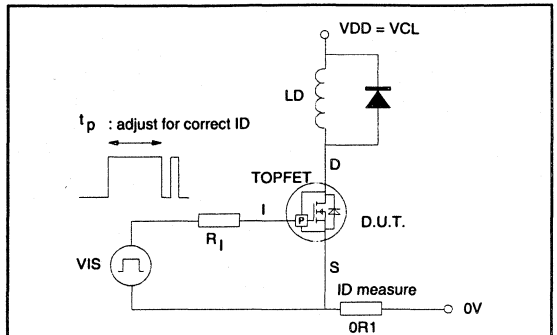


Fig.23. Test circuit for inductive load switching times.

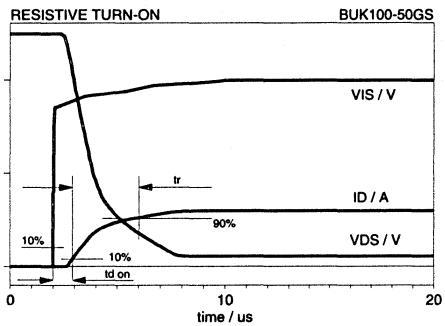


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 °C.

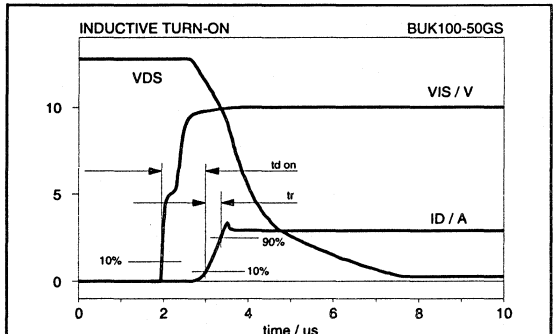


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 °C.

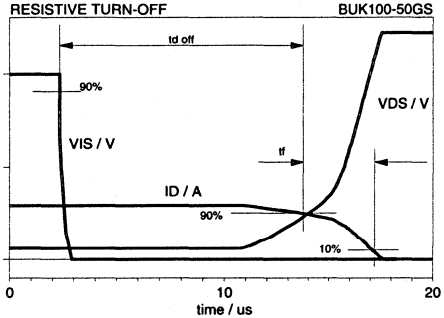


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 °C.

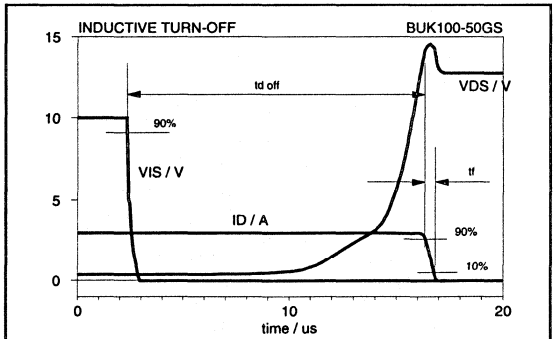


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 °C.

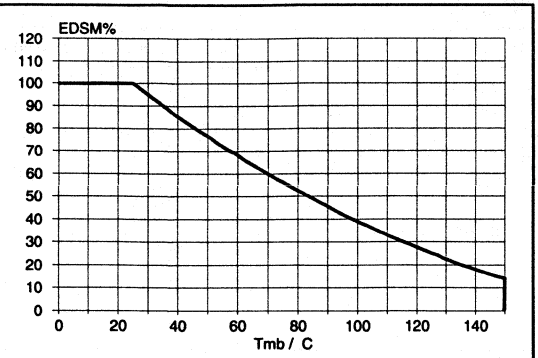


Fig.26. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 15 A; V_{IS} = 10 V

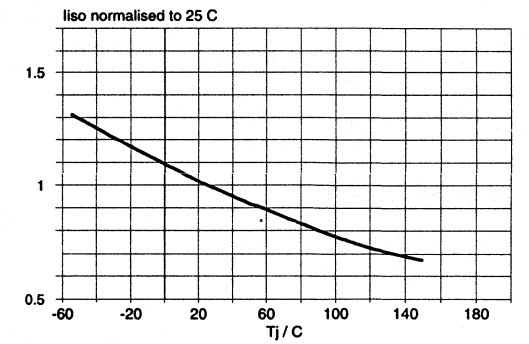


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^{\circ}C = f(T_j)$; V_{IS} = 10 V

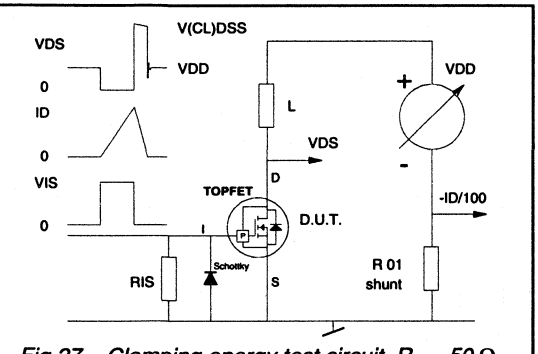


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

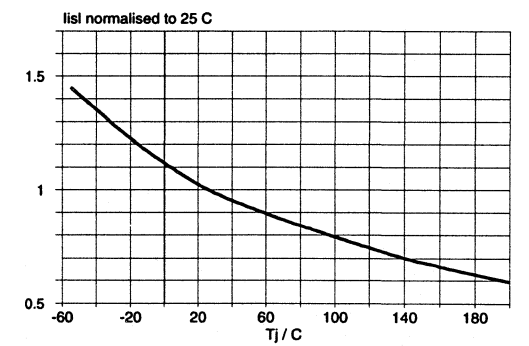


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^{\circ}C = f(T_j)$; V_{IS} = 10 V

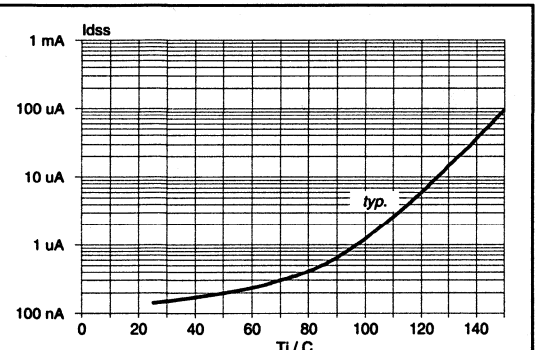


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

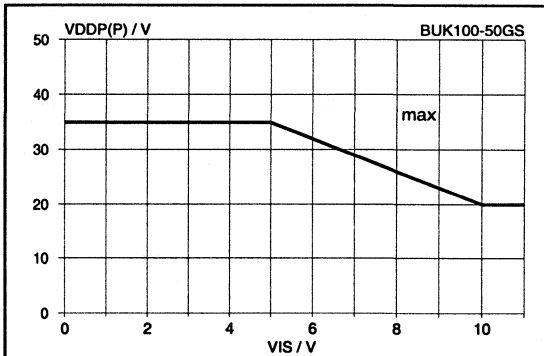


Fig.31. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150\ ^{\circ}C$

PowerMOS transistor Logic level TOPFET

BUK101-50DL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Lower operating input current permits direct drive by micro-controller
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MAX.	UNIT
V_{DS}	Continuous drain source voltage		50	V
I_D	Continuous drain current		26	A
P_D	Total power dissipation		75	W
T_j	Continuous junction temperature		150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		60	mΩ
I_{ISL}	Input supply current	V_{IS} = 5 V	650	μA

FUNCTIONAL BLOCK DIAGRAM

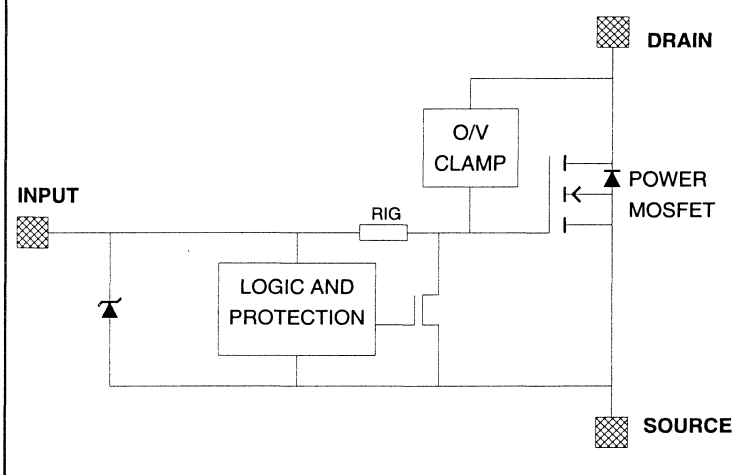
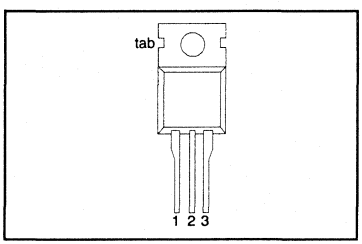


Fig.1. Elements of the TOPFET.

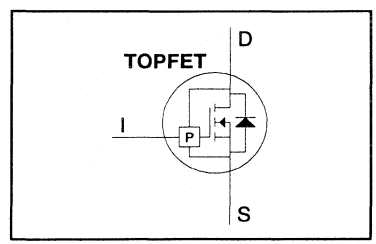
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	26	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; $V_{IS} = 5$ V	-	16	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	100	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	75	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 5$ V	-	50	V
	Short circuit load protection[4]				
$V_{DDP(P)}$	Protected drain source supply voltage[5]	$V_{IS} = 5$ V	-	20	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25$ °C	-	1.3	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0$ V	-	26	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; $I_{DM} = 26$ A; $V_{DD} \leq 20$ V; inductive load	-	625	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; $I_{DM} = 8$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	40	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

5 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than $V_{DDP(P)}$ maximum.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base		-	1.3	1.67	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[1]	V_{IS} = 5 V; I_{DM} = 13 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	45	60	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[2]	T_{mb} = 25 °C; L ≤ 10 µH; R_L = 10 mΩ				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.4	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
$I_{D(SC)}$	Drain current[3]	V_{DD} = 13 V; V_{IS} = 5 V	-	45	-	A
$I_{DM(SC)}$	Peak drain current[4]	V_{IS} = 5 V; V_{DD} = 13 V	-	105	-	A
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 1$ A[5]	150	-	-	°C

TRANSFER CHARACTERISTIC

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 13 A $t_p \leq 300$ µs; $\delta \leq 0.01$	10	16	-	S

1 Continuous input voltage. The specified pulse width is for the drain current.

2 Refer to OVERLOAD PROTECTION LIMITING VALUES.

3 Continuous drain-source supply voltage. Pulsed input voltage.

4 Continuous input voltage. Momentary short circuit load connection. (The higher peak current is due to the effect of capacitance Cgd).

5 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	100	200	350	µA
			V_{IS} = 4 V	-	160	270	µA
V_{ISR}	Protection reset voltage[1]		T_j = 25 °C	2.0	2.6	3.5	V
			T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	330	650	µA
			V_{IS} = 3.5 V	-	240	430	µA
$V_{(BR)IS}$	Input breakdown voltage	I_I = 10 mA		6	-	-	V
R_{IG}	Input series resistance		T_j = 25 °C	-	33	-	kΩ
	to gate of power MOSFET		T_j = 150 °C	-	50	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	17	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	75	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	60	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	70	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	26	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDO}	Forward voltage	I_S = 26 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

1 The input voltage below which the overload protection circuits will be reset.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

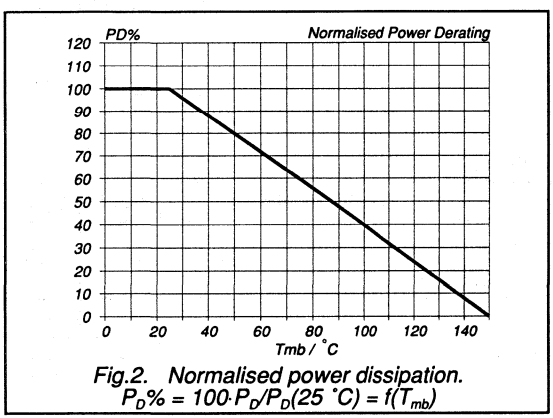


Fig.2. Normalised power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

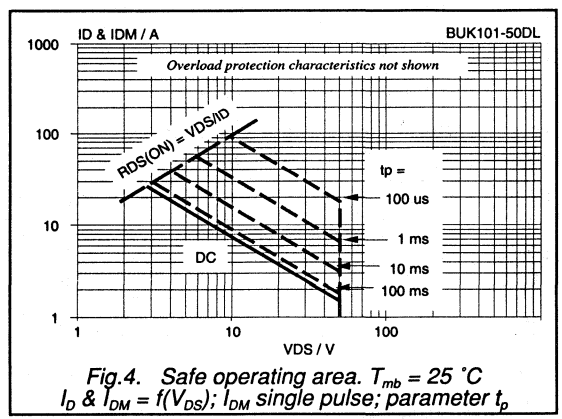


Fig.4. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = $f(V_{DS})$; I_{DM} single pulse; parameter t_p

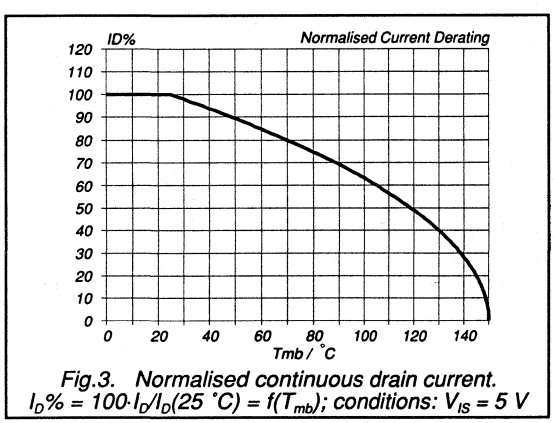


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; *conditions:* V_{IS} = 5 V

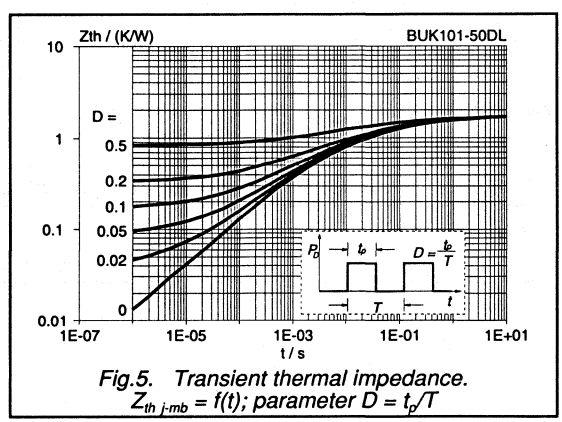


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; *parameter* $D = t_p/T$

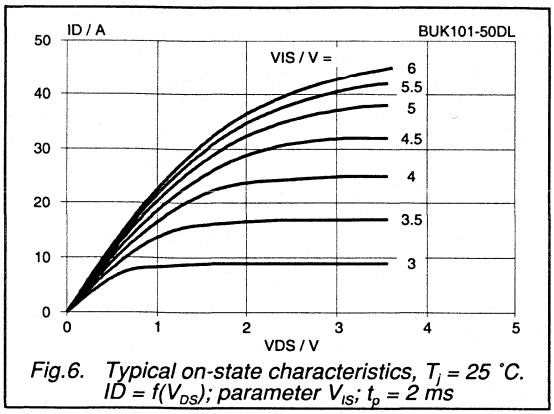


Fig.6. Typical on-state characteristics, T_j = 25 °C. ID = f(V_{DS}); parameter V_{IS}; t_p = 2 ms

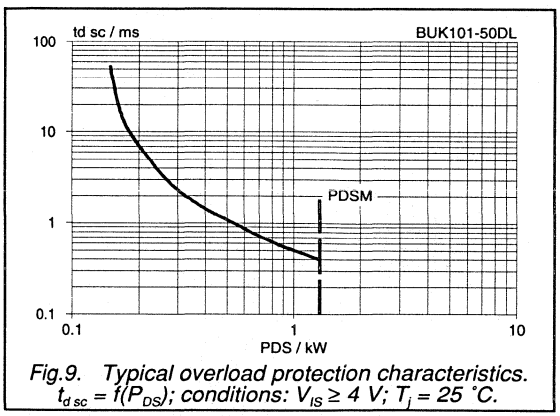


Fig.9. Typical overload protection characteristics. $t_{d\,sc}$ = f(P_{DS}); conditions: $V_{IS} \geq 4$ V; T_j = 25 °C.

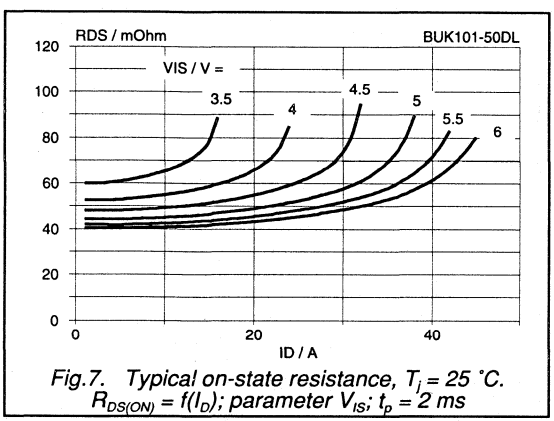


Fig.7. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)}$ = f(I_D); parameter V_{IS}; t_p = 2 ms

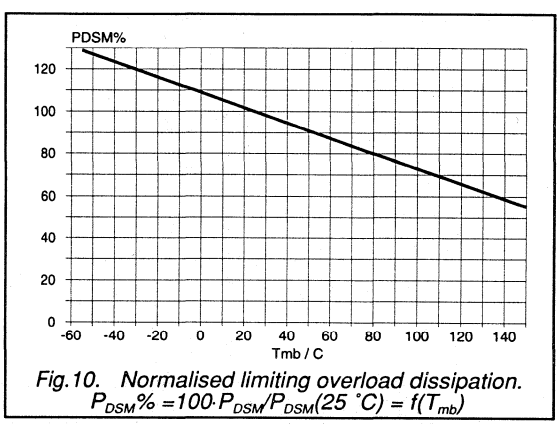


Fig.10. Normalised limiting overload dissipation. P_{DSM}% =100·P_{DSM}/P_{DSM}(25 °C) = f(T_{mb})

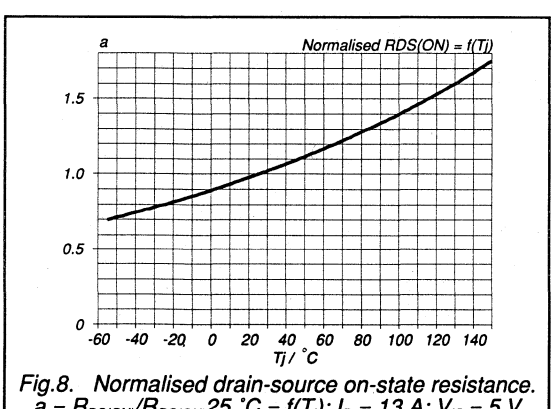


Fig.8. Normalised drain-source on-state resistance. a = $R_{DS(ON)}$/$R_{DS(ON)}$25 °C = f(T_j); I_D = 13 A; V_{IS} = 5 V

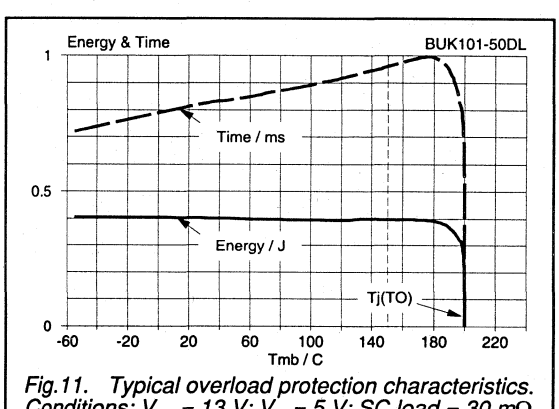


Fig.11. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

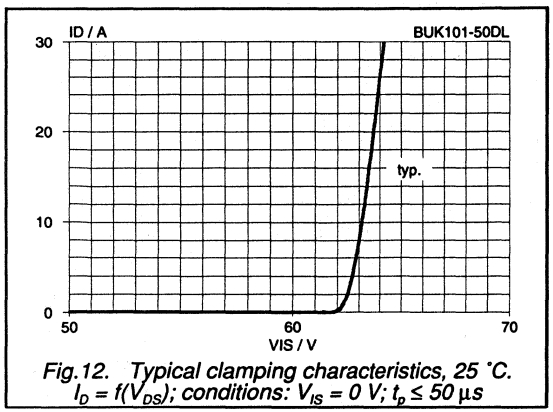


Fig.12. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50$ µs

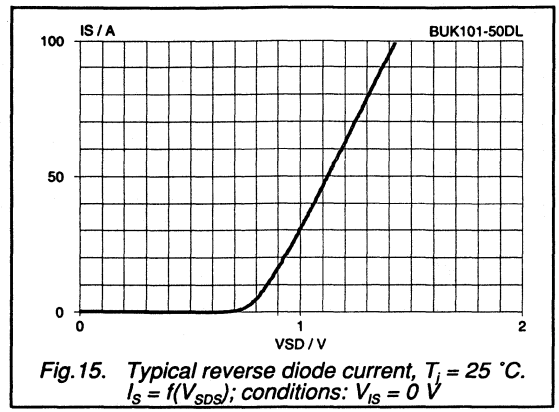


Fig.15. Typical reverse diode current, $T_j = 25$ °C. $I_S = f(V_{SDS})$; conditions: $V_{IS} = 0$ V

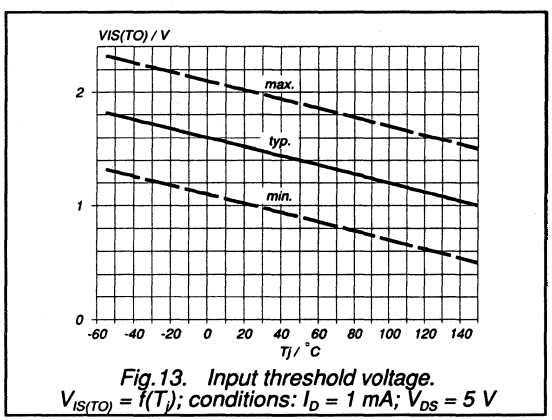


Fig.13. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

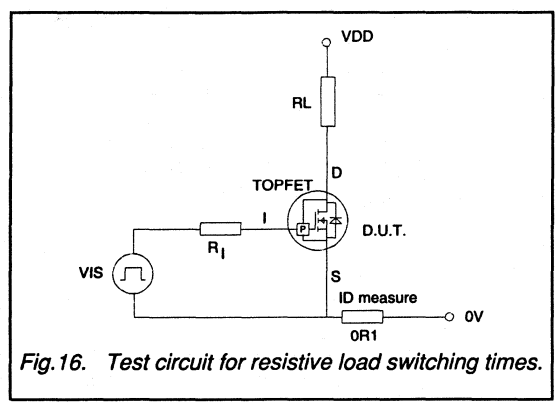


Fig.16. Test circuit for resistive load switching times.

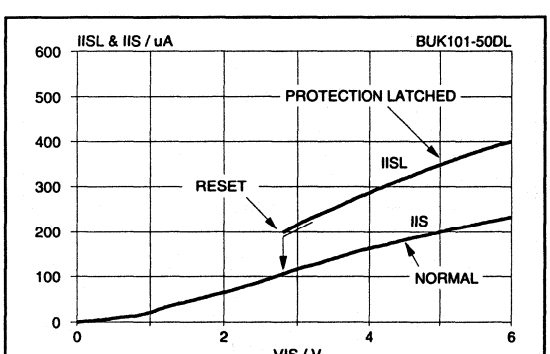


Fig.14. Typical DC input characteristics, $T_j = 25$ °C. I_{ISL} & $I_{IS} = f(V_{IS})$; protection latched & normal operation

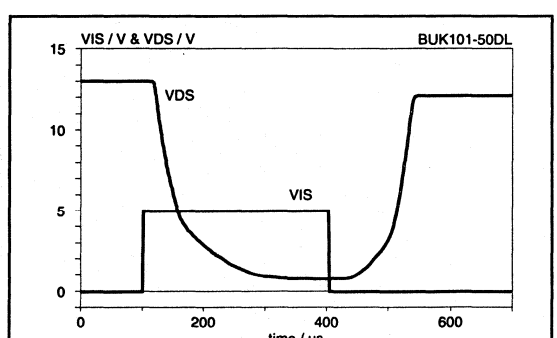


Fig.17. Typical switching waveforms, resistive load. $V_{DD} = 13$ V; $R_L = 2.1$ Ω; $R_I = 50$ Ω, $T_j = 25$ °C.

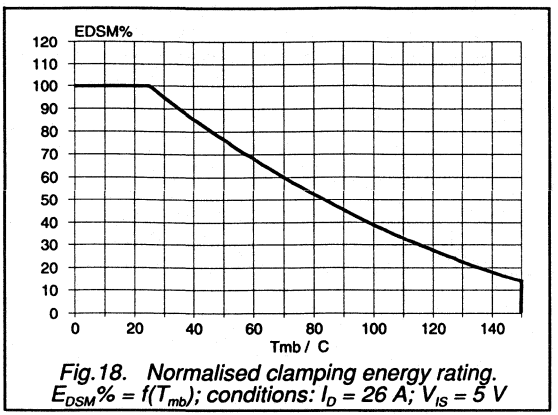


Fig.18. Normalised clamping energy rating. E_{DSM}% = f(T_{mb}); conditions: I_D = 26 A; V_{IS} = 5 V

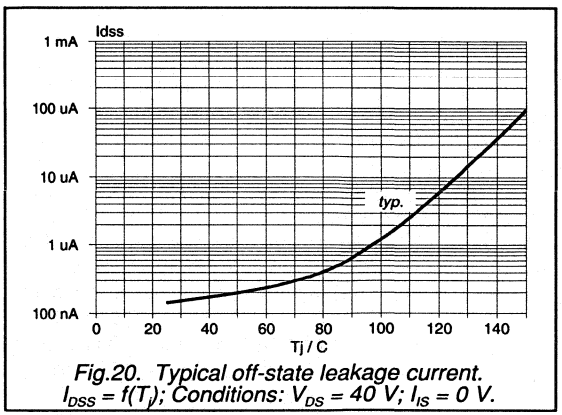


Fig.20. Typical off-state leakage current. I_{DSS} = f(T_j); Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

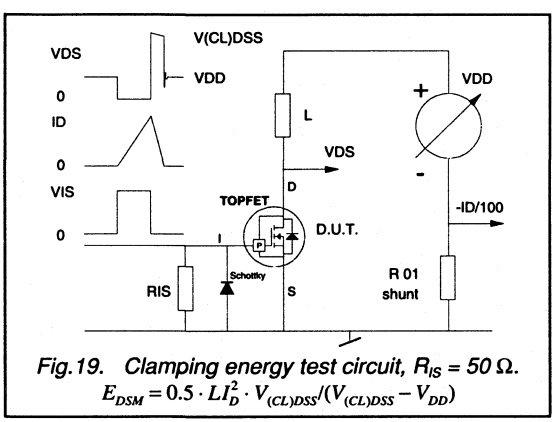


Fig.19. Clamping energy test circuit, R_{IS} = 50 Ω.
$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$

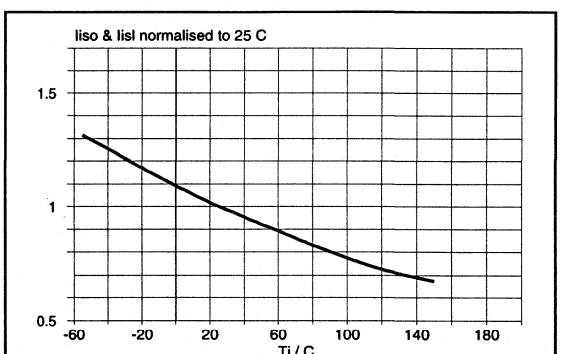


Fig.21. Normalised input currents (normal & latched). $I_{ISO}/I_{ISO}25°C$ & $I_{ISL}/I_{ISL}25°C$ = f(T_j); V_{IS} = 5 V

BUK101-50DL - a microcontroller compatible TOPFET

Application report

The TOPFET version BUK101-50**DL** can be directly controlled by the port outputs of standard microcontrollers and other high impedance driver stages. This member of the TOPFET family has the same functional features as its predecessors BUK101-50**GS** and BUK101-50**GL**. All these versions are 3-pin devices for the replacement of Power MOSFETs or partially protected Power MOSFETs. They are internally protected against over temperature, short circuit load, overvoltage and electrostatic discharge. For more information concerning the basic technical concept of TOPFET see Philips Technical Publication 'TOPFET - A NEW CONCEPT IN PROTECTED MOSFET'. This section covers the special features of the BUK101-50**DL** version, criteria for driver stage design and application.

Overview on BUK101-50 versions

The GS, GL and DL versions of the BUK101-50 TOPFET each have the same functionality but differ in their input characteristics. Table 1 gives an overview on these characteristics.

Type	Nominal Input Voltage (V)	Normal Input Current (mA)	Latched Input Current (mA)	Max. Input Voltage (V)
GS	10	1.0	4.0	11
GL	5	0.35	2.0	6
DL	5	0.35	0.65	6

Table 1. Comparison of GS, GL and DL versions

Table 1 shows that the GS version (S for Standard type) is specified for 10V driver outputs while the GL and DL versions (L for Logic Level type) are specified for 5V logic level driver outputs. The two logic level types differ in the input current, I_{ISL}, which flows when the device is in its 'latched' state i.e. shutdown has occurred due to over temperature or short circuit load. The GL version is suitable for pulsed applications up to 1kHz and needs a push-pull driver stage while the DL version is optimised for high impedance drive circuits and can handle pulsed applications up to 100Hz.

Criteria for choice/design of driver stage

Figure 1 shows a simplified circuit diagram for the input of a 3-pin TOPFET. Also indicated is the high level output impedance of the driver stage R_{out}.

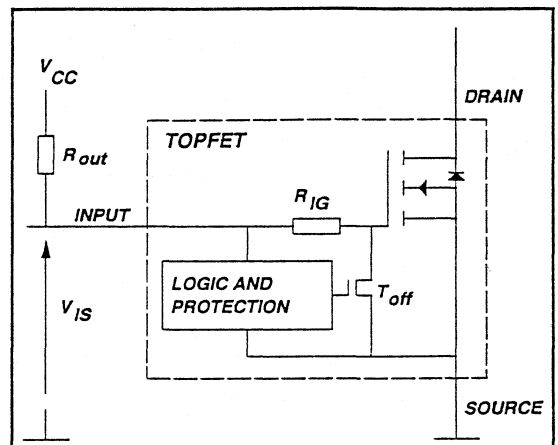


Fig. 1 Diagram of 3-pin TOPFET input

For all versions the internal circuits for over temperature and short circuit load protection are supplied from the input pin. This determines the input current I_{IS} under normal conditions, i.e. the Power MOS transistor is on and T_{off} in Fig. 1 is off. To ensure proper function of the protection circuits, a minimum input voltage $V_{IS} = 4V$ has to be applied. If, however, the device has turned off due to over temperature or short circuit load (i.e. transistor T_{off} in Fig. 1 is on), a minimum of $V_{IS} = 3.5V$ is required to keep the device in its 'latched' state. Latched means that the device will stay off even if the error condition has disappeared. Figure 1 indicates that under this condition the input current I_{ISL} will be increased due to the additional current that has to be sourced into resistor R_{IG}. R_{IG} allows the Power MOS gate to be pulled down internally while the input pin is at high level. The typical value of R_{IG} in the GL version is 4kΩ, while for the DL version this value has been increased to 30kΩ. Thus the maximum input current has been reduced to allow for high impedance driver stages such as microcontroller port outputs.

The criteria stated above result in the following requirements on the driver stage output resistance R_{out}:

$$Normal: \quad R_{out} \leq \frac{V_{cc} - 4V}{I_{IS}(V_{IS} = 4V)} \qquad (1)$$

$$Latched: \quad R_{out} \leq \frac{V_{cc} - 3.5V}{I_{IS}(V_{IS} = 3.5V)} \qquad (2)$$

The maximum input currents of the BUK101-50DL are specified as follows:

$I_{IS,max}$ = 270µA at V_{IS} = 4V
$I_{ISL,max}$ = 430µA at V_{IS} = 3.5V

Considering a 5V supply, equation (2) leads to a maximum output resistance $R_{out,max}$ = 3.5kΩ.

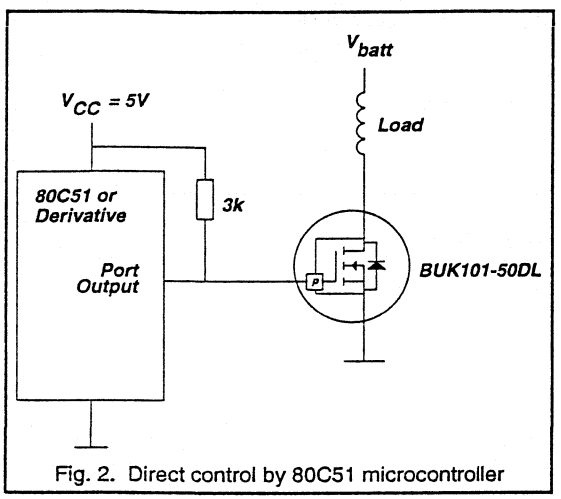


Fig. 2. Direct control by 80C51 microcontroller

Application example - 80C51 microcontroller as TOPFET driver

Figure 2 shows an application that takes advantage of the low input current of the BUK101-50DL. As has been shown above, the external pull-up resistor $R_{pull-up}$ in this circuit should have a maximum value of 3.5kΩ at V_{CC} = 5V for safe operation of the TOPFET protection circuits. An additional requirement is that the TOPFET must be off when the port output is at low level. Thus the limited sinking capability of the port output demands a minimum value for $R_{pull-up}$. For the 80C51 microcontroller family a maximum output voltage of $V_{out,low}$ = 0.45V is specified at a sink current of 1.6mA for ports 1 to 3 and 3.2mA for port 0. This voltage level is safely below the minimum turn-on threshold $V_{IS(TO)}$ = 1V of the TOPFET. Considering V_{CC} = 5V and the above specification of the port output, the minimum value for $R_{pull-up}$ is:

$$R_{pullup} \geq \frac{5V - 0.45V}{1.6mA} = 2.8k\Omega$$

Thus a value of 3kΩ meets the requirements.

Other applications for the BUK101-50DL

Logic IC as driver

Besides microcontroller port outputs the BUK101-50DL can also be driven by standard 5V logic IC families. Table 2 gives an overview on these families and states - if necessary - the minimum value for a pull-up resistor.

Family	$R_{pull-up\ min}$
TTL	300Ω
LSTTL	620Ω
STTL	240Ω
HE4000B	no $R_{pull-up}$ required
HCMOS	no $R_{pull-up}$ required
ACL	no $R_{pull-up}$ required

Table 2. 5 V logic IC families driving the BUK101-50DL

High Side driver

The low input current of the BUK101-50DL is also advantageous, when using the device as a high side switch. In this configuration the low drive requirements mean that smaller capacitors are needed in charge pump or bootstrap circuits. This subject is described more fully in section 5.3.6.

PowerMOS transistor Logic level TOPFET

BUK101-50GL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	26	A
P_D	Total power dissipation	75	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 5 V	60	mΩ

FUNCTIONAL BLOCK DIAGRAM

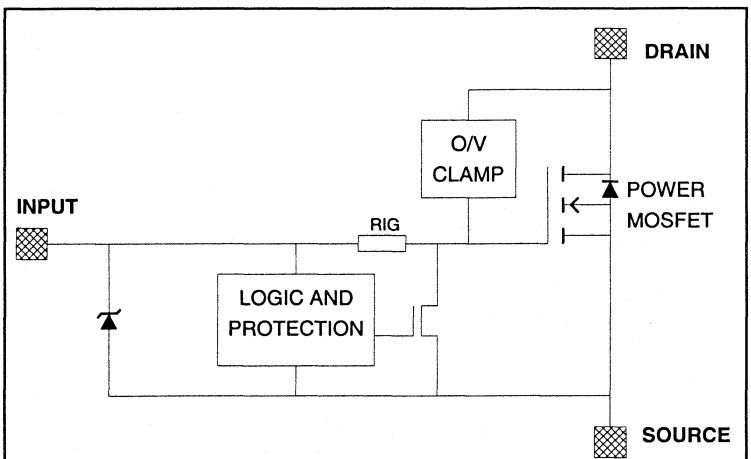
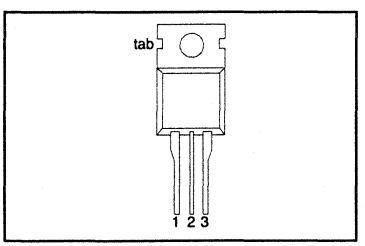


Fig.1. Elements of the TOPFET.

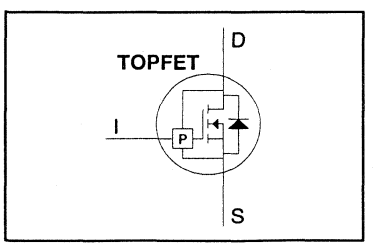
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	26	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 5 V	-	16	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	100	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	75	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[1]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[2]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 5 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[3]	V_{IS} = 5 V	-	35	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	1.3	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	26	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 26 A; $V_{DD} \leq 20$ V; inductive load	-	625	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; I_{DM} = 8 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	40	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

2 The input voltage for which the overload protection circuits are functional.

3 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.3	1.67	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{IS} = 5 V; I_{DM} = 13 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	45	60	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.4	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 1$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 5 V; normal operation	-	0.2	0.35	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 5 V; protection latched	0.5	1.2	2.0	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	6	7	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	4	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 13 A $t_p \leq$ 300 µs; $\delta \leq 0.01$	10	16	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 5 V	-	40	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	2.5	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	15	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	10	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	7	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 10 V; V_{IS} = 5 V	-	2	-	µs
t_r	Rise time	inductive load I_{DM} = 6 A	-	4	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 10 V; V_{IS} = 0 V	-	15	-	µs
t_f	Fall time	inductive load I_{DM} = 6 A	-	1	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq$ 25 °C	-	26	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 26 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

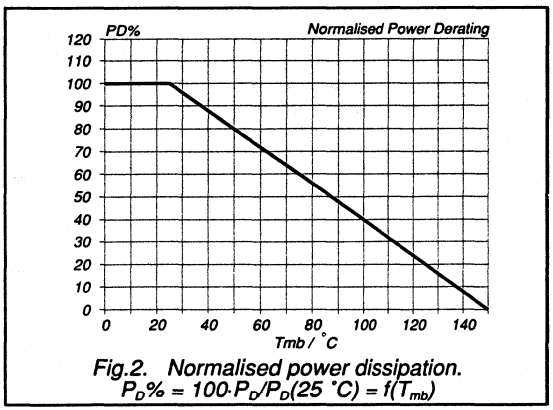


Fig.2. Normalised power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ °C) = f(T_{mb})$

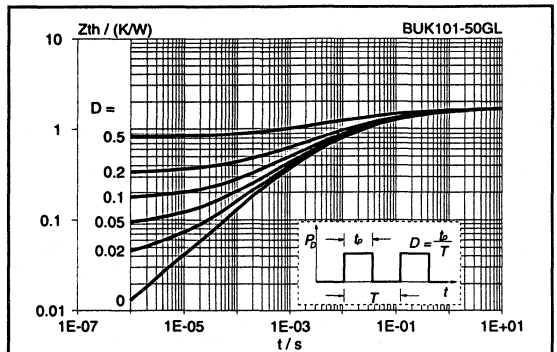


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

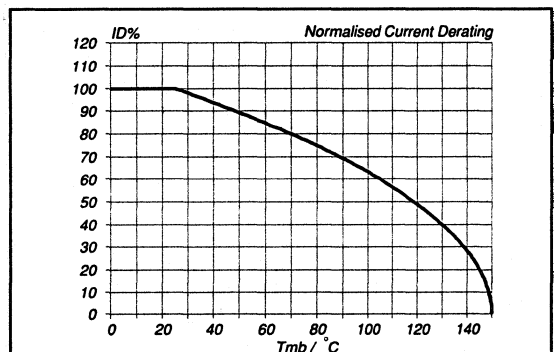


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ °C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

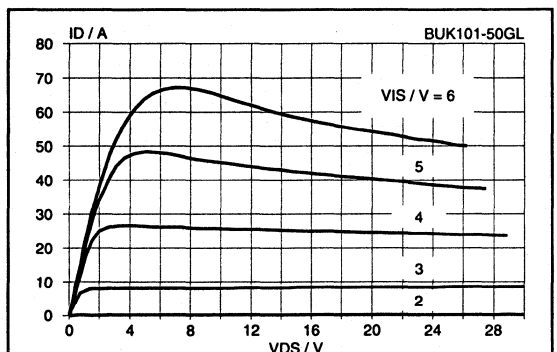


Fig.6. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

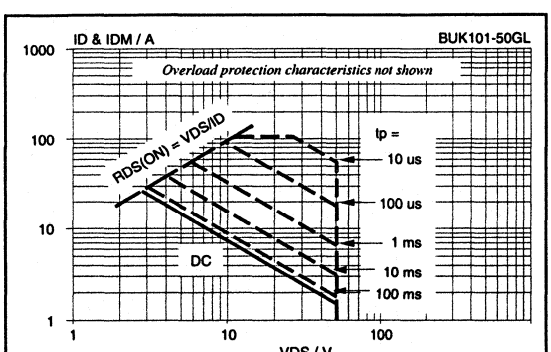


Fig.4. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

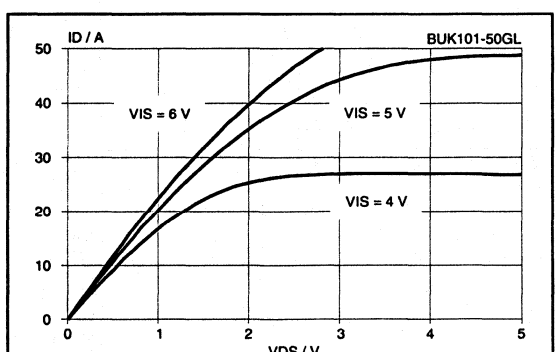


Fig.7. Typical on-state characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

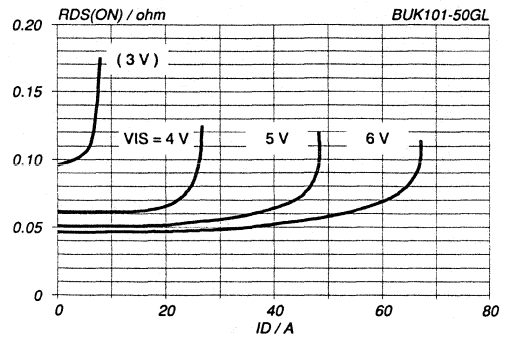


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

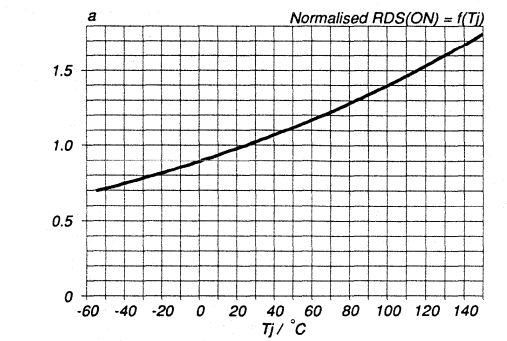


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25$ °C = $f(T_j)$; I_D = 13 A; V_{IS} = 5 V

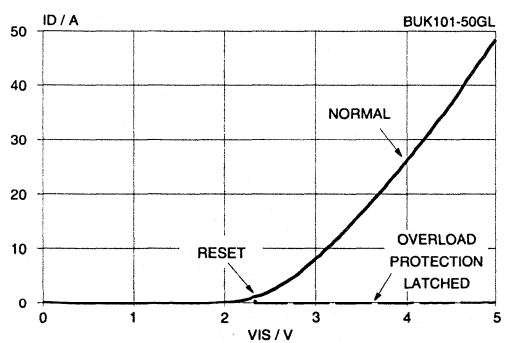


Fig.9. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

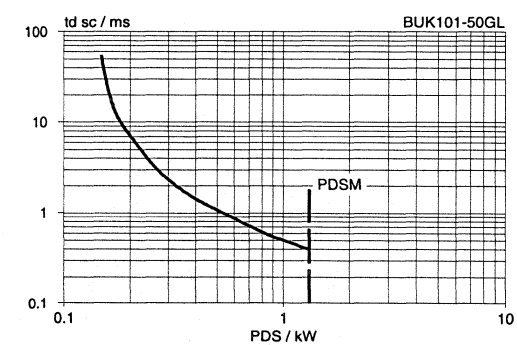


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; T_j = 25 °C.

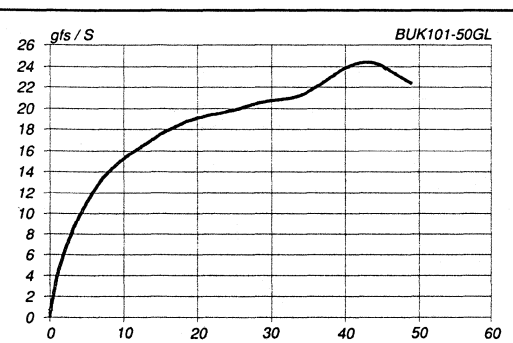


Fig.10. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

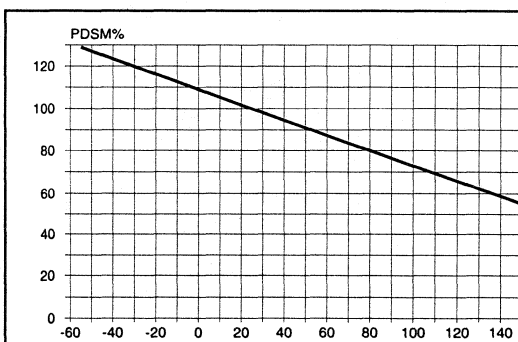


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

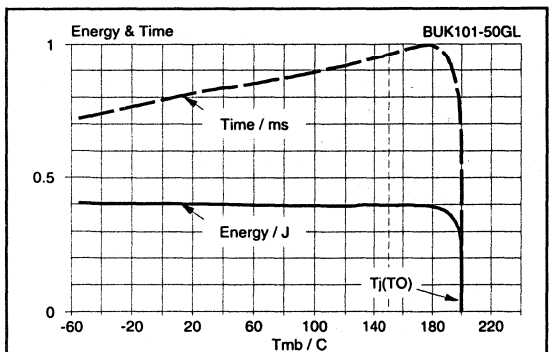


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

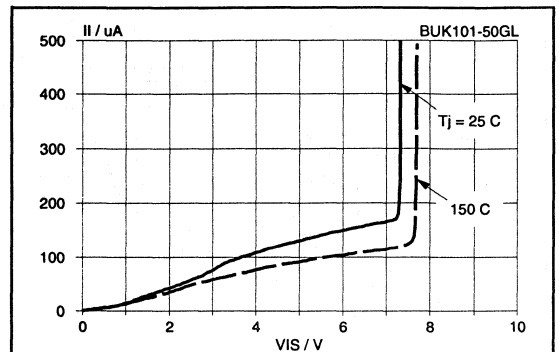


Fig.17. Typical DC input characteristics. $I_I = f(V_{IS})$; normal operation; parameter: T_j

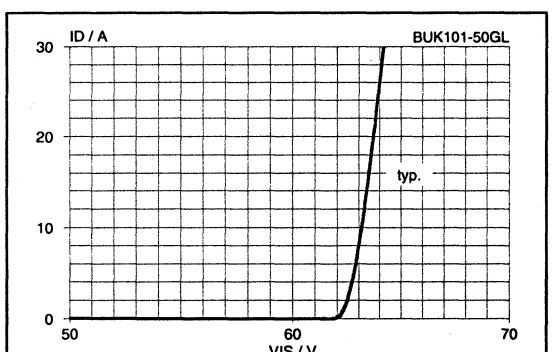


Fig.15. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

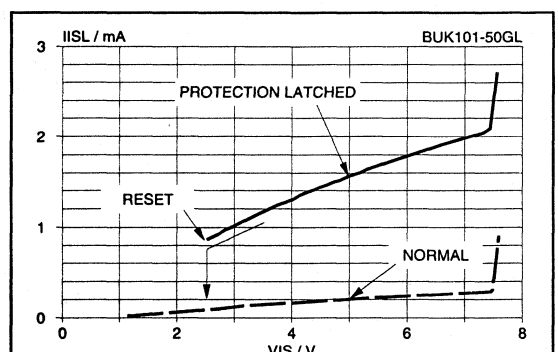


Fig.18. Typical DC input characteristics, T_j = 25 °C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

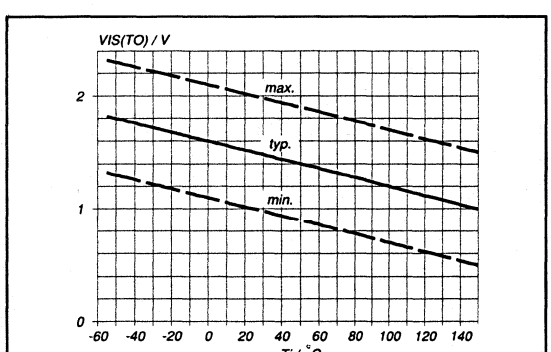


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

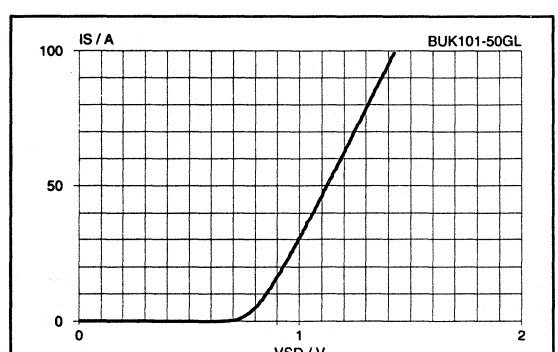


Fig.19. Typical reverse diode current, T_j = 25 °C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V

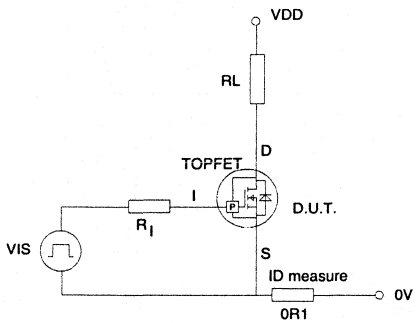


Fig.20. Test circuit for resistive load switching times.

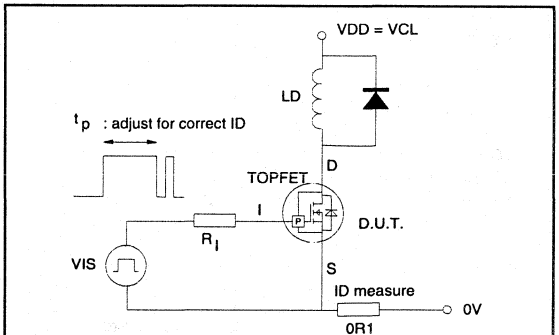


Fig.23. Test circuit for inductive load switching times.

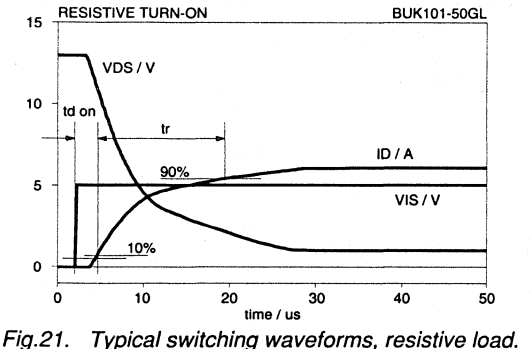


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 °C.

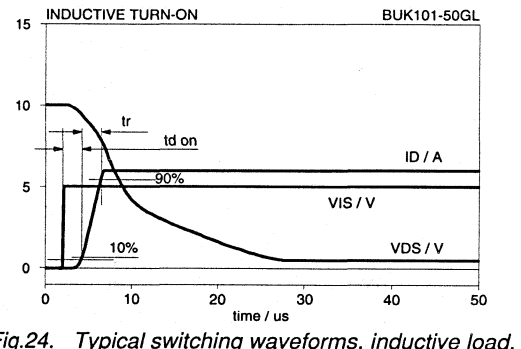


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 10 V; I_D = 6 A; R_I = 50 Ω, T_j = 25 °C.

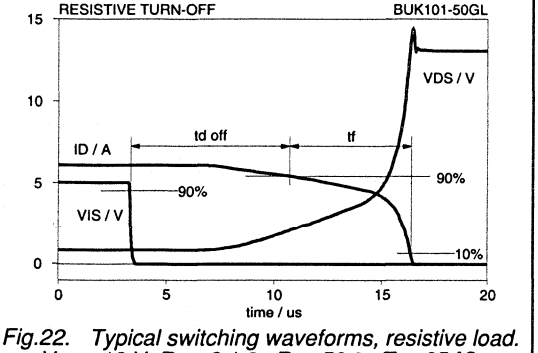


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 °C.

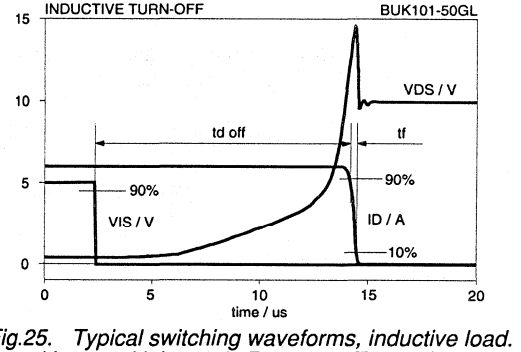


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 10 V; I_D = 6 A; R_I = 50 Ω, T_j = 25 °C.

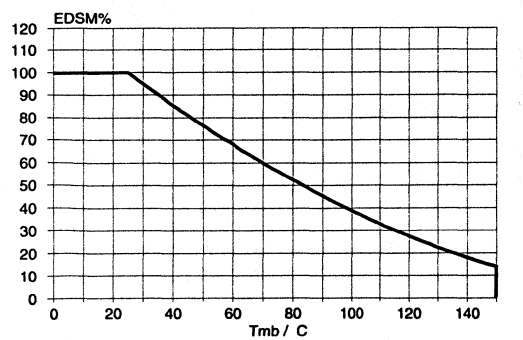


Fig.26. Normalised clamping energy rating. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 26 A; V_{IS} = 5 V

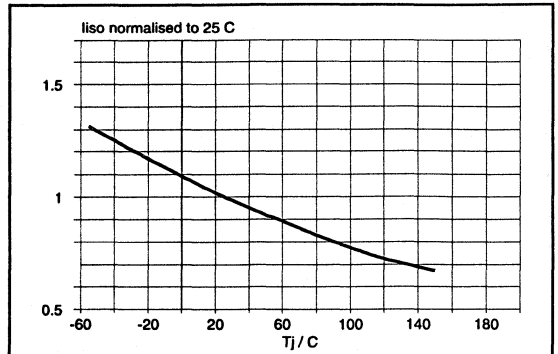


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^\circ C = f(T_j)$; V_{IS} = 5 V

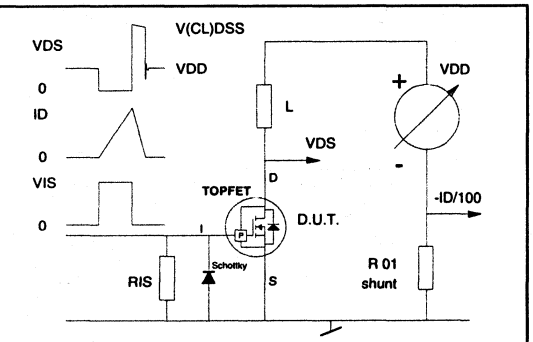


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.
$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$

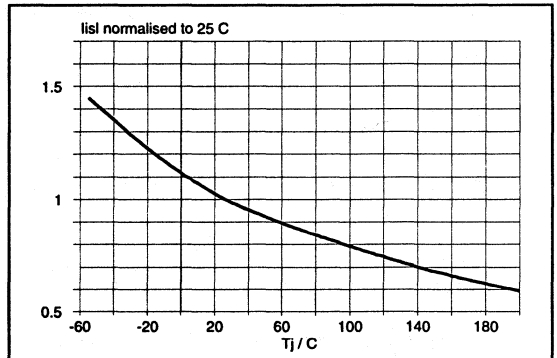


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^\circ C = f(T_j)$; V_{IS} = 5 V

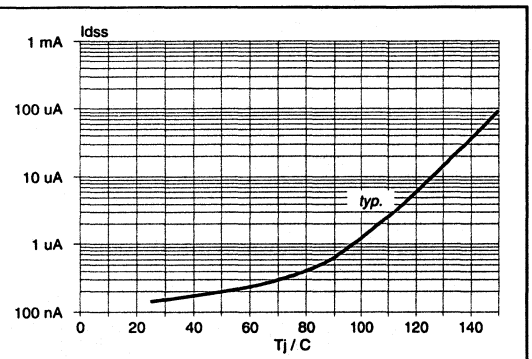


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

PowerMOS transistor TOPFET

BUK101-50GS

DESCRIPTION

Monolithic temperature and overload protected power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 10 V input level
- Low threshold voltage also allows 5 V control
- Control of power MOSFET and supply of overload protection circuits derived from input
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	29	A
P_D	Total power dissipation	75	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 10 V	50	mΩ

FUNCTIONAL BLOCK DIAGRAM

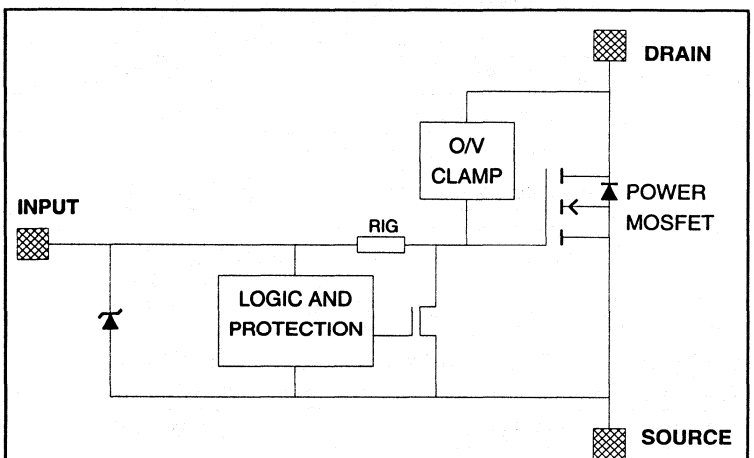
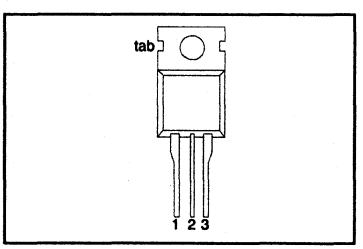


Fig.1. Elements of the TOPFET.

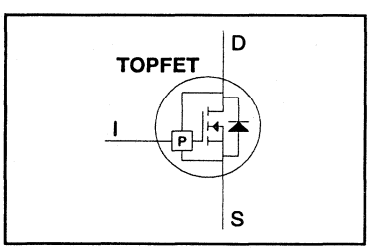
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	11	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	29	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 10 V	-	18	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	120	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	75	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	5	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V	-	20	V
		V_{IS} = 5 V	-	35	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	1.3	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	29	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 27 A; $V_{DD} \leq 20$ V; inductive load	-	625	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; I_{DM} = 8 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	40	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.3	1.67	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA		50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$		-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V		-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V		-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	I_{DM} = 13 A; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	V_{IS} = 10 V	-	35	50	mΩ
			V_{IS} = 5 V	-	45	60	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 10 V	-	0.4	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 10 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 10 V; from $I_D \geq 1$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 10 V; normal operation	-	0.4	1.0	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 10 V; protection latched	1.0	2.5	4.0	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	11	13	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	4	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 13 A $t_p \leq 300$ µs; $\delta \leq 0.01$	10	16	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 10 V	-	80	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 10 V	-	1.5	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	6	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	18	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	9	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 10 V; V_{IS} = 10 V	-	2	-	µs
t_r	Rise time	inductive load I_{DM} = 6 A	-	1	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 10 V; V_{IS} = 0 V	-	22	-	µs
t_f	Fall time	inductive load I_{DM} = 6 A	-	1	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	29	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 29 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

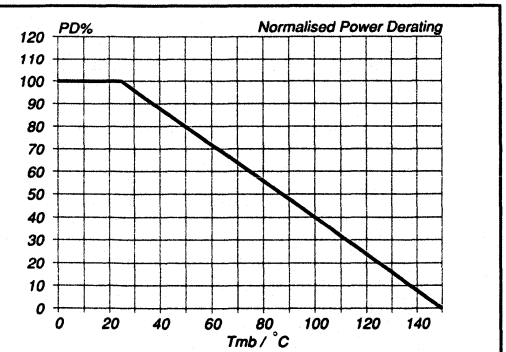


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D / P_D(25\ ^\circ C) = f(T_{mb})$

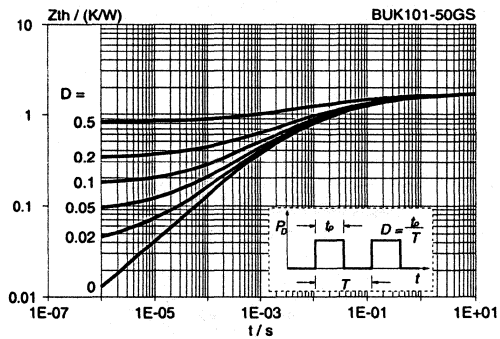


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

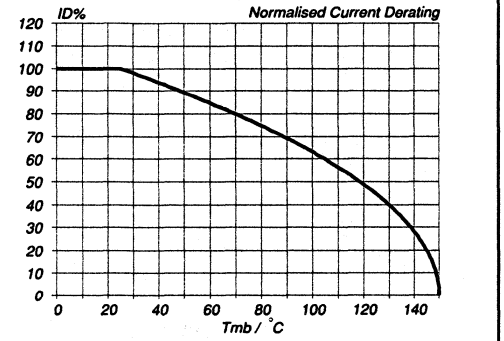


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D / I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

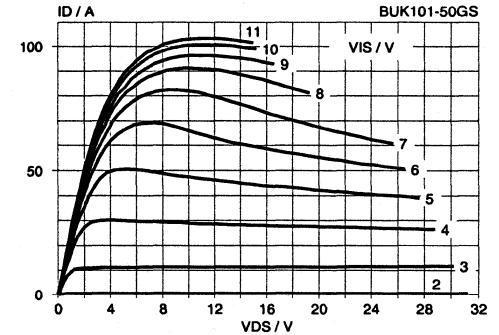


Fig.6. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

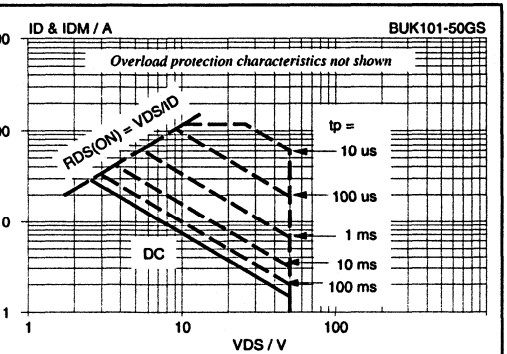


Fig.4. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

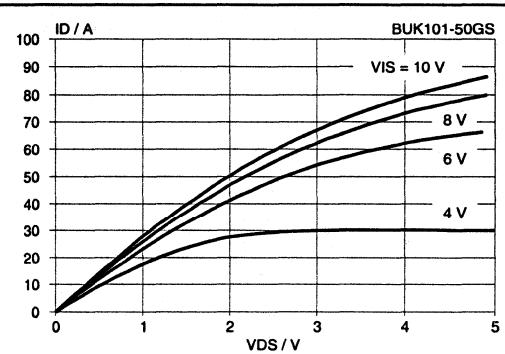


Fig.7. Typical on-state characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

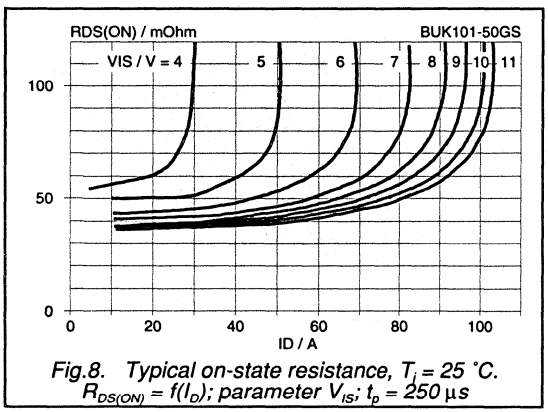


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

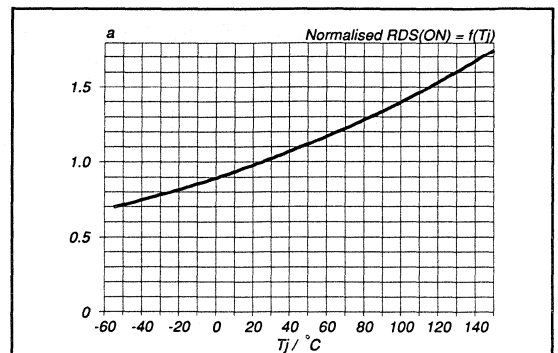


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ °C = f(T_j)$; I_D = 13 A; V_{IS} = 10 V

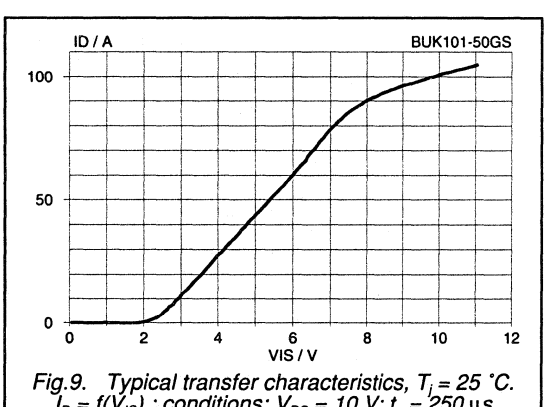


Fig.9. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

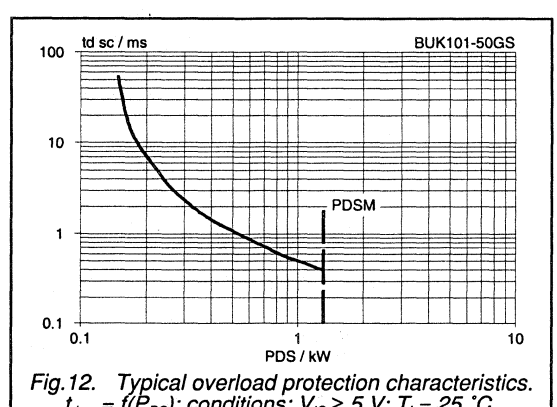


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq$ 5 V; T_j = 25 °C.

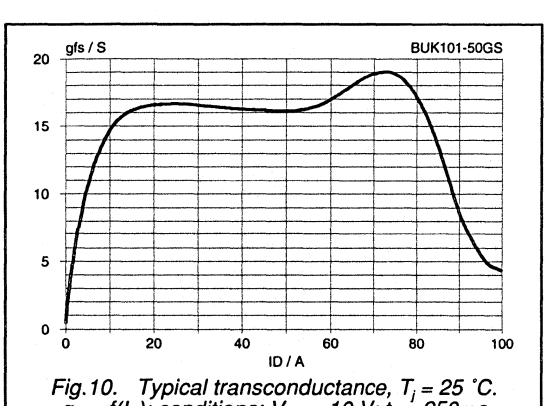


Fig.10. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

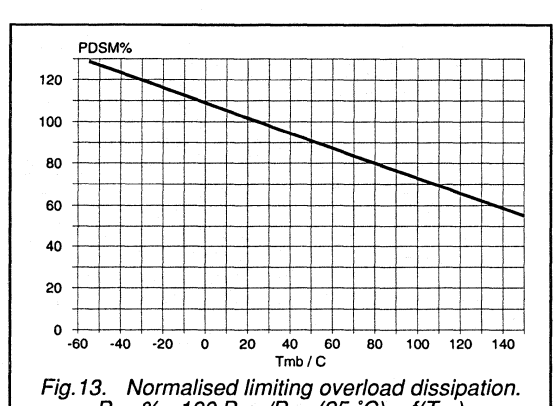


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

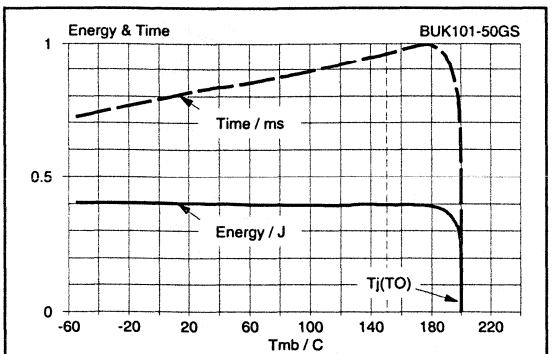


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 10 V; SC load = 30 mΩ

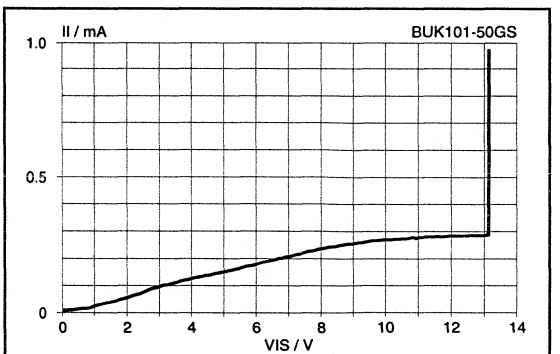


Fig.17. Typical DC input characteristics, T_j = 25 °C. $I_{IS} = f(V_{IS})$; normal operation

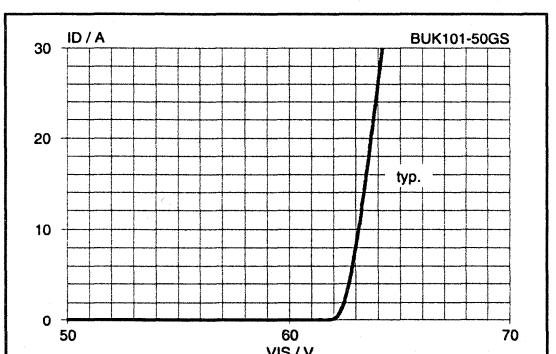


Fig.15. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

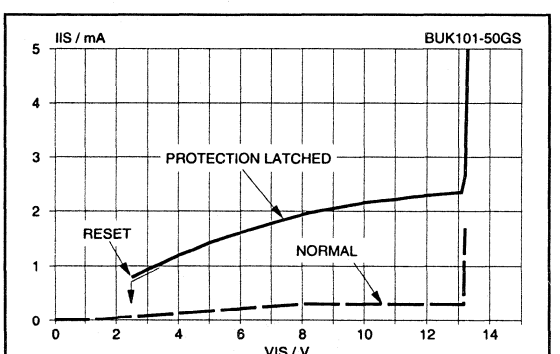


Fig.18. Typical DC input characteristics, T_j = 25 °C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

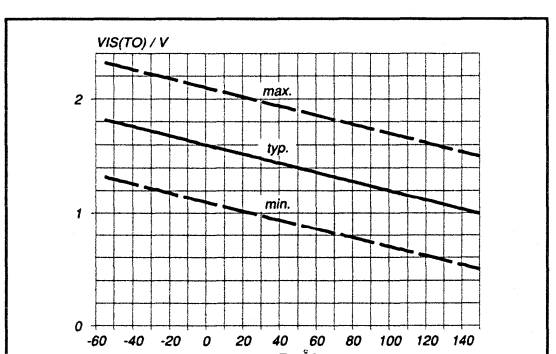


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

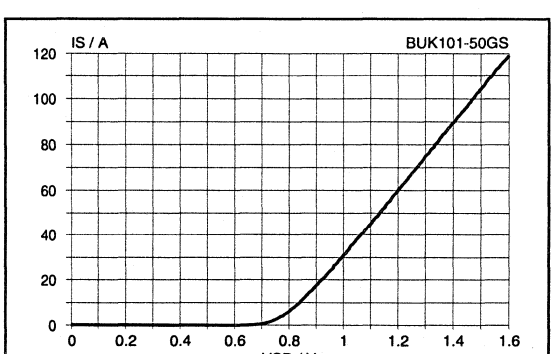


Fig.19. Typical reverse diode current, T_j = 25 °C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

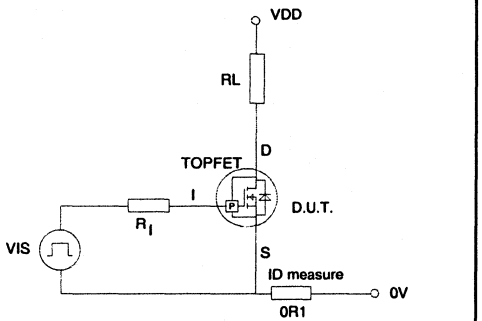


Fig.20. Test circuit for resistive load switching times.

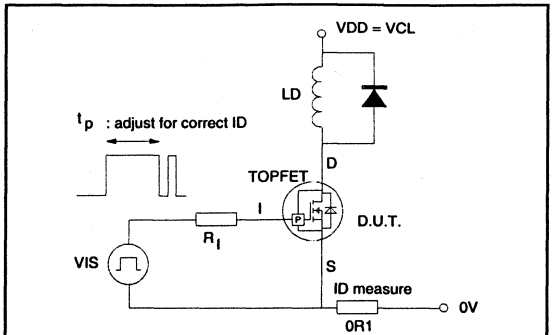


Fig.23. Test circuit for inductive load switching times.

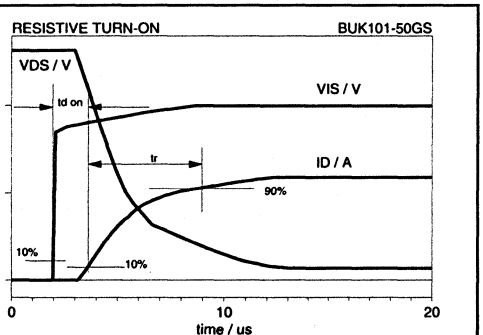


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 °C.

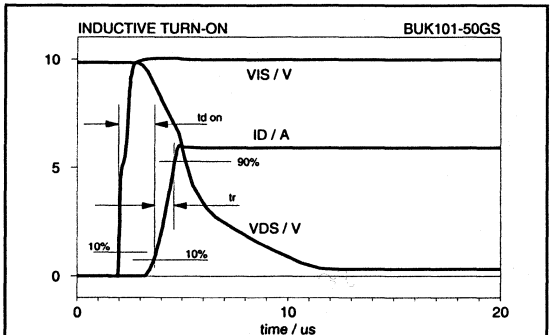


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 10 V; I_D = 6 A; R_I = 50 Ω, T_j = 25 °C.

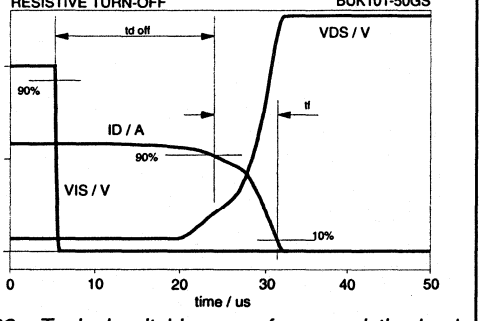


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 °C.

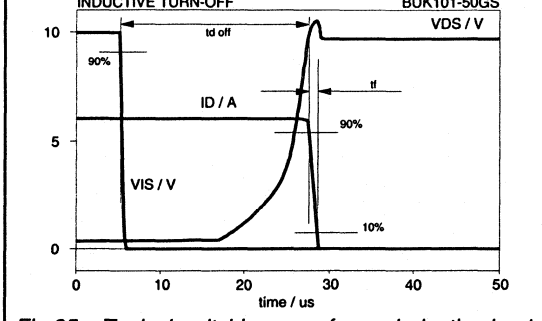


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 10 V; I_D = 6 A; R_I = 50 Ω, T_j = 25 °C.

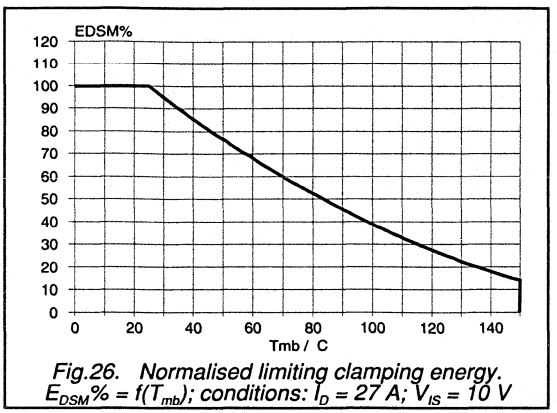


Fig.26. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 27 A; V_{IS} = 10 V

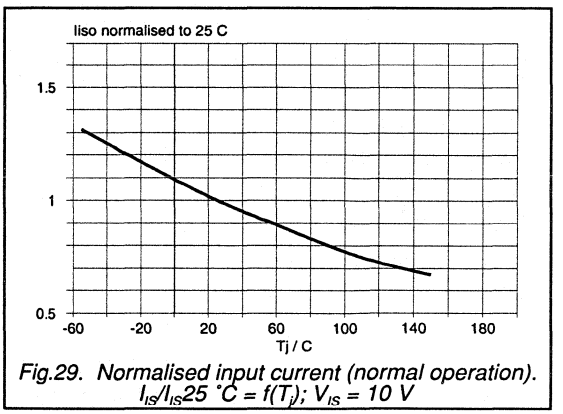


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^{\circ}C = f(T_j)$; V_{IS} = 10 V

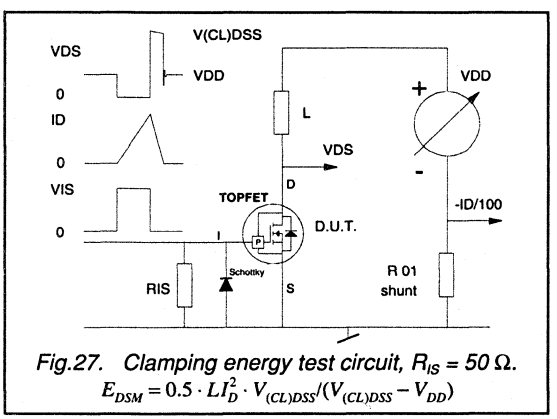


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

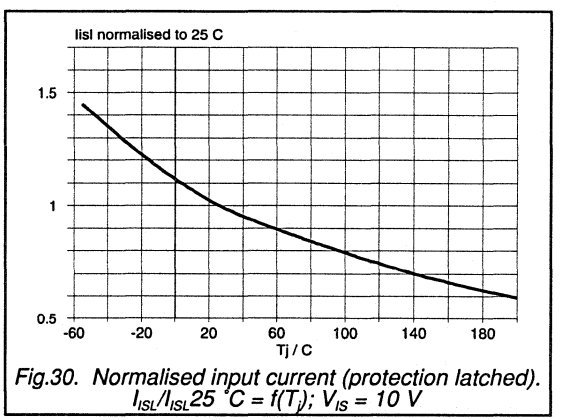


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^{\circ}C = f(T_j)$; V_{IS} = 10 V

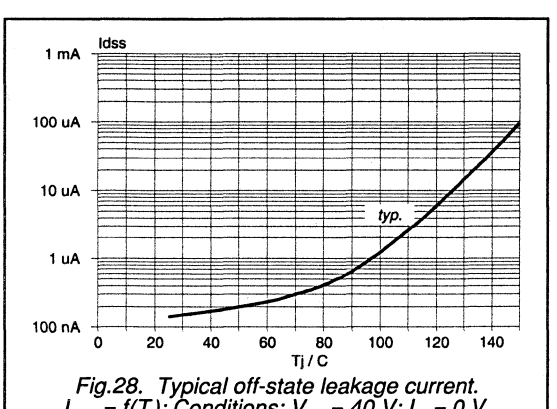


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

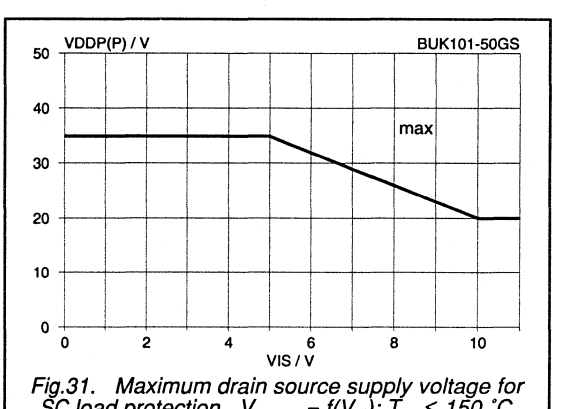


Fig.31. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150\ ^{\circ}C$

PowerMOS transistor Logic level TOPFET

BUK102-50DL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Lower operating input current permits direct drive by micro-controller
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MAX.	UNIT
V_{DS}	Continuous drain source voltage		50	V
I_D	Continuous drain current		45	A
P_D	Total power dissipation		125	W
T_j	Continuous junction temperature		150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		35	mΩ
I_{ISL}	Input supply current	V_{IS} = 5 V	650	µA

FUNCTIONAL BLOCK DIAGRAM

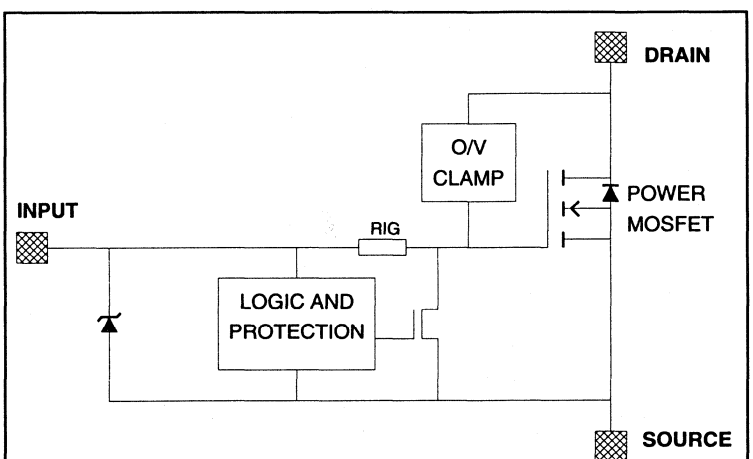
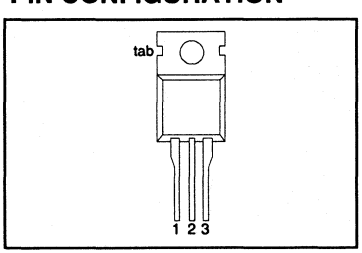


Fig.1. Elements of the TOPFET.

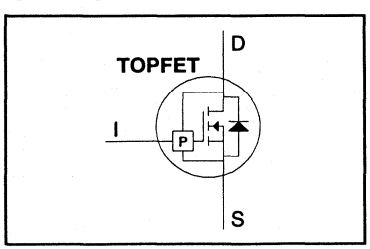
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	45	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; $V_{IS} = 5$ V	-	28	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	180	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 5$ V	-	50	V
	Short circuit load protection[4]				
$V_{DDP(P)}$	Protected drain source supply voltage[5]	$V_{IS} = 5$ V	-	16	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25$ °C	-	2.1	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0$ V	-	45	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; $I_{DM} = 25$ A; $V_{DD} \leq 20$ V; inductive load	-	1	J
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 85$ °C; $I_{DM} = 16$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	80	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

5 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than $V_{DDP(P)}$ maximum.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 4 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[1]	V_{IS} = 5 V; I_{DM} = 25 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	30	35	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[2]	T_{mb} = 25 °C; L ≤ 10 µH; R_L = 10 mΩ				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	1.1	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
$I_{D(SC)}$	Drain current[3]	V_{DD} = 13 V; V_{IS} = 5 V	-	75	-	A
$I_{DM(SC)}$	Peak drain current[4]	V_{IS} = 5 V; V_{DD} = 13 V	-	200	-	A
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 2$ A[5]	150	-	-	°C

TRANSFER CHARACTERISTIC

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 25 A $t_p \leq 300$ µs; $\delta \leq 0.01$	17	28	-	S

1 Continuous input voltage. The specified pulse width is for the drain current.

2 Refer to OVERLOAD PROTECTION LIMITING VALUES.

3 Continuous drain-source supply voltage. Pulsed input voltage.

4 Continuous input voltage. Momentary short circuit load connection. (The higher peak current is due to the effect of capacitance Cgd).

5 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	100	200	350	µA
			V_{IS} = 4 V	-	160	270	µA
V_{ISR}	Protection reset voltage[1]		T_j = 25 °C	2.0	2.6	3.5	V
			T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	330	650	µA
			V_{IS} = 3.5 V	-	240	430	µA
$V_{(BR)IS}$	Input breakdown voltage	I_I = 10 mA		6	-	-	V
R_{IG}	Input series resistance		T_j = 25 °C	-	33	-	kΩ
	to gate of power MOSFET		T_j = 150 °C	-	50	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	30	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	150	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	120	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	120	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	45	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDO}	Forward voltage	I_S = 45 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

1 The input voltage below which the overload protection circuits will be reset.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

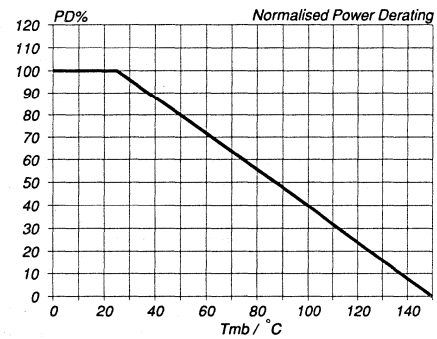


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

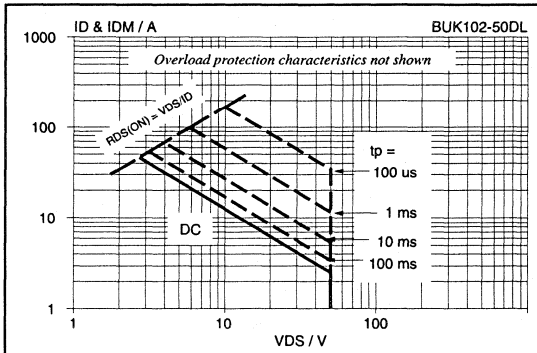


Fig.4. Safe operating area. T_{mb} = 25 °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

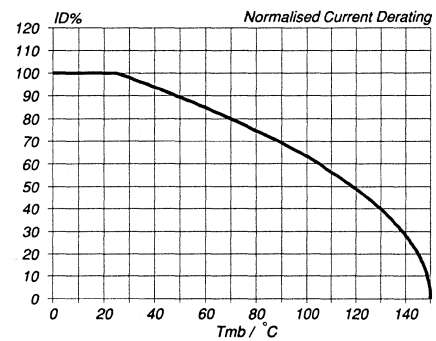


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: V_{IS} = 5 V

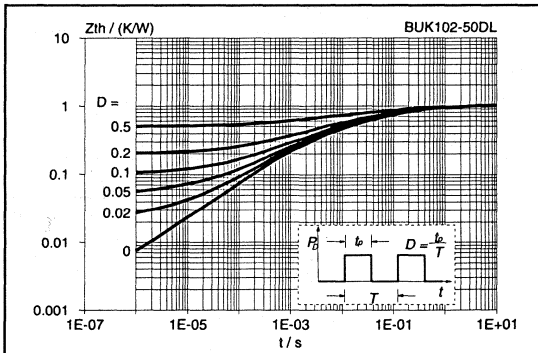


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

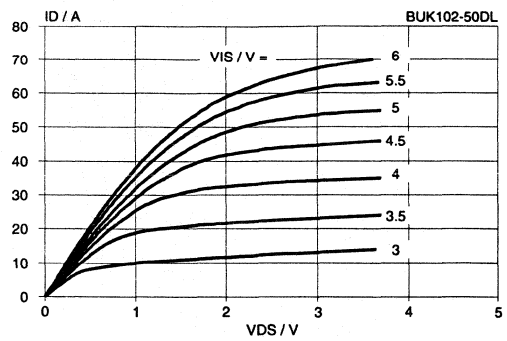


Fig.6. Typical on-state characteristics, T_j = 25 °C. ID = f(V_{DS}); parameter V_{IS}; t_p = 2 ms

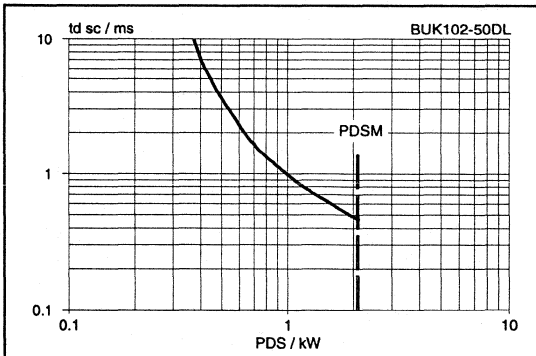


Fig.9. Typical overload protection characteristics. $t_{d\,sc}$ = f(P_{DS}); conditions: $V_{IS} \geq$ 4 V; T_j = 25 °C.

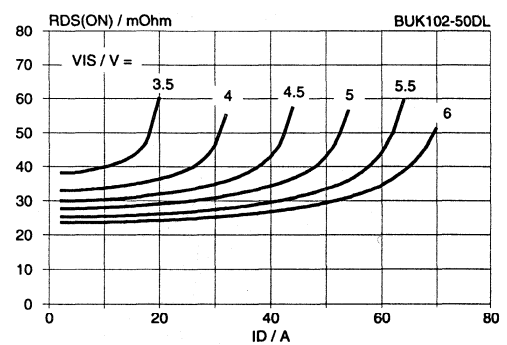


Fig.7. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)}$ = f(I_D); parameter V_{IS}; t_p = 2 ms

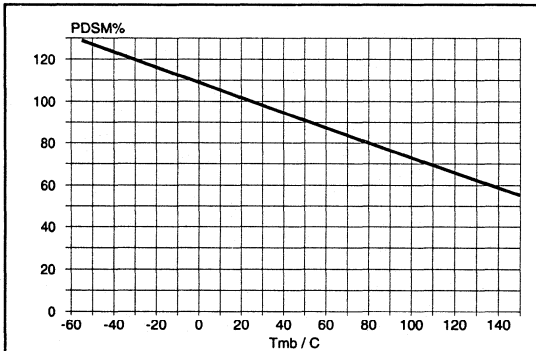


Fig.10. Normalised limiting overload dissipation. P_{DSM}% =100·P_{DSM}/P_{DSM}(25 °C) = f(T_{mb})

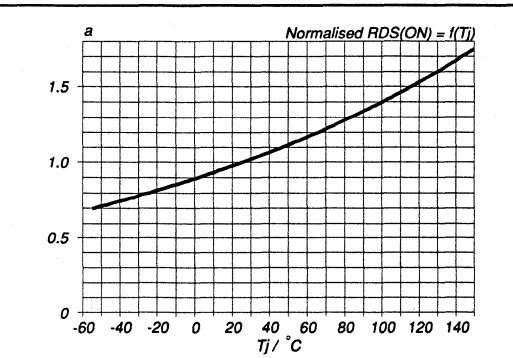


Fig.8. Normalised drain-source on-state resistance. a = $R_{DS(ON)}$/$R_{DS(ON)}$25 °C = f(T_j); I_D = 25 A; V_{IS} = 5 V

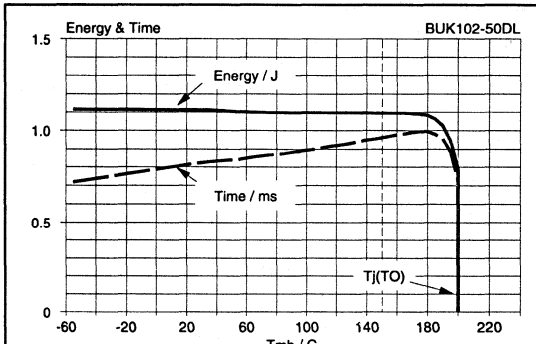


Fig.11. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

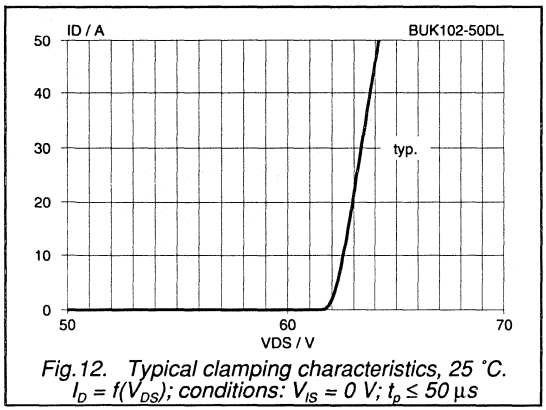


Fig.12. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50$ µs

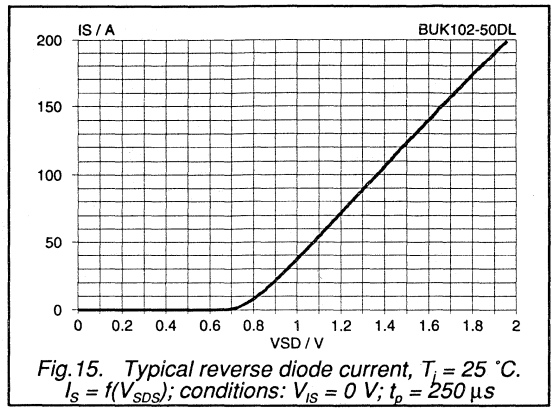


Fig.15. Typical reverse diode current, $T_j = 25$ °C. $I_S = f(V_{SDS})$; conditions: $V_{IS} = 0$ V; $t_p = 250$ µs

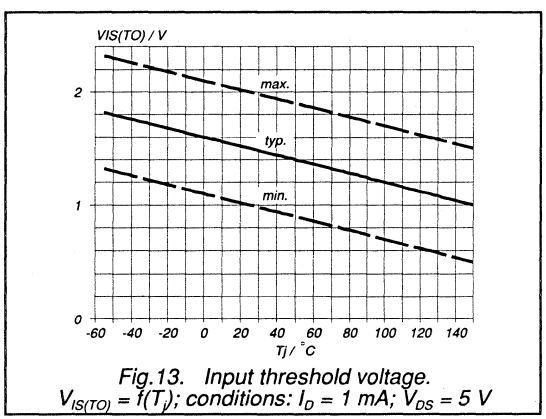


Fig.13. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

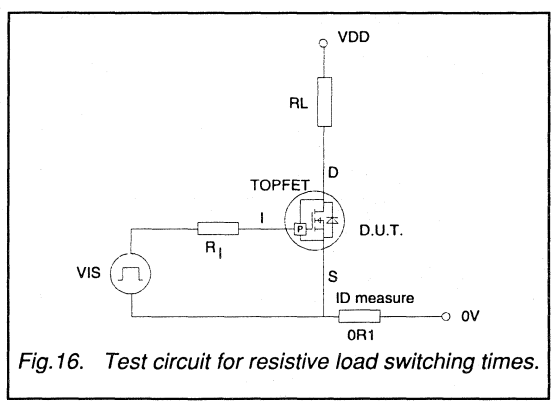


Fig.16. Test circuit for resistive load switching times.

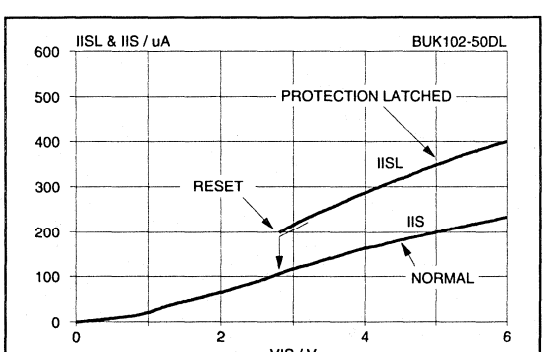


Fig.14. Typical DC input characteristics, $T_j = 25$ °C. I_{ISL} & $I_{IS} = f(V_{IS})$; protection latched & normal operation

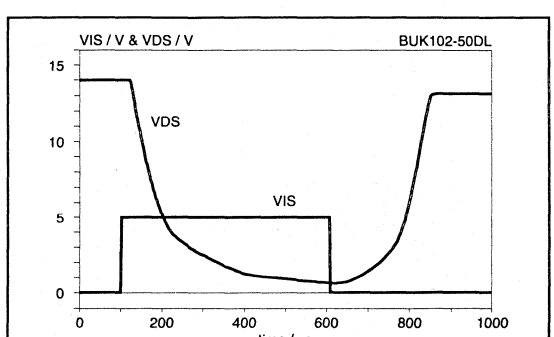


Fig.17. Typical switching waveforms, resistive load. $V_{DD} = 13$ V; $R_L = 1.1\ \Omega$; $R_I = 50\ \Omega$, $T_j = 25$ °C.

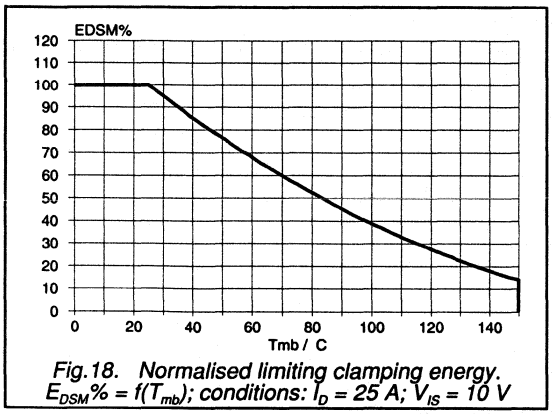


Fig.18. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: $I_D = 25$ A; $V_{IS} = 10$ V

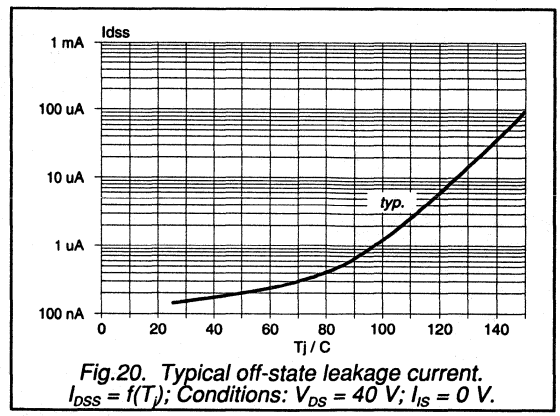


Fig.20. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: $V_{DS} = 40$ V; $I_{IS} = 0$ V.

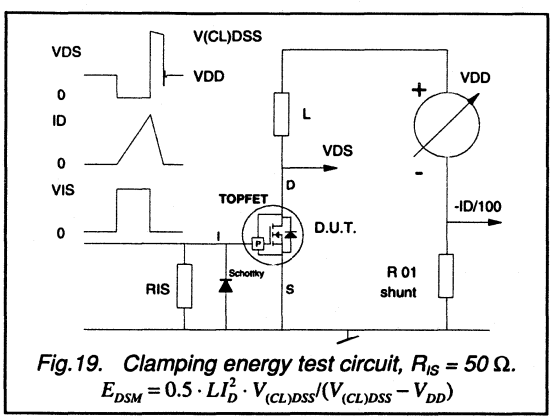


Fig.19. Clamping energy test circuit, $R_{IS} = 50\ \Omega$.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

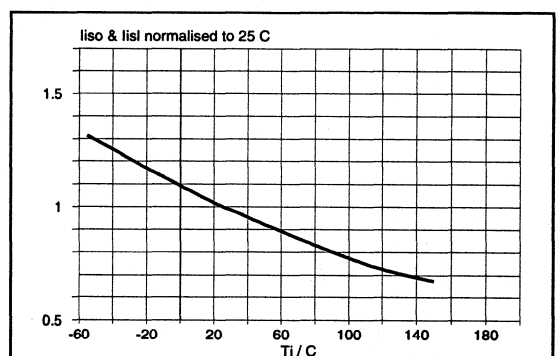


Fig.21. Normalised input currents (normal & latched). $I_{ISO}/I_{ISO}25^{\circ}C$ & $I_{ISL}/I_{ISL}25^{\circ}C = f(T_j)$; $V_{IS} = 5$ V

PowerMOS transistor Logic level TOPFET

BUK102-50GL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V input level
- Low threshold voltage also allows 5 V control
- Control of power MOSFET and supply of overload protection circuits derived from input
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	45	A
P_D	Total power dissipation	125	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 5 V	35	mΩ

FUNCTIONAL BLOCK DIAGRAM

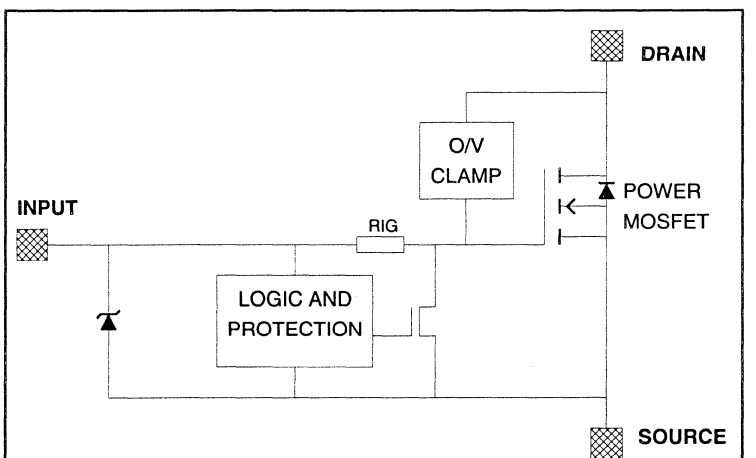
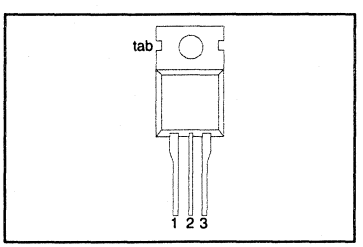


Fig.1. Elements of the TOPFET.

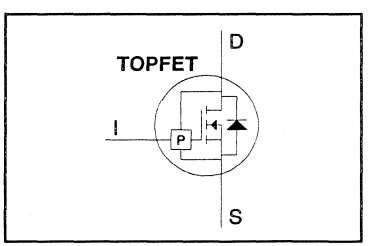
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	45	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 5 V	-	28	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	180	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 5 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 5 V	-	24	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	2.1	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	45	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 25 A; $V_{DD} \leq 25$ V; inductive load	-	1	J
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 85$ °C; I_{DM} = 16 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	80	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1.0	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	I_{DM} = 25 A; V_{IS} = 5 V; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	-	30	35	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	1.1	-	J
$t_{d\,sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 2$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 5 V; normal operation	-	0.2	0.35	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 5 V; protection latched	2	3.8	10	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	6	-	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	1.5	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 25 A $t_p \leq 300$ μs; $\delta \leq 0.01$	17	28	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 5 V	-	60	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	2	-	μs
t_r	Rise time	resistive load R_L = 1.1 Ω	-	8	-	μs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	8	-	μs
t_f	Fall time	resistive load R_L = 1.1 Ω	-	8	-	μs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	3.7	-	μs
t_r	Rise time	inductive load I_{DM} = 11 A	-	3.7	-	μs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	13	-	μs
t_f	Fall time	inductive load I_{DM} = 11 A	-	1.4	-	μs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	50	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 50 A; V_{IS} = 0 V; t_p = 300 μs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

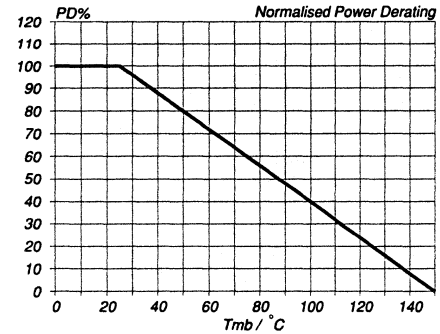


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

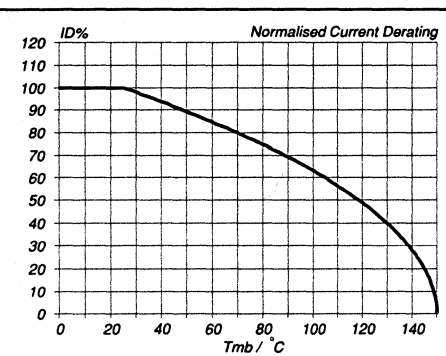


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; *conditions:* $V_{IS} = 5$ V

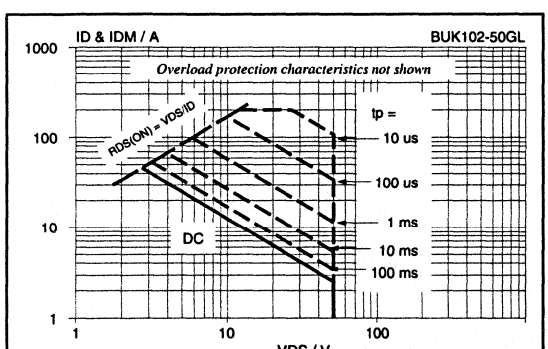


Fig.4. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} *single pulse; parameter* t_p

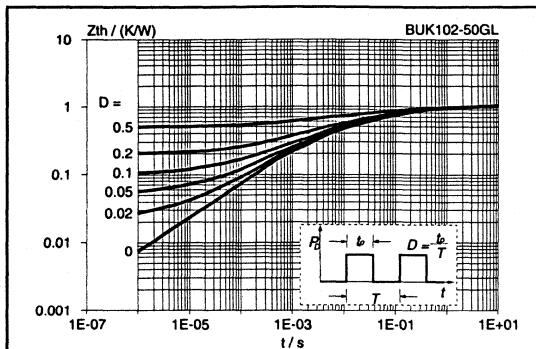


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; *parameter* $D = t_p/T$

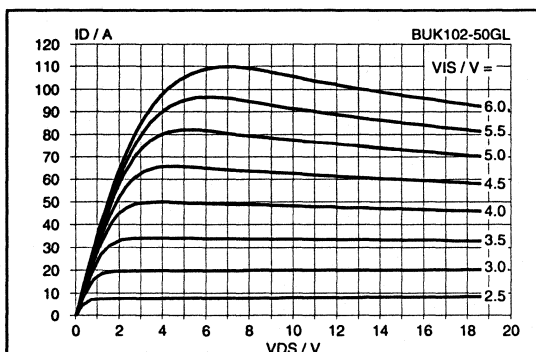


Fig.6. Typical output characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; *parameter* V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

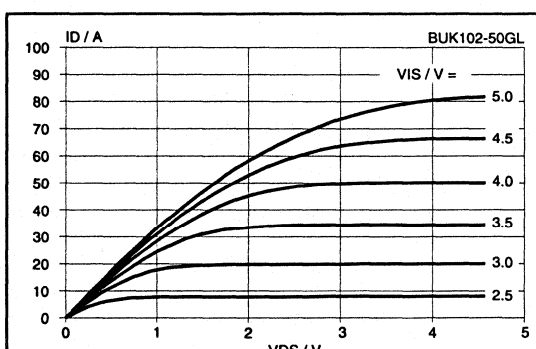


Fig.7. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; *parameter* V_{IS}; $t_p = 250\ \mu s$

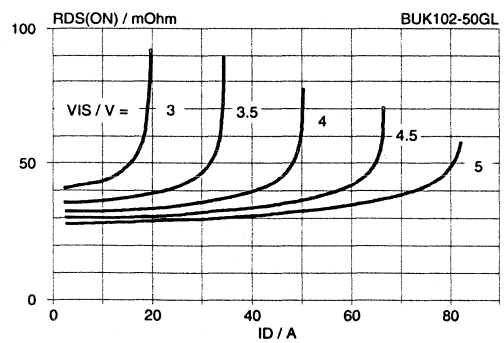


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

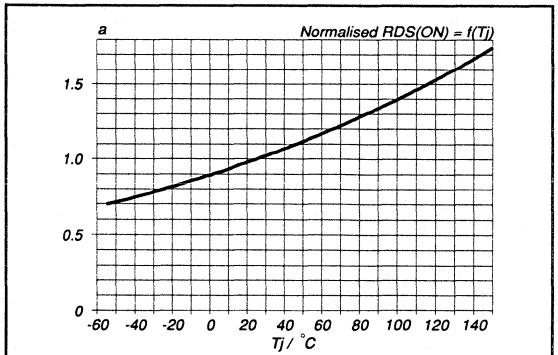


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}$25 °C = $f(T_j)$; I_D = 25 A; V_{IS} = 5 V

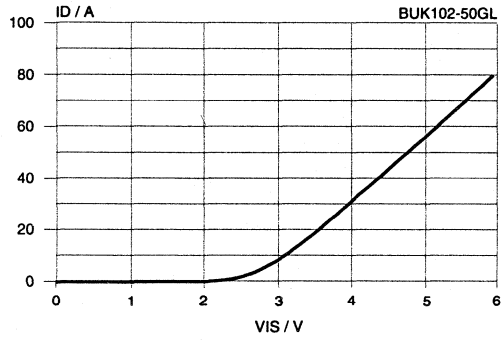


Fig.9. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

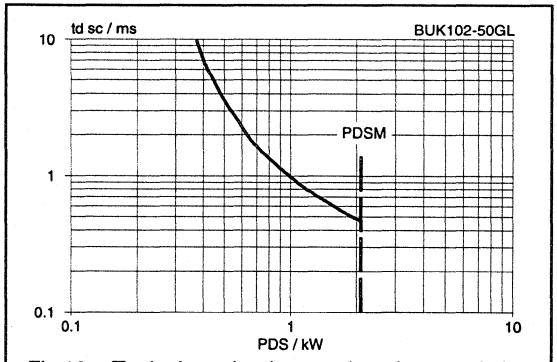


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; T_j = 25 °C.

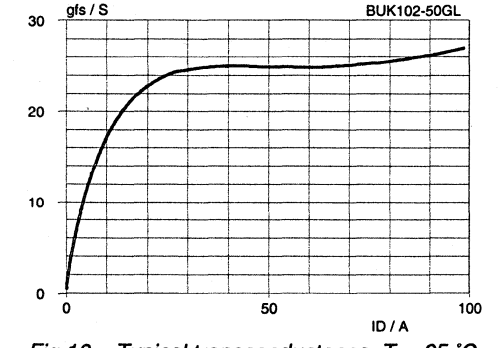


Fig.10. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

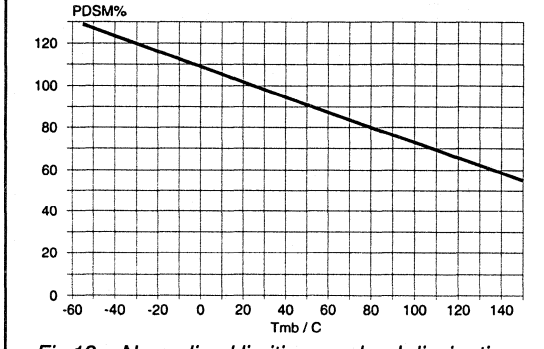


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

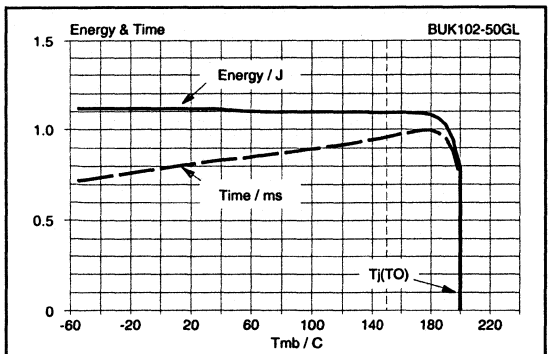


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

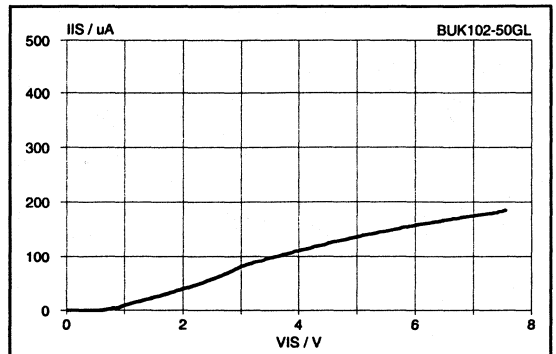


Fig.17. Typical DC input characteristics, T_j = 25 °C. $I_{IS} = f(V_{IS})$; normal operation

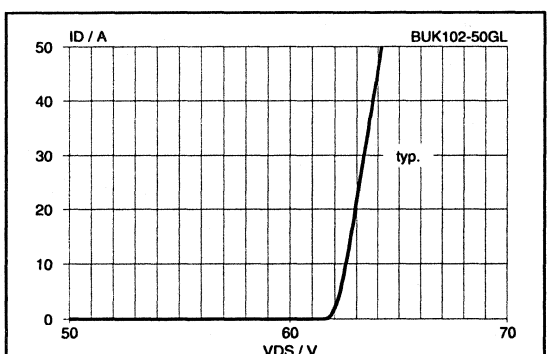


Fig.15. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

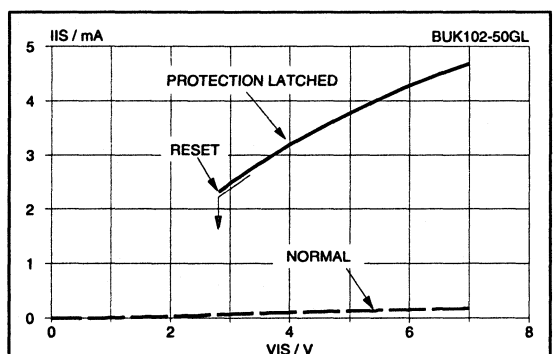


Fig.18. Typical DC input characteristics, T_j = 25 °C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

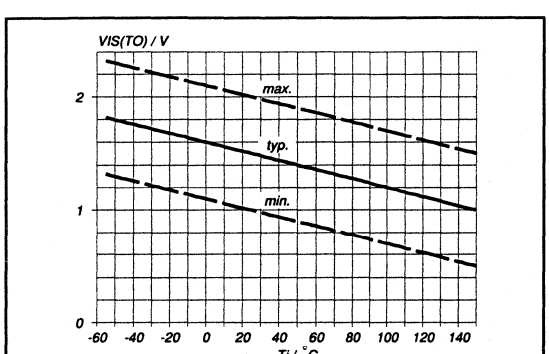


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

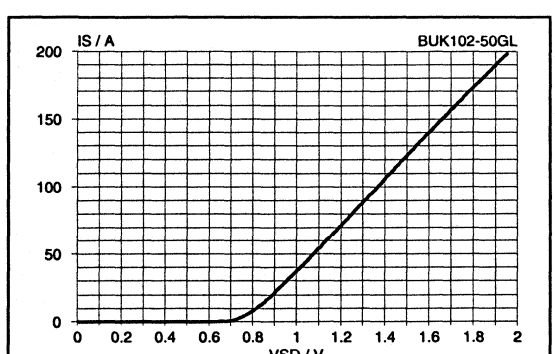


Fig.19. Typical reverse diode current, T_j = 25 °C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

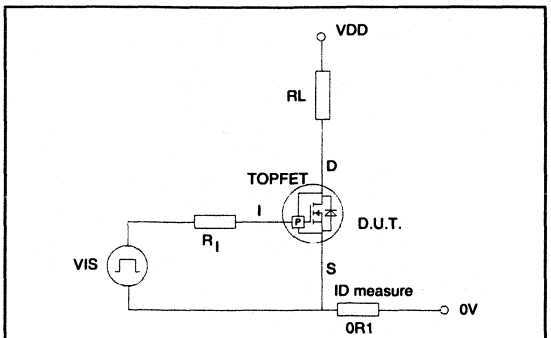


Fig.20. Test circuit for resistive load switching times.

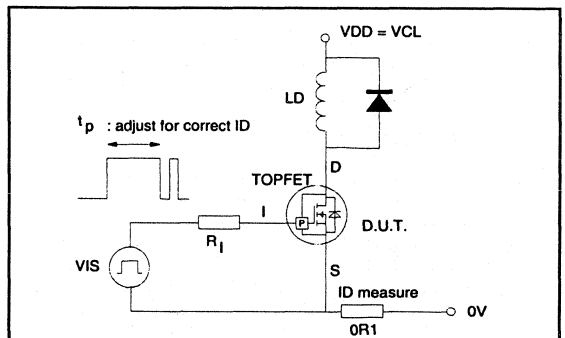


Fig.23. Test circuit for inductive load switching times.

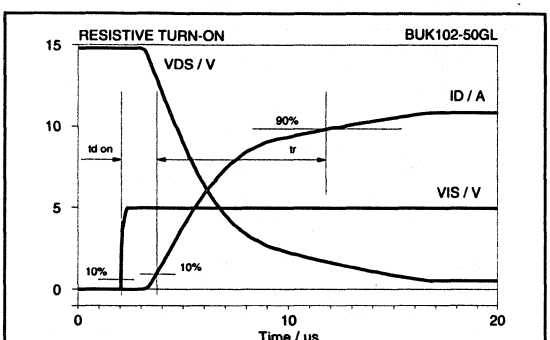


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 °C.

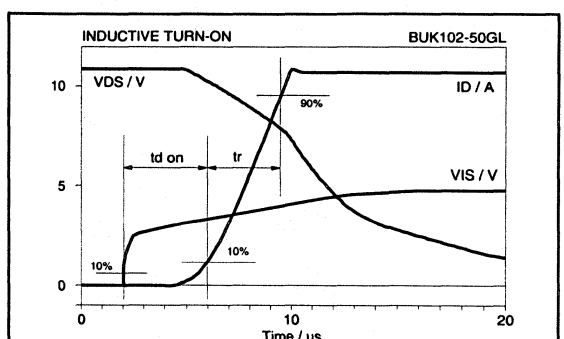


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 11 A; R_I = 50 Ω, T_j = 25 °C.

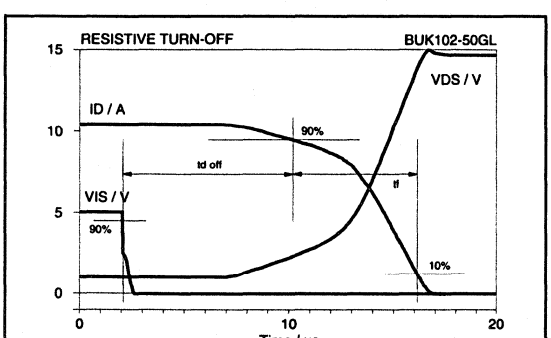


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 °C.

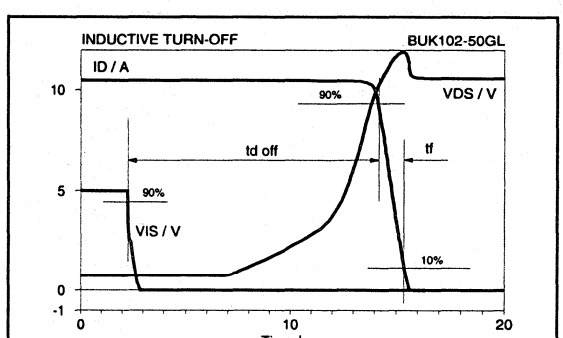


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 11 A; R_I = 50 Ω, T_j = 25 °C.

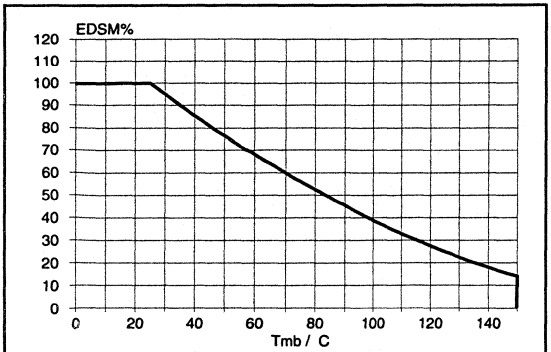


Fig.26. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 25 A; V_{IS} = 10 V

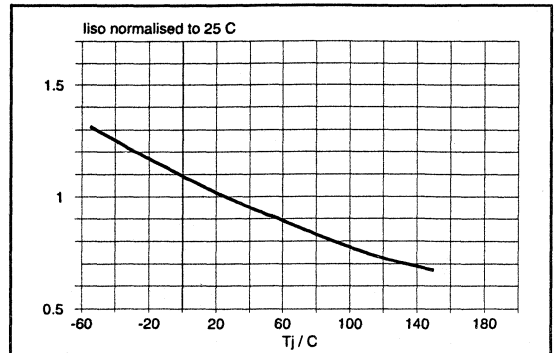


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^{\circ}C = f(T_j)$; V_{IS} = 5 V

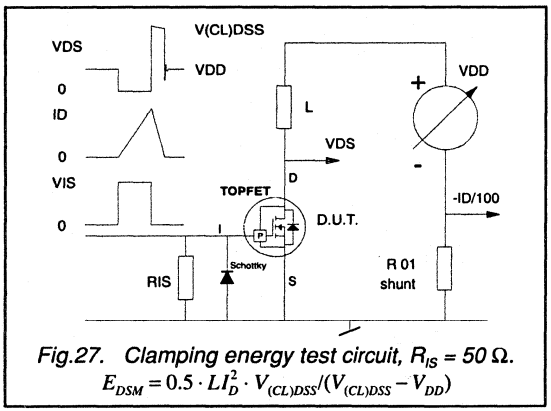


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

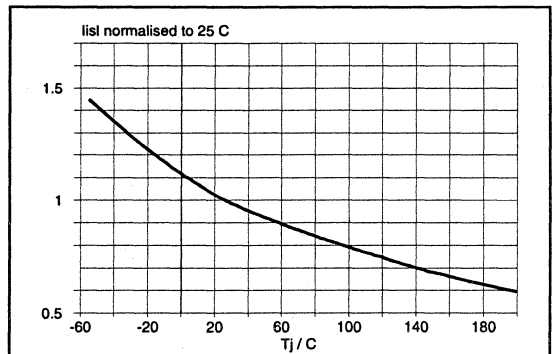


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^{\circ}C = f(T_j)$; V_{IS} = 5 V

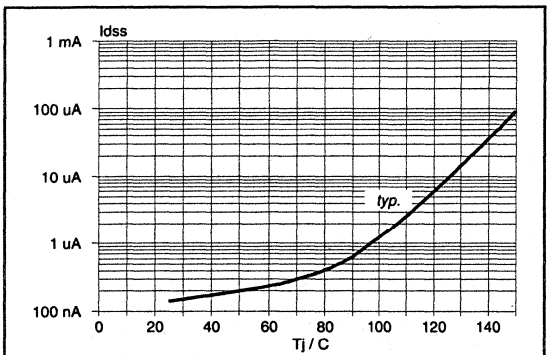


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

PowerMOS transistor TOPFET

BUK102-50GS

DESCRIPTION

Monolithic temperature and overload protected power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 10 V input level
- Low threshold voltage also allows 5 V control
- Control of power MOSFET and supply of overload protection circuits derived from input
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	50	A
P_D	Total power dissipation	125	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 10 V	28	mΩ

FUNCTIONAL BLOCK DIAGRAM

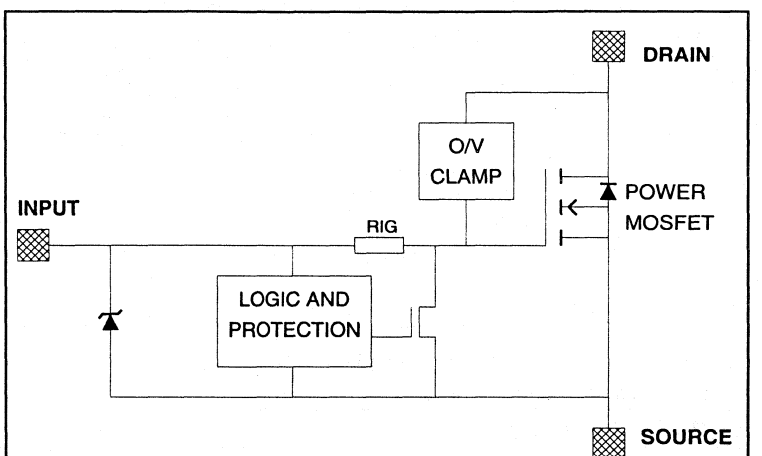
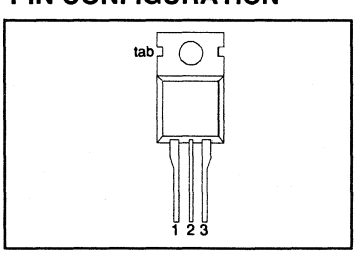


Fig.1. Elements of the TOPFET.

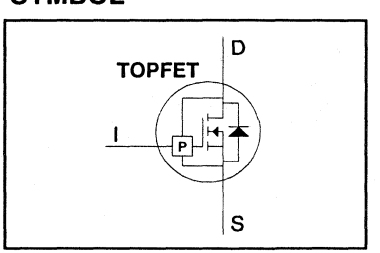
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	11	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	50	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 10 V	-	31	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	200	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	5	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V	-	16	V
		V_{IS} = 5 V	-	24	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	2.1	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	50	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 25 A; $V_{DD} \leq 25$ V; inductive load	-	1	J
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 85$ °C; I_{DM} = 16 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	80	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1.0	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA		50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \le 300$ µs; $\delta \le 0.01$		-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V		-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V		-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	I_{DM} = 25 A; $t_p \le 300$ µs; $\delta \le 0.01$	V_{IS} = 10 V	-	22	28	mΩ
			V_{IS} = 5 V	-	30	35	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 10 V	-	1.1	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 10 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 10 V; from $I_D \ge 2$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 10 V; normal operation	-	0.4	1.0	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 10 V; protection latched	2	6	20	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	11	13	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	1.5	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 25 A $t_p \leq 300$ µs; $\delta \leq 0.01$	17	28	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 10 V	-	150	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 10 V	-	1.5	-	µs
t_r	Rise time	resistive load R_L = 1.1 Ω	-	5.5	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	13	-	µs
t_f	Fall time	resistive load R_L = 1.1 Ω	-	9	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 10 V	-	1.5	-	µs
t_r	Rise time	inductive load I_{DM} = 11 A	-	1.3	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	18	-	µs
t_f	Fall time	inductive load I_{DM} = 11 A	-	1.4	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	50	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 50 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

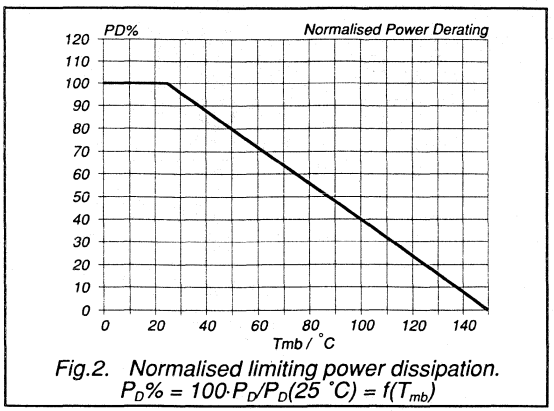


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

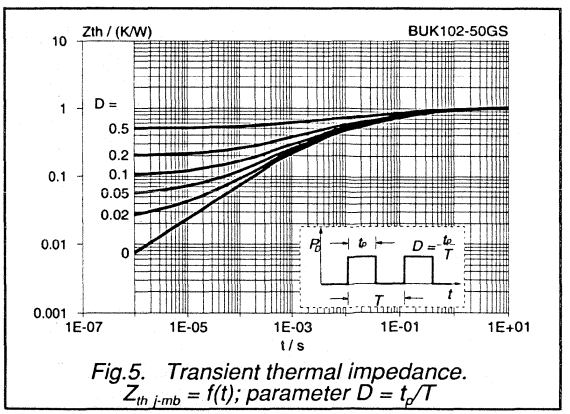


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

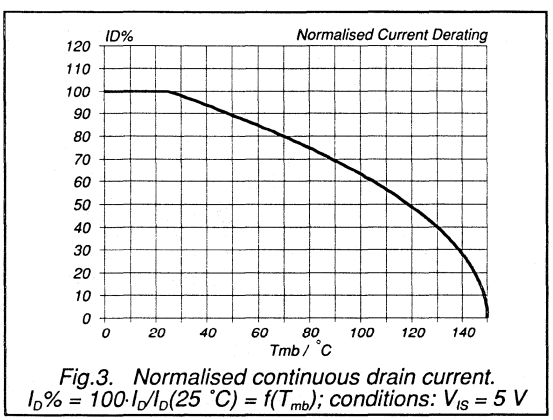


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

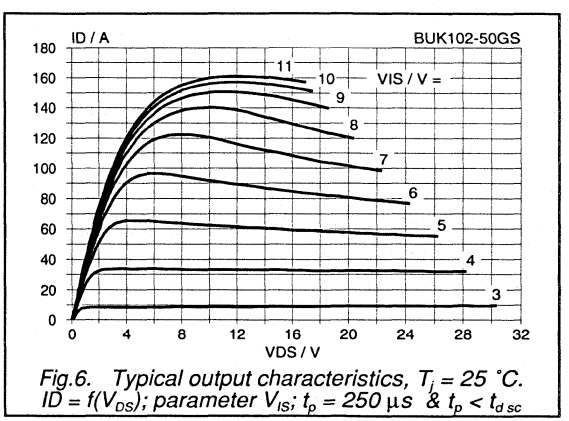


Fig.6. Typical output characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

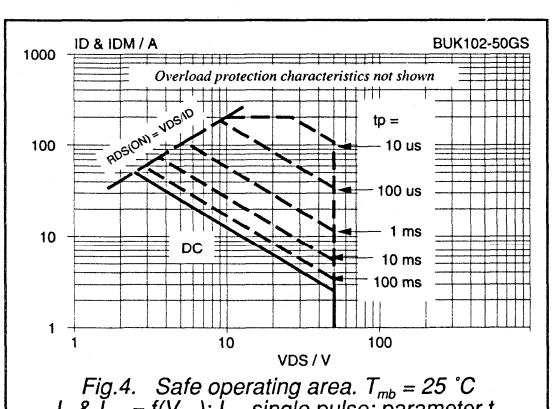


Fig.4. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

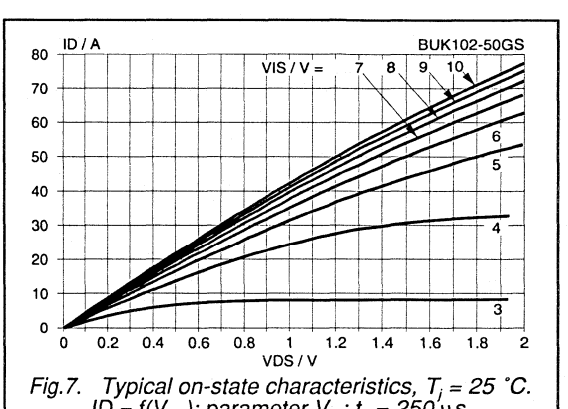


Fig.7. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

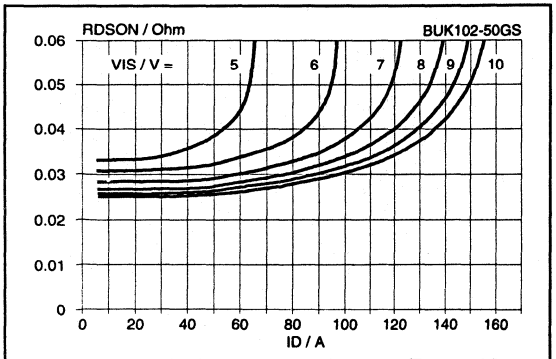


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

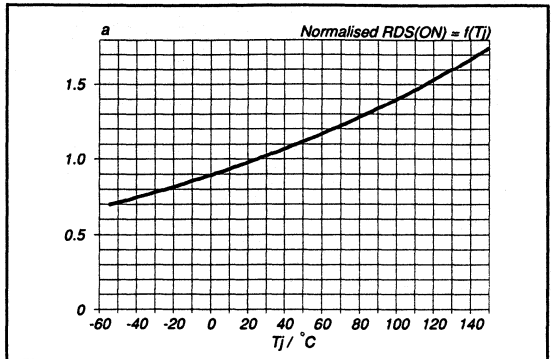


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ °C = f(T_j)$; I_D = 25 A; V_{IS} = 10 V

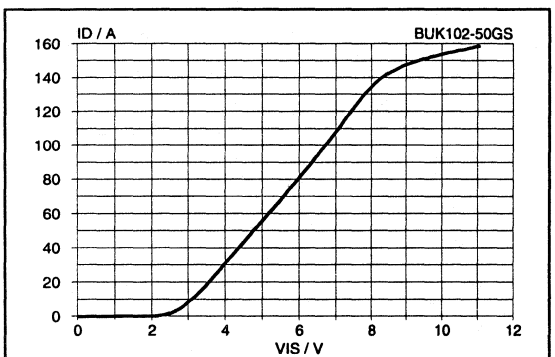


Fig.9. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

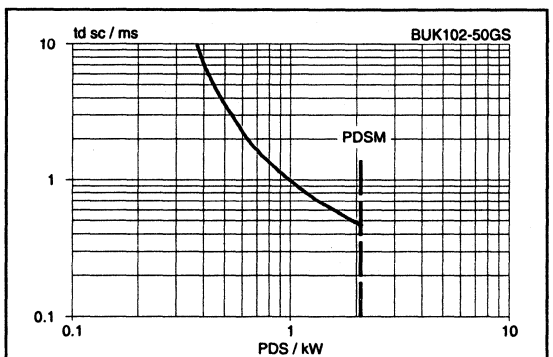


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 5$ V; T_j = 25 °C.

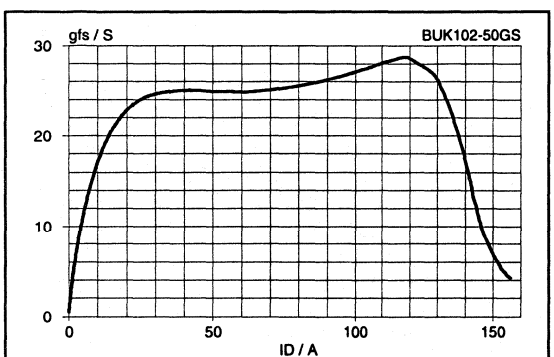


Fig.10. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

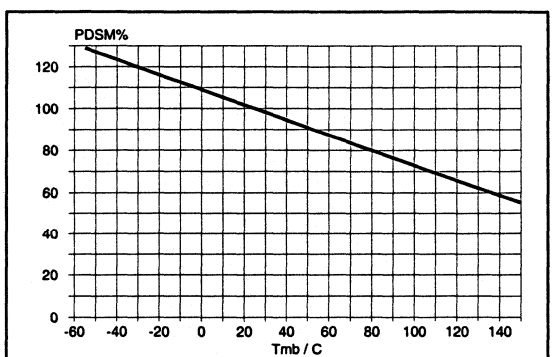


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

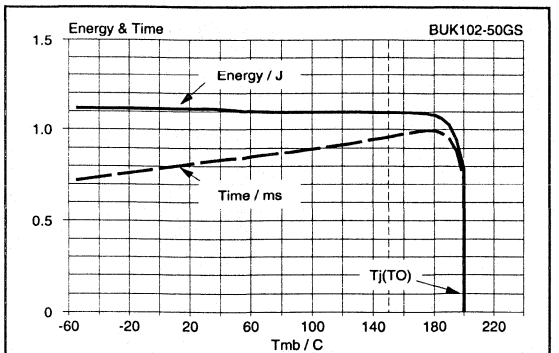


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 10 V; SC load = 30 mΩ

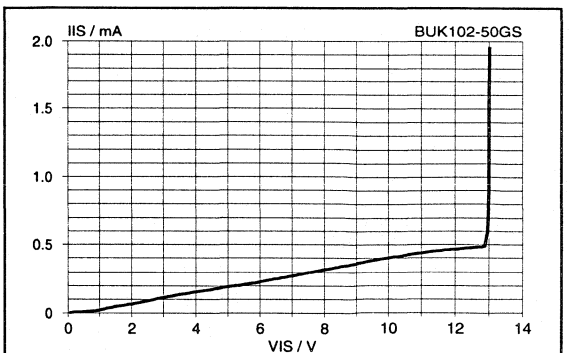


Fig.17. Typical DC input characteristics, T_j = 25 °C. $I_{IS} = f(V_{IS})$; normal operation

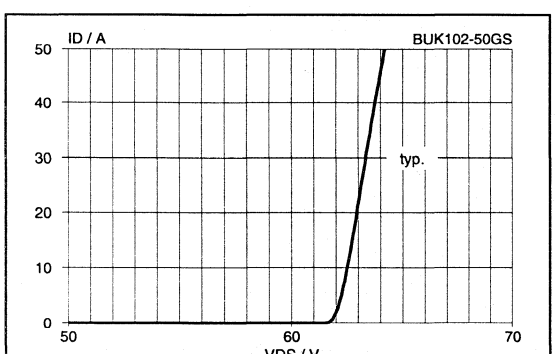


Fig.15. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

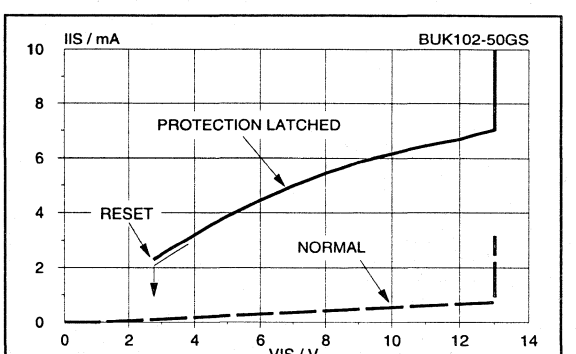


Fig.18. Typical DC input characteristics, T_j = 25 °C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

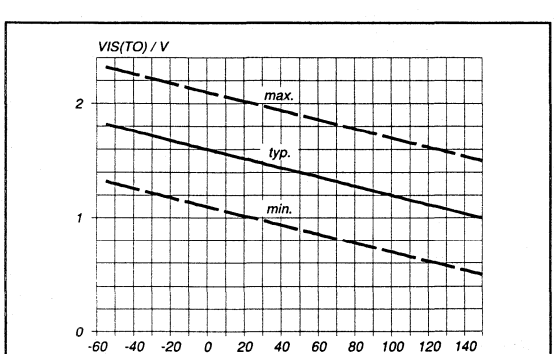


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

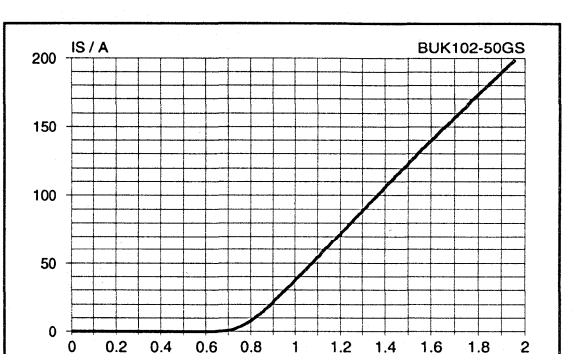


Fig.19. Typical reverse diode current, T_j = 25 °C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

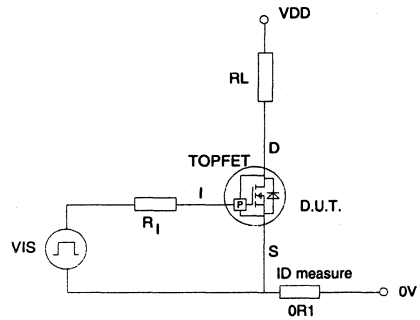


Fig.20. Test circuit for resistive load switching times.

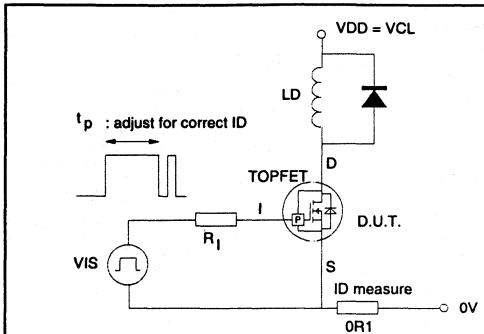


Fig.23. Test circuit for inductive load switching times.

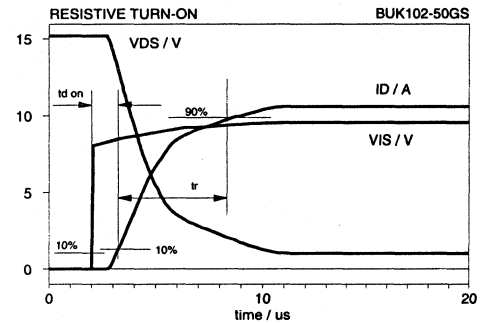


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 °C.

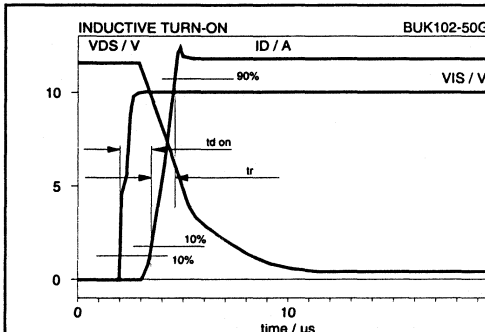


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 11 A; R_I = 50 Ω, T_j = 25 °C.

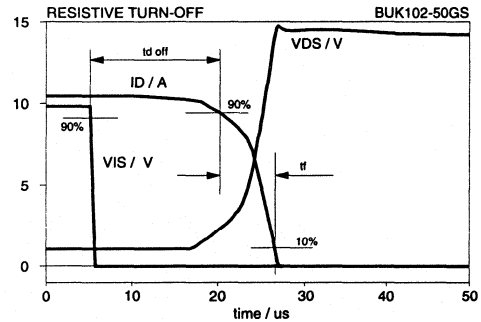


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 °C.

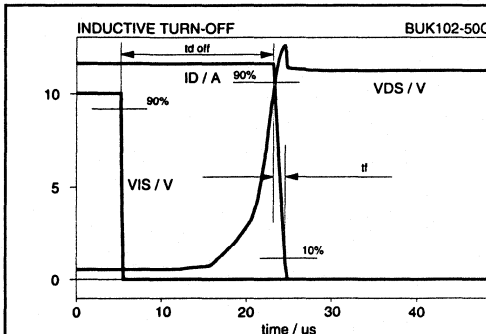


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 11 A; R_I = 50 Ω, T_j = 25 °C.

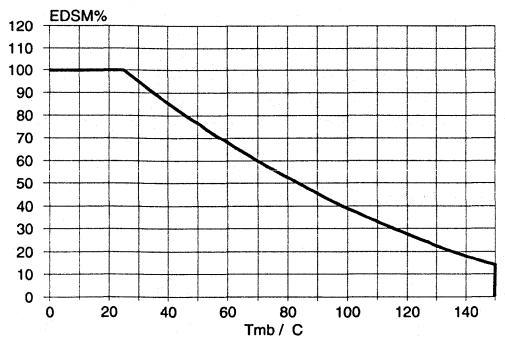


Fig.26. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 25 A; V_{IS} = 10 V

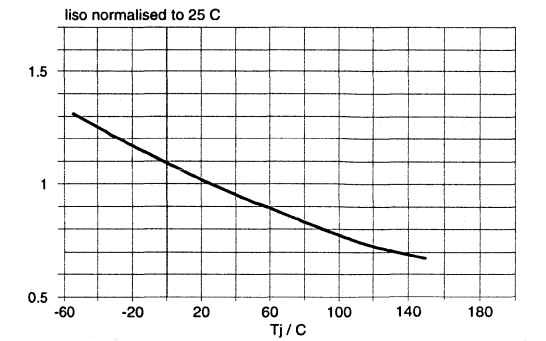


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^\circ C = f(T_j)$; V_{IS} = 10 V

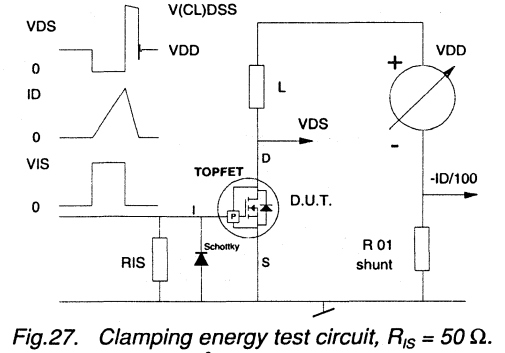


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

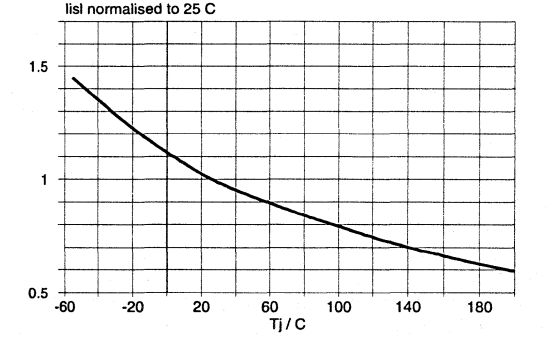


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^\circ C = f(T_j)$; V_{IS} = 10 V

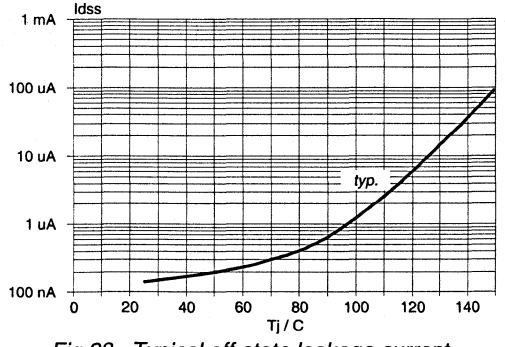


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

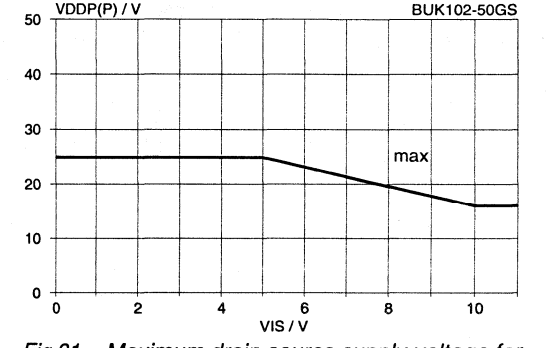


Fig.31. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150\ ^\circ C$

An introduction to the 5-pinTOFET

Application report

The TOPFET (Temperature and Overload Protected MOSFET) concept has been developed by Philips Semiconductors and is achieved by the addition of a series of dedicated on-chip protection circuits to a low voltage power MOSFET. The resulting device has the advantages of a conventional power MOSFET (low $R_{DS(on)}$, logic level gate voltage drive) with the additional benefit of integrated protection from hazardous overstress conditions.

TOPFETs are designed for operation in low voltage power applications, particularly automotive electronic systems. The operation and protection features of the TOPFET range of devices also make them suitable for other low voltage power systems. TOPFETs can be used for all common load types currently controlled by conventional power MOSFETs.

The second generation of TOPFET devices offers enhanced protection and drive capabilities making them suitable for a wide variety of applications, including those requiring fast switching (eg PWM control) or linear control. The circuit diagram for the 5-pin TOPFET types is shown in Fig. 1. The key features of these devices are:

- Overtemperature protection
- Short circuit load protection
- Overvoltage protection
- Full ESD protection
- Direct access to the gate of the Power MOSFET.
- Flag signal reporting of certain fault conditions
- Separate protection circuit supply

The 5-pin TOPFET range is summarised in Table 1.

Overtemperature protection

TOPFETs include an on-chip protection circuit which measures the absolute temperature of the device. If the chip temperature rises to a dangerous level then the overtemperature protection circuit operates to turn off the power MOSFET stage. Once tripped the device remains protected until it is reset via the protection supply pin.

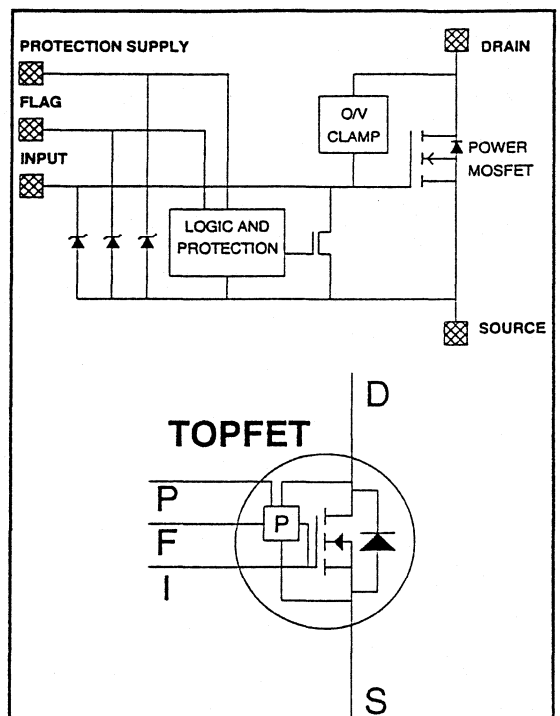


Fig. 1 Schematic diagram and circuit of 5-pin TOPFET

TOPFET	Package	V_{DS} (V)	$R_{DS(ON)}$ (mΩ)	at V_{IS} (V)	for V_{PSP} > (V)
BUK105-50L	SOT263	50	60	5	4
			50	7	4.4
BUK105-50S	SOT263	50	60	5	5
			50	7	5.4

Table 1. 5-pin TOPFET type range

In the tripped condition the gate of the power MOSFET stage is pulled down by the control logic and so current is drawn by the input pin of the TOPFET. A minimum value of external gate drive resistor is specified in order that the protection circuit can turn off the PowerMOS stage and thus protect the device. The flag pin gives a logic high output to indicate that a fault has occurred. If the overtemperature condition persists after the protection supply has been reset then the protection circuit is reactivated.

Short circuit protection

In the case of short circuit faults the rate of rise of temperature in a MOSFET switch can be very rapid. Guaranteed protection under this type of condition is best achieved using the on-chip protection strategy which is implemented in the TOPFET range of devices. The short circuit protection circuit acts rapidly to protect the device if the temperature of the TOPFET rises excessively.

The TOPFET does not limit the current in the power circuit under normal operation. This ensures that the TOPFET does not affect the operation of circuits where large inrush currents are required. As with the overtemperature protection circuit the short circuit protection circuit turns off the power MOSFET gate via the control logic and provides a flag signal. The TOPFET is reset by taking the protection supply pin low.

Overvoltage protection

Transient overvoltage protection is an additional feature of the TOPFET range. This is achieved by a combination of a rugged avalanche breakdown characteristic in the PowerMOS stage and an internal dynamic clamp circuit.

ESD protection

The input pin, flag pin and protection supply pins of the TOPFET are all protected with ESD protection zeners. These devices protect the PowerMOS gate and the TOPFET circuits from ESD transients. The protection devices cannot be used in continuous breakdown.

Protection supply

An error condition is recorded and the flag signal is activated if the protection supply is absent. Valid protection is only guaranteed once the protection supply is in excess of V_{PSP} (See Table 1).

One feature of the implementation of the protection circuits used in this generation of TOPFET devices is that the input, flag or protection supply pins cannot be reverse biased with respect to the source. This must be adhered to at all times. When the TOPFET is in reverse conduction the protection circuits are not active.

Protection with 5-pin TOPFETs

Application report

TOPFETs in the 5-pin SOT263 outline extend the range of application of TOPFET to circuits requiring faster switching or protected linear operation. 3-pin TOPFETs are ideal for use in DC and low frequency switching applications but the need to generate the protection supply from the input is a limitation. Providing a separate pin for the protection supply gives the designer freedom to control the input / MOSFET gate in the way he chooses.

This note will look at the organisation of the 5-pin devices and then discuss some of the more important operational considerations. Application examples will be presented in the later sections in this chapter.

Functional description

The logic and protection circuits within this device are similar to those in the 3-pin TOPFETs but the configuration has been modified (see Fig. 1) to give greater operational versatility.

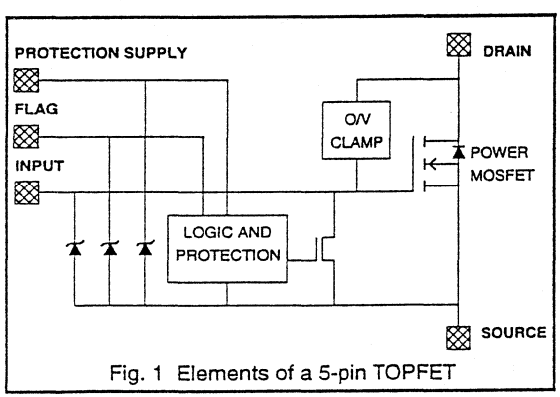


Fig. 1 Elements of a 5-pin TOPFET

These devices use pin 2 of the SOT263 as a flag and pin 4 as the supply / reset to the logic and protection circuits. Separating the protection supply from the input has allowed the internal input gate resistor to be removed. (In a 3-pin TOPFET, this resistor is needed to maintain the protection supply during latched fault conditions).

The operation of the protection circuits has not been changed. If there is an overvoltage between drain and source, the overvoltage protection circuit will still try to turn the MOSFET partially ON. In an overtemperature or overload situation the TOPFET will turn on the gate pull-down transistor and attempt to turn itself OFF.

The flag indicates when the TOPFET has been tripped by an overtemperature, overload or short circuit condition. It will also indicate if the protection supply is absent, for example during a reset. It should be pointed out that the flag low state does not mean that the protection supply is high enough, just that it is present.

The flag is the open drain of a MOS transistor which is OFF to indicate a fault. It is intended that the flag pin is connected to a 10 kΩ pull-up resistor. This arrangement gives the flag a failsafe characteristic.

Operational considerations

Supplying the protection circuits from their own pin, rather than sharing a pin with the MOSFET gate drive, has several beneficial effects. One is that it allows the MOSFET gate to be independently controlled without adversely affecting the protection features. This is particularly useful when TOPFET is being used as a linear controller.

The removal of the input gate resistor gives the designer the opportunity of selecting the most appropriate value. It is important to understand that if TOPFET is to protect itself, it needs to control its gate by overriding the external drive circuit. It can only do this if the impedance of the driver is high enough. The conditions for satisfactory operation are given in Table 1.

Protection level	Minimum driver impedance		
	ON drive		OFF drive
	5 V	10 V	input / source
Full self protection	1 kΩ	2 kΩ	100 Ω
Overvoltage protection only	0 Ω	0 Ω	100 Ω
Overtemperature, overload and short circuit protection only	1 kΩ	2 kΩ	0 Ω

Table 1. Driver impedance and protection level

The simplest way of satisfying the self protection requirements is to fit a 2 kΩ resistor between the driver and the input pin. This is simple in a linear controller but may not be feasible in a switching controller where this resistance will result in a significant turn OFF delay. An alternative may be to have an ON drive via 2 kΩ and an OFF drive via 100 Ω.

If lower turn ON drive impedance is needed then the approach would be to use the flag output to control the signal being fed to the driver circuit. It should be noted that to have overvoltage protection the turn OFF impedance must still be > 100 Ω.

The S and L versions differ only in the protection supply voltage range. The L types are designed to be supplied from the output of 5 V logic ICs, like the 74HC/HCT families. The S types are intended to be supplied with a nominal 10 V from either HEF4000 type logic, linear ICs (e.g operational amplifiers) or discrete circuits.

One additional benefit of the independent protection supply is that, unlike 3-pin L types, the input of a 5-pin L type can be as high as 11 V, allowing a significantly lower $R_{DS(ON)}$ to be achieved.

It is important to realise that, at high levels of input voltage, the MOSFET transfer characteristic of both L and S types will allow a very high current to flow during shorted load situations. This current, flowing through the resistance in the connections between the chip's source metalisation and the source pad on the pcb, will give a significant volt drop. Since the return for the protection supply will be to the pcb source bond pad, the volt drop will subtract from the effective protection supply voltage. To compensate for this effect, the minimum protection supply voltage, V_{PSP}, is increased at high levels of input voltage, V_{IS}. For example the minimum V_{PSP} of the BUK105-50L is 4 V if $V_{IS} \leq 5$ V. If, however, the input is taken to 7 V, to achieve an $R_{DS(ON)}$ of 50 mΩ, V_{PSP} must be ≥ 4.4 V. A curve in data (reproduced as Fig. 2) gives minimum V_{PSP} values for VIS from 0 to 11 V.

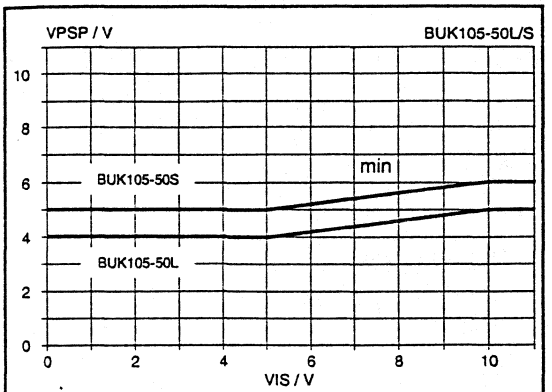


Fig. 2 Minimum protection supply for shorted load protection

The input, flag and protection supply pins are all protected against the effects of ESD by special diodes between the pin and source. It is important to realise that these devices are not designed to run in continuous forward or reverse conduction. This means that the continuous voltage between these pins and source should be > 0 and < 11 V.

Reverse Battery

There is always a risk that the car's battery could be reversed. If this happened to a system where a TOPFET is fitted then the TOPFET will survive provided:

- the current flowing through the body drain diode is restricted by the load to a level which does not cause the TOPFET to over dissipate,
- the current flowing out of the input, flag and protection supply pins is < 10 mA.

PowerMOS transistor
Logic level TOPFET

BUK104-50L/S
BUK104-50LP/SP

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 5 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	15	A
P_{tot}	Total power dissipation	40	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		
	V_{IS} = 5 V	125	mΩ
	V_{IS} = 7 V	100	mΩ
SYMBOL	**PARAMETER**	**NOM.**	**UNIT**
V_{PSN}	Protection supply voltage		
	BUK104-50L	5	V
	BUK104-50S	10	V

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Logic and protection supply from separate pin
- Low operating supply current
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by protection supply
- Protection circuit condition indicated by flag pin
- 5 V logic compatible input level
- Separate input pin for higher frequency drive
- ESD protection on input, flag and protection supply pins
- Over voltage clamping for turn off of inductive loads
- Both linear and switching operation are possible

FUNCTIONAL BLOCK DIAGRAM

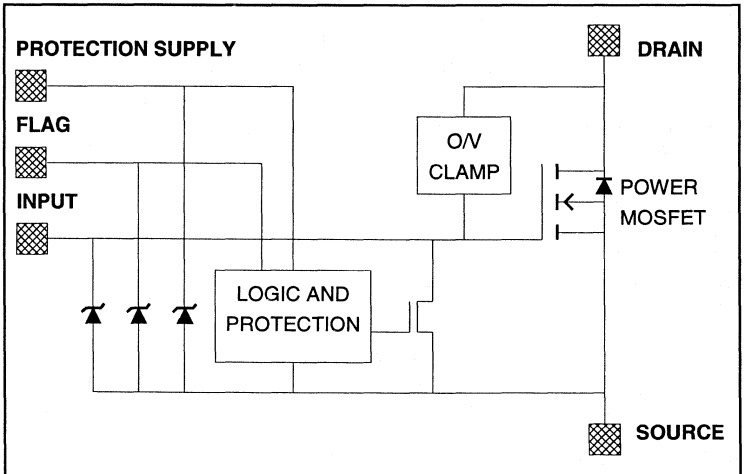


Fig.1. Elements of the TOPFET.

PINNING - SOT263

PIN	DESCRIPTION
1	input
2	flag
3	drain
4	protection supply
5	source
tab	drain

PIN CONFIGURATION

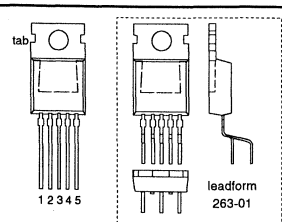


Fig. 2. Type numbers ending with suffix P refer to leadform 263-01.

SYMBOL

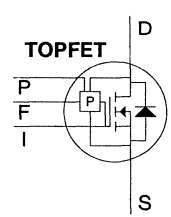


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Voltages				
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	11	V
V_{FS}	Continuous flag voltage	-	0	11	V
V_{PS}	Continuous supply voltage	-	0	11	V
	Currents	V_{IS} =	-	7 | 5	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C	-	15 | 13	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C	-	9.5 | 8.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C	-	60 | 54	A
	Thermal				
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	40	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Junction temperature[2]	continuous	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply connected, TOPFET can protect itself from two types of overload - over temperature and short circuit load.

An n-MOS transistor turns on between the input and source to quickly discharge the power MOSFET gate capacitance.

For internal overload protection to remain latched while the control circuit is high, external series input resistance must be provided. Refer to INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
		V_{IS} =	7 | 5	-	V
V_{PSP}	Protection supply voltage[3]	for valid protection			
		BUK104-50L	4.4 | 4	-	V
		BUK104-50S	5.4 | 5	-	V
	Over temperature protection	$V_{PS} = V_{PSN}$			
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-	50	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-	50	V
	Short circuit load protection	$V_{PS} = V_{PSN}$; L ≤ 10 µH			
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-	25	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-	45	V
P_{DSM}	Instantaneous overload dissipation		-	0.8	kW

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The minimum supply voltage required for correct operation of the overload protection circuits.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DRRM}	Repetitive peak clamping drain current	$R_{IS} \geq 100\ \Omega$[1]	-	15	A
E_{DSM}	Non-repetitive inductive turn-off energy[2]	$I_{DM} = 15$ A; $R_{IS} \geq 100\ \Omega$	-	200	mJ
E_{DRM}	Repetitive inductive turn-off energy	$R_{IS} \geq 100\ \Omega$; $T_{mb} \leq 95$ °C; $I_{DM} = 4$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ
I_{DIRM}	Repetitive peak drain to input current[3]	$R_{IS} = 0\ \Omega$; $t_p \leq 1$ ms	-	50	mA

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} = 25$ °C; $V_{IS} = V_{PS} = V_{FS} = 0$ V	-	15	A

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_D = 10$ mA		50	-	65	V
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_{DM} = 1$ A; $t_p \leq 300$ µs; $\delta \leq 0.01$		50	-	70	V
I_{DSS}	Zero input voltage drain current	$V_{DS} = 12$ V; $V_{IS} = 0$ V		-	0.5	10	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 50$ V; $R_{IS} = 100\ \Omega$;		-	1	20	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$; $T_j = 125$ °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	$I_{DM} = 7.5$ A; $t_p \leq 300$ µs; $\delta \leq 0.01$	$V_{IS} = 7$ V	-	75	100	mΩ
			$V_{IS} = 5$ V	-	95	125	mΩ

1 The input pin must be connected to the source pin by a specified external resistance to allow the power MOSFET gate source voltage to become sufficiently positive for active clamping. Refer to INPUT CHARACTERISTICS.

2 While the protection supply voltage is connected, during overvoltage clamping it is possible that the overload protection may operate at energies close to the limiting value. Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 Shorting the input to source with low resistance inhibits the internal overvoltage protection by preventing the power MOSFET gate source voltage becoming positive.

OVERLOAD PROTECTION CHARACTERISTICS

With adequate protection supply voltage TOPFET detects when one of the overload thresholds is exceeded.

Provided there is adequate input series resistance it switches off and remains latched off until reset by the protection supply pin.

Refer also to OVERLOAD PROTECTION LIMITING VALUES and INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	$V_{PS} = V_{PSN}$[2]; $T_{mb} = 25$ °C; $L \leq 10$ µH; $R_I \geq 2$ kΩ				
$E_{DS(TO)}$	Overload threshold energy	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	150	-	mJ
$t_{d\,sc}$	Response time	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	375	-	µs
	Over temperature protection	$V_{PS} = V_{PSN}$; $R_I \geq 2$ kΩ				
$T_{j(TO)}$	Threshold junction temperature	from $I_D \geq 0.65$ A[3]	150	-	-	°C

TRANSFER CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 10$ V; $I_{DM} = 7.5$ A $t_p \leq 300$ µs; $\delta \leq 0.01$	5	9	-	S
I_D	Drain current[4]	$V_{DS} = 13$ V; $V_{IS} = 5$ V	-	25	-	A
		$V_{IS} = 10$ V		40	-	A

PROTECTION SUPPLY CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Protection supply					
I_{PS}, I_{PSL}	Protection supply current	normal operation or protection latched				
		BUK104-50L $V_{PS} = 5$ V	-	0.2	0.35	mA
		BUK104-50S $V_{PS} = 10$ V	-	0.4	1.0	mA
V_{PSR}	Protection reset voltage[5]		1.5	2.5	3.5	V
		$T_j = 150$ °C	1.0	-	-	V
$V_{(CL)PS}$	Protection clamp voltage	$I_P = 1.35$ mA	11	13	-	V

REVERSE DIODE CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	$I_S = 15$ A; $V_{IS} = V_{PS} = V_{FS} = 0$ V; $t_p = 300$ µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[6]	-	-	-	-

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum.

2 At the appropriate nominal protection supply voltage for each type. Refer to QUICK REFERENCE DATA.

3 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

4 During overload condition. Refer also to OVERLOAD PROTECTION LIMITING VALUES and CHARACTERISTICS.

5 The supply voltage below which the overload protection circuits will be reset.

6 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
	Normal operation						
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
			T_{mb} = 150 °C	0.5	-	-	V
I_{IS}	Input current	V_{IS} = 10 V		-	10	100	nA
$V_{(CL)IS}$	Input clamp voltage	I_I = 1 mA		11	13	-	V
	Overload protection latched						
R_{ISL}	Input resistance[1]	V_{PS} = 5 V	I_I = 5 mA;	-	55	-	Ω
			T_{mb} = 150 °C	-	95	-	Ω
		V_{PS} = 10 V	I_I = 5 mA;	-	35	-	Ω
			T_{mb} = 150 °C	-	60	-	Ω
	Application information						
	External input resistances for	(see figure 29)					
R_{IS}	internal overvoltage clamping[2]	R_I = ∞ Ω;	V_{DS} > 30 V	100	-	-	Ω
R_I	internal overload protection[3]	R_{IS} = ∞ Ω;	V_{II} = 5 V	1	-	-	kΩ
			V_{II} = 10 V	2	-	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C; R_I = 50 Ω; R_{IS} = 50 Ω (see figure 29); resistive load R_L = 10 Ω. For waveforms see figure 28.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; V_{IS}: 0 V ⇒ 10 V	-	8	-	ns
t_r	Rise time		-	13	-	ns
$t_{d\,off}$	Turn-off delay time	V_{DD} = 15 V; V_{IS}: 10 V ⇒ 0 V	-	100	-	ns
t_f	Fall time		-	45	-	ns

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{iss}	Input capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	415	600	pF
C_{oss}	Output capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	275	400	pF
C_{rss}	Reverse transfer capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	55	80	pF
C_{pso}	Protection supply pin capacitance	V_{PS} = 10 V	-	30	-	pF
C_{fso}	Flag pin capacitance	V_{FS} = 10 V; V_{PS} = 0 V	-	20	-	pF

1 The resistance of the internal transistor which discharges the power MOSFET gate capacitance when overload protection operates. The external drive circuit should be such that the input voltage does not exceed $V_{IS(TO)}$ minimum when the overload protection has operated. Refer also to figure for latched input characteristics.

2 Applications using a lower value for R_{IS} would require external overvoltage protection.

3 For applications requiring a lower value for R_I, an external overload protection strategy is possible using the flag pin to 'tell' the control circuit to switch off the input.

FLAG DESCRIPTION

The flag pin provides a means to detect the presence of the protection supply and indicate the state of the overload detectors. The flag is the open drain of an n-MOS transistor and requires an external pull-up resistor[1]. It is suitable for both 5 V and 10 V logic. Flag may be used to implement an external protection strategy[2] for applications which require low input drive impedance.

TRUTH TABLE

CONDITION	DESCRIPTION	FLAG
NORMAL	Normal operation and adequate protection supply voltage	LOGIC LOW
OVER TEMP.	Over temperature detected	LOGIC HIGH
SHORT CIRCUIT	Overload condition detected	LOGIC HIGH
SUPPLY FAULT	Inadequate protection supply voltage	LOGIC HIGH

FLAG CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Flag 'low'	normal operation				
V_{FS}	Flag voltage	I_F = 1.6 mA	-	0.15	0.4	V
I_{FSS}	Flag saturation current	V_{FS} = 10 V	-	15	-	mA
	Flag 'high'	overload or fault				
I_{FS}	Flag leakage current	V_{FS} = 10 V	-	-	10	µA
V_{PSF}	Protection supply threshold voltage	V_{FF} = 5 V; R_F = 3 kΩ; **BUK104-50L**	2.5	3.3	4	V
		BUK104-50S	3.3	4.2	5	V
$V_{(CL)FS}$	Flag clamping voltage	I_F = 1 mA; V_{PS} = 0 V	11	13	-	V
	Application information					
R_F	Suitable external pull-up resistance	V_{FF} =5 V	1	10	50	kΩ
		V_{FF} =10 V	2	20	100	kΩ

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 Even if the flag pin is not used, it is recommended that it is connected to the protection supply via a pull-up resistor. It should not be left floating.

2 Low pass filtering of the flag signal may be advisable to prevent false tripping.

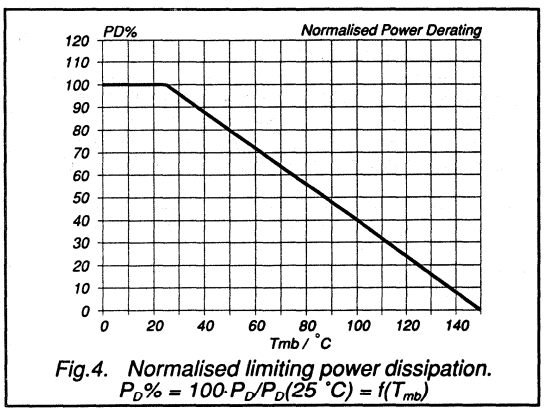


Fig.4. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

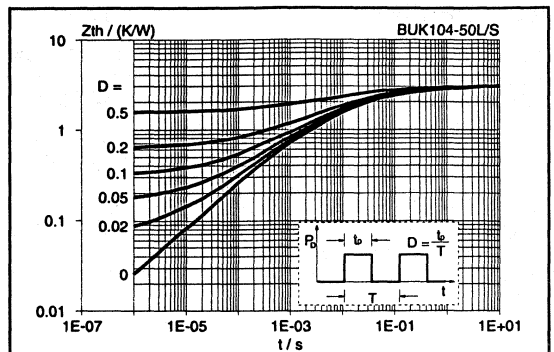


Fig.7. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

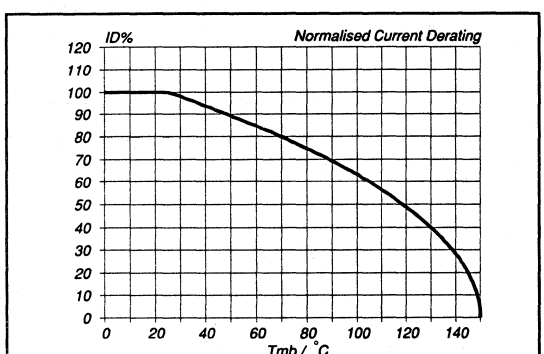


Fig.5. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

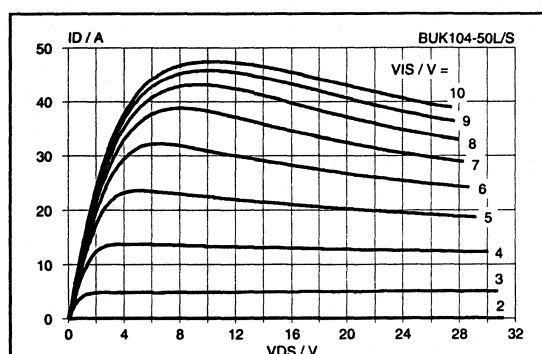


Fig.8. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

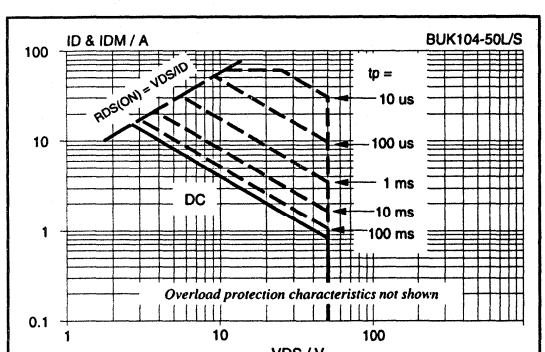


Fig.6. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

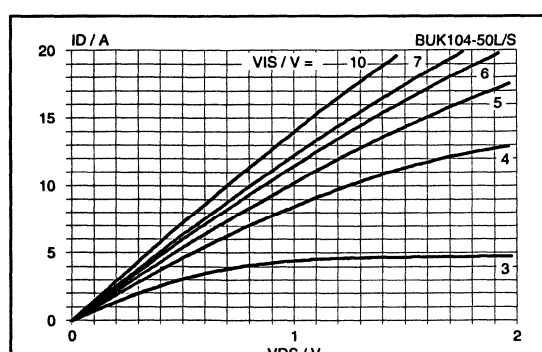


Fig.9. Typical on-state characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

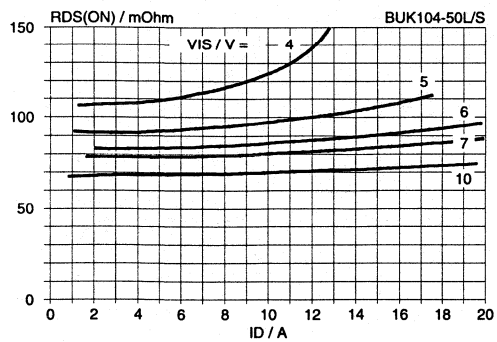


Fig.10. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

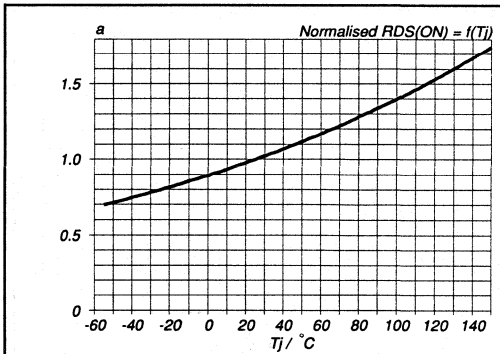


Fig.13. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ °C = f(T_j)$; I_D = 7.5 A; $V_{IS} \geq 5$ V

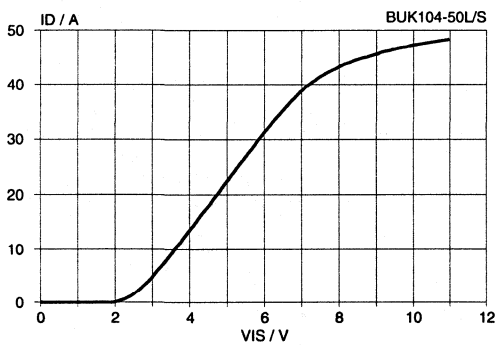


Fig.11. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

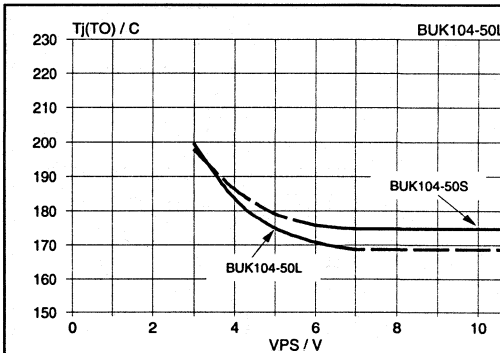


Fig.14. Typical over temperature protection threshold $T_{j(TO)} = f(V_{PS})$; conditions: V_{DS} > 0.1 V

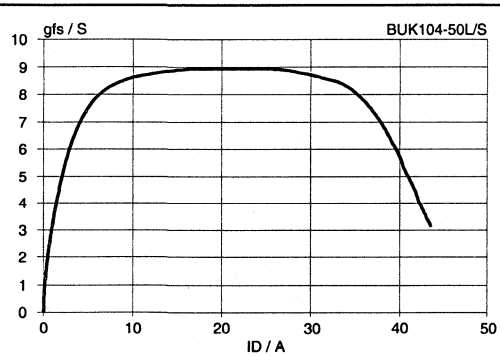


Fig.12. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

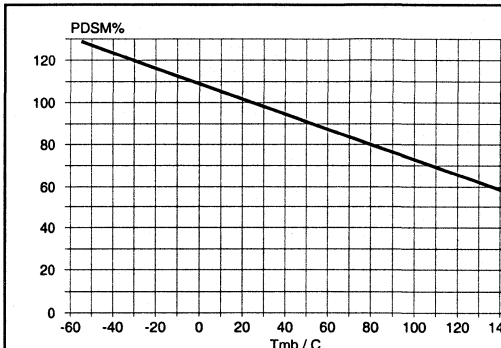


Fig.15. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

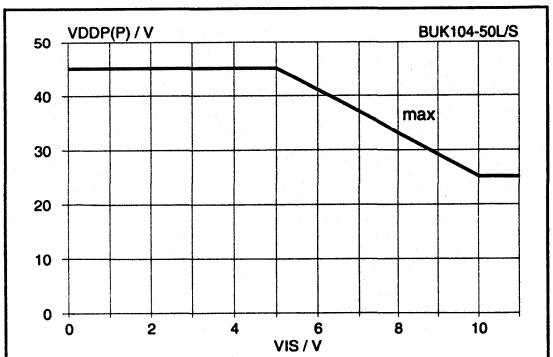


Fig.16. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150$ °C

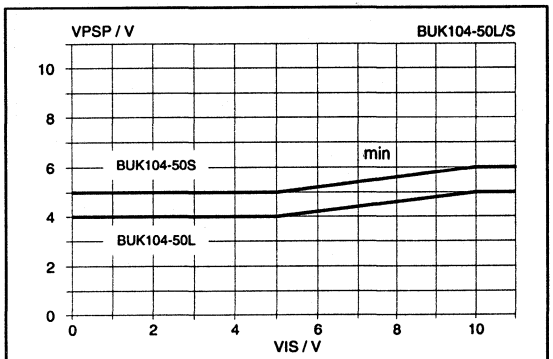


Fig.17. Minimum protection supply voltage for SC load protection. $V_{PSP} = f(V_{IS})$; $T_{mb} \geq 25$ °C

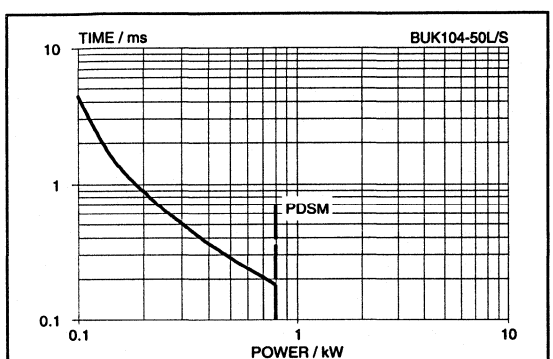


Fig.18. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{PS} \geq V_{PSP}$; $V_{IS} \geq 5$ V

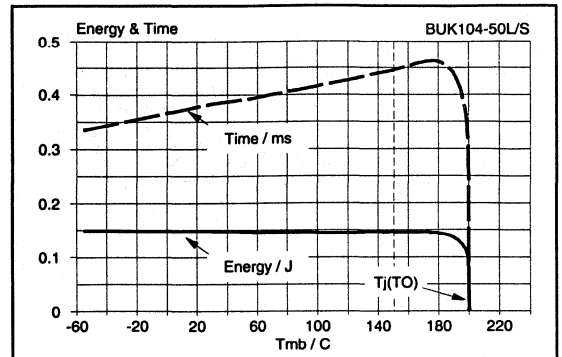


Fig.19. Typical overload protection characteristics. Conditions: $V_{DD} = 13$ V; $V_{PS} = V_{PSN}$, $V_{IS} = 7$ V; SC load

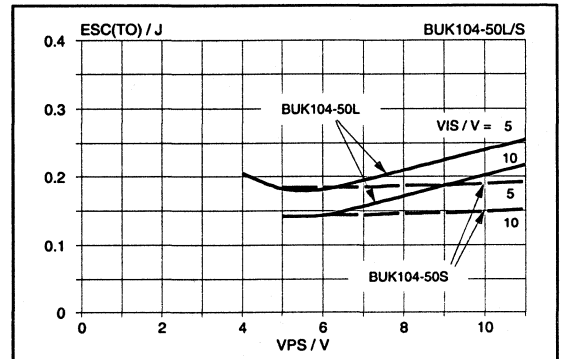


Fig.20. Typical overload protection energy, $T_j = 25$ °C $E_{SC(TO)} = f(V_{PS})$; conditions: $V_{DS} = 13$ V, parameter V_{IS}

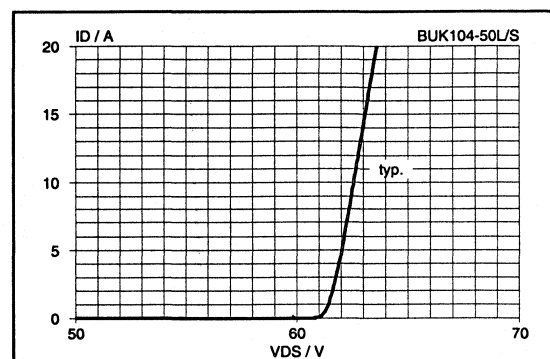


Fig.21. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: $R_{IS} = 100\ \Omega$; $t_p \leq 50\ \mu s$

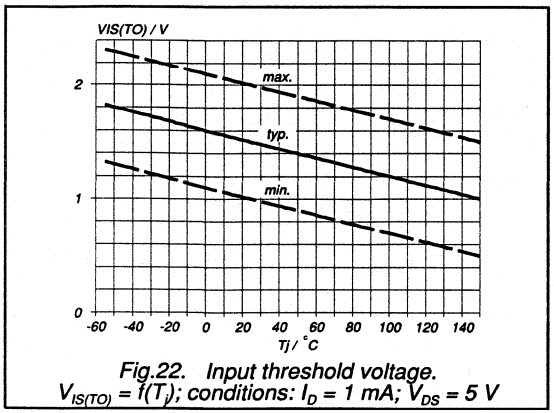


Fig.22. Input threshold voltage.
$V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

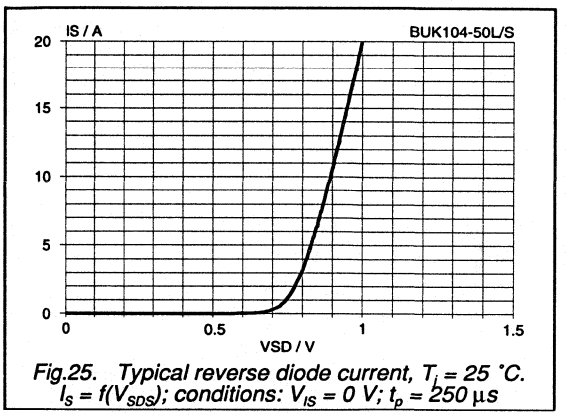


Fig.25. Typical reverse diode current, $T_j = 25$ °C.
$I_S = f(V_{SDS})$; conditions: $V_{IS} = 0$ V; $t_p = 250$ µs

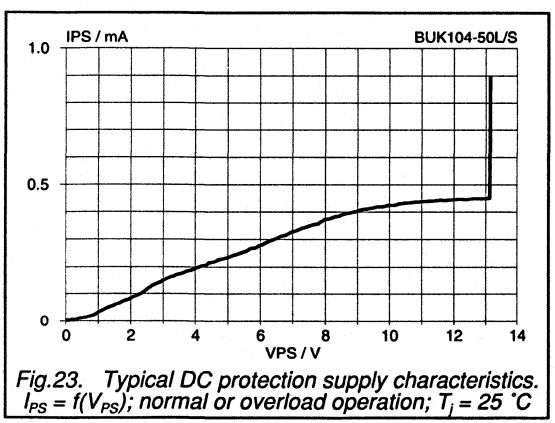


Fig.23. Typical DC protection supply characteristics.
$I_{PS} = f(V_{PS})$; normal or overload operation; $T_j = 25$ °C

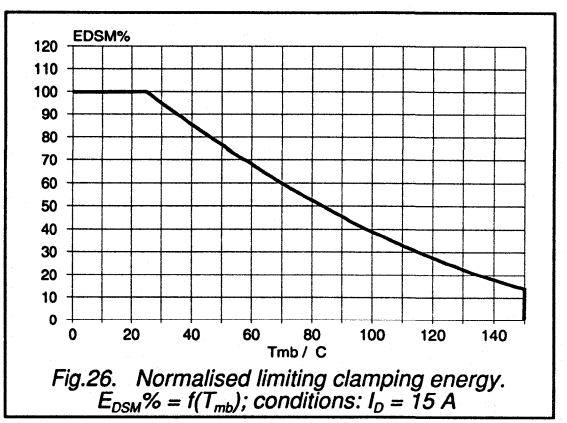


Fig.26. Normalised limiting clamping energy.
$E_{DSM}\% = f(T_{mb})$; conditions: $I_D = 15$ A

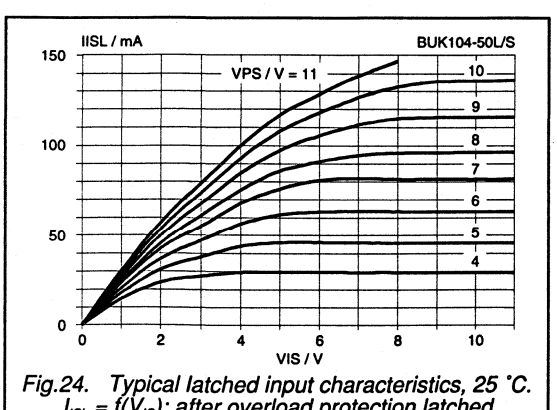


Fig.24. Typical latched input characteristics, 25 °C.
$I_{ISL} = f(V_{IS})$; after overload protection latched

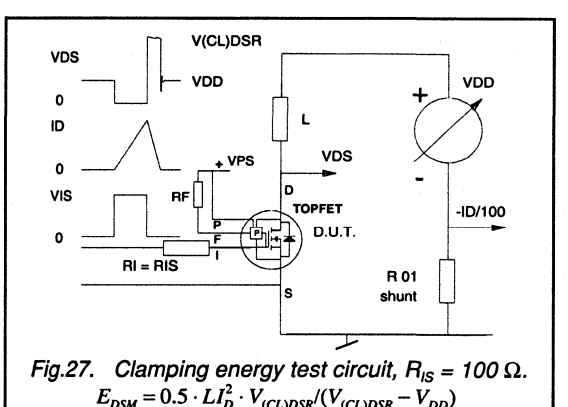


Fig.27. Clamping energy test circuit, $R_{IS} = 100\ \Omega$.
$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSR}/(V_{(CL)DSR} - V_{DD})$

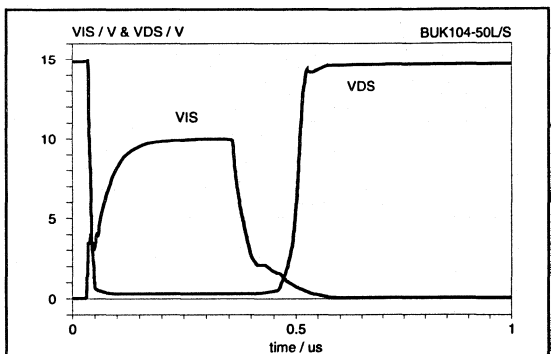


Fig.28. Typical resistive load switching waveforms $R_I = R_{IS} = 50\ \Omega$; $R_L = 10\ \Omega$; $V_{DD} = 15$ V; $T_j = 25$ °C

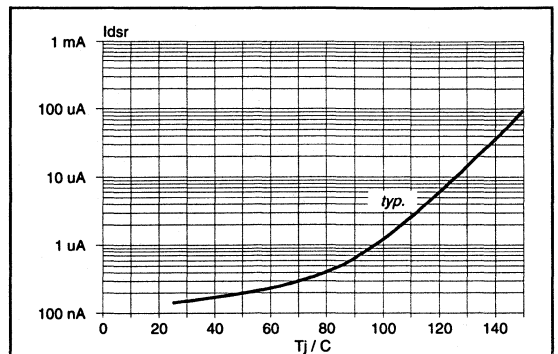


Fig.31. Typical off-state leakage current. $I_{DSR} = f(T_j)$; Conditions: $V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$.

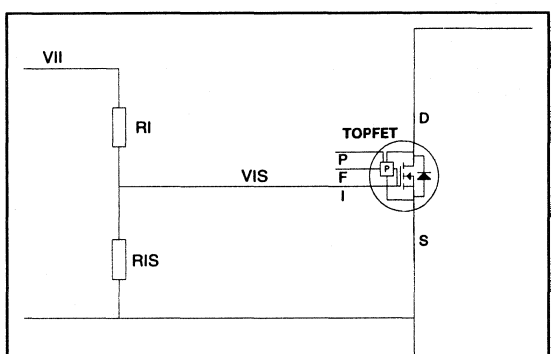


Fig.29. External input resistances R_I and R_{IS}, generator voltage V_{II} and input voltage V_{IS}.

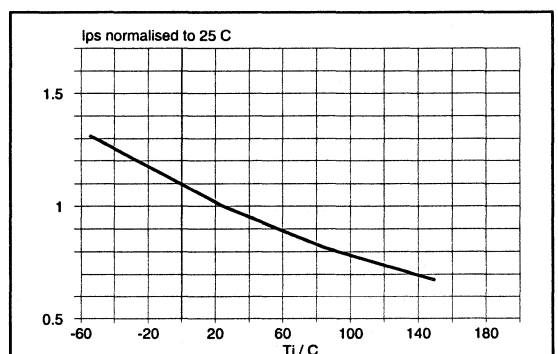


Fig.32. Normalised protection supply current. $I_{PS}/I_{PS}25\ ^\circ C = f(T_j)$; $V_{PS} = V_{PSN}$

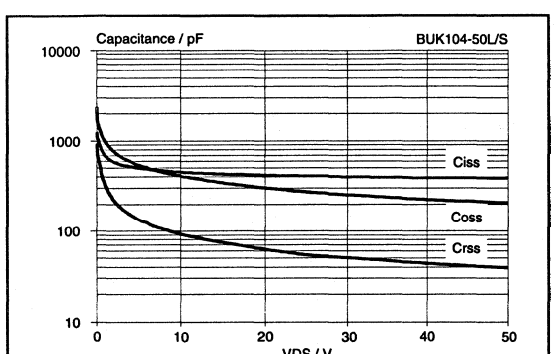


Fig.30. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $f = 1$ MHz

PowerMOS transistor
Logic level TOPFET

BUK105-50L/S
BUK105-50LP/SP

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 5 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	29	A
P_{tot}	Total power dissipation	75	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		
	V_{IS} = 5 V	60	mΩ
	V_{IS} = 7 V	50	mΩ
SYMBOL	**PARAMETER**	**NOM.**	**UNIT**
V_{PSN}	Protection supply voltage		
	BUK105-50L	5	V
	BUK105-50S	10	V

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Logic and protection supply from separate pin
- Low operating supply current
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by protection supply
- Protection circuit condition indicated by flag pin
- 5 V logic compatible input level
- Separate input pin for higher frequency drive
- ESD protection on input, flag and protection supply pins
- Over voltage clamping for turn off of inductive loads
- Both linear and switching operation are possible

FUNCTIONAL BLOCK DIAGRAM

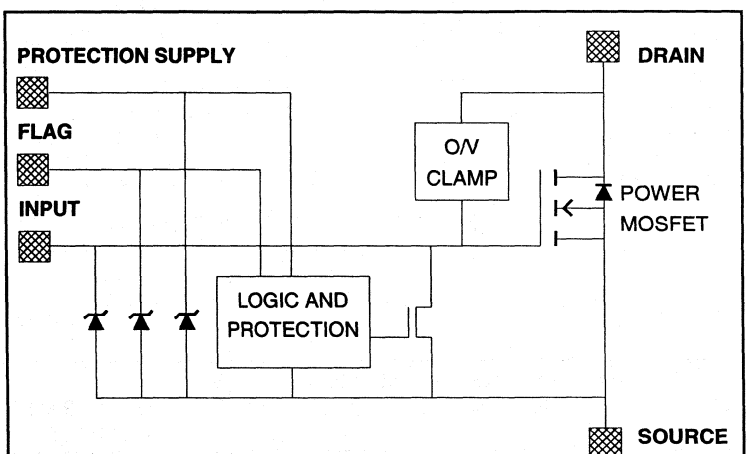


Fig.1. Elements of the TOPFET.

PINNING - SOT263

PIN	DESCRIPTION
1	input
2	flag
3	drain
4	protection supply
5	source
tab	drain

PIN CONFIGURATION

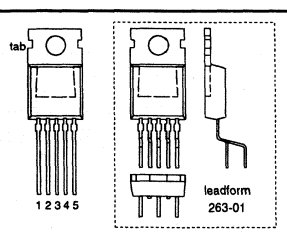


Fig. 2. Type numbers ending with suffix P refer to leadform 263-01.

SYMBOL

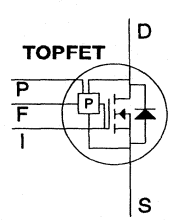


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Voltages				
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	11	V
V_{FS}	Continuous flag voltage	-	0	11	V
V_{PS}	Continuous supply voltage	-	0	11	V
	Currents	V_{IS} =	-	7 | 5	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C	-	29 | 26	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C	-	18 | 16	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C	-	120 | 100	A
	Thermal				
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Junction temperature[2]	continuous	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply connected, TOPFET can protect itself from two types of overload - over temperature and short circuit load.

An n-MOS transistor turns on between the input and source to quickly discharge the power MOSFET gate capacitance.

For internal overload protection to remain latched while the control circuit is high, external series input resistance must be provided. Refer to INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
		V_{IS} =	7 | 5	-	V
V_{PSP}	Protection supply voltage[3]	for valid protection			
		BUK105-50L	4.4 | 4	-	V
		BUK105-50S	5.4 | 5	-	V
	Over temperature protection	$V_{PS} = V_{PSN}$			
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-	50	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-	50	V
	Short circuit load protection	$V_{PS} = V_{PSN}$; L ≤ 10 µH			
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-	20	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-	35	V
P_{DSM}	Instantaneous overload dissipation		-	1.3	kW

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The minimum supply voltage required for correct operation of the overload protection circuits.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DRRM}	Repetitive peak clamping drain current	$R_{IS} \geq 100\ \Omega$[1]	-	29	A
E_{DSM}	Non-repetitive inductive turn-off energy[2]	$I_{DM} = 29$ A; $R_{IS} \geq 100\ \Omega$	-	325	mJ
E_{DRM}	Repetitive inductive turn-off energy	$R_{IS} \geq 100\ \Omega$; $T_{mb} \leq 95$ °C; $I_{DM} = 8$ A; $V_{DD} \leq 20$ V; $f = 250$ Hz	-	40	mJ
I_{DIRM}	Repetitive peak drain to input current[3]	$R_{IS} = 0\ \Omega$; $t_p \leq 1$ ms	-	50	mA

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} = 25$ °C; $V_{IS} = V_{PS} = V_{FS} = 0$ V	-	29	A

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.25	1.67	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_D = 10$ mA		50	-	65	V
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_{DM} = 1$ A; $t_p \leq 300\ \mu$s; $\delta \leq 0.01$		50	-	70	V
I_{DSS}	Zero input voltage drain current	$V_{DS} = 12$ V; $V_{IS} = 0$ V		-	0.5	10	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 50$ V; $R_{IS} = 100\ \Omega$;		-	1	20	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$; $T_j = 125$ °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	$I_{DM} = 13$ A; $t_p \leq 300\ \mu$s; $\delta \leq 0.01$	$V_{IS} = 7$ V	-	40	50	mΩ
			$V_{IS} = 5$ V	-	47	60	mΩ

1 The input pin must be connected to the source pin by a specified external resistance to allow the power MOSFET gate source voltage to become sufficiently positive for active clamping. Refer to INPUT CHARACTERISTICS.

2 While the protection supply voltage is connected, during overvoltage clamping it is possible that the overload protection may operate at energies close to the limiting value. Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 Shorting the input to source with low resistance inhibits the internal overvoltage protection by preventing the power MOSFET gate source voltage becoming positive.

OVERLOAD PROTECTION CHARACTERISTICS

With adequate protection supply voltage TOPFET detects when one of the overload thresholds is exceeded.

Provided there is adequate input series resistance it switches off and remains latched off until reset by the protection supply pin.

Refer also to OVERLOAD PROTECTION LIMITING VALUES and INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	$V_{PS} = V_{PSN}$[2]; $T_{mb} = 25$ °C; $L \leq 10$ µH				
$E_{DS(TO)}$	Overload threshold energy	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	300	-	mJ
$t_{d\,sc}$	Response time	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	0.6	-	ms
	Over temperature protection	$V_{PS} = V_{PSN}$				
$T_{j(TO)}$	Threshold junction temperature	from $I_D \geq 1.25$ A[3]	150	-	-	°C

TRANSFER CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 10$ V; $I_{DM} = 13$ A $t_p \leq 300$ µs; $\delta \leq 0.01$	10	16	-	S
I_D	Drain current[4]	$V_{DS} = 13$ V; $V_{IS} = 5$ V	-	50	-	A
		$V_{IS} = 10$ V		100	-	A

PROTECTION SUPPLY CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Protection supply					
I_{PS}, I_{PSL}	Protection supply current	normal operation or protection latched				
		BUK105-50L $V_{PS} = 5$ V	-	0.2	0.35	mA
		BUK105-50S $V_{PS} = 10$ V	-	0.4	1.0	mA
V_{PSR}	Protection reset voltage[5]		1.5	2.5	3.5	V
		$T_j = 150$ °C	1.0	-	-	V
$V_{(CL)PS}$	Protection clamp voltage	$I_P = 1.35$ mA	11	13	-	V

REVERSE DIODE CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	$I_S = 20$ A; $V_{IS} = V_{PS} = V_{FS} = 0$ V; $t_p = 300$ µs	-	1.0	1.4	V
t_{rr}	Reverse recovery time	not applicable[6]	-	-	-	-

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum.

2 At the appropriate nominal protection supply voltage for each type. Refer to QUICK REFERENCE DATA.

3 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

4 During overload condition. Refer also to OVERLOAD PROTECTION LIMITING VALUES and CHARACTERISTICS.

5 The supply voltage below which the overload protection circuits will be reset.

6 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Normal operation					
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
		T_{mb} = 150 °C	0.5	-	-	V
I_{IS}	Input current	V_{IS} = 10 V	-	10	100	nA
$V_{(CL)IS}$	Input clamp voltage	I_I = 1 mA	11	13	-	V
	Overload protection latched					
R_{ISL}	Input resistance[1]	V_{PS} = 5 V; I_I = 5 mA	-	40	-	Ω
		T_{mb} = 150 °C	-	70	-	Ω
		V_{PS} = 10 V; I_I = 5 mA	-	25	-	Ω
		T_{mb} = 150 °C	-	45	-	Ω
	Application information					
	External input resistances for	(see figure 29)				
R_{IS}	internal overvoltage clamping[2]	R_I = ∞ Ω; V_{DS} > 30 V	100	-	-	Ω
R_I	internal overload protection[3]	R_{IS} = ∞ Ω; V_{II} = 5 V	1	-	-	kΩ
		V_{II} = 10 V	2	-	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C; R_I = 50 Ω; R_{IS} = 50 Ω (see figure 29); resistive load R_L = 10 Ω. For waveforms see figure 28.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; V_{IS}: 0 V ⇒ 10 V	-	8	-	ns
t_r	Rise time		-	25	-	ns
$t_{d\,off}$	Turn-off delay time	V_{DD} = 15 V; V_{IS}: 10 V ⇒ 0 V	-	135	-	ns
t_f	Fall time		-	90	-	ns

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{iss}	Input capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	725	1050	pF
C_{oss}	Output capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	450	650	pF
C_{rss}	Reverse transfer capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	100	150	pF
C_{pso}	Protection supply pin capacitance	V_{PS} = 10 V	-	30	-	pF
C_{fso}	Flag pin capacitance	V_{FS} = 10 V; V_{PS} = 0 V	-	20	-	pF

1 The resistance of the internal transistor which discharges the power MOSFET gate capacitance when overload protection operates.
The external drive circuit should be such that the input voltage does not exceed $V_{IS(TO)}$ minimum when the overload protection has operated. Refer also to figure for latched input characteristics.

2 Applications using a lower value for R_{IS} would require external overvoltage protection.

3 For applications requiring a lower value for R_I, an external overload protection strategy is possible using the flag pin to 'tell' the control circuit to switch off the input.

FLAG DESCRIPTION

The flag pin provides a means to detect the presence of the protection supply and indicate the state of the overload detectors. The flag is the open drain of an n-MOS transistor and requires an external pull-up resistor[1]. It is suitable for both 5 V and 10 V logic. Flag may be used to implement an external protection strategy[2] for applications which require low input drive impedance.

TRUTH TABLE

CONDITION	DESCRIPTION	FLAG
NORMAL	Normal operation and adequate protection supply voltage	LOGIC LOW
OVER TEMP.	Over temperature detected	LOGIC HIGH
SHORT CIRCUIT	Overload condition detected	LOGIC HIGH
SUPPLY FAULT	Inadequate protection supply voltage	LOGIC HIGH

FLAG CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Flag 'low'	normal operation				
V_{FS}	Flag voltage	I_F = 1.6 mA	-	0.15	0.4	V
I_{FSS}	Flag saturation current	V_{FS} = 10 V	-	15	-	mA
	Flag 'high'	overload or fault				
I_{FS}	Flag leakage current	V_{FS} = 10 V	-	-	10	µA
V_{PSF}	Protection supply threshold voltage	V_{FF} = 5 V; R_F = 3 kΩ; **BUK105-50L**	2.5	3.3	4	V
		BUK105-50S	3.5	4.3	5	V
$V_{(CL)FS}$	Flag clamping voltage	I_F = 1 mA; V_{PS} = 0 V	11	13	-	V
	Application information					
R_F	Suitable external pull-up resistance	V_{FF} =5 V	1	10	50	kΩ
		V_{FF} =10 V	2	20	100	kΩ

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 Even if the flag pin is not used, it is recommended that it is connected to the protection supply via a pull-up resistor. It should not be left floating.

2 Low pass filtering of the flag signal may be advisable to prevent false tripping.

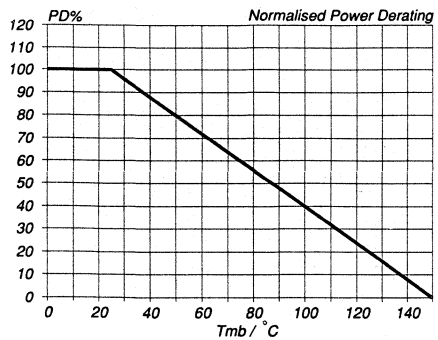


Fig.4. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

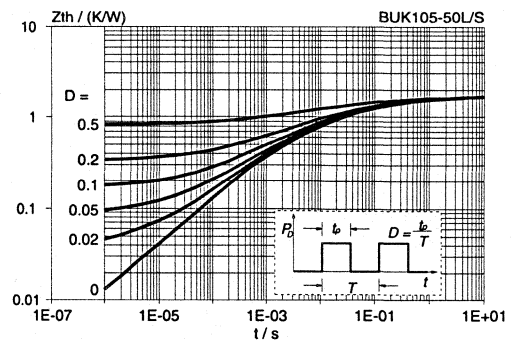


Fig.7. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

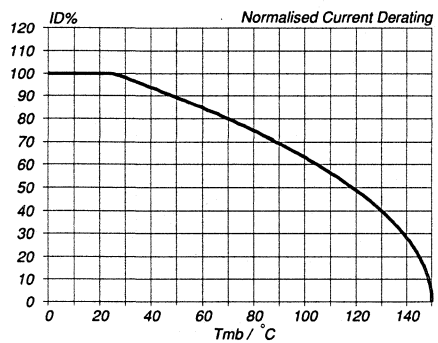


Fig.5. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

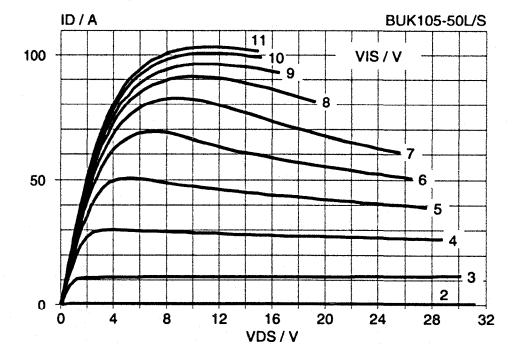


Fig.8. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

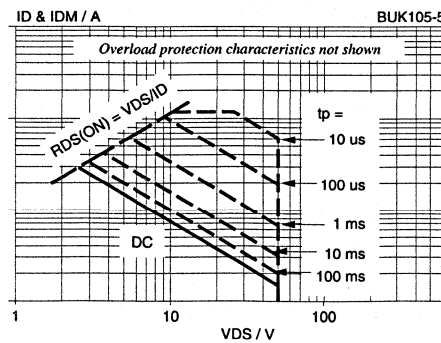


Fig.6. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

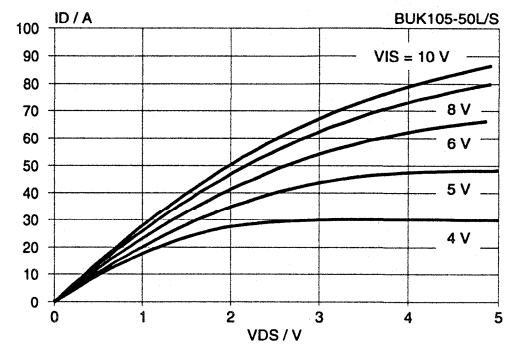


Fig.9. Typical on-state characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

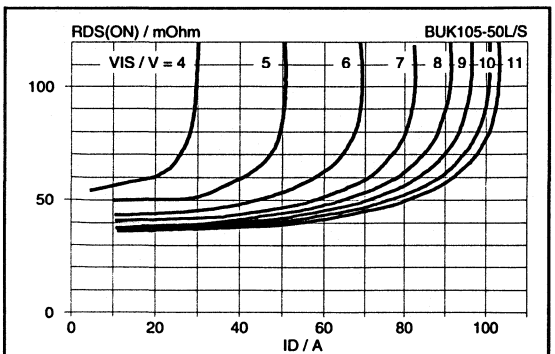


Fig.10. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

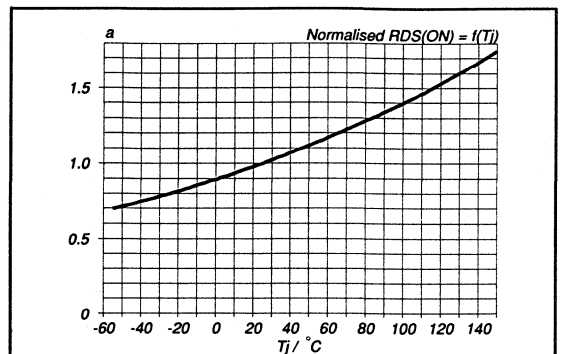


Fig.13. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ °C = f(T_j)$; I_D = 13 A; $V_{IS} \geq 5$ V

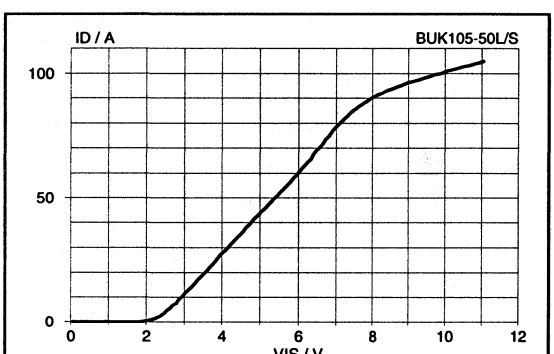


Fig.11. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

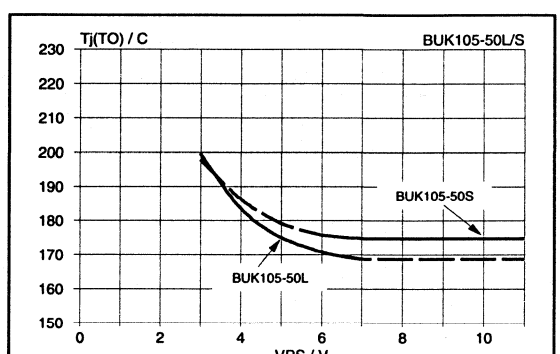


Fig.14. Typical over temperature protection threshold $T_{j(TO)} = f(V_{PS})$; conditions: V_{DS} > 0.1 V

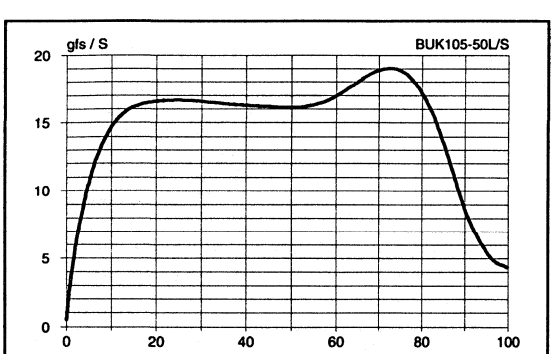


Fig.12. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

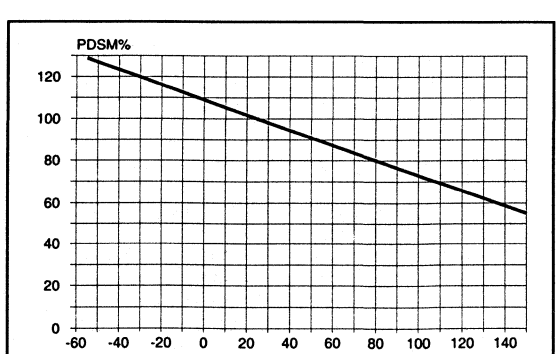


Fig.15. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

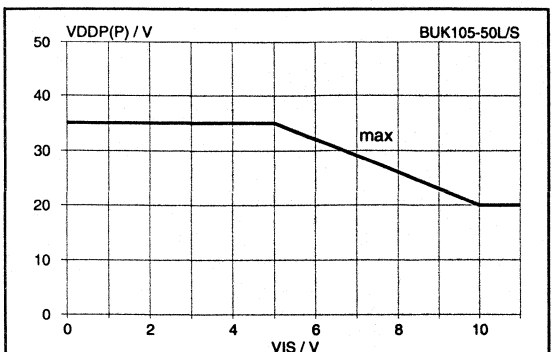


Fig.16. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150$ °C

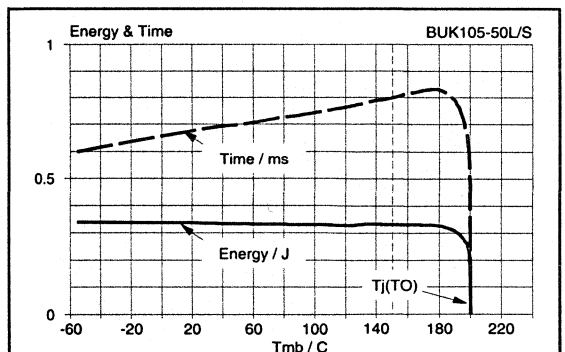


Fig.19. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; $V_{PS} = V_{PSN}$, V_{IS} = 7 V; SC load

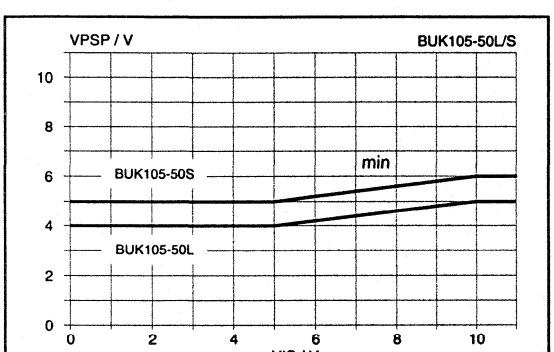


Fig.17. Minimum protection supply voltage for SC load protection. $V_{PSP} = f(V_{IS})$; $T_{mb} \geq 25$ °C

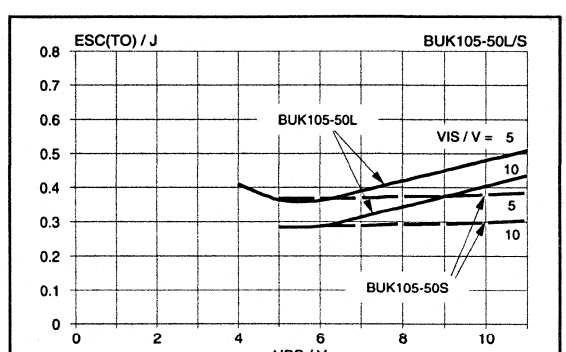


Fig.20. Typical overload protection energy, T_j = 25 °C $E_{SC(TO)} = f(V_{PS})$; conditions: V_{DS} = 13 V, parameter V_{IS}

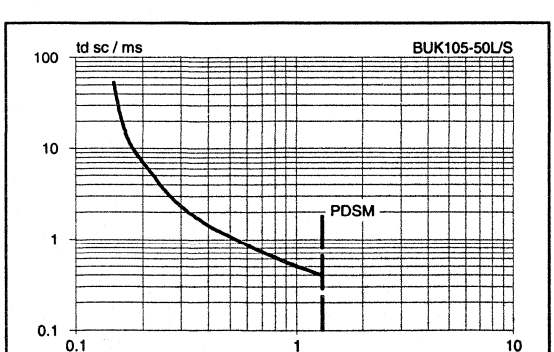


Fig.18. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{PS} \geq V_{PSP}$; $V_{IS} \geq 5$ V

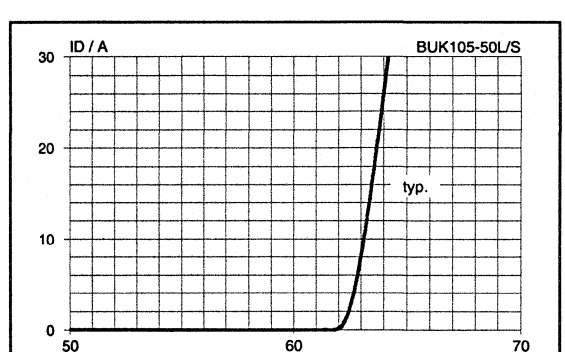


Fig.21. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: R_{IS} = 100 Ω; $t_p \leq 50$ µs

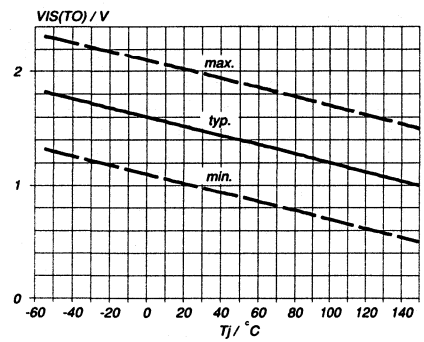


Fig.22. Input threshold voltage.
$V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

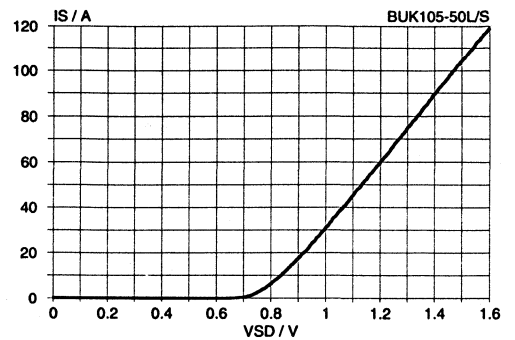


Fig.25. Typical reverse diode current, T_j = 25 °C.
$I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

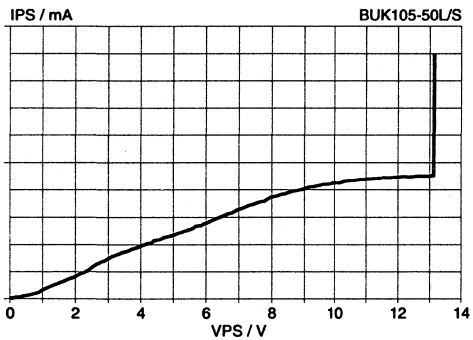


Fig.23. Typical DC protection supply characteristics.
$I_{PS} = f(V_{PS})$; normal or overload operation; T_j = 25 °C

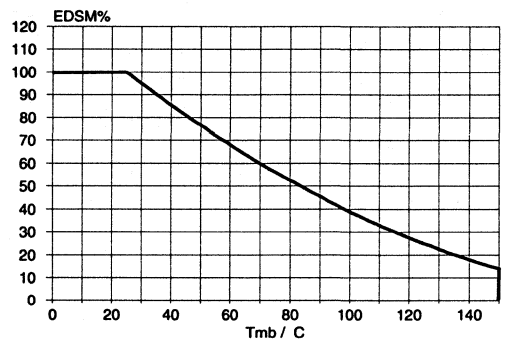


Fig.26. Normalised limiting clamping energy.
E_{DSM}% = $f(T_{mb})$; conditions: I_D = 29 A

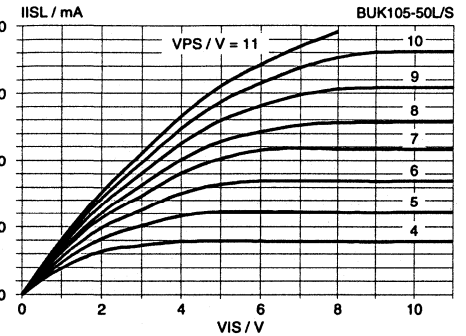


Fig.24. Typical latched input characteristics, 25 °C.
$I_{ISL} = f(V_{IS})$; after overload protection latched

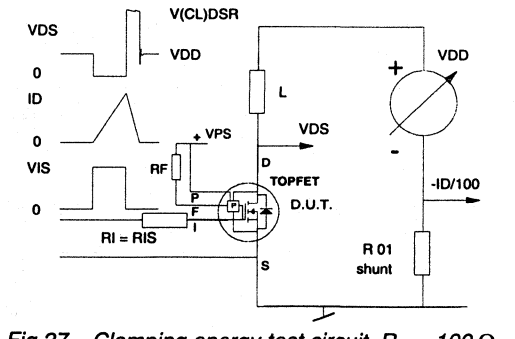


Fig.27. Clamping energy test circuit, R_{IS} = 100 Ω.
$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSR}/(V_{(CL)DSR} - V_{DD})$$

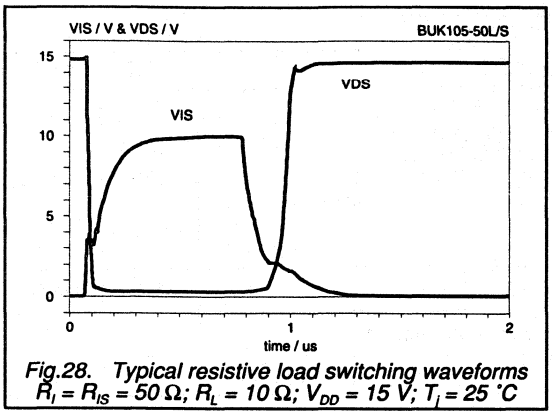


Fig.28. Typical resistive load switching waveforms $R_l = R_{IS} = 50\ \Omega$; $R_L = 10\ \Omega$; $V_{DD} = 15$ V; $T_j = 25$ °C

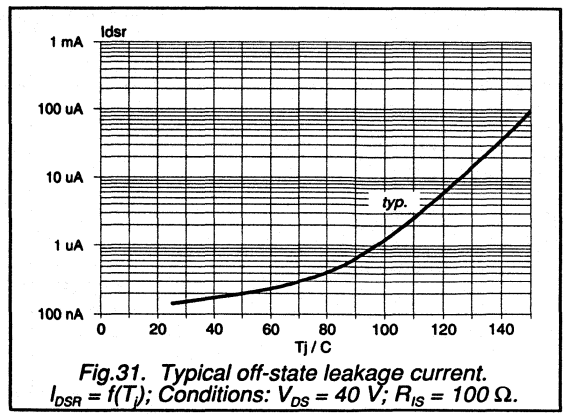


Fig.31. Typical off-state leakage current. $I_{DSR} = f(T_j)$; Conditions: $V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$.

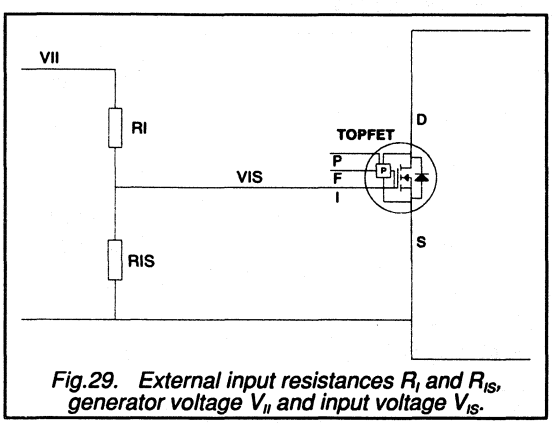


Fig.29. External input resistances R_I and R_{IS}, generator voltage V_{II} and input voltage V_{IS}.

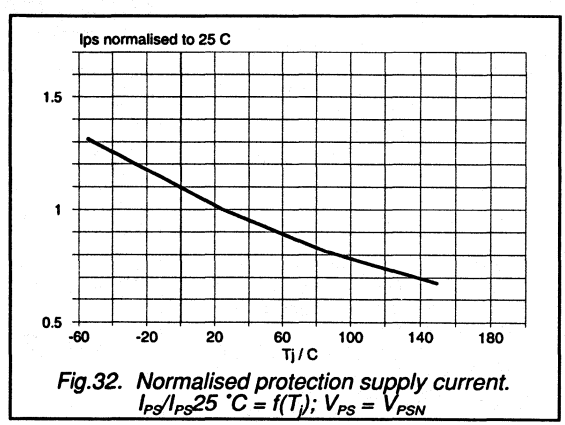


Fig.32. Normalised protection supply current. $I_{PS}/I_{PS}25\ °C = f(T_j)$; $V_{PS} = V_{PSN}$

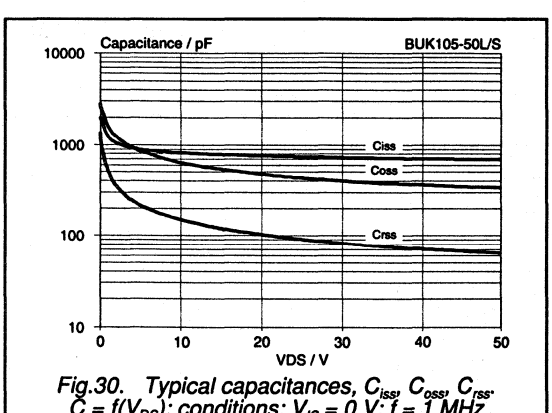


Fig.30. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $f = 1$ MHz

PowerMOS transistor
Logic level TOPFET

BUK106-50L/S
BUK106-50LP/SP

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 5 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Logic and protection supply from separate pin
- Low operating supply current
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by protection supply
- Protection circuit condition indicated by flag pin
- 5 V logic compatible input level
- Separate input pin for higher frequency drive
- ESD protection on input, flag and protection supply pins
- Over voltage clamping for turn off of inductive loads
- Both linear and switching operation are possible

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	50	A
P_{tot}	Total power dissipation	125	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		
	V_{IS} = 5 V	35	mΩ
	V_{IS} = 8 V	28	mΩ
SYMBOL	**PARAMETER**	**NOM.**	**UNIT**
V_{PSN}	Protection supply voltage		
	BUK106-50L	5	V
	BUK106-50S	10	V

FUNCTIONAL BLOCK DIAGRAM

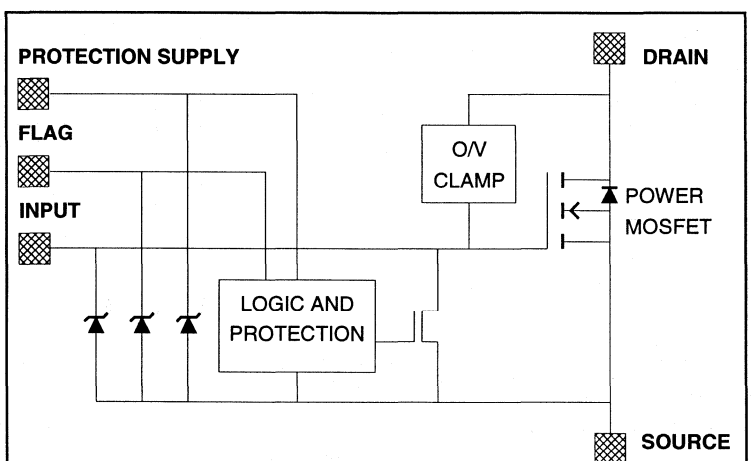


Fig.1. Elements of the TOPFET.

PINNING - SOT263

PIN	DESCRIPTION
1	input
2	flag
3	drain
4	protection supply
5	source
tab	drain

PIN CONFIGURATION

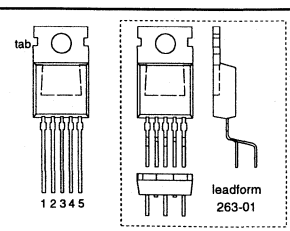


Fig. 2. Type numbers ending with suffix P refer to leadform 263-01.

SYMBOL

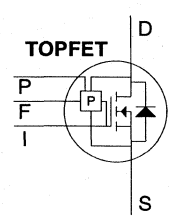


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
	Voltages					
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50		V
V_{IS}	Continuous input voltage	-	0	11		V
V_{FS}	Continuous flag voltage	-	0	11		V
V_{PS}	Continuous supply voltage	-	0	11		V
	Currents	V_{IS} =	-	8	5	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C	-	50	45	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C	-	31	28	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C	-	200	180	A
	Thermal					
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125		W
T_{stg}	Storage temperature	-	-55	150		°C
T_j	Junction temperature[2]	continuous	-	150		°C
T_{sold}	Lead temperature	during soldering	-	250		°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply connected, TOPFET can protect itself from two types of overload - over temperature and short circuit load.

An n-MOS transistor turns on between the input and source to quickly discharge the power MOSFET gate capacitance.

For internal overload protection to remain latched while the control circuit is high, external series input resistance must be provided. Refer to INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.		MAX.	UNIT
		V_{IS} =	8	5	-	V
V_{PSP}	Protection supply voltage[3]	for valid protection				
		BUK106-50L	4.4	4	-	V
		BUK106-50S	5.4	5	-	V
	Over temperature protection	$V_{PS} = V_{PSN}$				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-		50	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-		50	V
	Short circuit load protection	$V_{PS} = V_{PSN}$; L ≤ 10 µH				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-		24	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-		45	V
P_{DSM}	Instantaneous overload dissipation		-		4	kW

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The minimum supply voltage required for correct operation of the overload protection circuits.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DRRM}	Repetitive peak clamping drain current	$R_{IS} \geq 100\ \Omega$[1]	-	50	A
E_{DSM}	Non-repetitive inductive turn-off energy[2]	I_{DM} = 27 A; $R_{IS} \geq 100\ \Omega$	-	1	J
E_{DRM}	Repetitive inductive turn-off energy	$R_{IS} \geq 100\ \Omega$; $T_{mb} \leq 85$ °C; I_{DM} = 16 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	80	mJ
I_{DIRM}	Repetitive peak drain to input current[3]	R_{IS} = 0 Ω; $t_p \leq 1$ ms	-	50	mA

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	T_{mb} = 25 °C; $V_{IS} = V_{PS} = V_{FS}$ = 0 V	-	50	A

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1.0	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamping voltage	R_{IS} = 100 Ω; I_D = 10 mA		50	-	65	V
$V_{(CL)DSR}$	Drain-source clamping voltage	R_{IS} = 100 Ω; I_{DM} = 1 A; $t_p \leq 300$ µs; δ ≤ 0.01		50	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V		-	0.5	10	µA
I_{DSR}	Drain source leakage current	V_{DS} = 50 V; R_{IS} = 100 Ω;		-	1	20	µA
I_{DSR}	Drain source leakage current	V_{DS} = 40 V; R_{IS} = 100 Ω; T_j = 125 °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	I_{DM} = 25 A; $t_p \leq 300$ µs; δ ≤ 0.01	V_{IS} = 8 V	-	22	28	mΩ
			V_{IS} = 5 V	-	28	35	mΩ

1 The input pin must be connected to the source pin by a specified external resistance to allow the power MOSFET gate source voltage to become sufficiently positive for active clamping. Refer to INPUT CHARACTERISTICS.

2 While the protection supply voltage is connected, during overvoltage clamping it is possible that the overload protection may operate at energies close to the limiting value. Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 Shorting the input to source with low resistance inhibits the internal overvoltage protection by preventing the power MOSFET gate source voltage becoming positive.

OVERLOAD PROTECTION CHARACTERISTICS

With adequate protection supply voltage TOPFET detects when one of the overload thresholds is exceeded.

Provided there is adequate input series resistance it switches off and remains latched off until reset by the protection supply pin.

Refer also to OVERLOAD PROTECTION LIMITING VALUES and INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	$V_{PS} = V_{PSN}$[2]; $T_{mb} = 25$ °C; $L \leq 10$ µH				
$E_{DS(TO)}$	Overload threshold energy	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	550	-	mJ
$t_{d\,sc}$	Response time	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	0.4	-	ms
	Over temperature protection	$V_{PS} = V_{PSN}$				
$T_{j(TO)}$	Threshold junction temperature	from $I_D \geq 2.5$ A[3]	150	-	-	°C

TRANSFER CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 12$ V; $I_{DM} = 25$ A $t_p \leq 300$ µs; $\delta \leq 0.01$	17	28	-	S
I_D	Drain current[4]	$V_{DS} = 13$ V; $V_{IS} = 5$ V	-	80	-	A
		$V_{IS} = 10$ V		160	-	A

PROTECTION SUPPLY CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Protection supply					
I_{PS}, I_{PSL}	Protection supply current	normal operation or protection latched				
		BUK106-50L $V_{PS} = 5$ V	-	0.2	0.35	mA
		BUK106-50S $V_{PS} = 10$ V	-	0.4	1.0	mA
V_{PSR}	Protection reset voltage[5]		1.5	2.5	3.5	V
		$T_j = 150$ °C	1.0	-	-	V
$V_{(CL)PS}$	Protection clamp voltage	$I_P = 1.35$ mA	11	13	-	V

REVERSE DIODE CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	$I_S = 20$ A; $V_{IS} = V_{PS} = V_{FS} = 0$ V; $t_p = 300$ µs	-	0.9	1.2	V
t_{rr}	Reverse recovery time	not applicable[6]	-	-	-	-

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum.

2 At the appropriate nominal protection supply voltage for each type. Refer to QUICK REFERENCE DATA.

3 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

4 During overload condition. Refer also to OVERLOAD PROTECTION LIMITING VALUES and CHARACTERISTICS.

5 The supply voltage below which the overload protection circuits will be reset.

6 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
	Normal operation						
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
			T_{mb} = 150 °C	0.5	-	-	V
I_{IS}	Input current	V_{IS} = 10 V		-	10	100	nA
$V_{(CL)IS}$	Input clamp voltage	I_I = 1 mA		11	13	-	V
	Overload protection latched						
R_{ISL}	Input resistance[1]	V_{PS} = 5 V	I_L = 5 mA;	-	55	-	Ω
			T_{mb} = 150 °C	-	95	-	Ω
		V_{PS} = 10 V	I_L = 5 mA;	-	35	-	Ω
			T_{mb} = 150 °C	-	60	-	Ω
	Application information						
	External input resistances for	(see figure 29)					
R_{IS}	internal overvoltage clamping[2]	R_I = ∞ Ω;	V_{DS} > 30 V	100	-	-	Ω
R_I	internal overload protection[3]	R_{IS} = ∞ Ω;	V_{II} = 5 V	1	-	-	kΩ
			V_{II} = 10 V	2	-	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C; R_I = 50 Ω; R_{IS} = 50 Ω (see figure 29); resistive load R_L = 10 Ω. For waveforms see figure 28.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; V_{IS}: 0 V ⇒ 10 V	-	10	-	ns
t_r	Rise time		-	35	-	ns
$t_{d\,off}$	Turn-off delay time	V_{DD} = 15 V; V_{IS}: 10 V ⇒ 0 V	-	280	-	ns
t_f	Fall time		-	120	-	ns

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{iss}	Input capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	1250	1800	pF
C_{oss}	Output capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	650	1000	pF
C_{rss}	Reverse transfer capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	150	250	pF
C_{pso}	Protection supply pin capacitance	V_{PS} = 10 V	-	30	-	pF
C_{fso}	Flag pin capacitance	V_{FS} = 10 V; V_{PS} = 0 V	-	20	-	pF

1 The resistance of the internal transistor which discharges the power MOSFET gate capacitance when overload protection operates.
The external drive circuit should be such that the input voltage does not exceed $V_{IS(TO)}$ minimum when the overload protection has operated. Refer also to figure for latched input characteristics.

2 Applications using a lower value for R_{IS} would require external overvoltage protection.

3 For applications requiring a lower value for R_I, an external overload protection strategy is possible using the flag pin to 'tell' the control circuit to switch off the input.

FLAG DESCRIPTION

The flag pin provides a means to detect the presence of the protection supply and indicate the state of the overload detectors. The flag is the open drain of an n-MOS transistor and requires an external pull-up resistor[1]. It is suitable for both 5 V and 10 V logic. Flag may be used to implement an external protection strategy[2] for applications which require low input drive impedance.

TRUTH TABLE

CONDITION	DESCRIPTION	FLAG
NORMAL	Normal operation and adequate protection supply voltage	LOGIC LOW
OVER TEMP.	Over temperature detected	LOGIC HIGH
SHORT CIRCUIT	Overload condition detected	LOGIC HIGH
SUPPLY FAULT	Inadequate protection supply voltage	LOGIC HIGH

FLAG CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Flag 'low'	normal operation				
V_{FS}	Flag voltage	I_F = 1.6 mA	-	0.15	0.4	V
I_{FSS}	Flag saturation current	V_{FS} = 10 V	-	15	-	mA
	Flag 'high'	overload or fault				
I_{FS}	Flag leakage current	V_{FS} = 10 V	-	-	10	µA
V_{PSF}	Protection supply threshold voltage	V_{FF} = 5 V; R_F = 3 kΩ;				
		BUK106-50L	2.5	3.3	4	V
		BUK106-50S	3.3	4.2	5	V
$V_{(CL)FS}$	Flag clamping voltage	I_F = 1 mA; V_{PS} = 0 V	11	13	-	V
	Application information					
R_F	Suitable external pull-up resistance	V_{FF} =5 V	1	10	50	kΩ
		V_{FF} =10 V	2	20	100	kΩ

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 Even if the flag pin is not used, it is recommended that it is connected to the protection supply via a pull-up resistor. It should not be left floating.

2 Low pass filtering of the flag signal may be advisable to prevent false tripping.

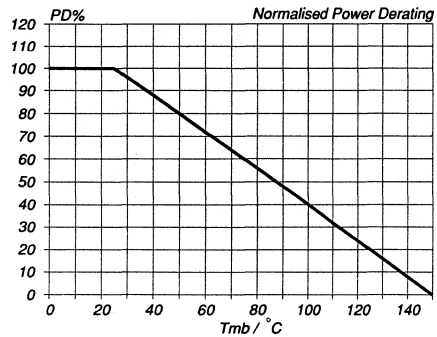


Fig.4. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D / P_D(25\ ^\circ C) = f(T_{mb})$

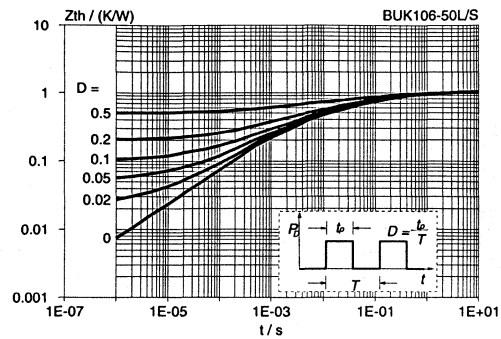


Fig.7. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

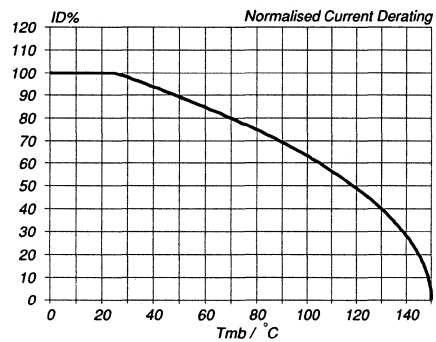


Fig.5. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D / I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

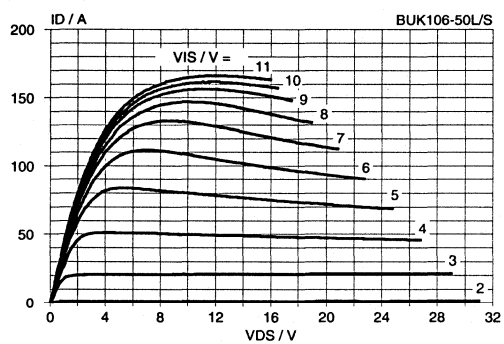


Fig.8. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

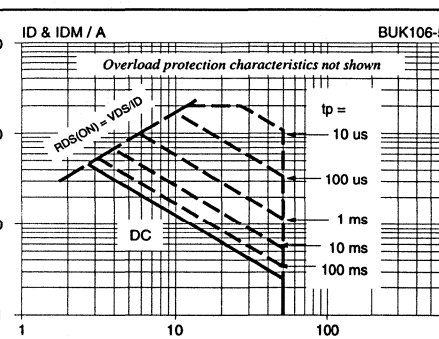


Fig.6. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

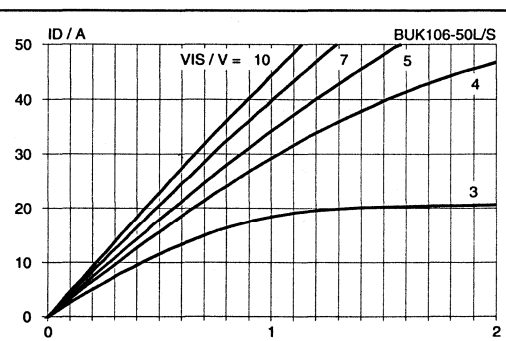


Fig.9. Typical on-state characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

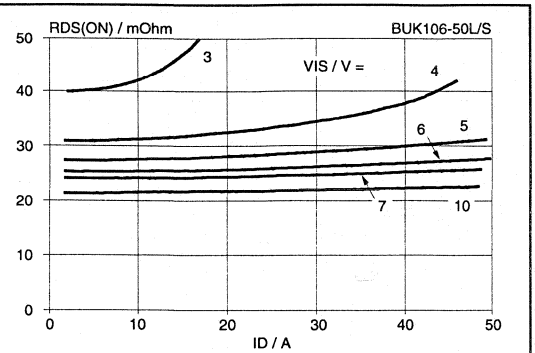


Fig.10. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

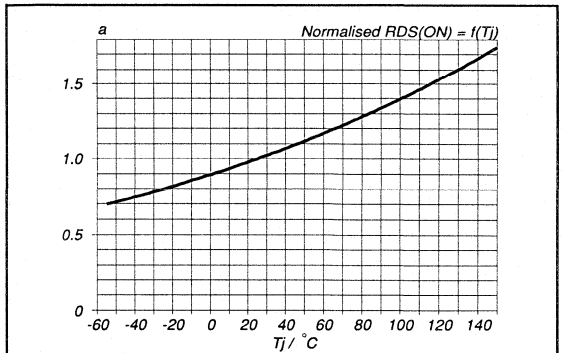


Fig.13. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ °C = f(T_j)$; I_D = 25 A; $V_{IS} \geq 5$ V

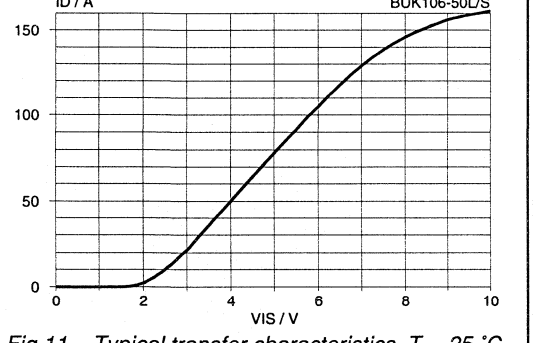


Fig.11. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 12 V; t_p = 250 µs

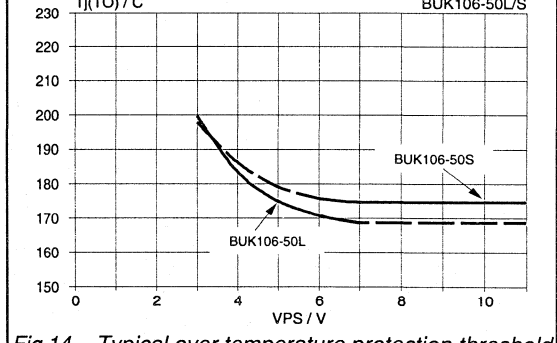


Fig.14. Typical over temperature protection threshold $T_{j(TO)} = f(V_{PS})$; conditions: $V_{DS} > 0.1$ V

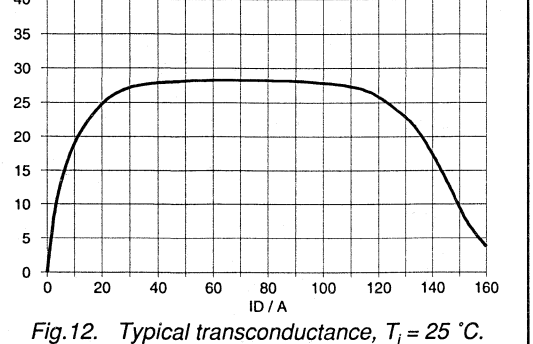


Fig.12. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 12 V; t_p = 250 µs

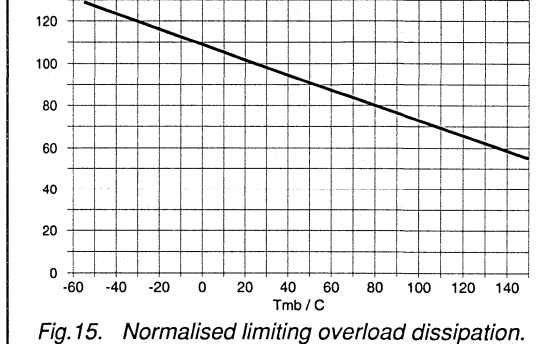


Fig.15. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

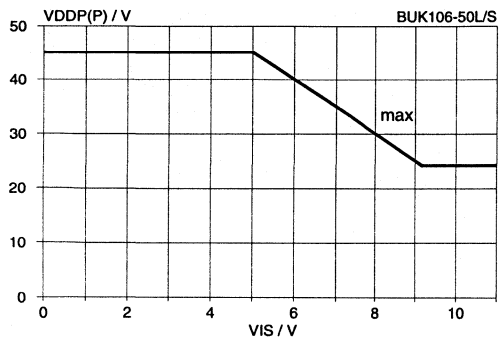


Fig.16. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150$ °C

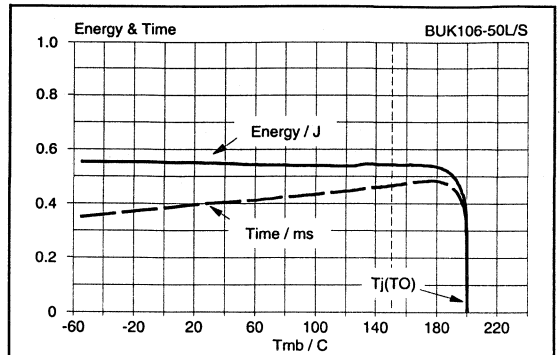


Fig.19. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; $V_{PS} = V_{PSN}$, V_{IS} = 8 V; SC load

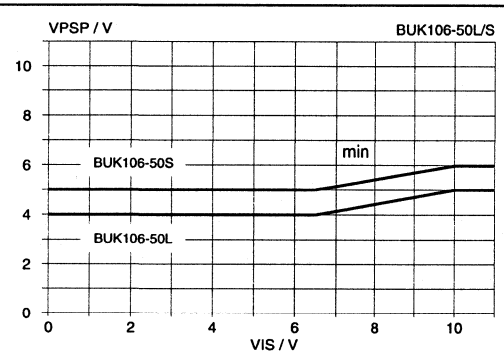


Fig.17. Minimum protection supply voltage for SC load protection. $V_{PSP} = f(V_{IS})$; $T_{mb} \geq 25$ °C

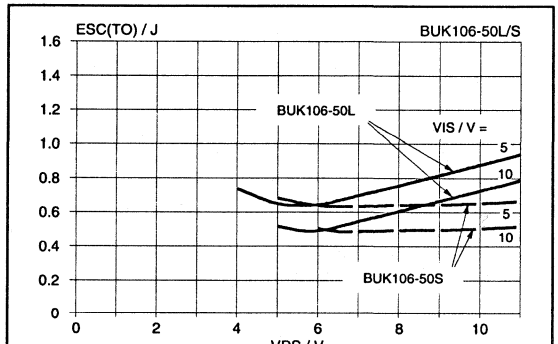


Fig.20. Typical overload protection energy, T_j = 25 °C $E_{SC(TO)} = f(V_{PS})$; conditions: V_{DS} = 13 V, parameter V_{IS}

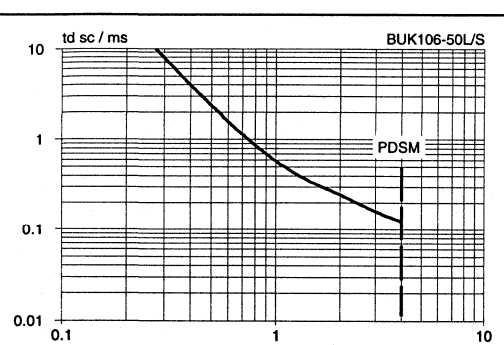


Fig.18. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{PS} \geq V_{PSP}$; $V_{IS} \geq 5$ V

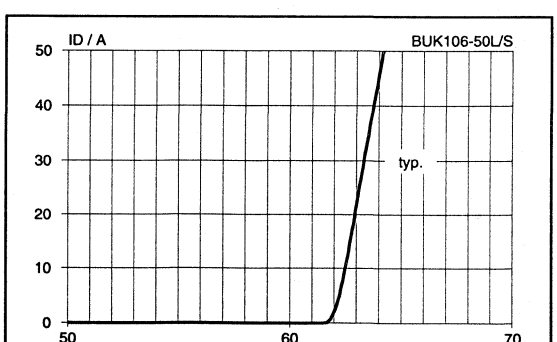


Fig.21. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: R_{IS} = 100 Ω; $t_p \leq 50$ µs

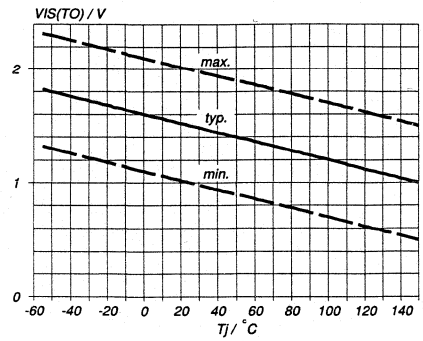


Fig.22. Input threshold voltage.
$V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

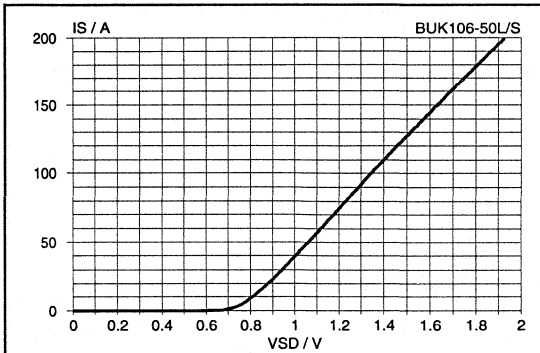


Fig.25. Typical reverse diode current, T_j = 25 °C.
$I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

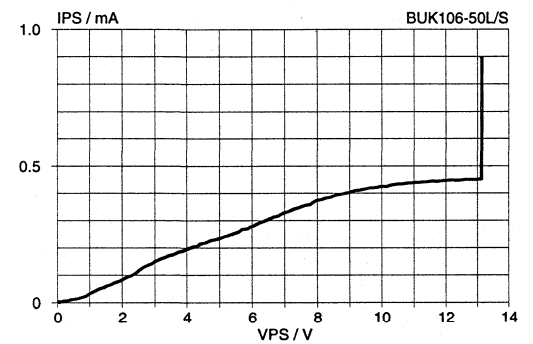


Fig.23. Typical DC protection supply characteristics.
$I_{PS} = f(V_{PS})$; normal or overload operation; T_j = 25 °C

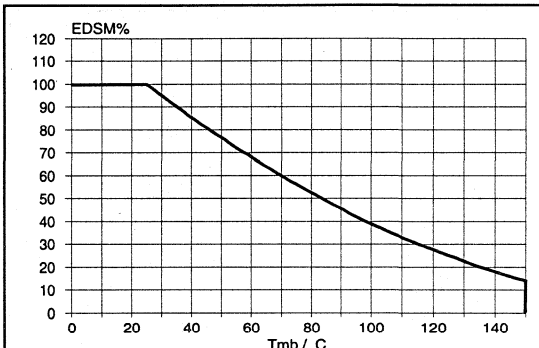


Fig.26. Normalised limiting clamping energy.
$E_{DSM}\% = f(T_{mb})$; conditions: I_D = 27 A

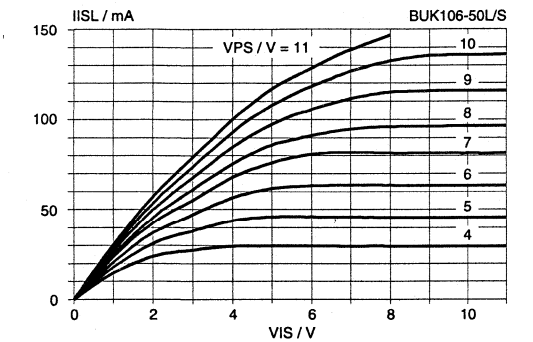


Fig.24. Typical latched input characteristics, 25 °C.
$I_{ISL} = f(V_{IS})$; after overload protection latched

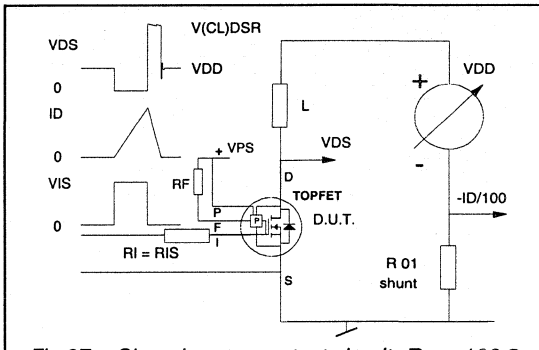


Fig.27. Clamping energy test circuit, R_{IS} = 100 Ω.
$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSR}/(V_{(CL)DSR} - V_{DD})$

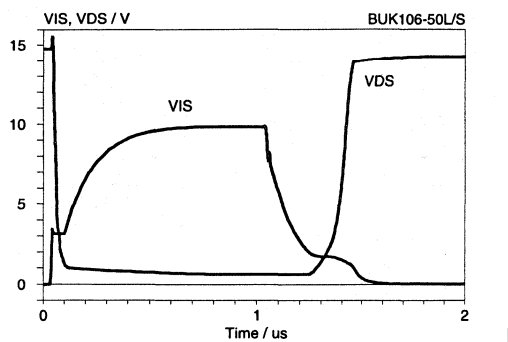


Fig.28. Typical resistive load switching waveforms $R_I = R_{IS} = 50\ \Omega$; $R_L = 10\ \Omega$; $V_{DD} = 15$ V; $T_j = 25$ °C

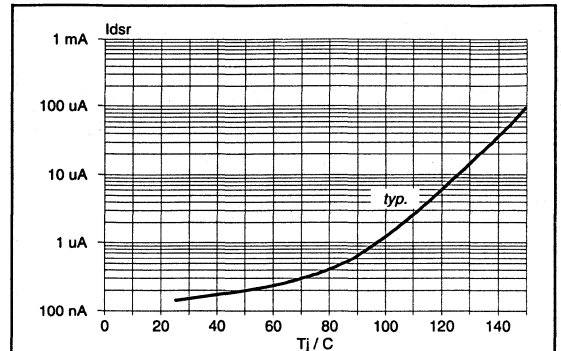


Fig.31. Typical off-state leakage current. $I_{DSR} = f(T_j)$; Conditions: $V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$.

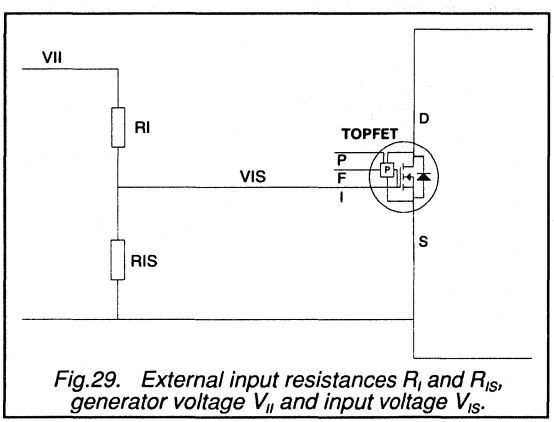


Fig.29. External input resistances R_I and R_{IS}, generator voltage V_{II} and input voltage V_{IS}.

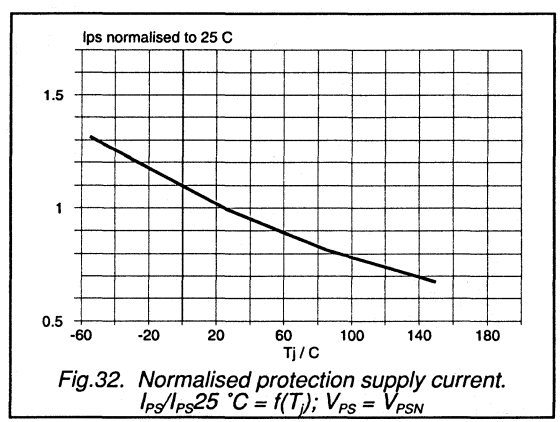


Fig.32. Normalised protection supply current. $I_{PS}/I_{PS}25\ ^\circ C = f(T_j)$; $V_{PS} = V_{PSN}$

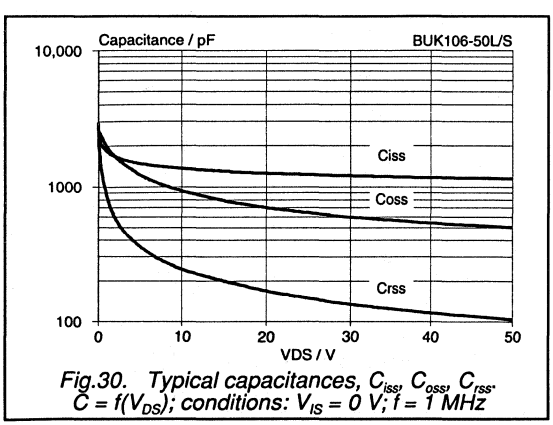


Fig.30. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $f = 1$ MHz

Highside PWM lamp dimmer using TOPFET

Application report

Although the 3-pin TOPFETs were designed for low side switch applications, they can, by using standard MOSFET bootstrap techniques, be used in applications which need high side control. One such application is the dimming of automotive headlamps and panel lamps. These applications need not only a high side switch but also slow, controlled switching to reduce problems of EMI.

This note will give details of a circuit which fulfils the operational requirements of this application and, because it uses a TOPFET, is well protected against shorted load and overvoltage faults.

Circuit Description

The circuit shown in Fig. 1 shows the high side PWM dimmer circuit. All the main components are shown, the only exception being the source of the PWM control signal. This could be either the system controller or a dedicated oscillator depending on the nature of the overall system. The circuit of Fig. 1 assumes that the signal is a rectangular pulse train of the required frequency and duty cycle, with an amplitude of 10 V.

The input signal is attenuated by R2 and R3 and fed to the base of Q1. The combination of R1 and Q1 will invert and level shift the signal and feed it to the input of the BUK101-50GS TOPFET.

D1, C1 and the TOPFET form the bootstrap circuit. The low end of C1 is connected to the TOPFET source. When TOPFET is OFF its source is close to ground, so C1 charges to Vbat via D1. When TOPFET turns ON, its source rises to nearly Vbat, lifting the high end of C1 well above Vbat. C1 can, therefore, provide more than enough voltage to drive the TOPFET input. In fact, when Vbat is higher than normal, the voltage would exceed the continuous V_{IS} rating of the BUK101-50GS, so D3 is included to restrict the input voltage to below 11 V.

Capacitor C2 adds to the Miller capacitance of Q1 and limits the rate of change of collector voltage. The TOPFET acts like a source follower circuit, so the load voltage rises and falls at the same rate as the collector-emitter voltage of Q1.

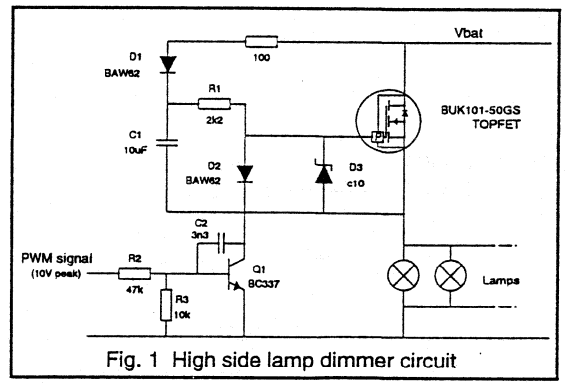


Fig. 1 High side lamp dimmer circuit

Component Values

With the components specified the circuit will operate at a frequency between 50 and 200 Hz and has rise and fall times of about 300 µs. This slow switching means that the minimum OFF time, for satisfactory bootstrap operation, is about 1 ms. At 50 Hz this gives a maximum duty cycle of 95%.

The value of C1 has been chosen to ensure that TOPFET input current does not cause the C1 voltage to fall significantly during the maximum ON time. This means that the lowest on state dissipation is being achieved. Lower values could be used but the voltage droop would be greater and care would be needed to ensure that the input voltage does not fall below the V_{ISP} of the TOPFET, otherwise the protection features may not function.

The rate of switching can be changed by adjusting the value of C2. Larger values would reduce switching speed. Considerable care is needed when switching times become very long because while the input voltage is below the V_{ISP} the TOPFET is unprotected. Switching times can be reduced to about 50 µs by reducing the value of C2 to 470 pF. To reduce the switching times further will mean a change to the input drive.

Highside PWM lamp dimmer using TOPFET

Application report

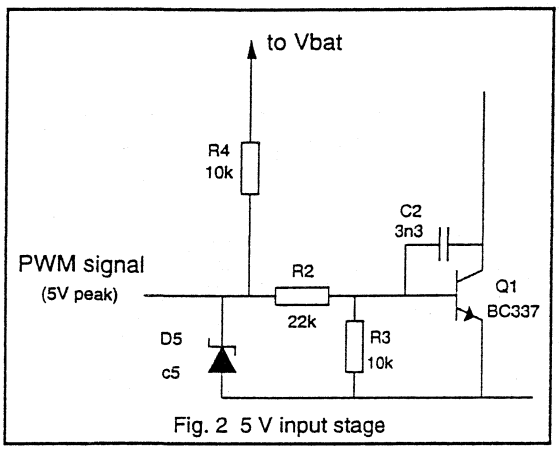


Fig. 2 5 V input stage

Switching rate, in particular the turn-off rate, is also influenced by the amplitude of the input signal. R2 and R3 have been chosen to give similar rise and fall times with an input of 10 V. If the input amplitude is lower the fall time would increase. This can be compensated for by lower attenuation. An input modified for 5 V input is shown in Fig. 2. This arrangement also includes D5 to clamp the input voltage to 5 V and R4 to allow the use of an open collector or drain drivers.

Operation in fault conditions

TOPFET will protect itself against high voltage supply line transients by partially turning on and restricting the applied voltage to about 60 V. In high side applications the remainder of high voltage may appear across the load. In many systems the grounding and smoothing arrangements will ensure that this will not be problem. In some configurations the TOPFET source will rise above ground while the input is held at ground. This means that the TOPFET input will be negative while its drain-source voltage is high. This may damage the TOPFET. This difficulty can be eliminated by the input circuit shown in Fig. 3. In this circuit diode D4 will turn off if the source voltage rises. The input is, therefore, no longer clamped by the drive and can rise with the source, eliminating the risk of damage.

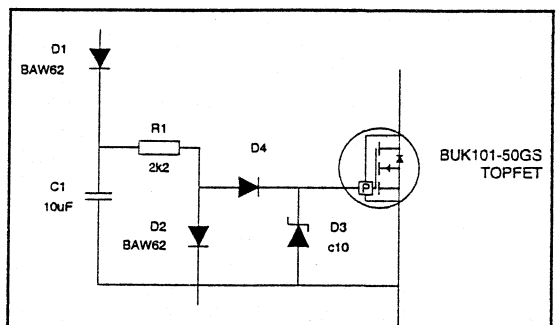


Fig. 3 Protection against negative input

If the load becomes short circuit, TOPFET will trip as soon as the temperature of the power part of the chip becomes too high. Since this circuit is a PWM controller the TOPFET will be reset at the end of the ON period. During the period between tripping and the start of the next cycle the TOPFET will cool. It will, therefore, turn on when the input goes high again and the short circuit current will flow until TOPFET is tripped once more.

TOPFET is able to withstand this type of operation for a considerable period of time but not necessarily indefinitely. The dissipation is considerable, the temperatures could be high and operating life may be affected. It is advisable, therefore, that short circuit operation is evaluated.

An introduction to the highside TOPFET

Application report

The introduction of high side TOPFETs enhances the range of protected power MOSFETs available from Philips. These devices combine the real power handling ability of low $R_{DS(ON)}$ MOSFETs with protection circuits and the interfacing to allow ground referenced logic signals to control a high side switch.

Type range

Table 1 shows the range of high side TOPFETs. Included in the range are devices with on-state resistance in the range 38 to 220 mΩ. For each of the types an 'X' or 'Y' variant can be supplied ('Y' types have an additional internal resistor in the ground line). All the devices are 50 V types designed for use in 12 V automotive systems.

Type	$R_{DS(ON)}$ (mΩ)
BUK200-50X / BUK200-50Y	100
BUK201-50X / BUK201-50Y	60
BUK202-50X / BUK202-50Y	38
BUK203-50X / BUK203-50Y	220

Table 1. High side TOPFET type range

Features

Particular care has been taken during the development of the high side TOPFET to make a device which closely matches the requirements of the automotive designer.

Overload Protection -

High side TOPFETs are protected from the full range of overload conditions. Low level overloads which result in higher than expected dissipation can cause the TOPFET to overheat. In this case the overtemperature sensor will trip and the TOPFET will turn itself off until the chip temperature falls below the reset point. In the event of a medium level overload, which could allow a high current to flow, TOPFET will limit the current, and hence dissipation, to a level which allows the overtemperature sensor time to react and turn the TOPFET off until it cools sufficiently. In high overload situations, like hard short circuits, the voltage developed across the TOPFET will cause the short circuit detector to react and latch the TOPFET off until it is reset by toggling the input. Both modes of overload turn-off are reported by pulling the status pin low.

Supply undervoltage lockout -

If the battery to ground voltage is too low for its circuits to work correctly a high side TOPFET will turn off.

Open load detection -

TOPFET monitors its own on-state voltage drop. If the drop is too low, indicating that the current is very small probably because the load is open circuit, TOPFET will report this by pulling the status pin low.

Quiescent current -

One factor of great importance, particularly as the number of devices in a car increases, is quiescent current. In TOPFETs, the supply which feeds the circuits is turned off when the input is low. This reduces off state current consumption from typically 25 μA to less than 1 μA.

Ground resistor -

For the fullest protection against the harsh automotive electrical environment, it is often necessary to fit a resistor between the ground pin of a high side device and module ground. To help with this the Y types of the TOPFET range have this resistor integrated on the chip. Apart from the obvious saving in component count, this approach has the advantage that the resistor is now in a package where its dissipation can be easily handled. (This feature is particularly useful when long duration reverse battery situations are being considered).

Inductive load turn-off clamping -

TOPFETs have a network between the MOSFET gate and the ground pin. This network sets the maximum negative potential between the load and ground pins. If the potential tries to exceed this figure, for example during inductive load turn-off, TOPFET will partially turn on, clamping the voltage at the load pin.

EMC

Electromagnetic compatibility is an increasingly important factor in all electronic designs. EMC covers the immunity and the emissions, both conducted and radiated, of electronic units and systems. The directives and tests are rarely applicable to individual electronic components although the behaviour of devices can have a significant influence on EMC performance. In recognition of this, TOPFET has been designed to create as few EMC problems as possible.

	Test Voltage	Pulse width
Pulse 1a	-100 V	0.05 ms
Pulse 1b		2 ms
Pulse 2a	+100 V	0.05 ms
Pulse 2b		0.5 ms
Pulse 3a	-200 V	0.1 µs
Pulse 3b	+200 V	0.1 µs
Pulse 5	+46.5 V	400 ms

Table 2. TOPFET transient tests

Conducted immunity -

One area where TOPFET helps with EMC is with its inherent immunity to conducted transients. The voltage supply of a vehicle is notorious for its transients and circuits and systems have to be designed to handle them. On the TOPFET chip are separate circuits which allow the output MOSFET and the control circuits to withstand transients between the battery and both the load and ground pins. The range of transients which high side TOPFETs can survive is shown in Table 2.

Low emission -

High side switch devices generate their gate drive voltage with oscillators and charge pumps running at high frequency - often in excess of 1 MHz. Unless care is taken in the basic design of the device, emissions at the oscillator frequency or its harmonics can appear at the ground and load pins.

The TOPFET designers have taken the necessary care. The appropriate choice of oscillator and charge pump circuits and the inclusion of on-chip filtering have reduced emissions considerably. Some indication of the improvement can be obtained by simply looking at the current in the ground pin with an AC coupled current probe. Waveforms for the ground pin current of a Philips TOPFET and another manufacturer's high side switch are shown in Fig. 1.

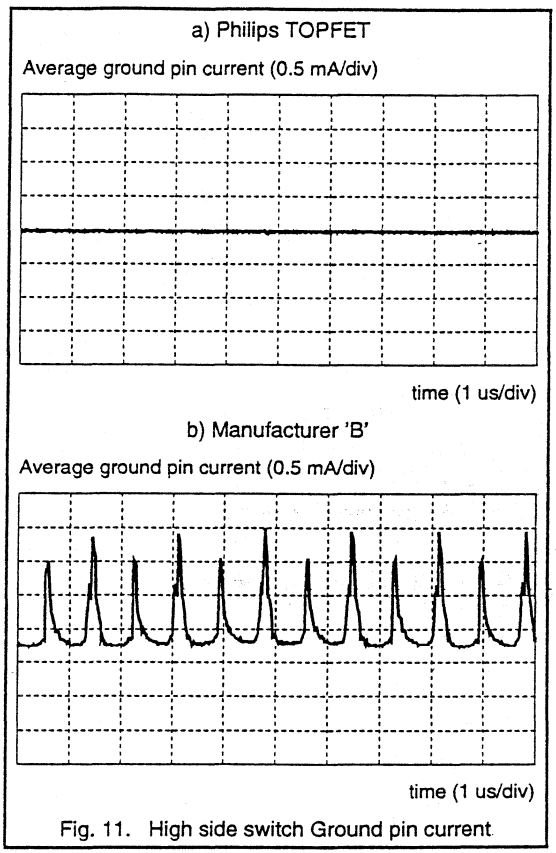


Fig. 11. High side switch Ground pin current

Conclusions

High side TOPFETs are real power devices designed for controlling a wide range of automotive loads. The care taken during their design means that TOPFETs are compatible with circuit designers' protection and EMC requirements.

PowerMOS transistor TOPFET high side switch

BUK202-50X

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	9	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	20	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	38	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input with hysteresis
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection with external ground resistor

FUNCTIONAL BLOCK DIAGRAM

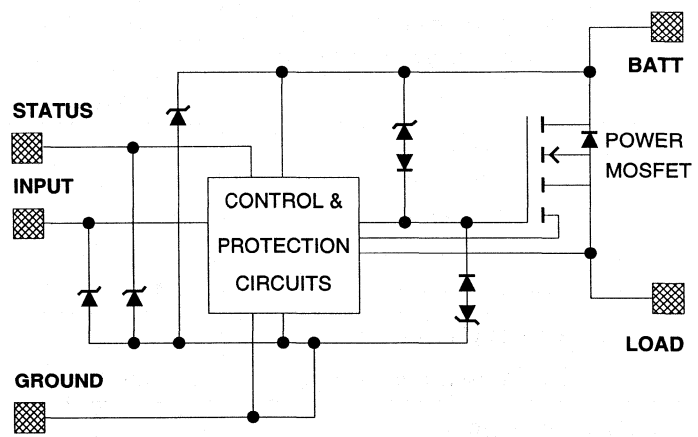


Fig.1. Elements of the TOPFET HSS.

PINNING - SOT263

PIN	DESCRIPTION
1	Ground
2	Input
3	Battery (+ve supply)
4	Status
5	Load
tab	connected to pin 3

PIN CONFIGURATION

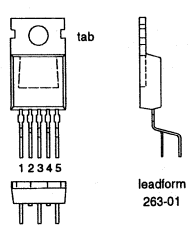


Fig. 2.

SYMBOL

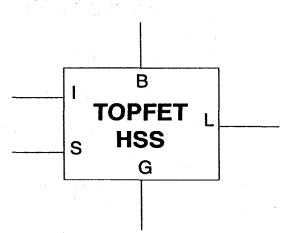


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 110$ °C	-	20	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	T_{mb} = 150 °C prior to turn-off	-	1.7	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	75	K/W

1 Reverse battery voltage is allowed only with external ground, input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	9	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 10 A; t_p = 300 µs	-	28	38	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 2 A; t_p = 300 µs	-	36	48	mΩ

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7	8	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.4	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	1.7	-	V
ΔV_{IG}	Input turn-on hysteresis		-	0.4	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	150	450	750	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	6	8	10	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	9	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 230 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.5 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.1 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 10 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq$ 10 mΩ				
$t_{d\,sc}$	Response time	V_{IG} = 5 V	-	160	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	42	-	A
	Overload protection[3]	eg $R_L \approx$ 0.25 Ω				
$I_{L(lim)}$	Load current limiting	V_{BL} = 6 V; t_p = 1 ms	20	35	60	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	0.7	2	V/µs
t_{on}	Total switching time	to 90% V_L	-	140	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	40	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	0.7	2	V/µs
t_{off}	Total switching time	to 10% V_L	-	70	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	500	700	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

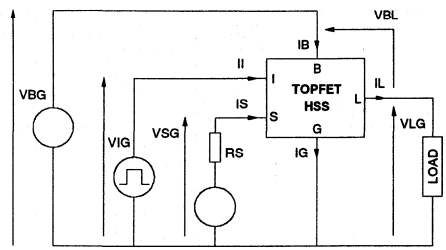


Fig.4. High side switch measurements schematic. (current and voltage conventions)

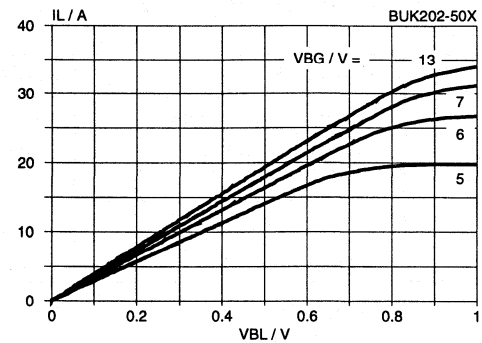


Fig.7. Typical on-state characteristics, T_j = 25 °C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

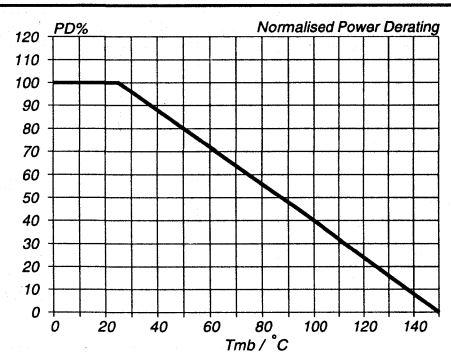


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ °C) = f(T_{mb})$

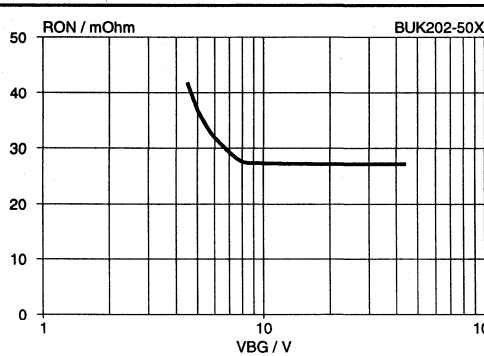


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{ON} = f(V_{BG})$; conditions: I_L = 10 A; t_p = 300 µs

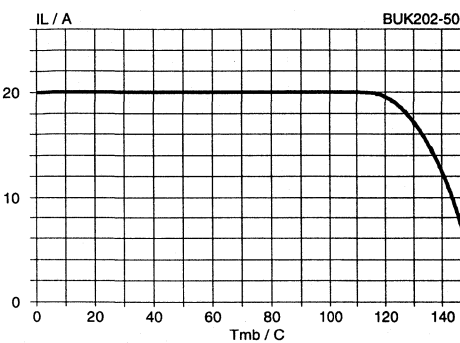


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

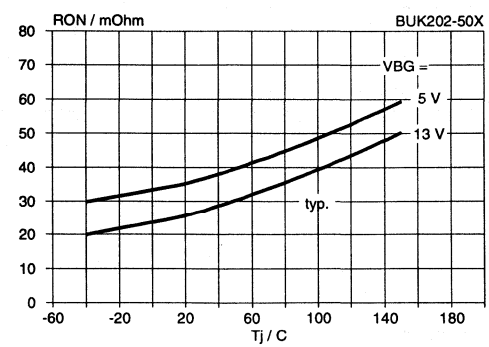


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 2 A

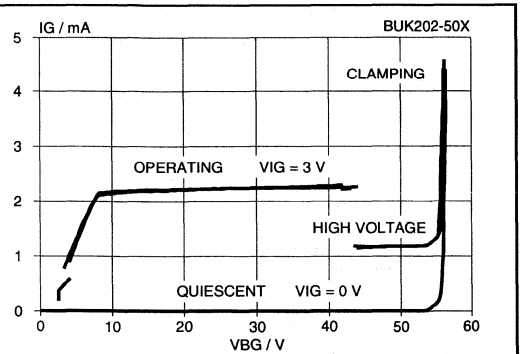


Fig.10. Typical supply characteristics, 25 °C. $I_G = f(V_{BG})$; parameter V_{IG}

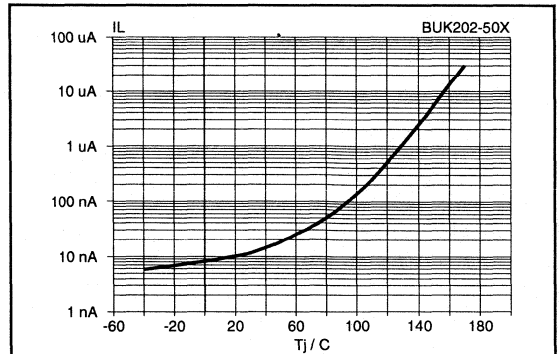


Fig.13. Typical off-state leakage current. $I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

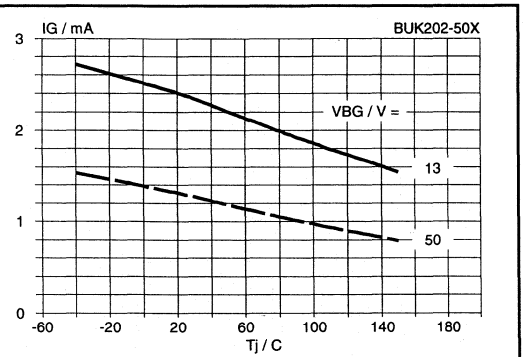


Fig.11. Typical operating supply current. $I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

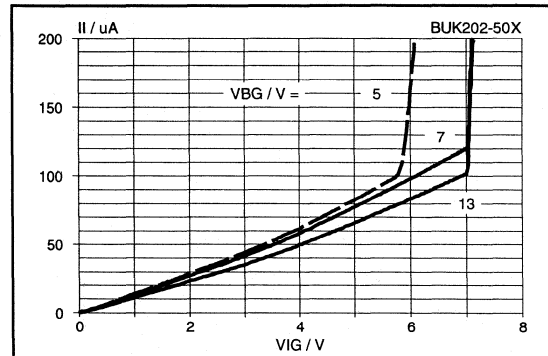


Fig.14. Typical input characteristics, T_j = 25 °C. $I_I = f(V_{IG})$; parameter V_{BG}

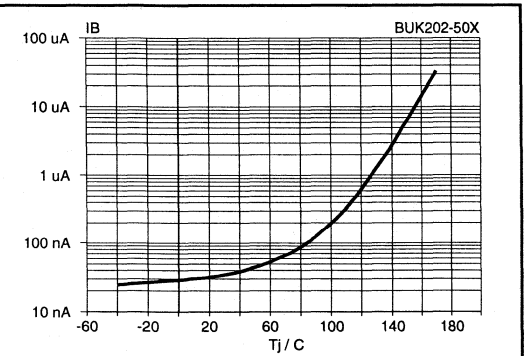


Fig.12. Typical supply quiescent current. $I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

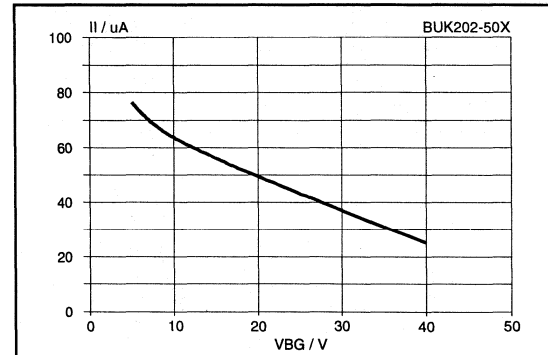


Fig.15. Typical input current, T_j = 25 °C. $I_I = f(V_{BG})$; condition V_{IG} = 5 V

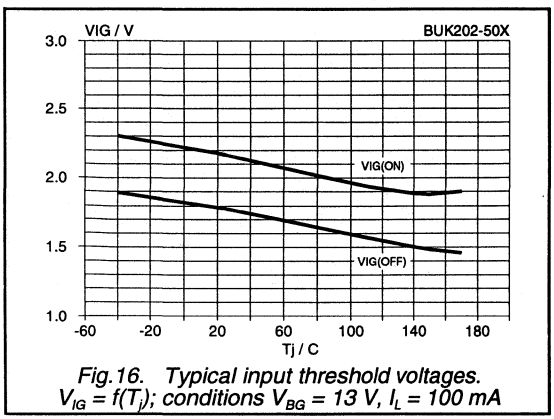


Fig.16. Typical input threshold voltages. $V_{IG} = f(T_j)$; conditions V_{BG} = 13 V, I_L = 100 mA

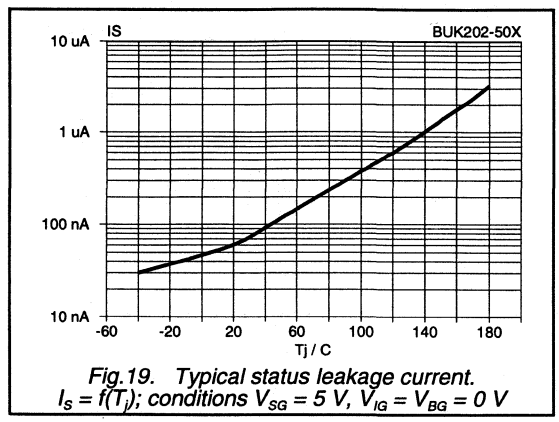


Fig.19. Typical status leakage current. $I_S = f(T_j)$; conditions V_{SG} = 5 V, $V_{IG} = V_{BG}$ = 0 V

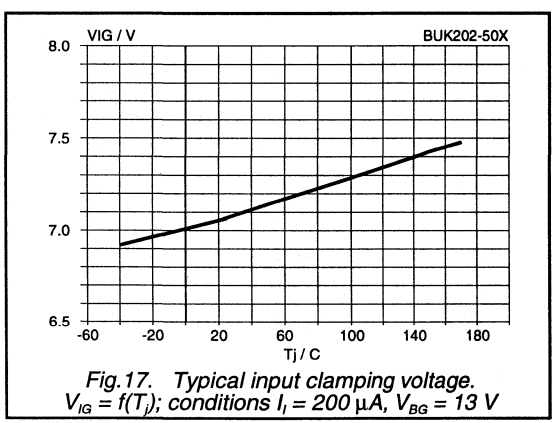


Fig.17. Typical input clamping voltage. $V_{IG} = f(T_j)$; conditions I_I = 200 µA, V_{BG} = 13 V

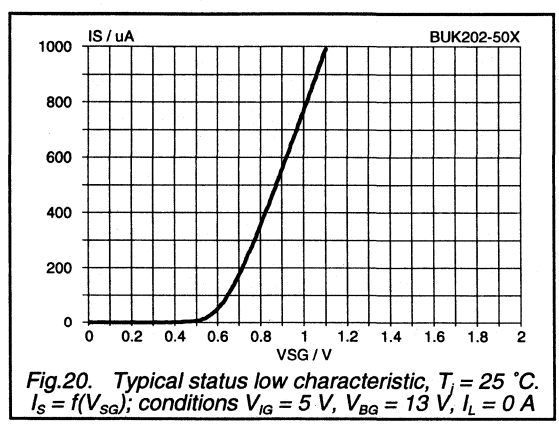


Fig.20. Typical status low characteristic, T_j = 25 °C. $I_S = f(V_{SG})$; conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

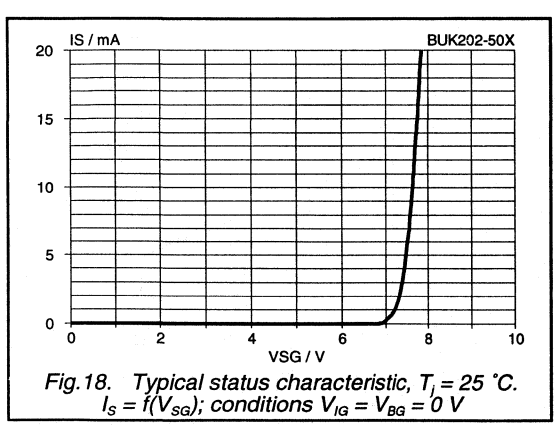


Fig.18. Typical status characteristic, T_j = 25 °C. $I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG}$ = 0 V

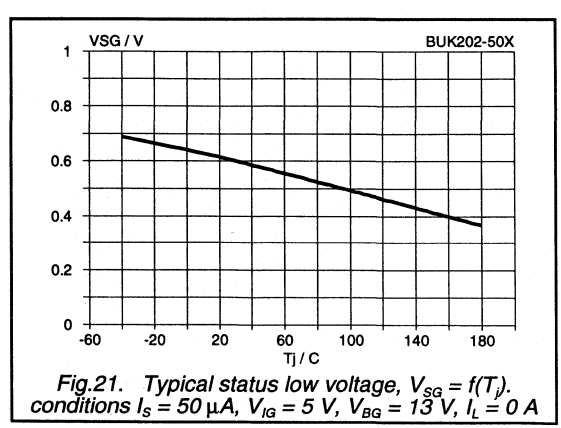


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$. conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

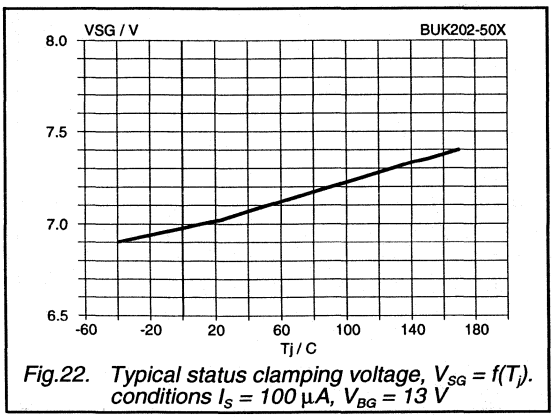


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

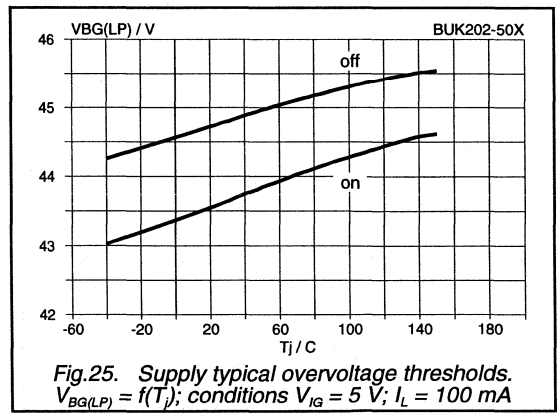


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 100\ mA$

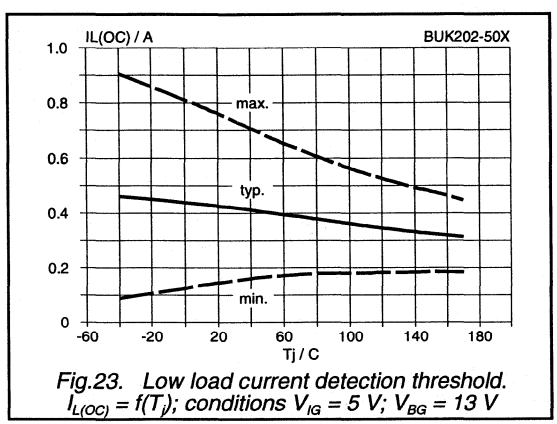


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

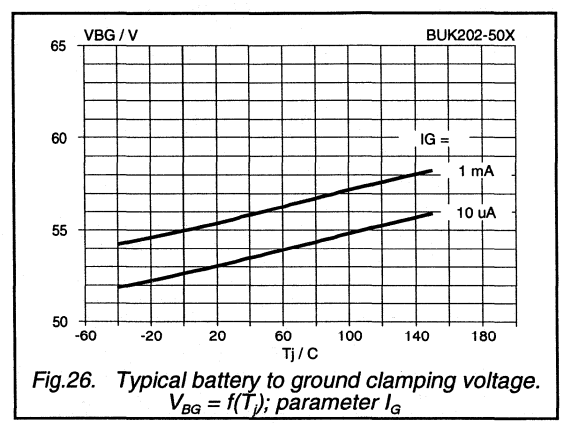


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

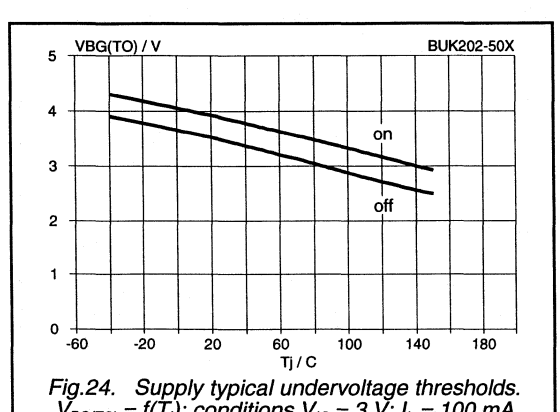


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 100\ mA$

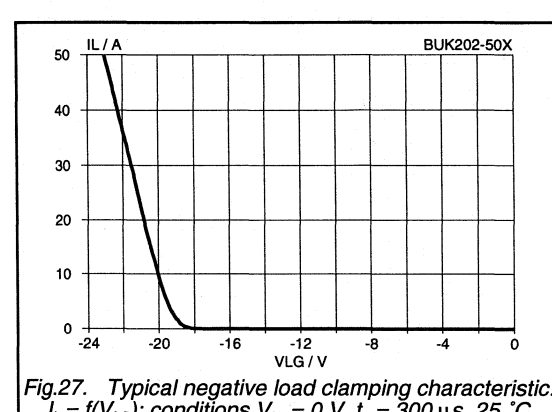


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

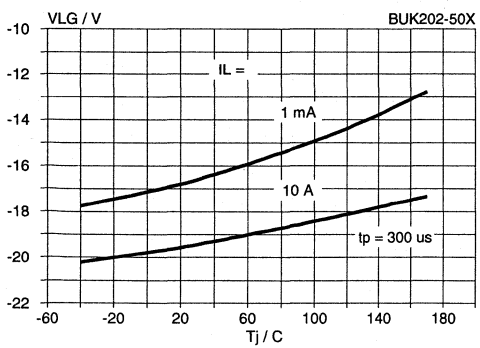


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

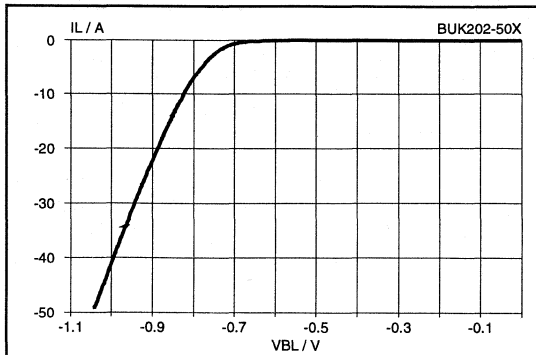


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

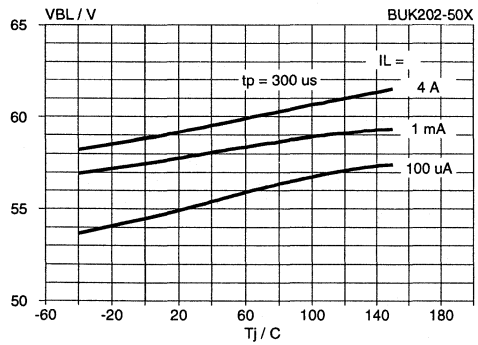


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

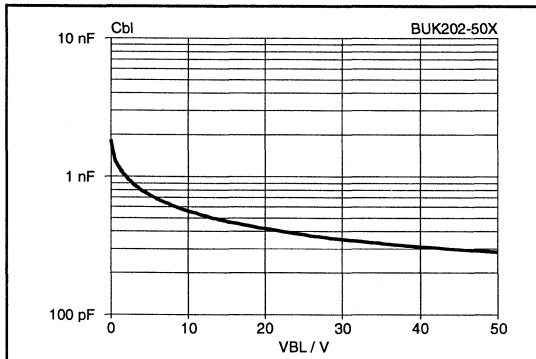


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions $f = 1$ MHz, $V_{IG} = 0$ V

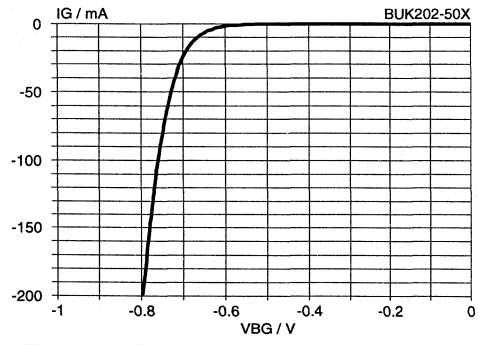


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

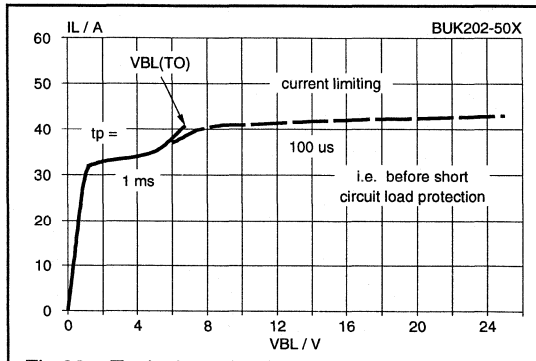


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

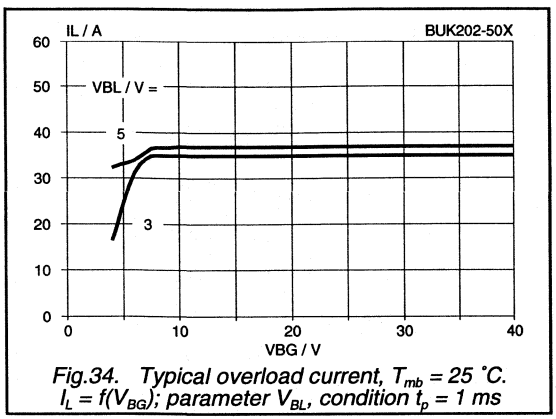


Fig.34. Typical overload current, T_{mb} = 25 °C. $I_L = f(V_{BG})$; parameter V_{BL}, condition t_p = 1 ms

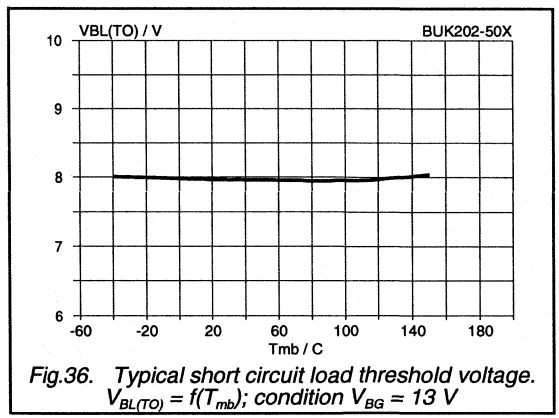


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

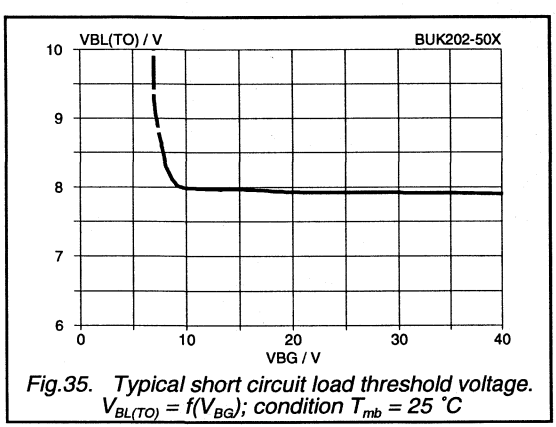


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

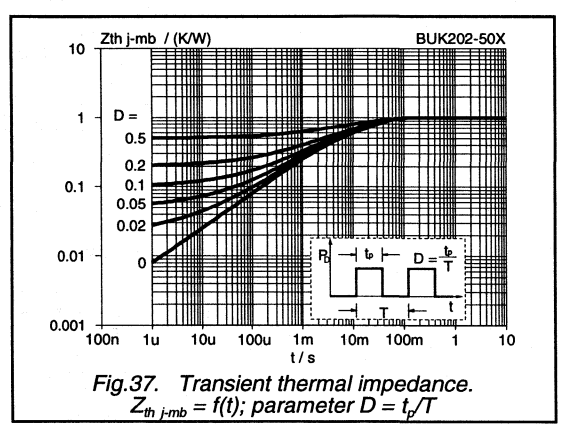
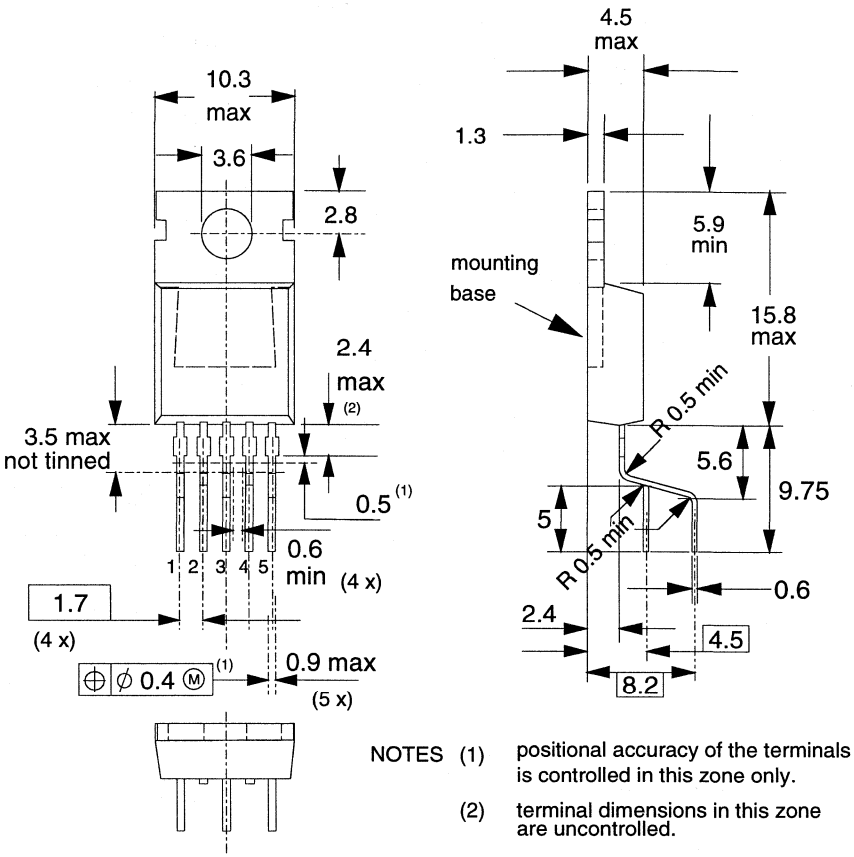


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g



NOTES (1) positional accuracy of the terminals is controlled in this zone only.

(2) terminal dimensions in this zone are uncontrolled.

Fig.38. SOT263 standard lead-form;

pin 3 connected to mounting base.

Note

1. Accessories supplied on request: refer to mounting instructions for TO220 envelopes.

PowerMOS transistor TOPFET high side switch

BUK202-50Y

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	9	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	20	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	38	mΩ

FUNCTIONAL BLOCK DIAGRAM

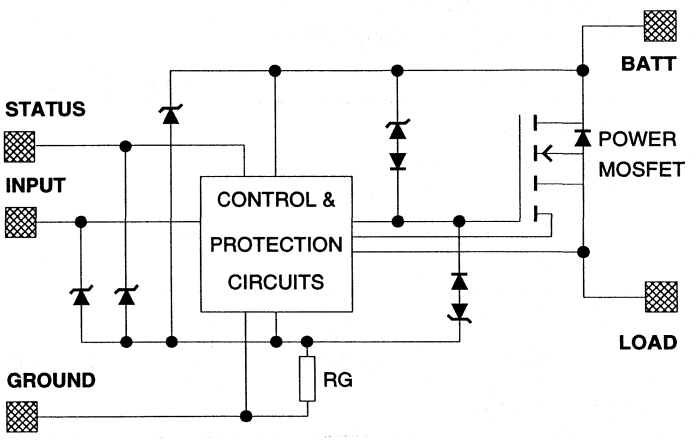


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT263

PIN	DESCRIPTION
1	Ground
2	Input
3	Battery (+ve supply)
4	Status
5	Load
tab	connected to pin 3

PIN CONFIGURATION

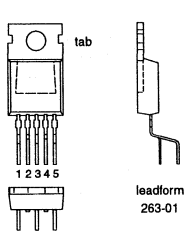


Fig. 2.

SYMBOL

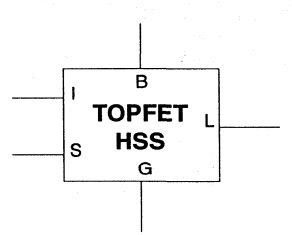


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 110$ °C	-	20	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150$ °C prior to turn-off	-	1.7	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	75	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	9	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 10 A; t_p = 300 µs	-	28	38	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 2 A; t_p = 300 µs	-	36	48	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the supply when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the supply with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	150	450	750	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[10]	1	0	0	6	8	10	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[14]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 230 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.5 V.

6 Overvoltage sensor causes the device to switch off. Typical hysteresis equals 1.3 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 10 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq$ 10 mΩ				
$t_{d\,sc}$	Response time		-	160	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	42	-	A
	Overload protection[3]	eg $R_L \approx$ 0.25 Ω				
$I_{L(lim)}$	Load current limiting	V_{BL} = 6 V; t_p = 1 ms	20	35	60	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	0.7	2	V/µs
t_{on}	Total switching time	to 90% V_L	-	140	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	40	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	0.7	2	V/µs
t_{off}	Total switching time	to 10% V_L	-	70	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	500	700	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

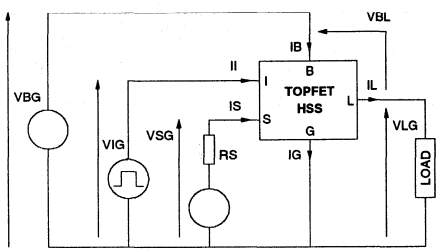


Fig.4. High side switch measurements schematic. (current and voltage conventions)

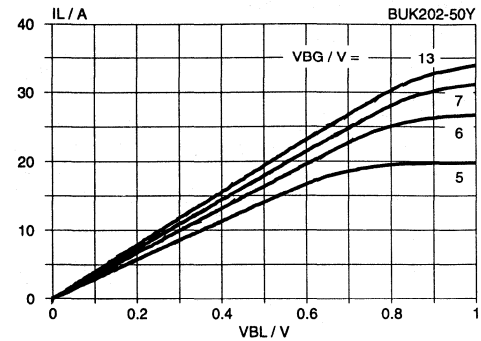


Fig.7. Typical on-state characteristics, T_j = 25 °C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

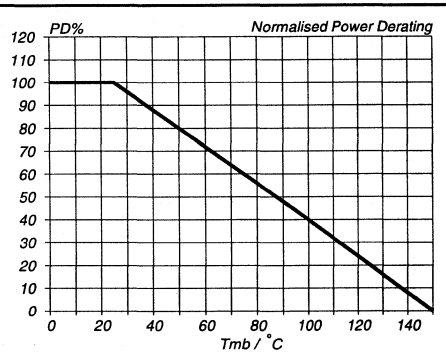


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ °C) = f(T_{mb})$

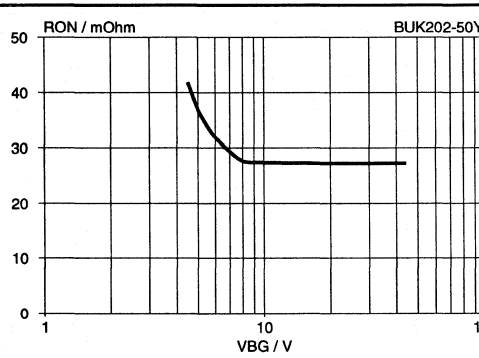


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{ON} = f(V_{BG})$; conditions: I_L = 10 A; t_p = 300 µs

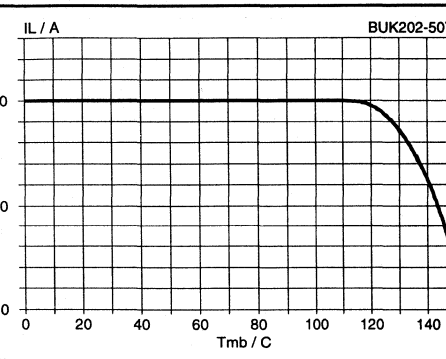


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

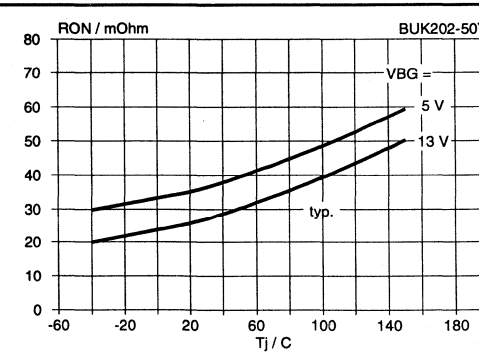


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 2 A

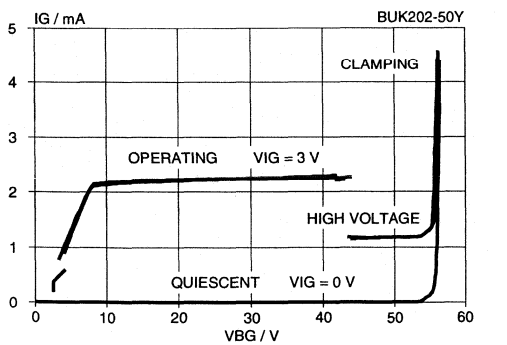


Fig.10. Typical supply characteristics, 25 °C. $I_G = f(V_{BG})$; parameter V_{IG}

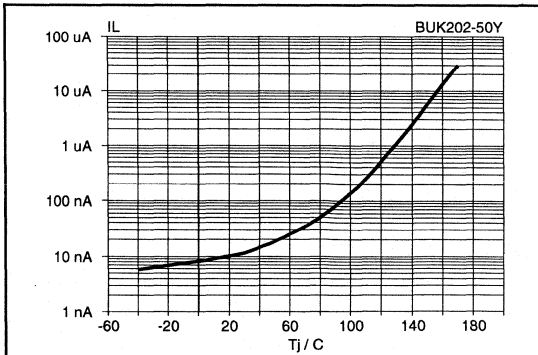


Fig.13. Typical off-state leakage current. $I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

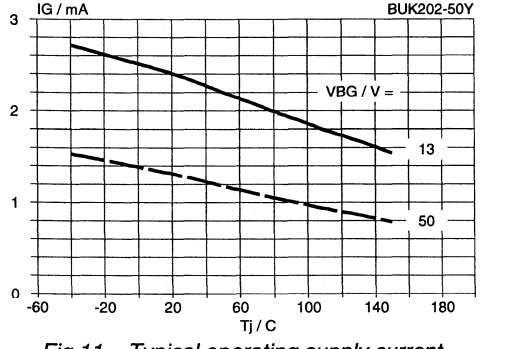


Fig.11. Typical operating supply current. $I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

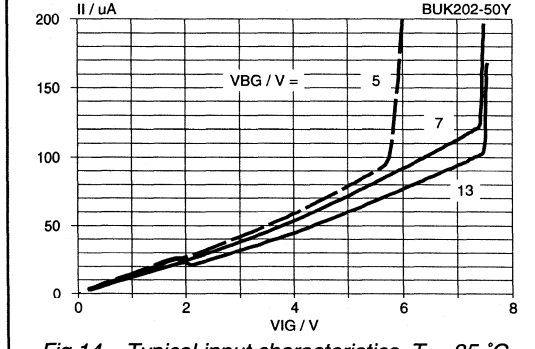


Fig.14. Typical input characteristics, T_j = 25 °C. $I_I = f(V_{IG})$; parameter V_{BG}

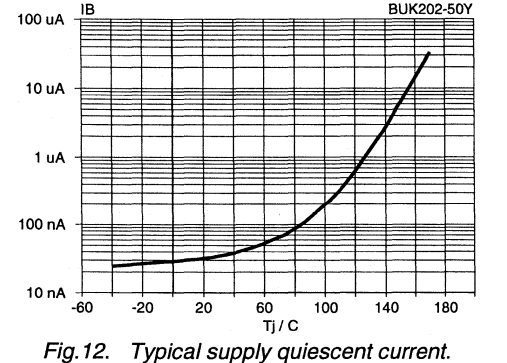


Fig.12. Typical supply quiescent current. $I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

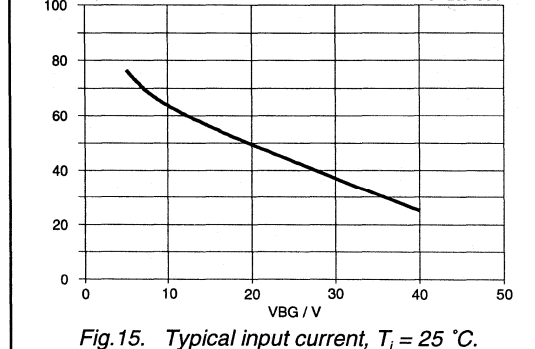


Fig.15. Typical input current, T_j = 25 °C. $I_I = f(V_{BG})$; condition V_{IG} = 5 V

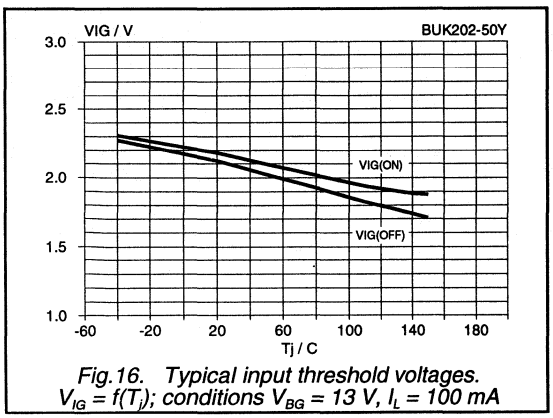


Fig.16. Typical input threshold voltages.
V_{IG} = f(T_j); conditions V_{BG} = 13 V, I_L = 100 mA

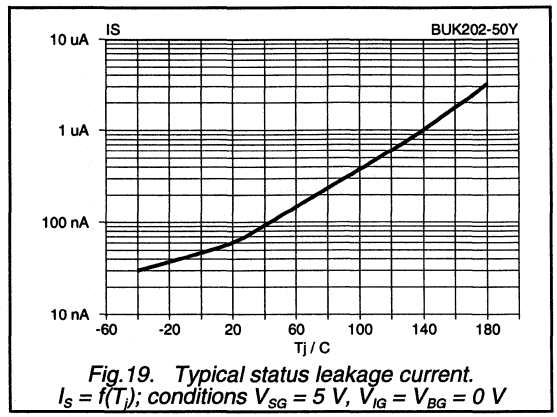


Fig.19. Typical status leakage current.
I_S = f(T_j); conditions V_{SG} = 5 V, V_{IG} = V_{BG} = 0 V

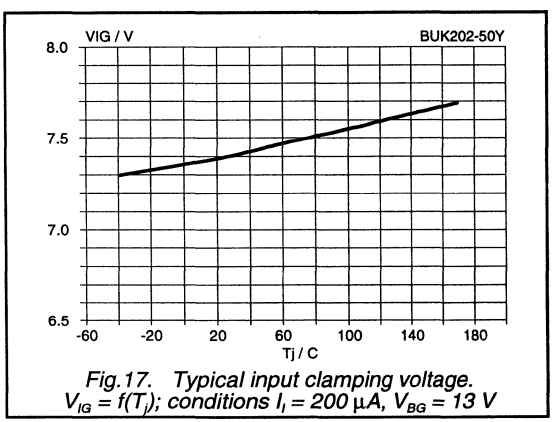


Fig.17. Typical input clamping voltage.
V_{IG} = f(T_j); conditions I_I = 200 µA, V_{BG} = 13 V

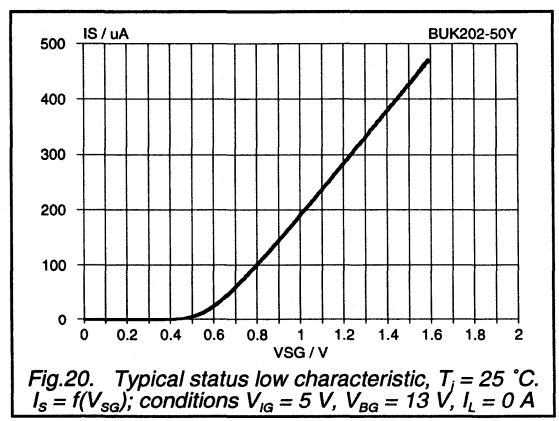


Fig.20. Typical status low characteristic, T_j = 25 °C.
I_S = f(V_{SG}); conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

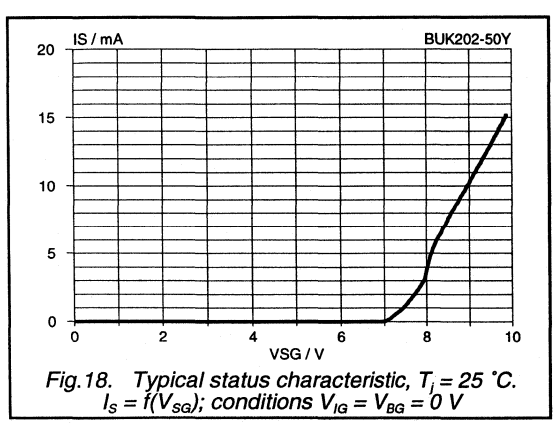


Fig.18. Typical status characteristic, T_j = 25 °C.
I_S = f(V_{SG}); conditions V_{IG} = V_{BG} = 0 V

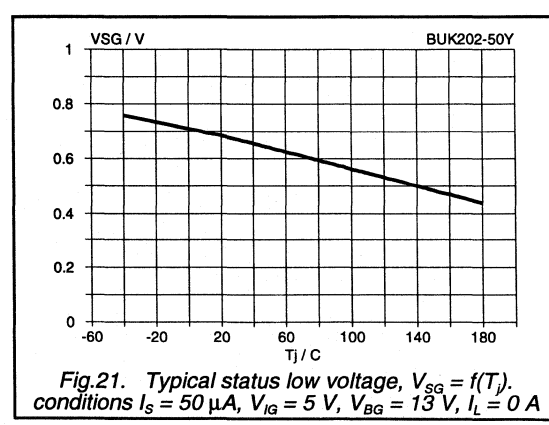


Fig.21. Typical status low voltage, V_{SG} = f(T_j).
conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

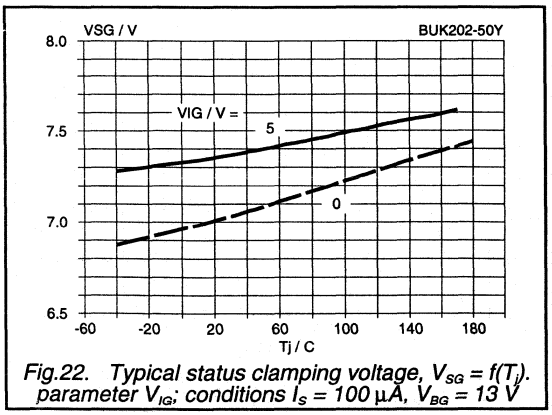


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions I_S = 100 µA, V_{BG} = 13 V

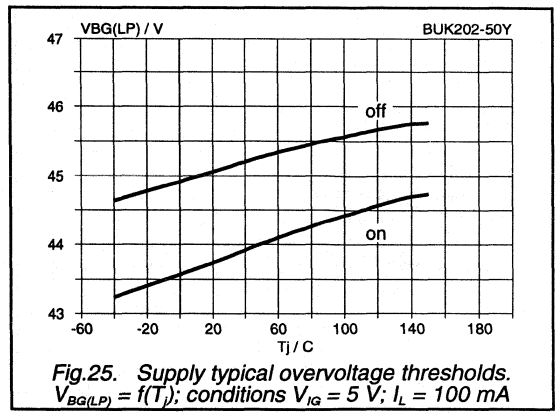


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions V_{IG} = 5 V; I_L = 100 mA

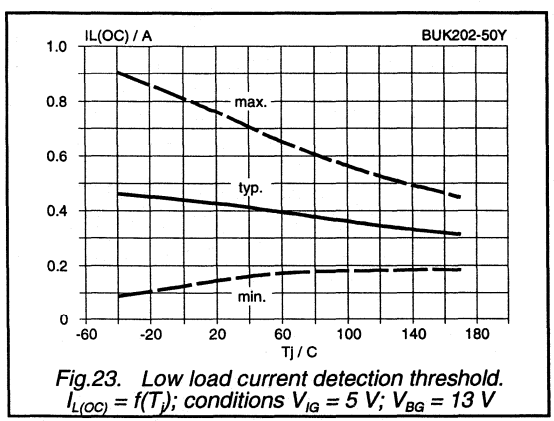


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions V_{IG} = 5 V; V_{BG} = 13 V

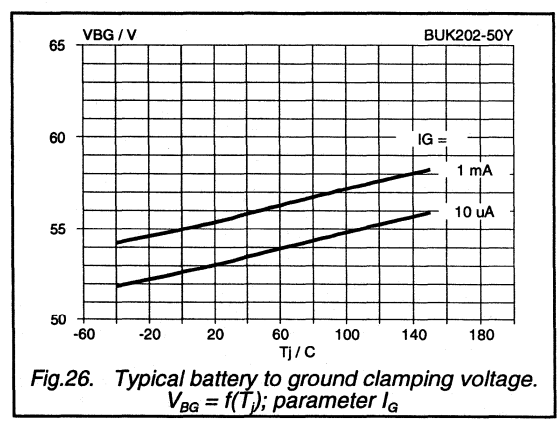


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

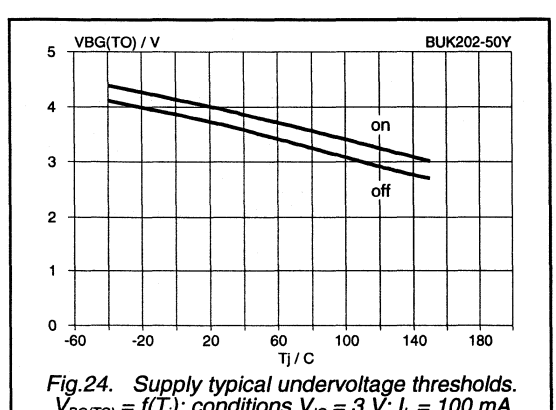


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions V_{IG} = 3 V; I_L = 100 mA

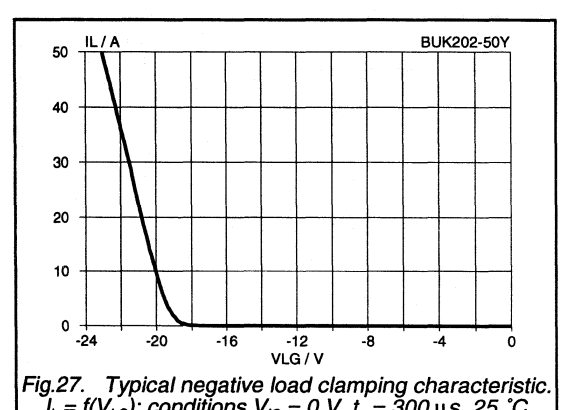


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions V_{IG} = 0 V, t_p = 300 µs, 25 °C

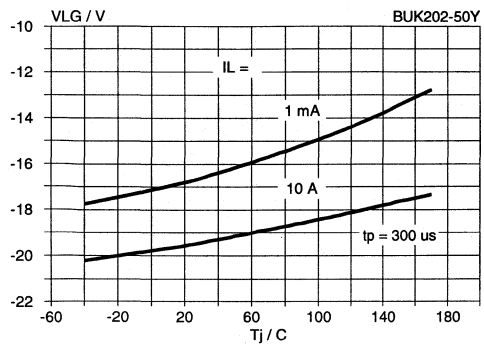


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

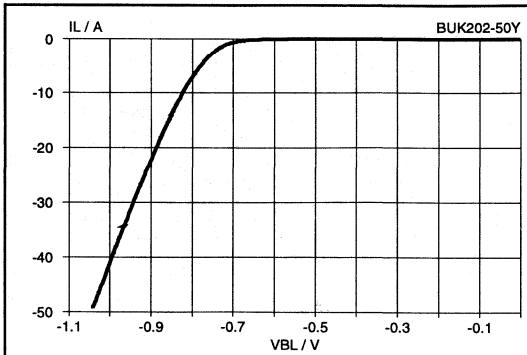


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

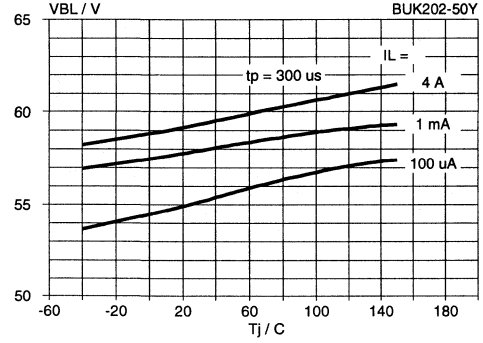


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

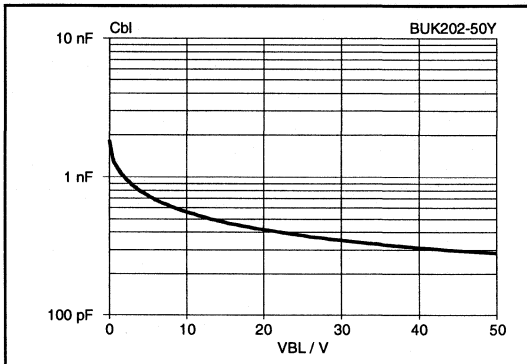


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions $f = 1$ MHz, $V_{IG} = 0$ V

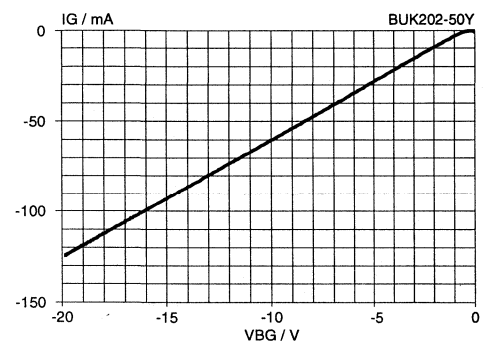


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

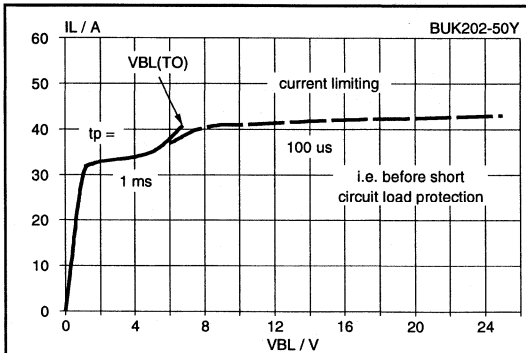


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

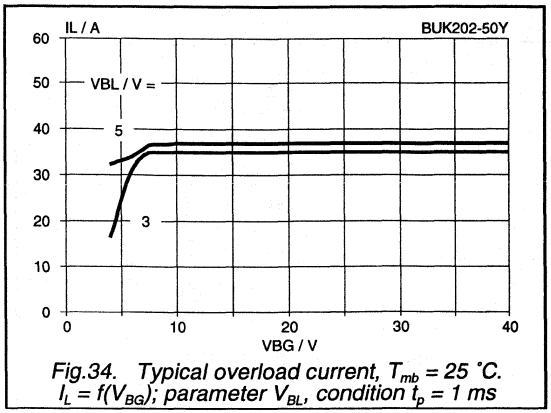


Fig.34. Typical overload current, T_{mb} = 25 ˚C. $I_L = f(V_{BG})$; parameter V_{BL}, condition t_p = 1 ms

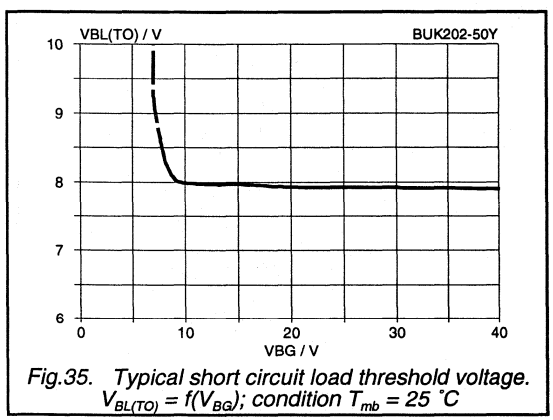


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 ˚C

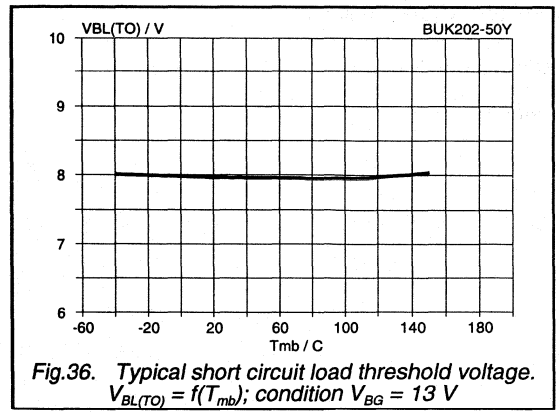


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

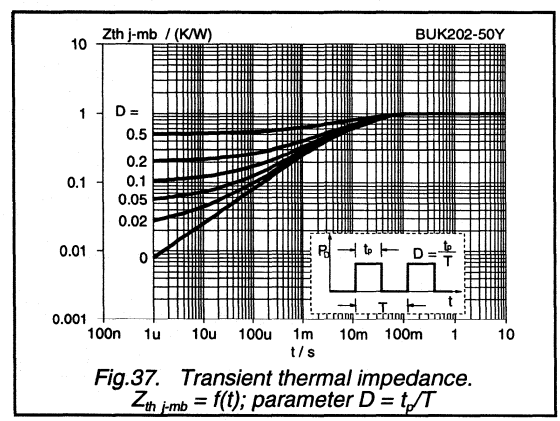
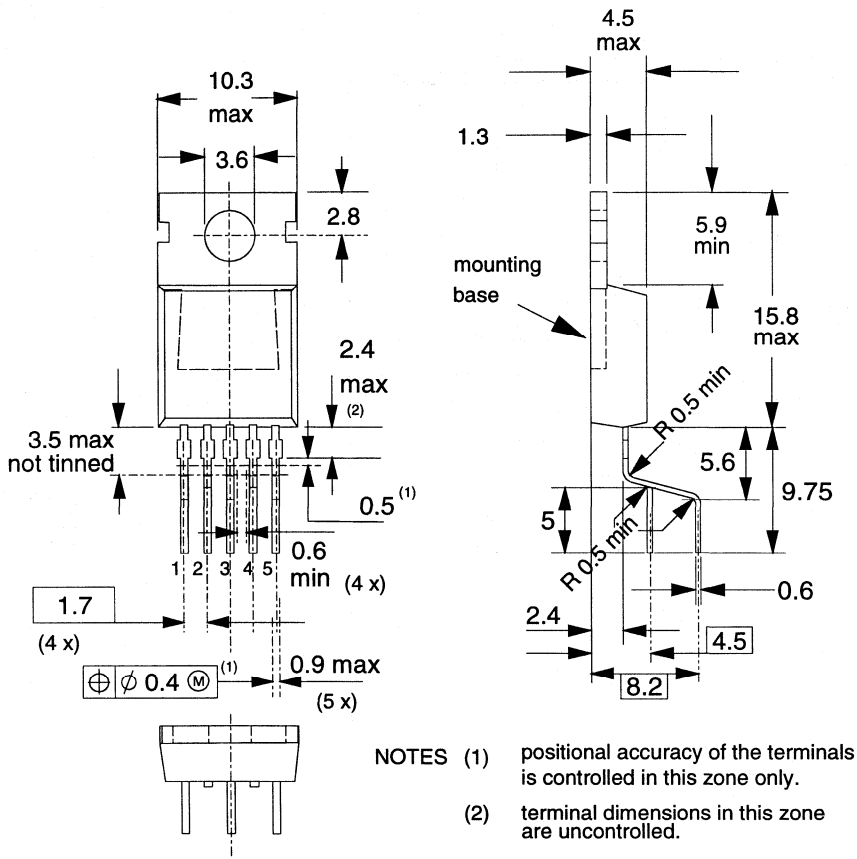


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g



NOTES (1) positional accuracy of the terminals is controlled in this zone only.

(2) terminal dimensions in this zone are uncontrolled.

Fig.38. SOT263 standard lead-form;

pin 3 connected to mounting base.

Note

1. Accessories supplied on request: refer to mounting instructions for TO220 envelopes.

PowerMOS transistor TOPFET high side switch

BUK203-50X

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	1.6	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	4	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	220	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input with hysteresis
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection with external ground resistor

FUNCTIONAL BLOCK DIAGRAM

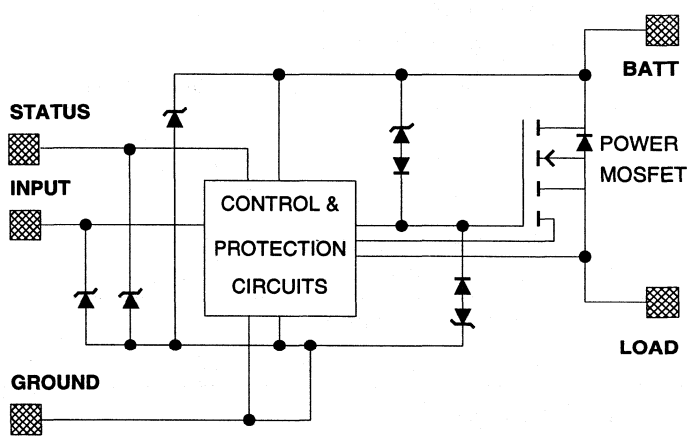


Fig.1. Elements of the TOPFET HSS.

PINNING - SOT263

PIN	DESCRIPTION
1	Ground
2	Input
3	Battery (+ve supply)
4	Status
5	Load
tab	connected to pin 3

PIN CONFIGURATION

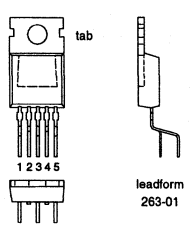


Fig. 2.

SYMBOL

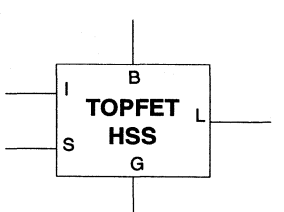


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 110$ °C	-	4	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	50	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	T_{mb} = 150 °C prior to turn-off	-	1.4	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2	2.5	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	75	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	1.6	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 2 A; t_p = 300 µs	-	160	220	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 0.5 A; t_p = 300 µs	-	225	320	mΩ

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7	8	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.4	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	1.7	-	V
ΔV_{IG}	Input turn-on hysteresis		-	0.4	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	30	90	150	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	6	8	10	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[11]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	9	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 25 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.5 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.1 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 2 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq 10$ mΩ				
$t_{d\,sc}$	Response time	V_{IG} = 5 V	-	160	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	11	-	A
	Overload protection[3]	eg $R_L \approx 1$ Ω				
$I_{L(lim)}$	Load current limiting	V_{BL} = 6 V; t_p = 1 ms	4	11	18	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1.3	3	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	20	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.6	3	V/µs
t_{off}	Total switching time	to 10% V_L	-	35	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	120	170	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

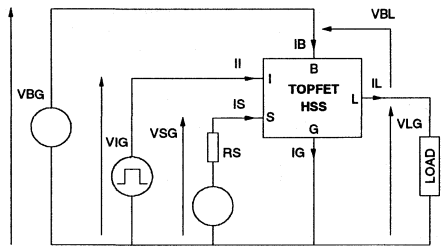


Fig.4. High side switch measurements schematic. (current and voltage conventions)

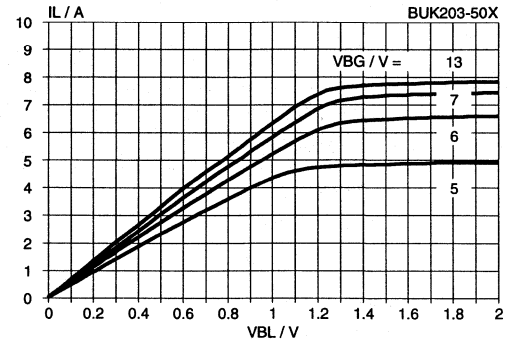


Fig.7. Typical on-state characteristics, T_j = 25 °C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

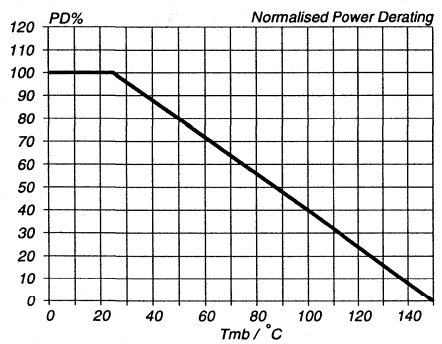


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ °C) = f(T_{mb})$

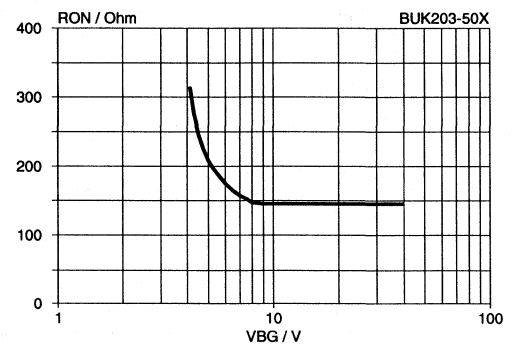


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{ON} = f(V_{BG})$; conditions: I_L = 2 A; t_p = 300 µs

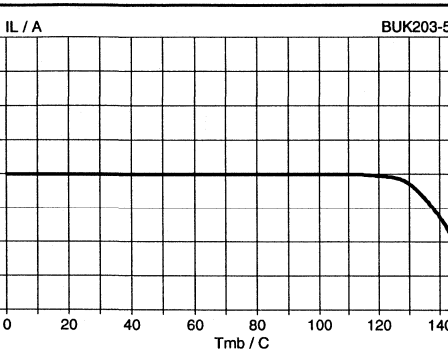


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

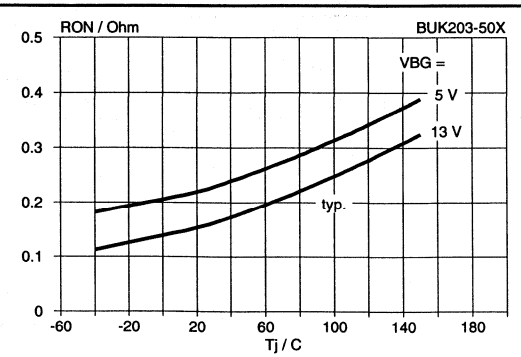


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 0.5 A

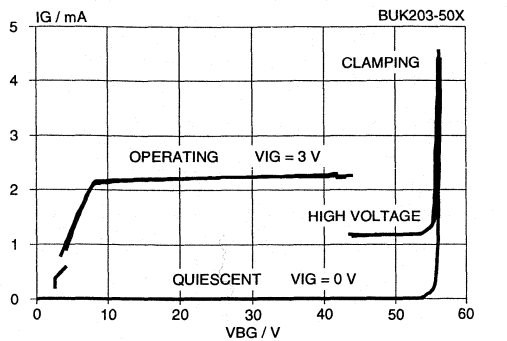


Fig.10. Typical supply characteristics, 25 °C.
$I_G = f(V_{BG})$; parameter V_{IG}

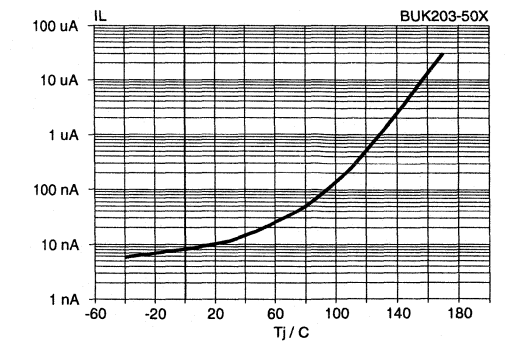


Fig.13. Typical off-state leakage current.
$I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

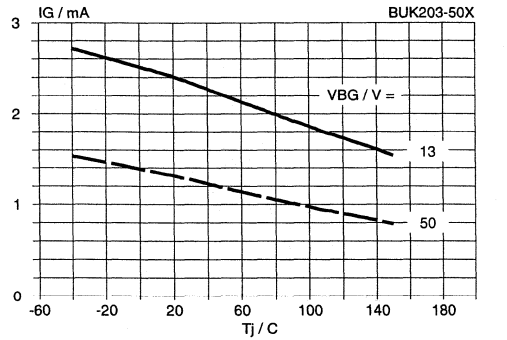


Fig.11. Typical operating supply current.
$I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

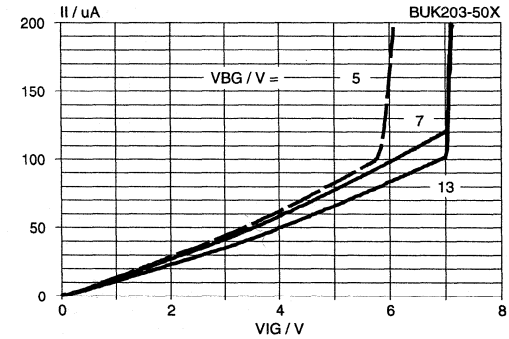


Fig.14. Typical input characteristics, T_j = 25 °C.
$I_I = f(V_{IG})$; parameter V_{BG}

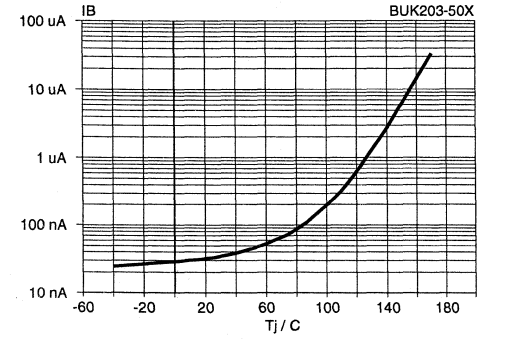


Fig.12. Typical supply quiescent current.
$I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

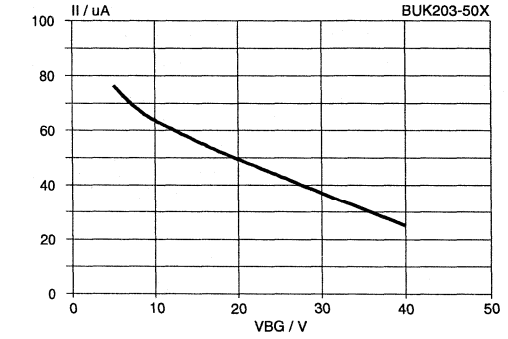


Fig.15. Typical input current, T_j = 25 °C.
$I_I = f(V_{BG})$; condition V_{IG} = 5 V

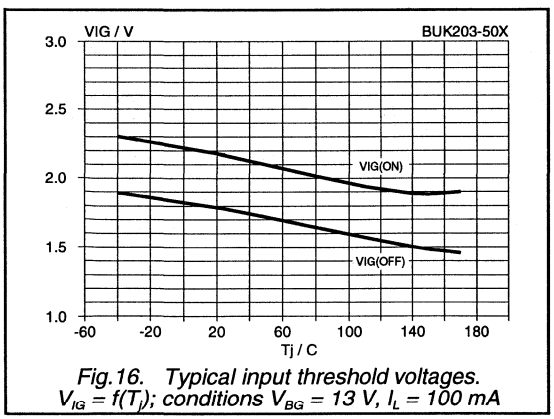


Fig.16. Typical input threshold voltages. $V_{IG} = f(T_j)$; conditions V_{BG} = 13 V, I_L = 100 mA

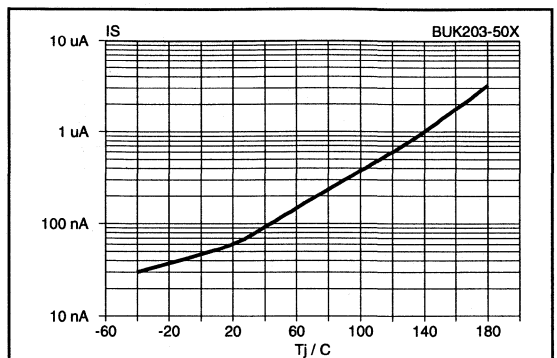


Fig.19. Typical status leakage current. $I_S = f(T_j)$; conditions V_{SG} = 5 V, $V_{IG} = V_{BG}$ = 0 V

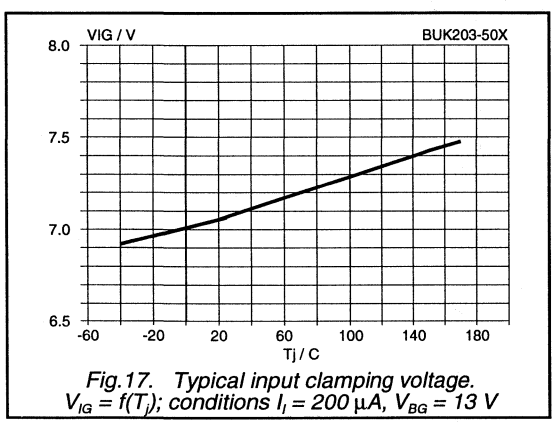


Fig.17. Typical input clamping voltage. $V_{IG} = f(T_j)$; conditions I_I = 200 µA, V_{BG} = 13 V

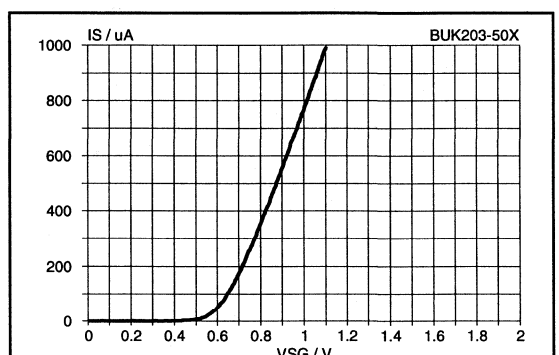


Fig.20. Typical status low characteristic, T_j = 25 °C. $I_S = f(V_{SG})$; conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

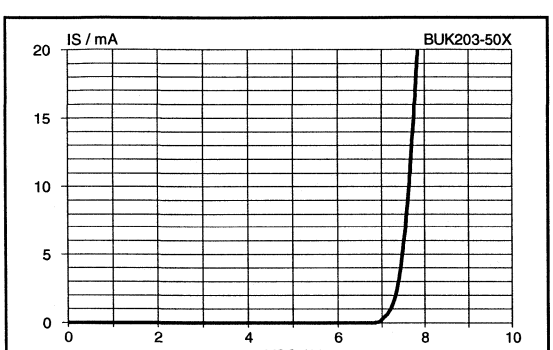


Fig.18. Typical status characteristic, T_j = 25 °C. $I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG}$ = 0 V

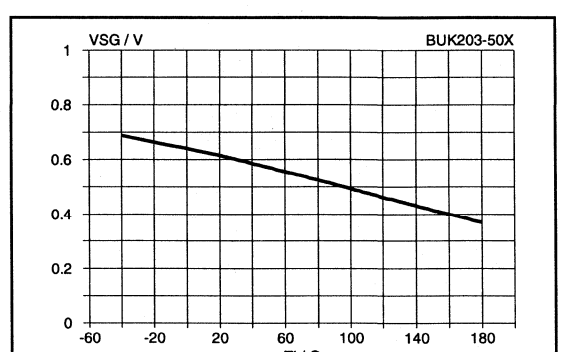


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$. conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

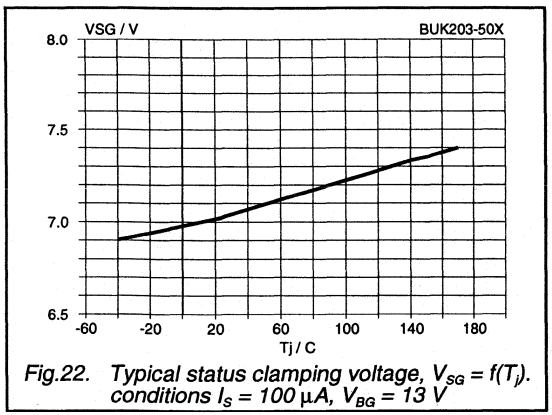


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

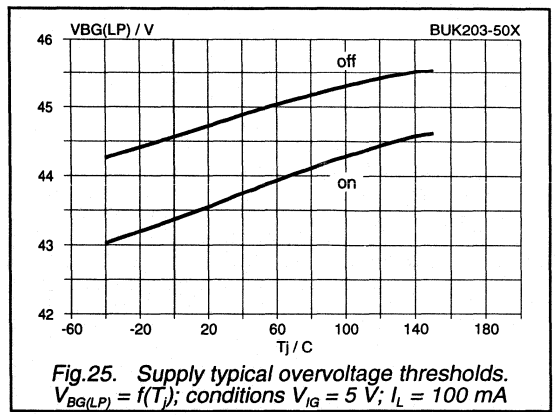


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 100\ mA$

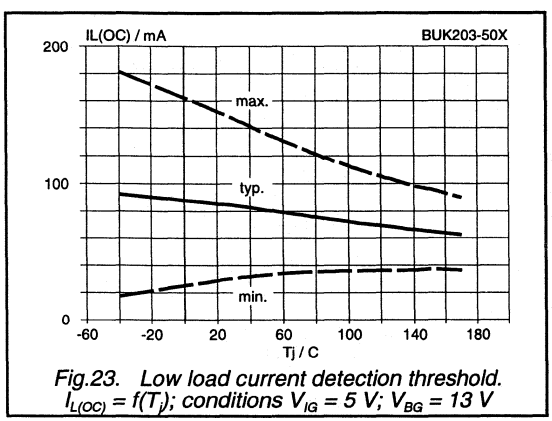


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

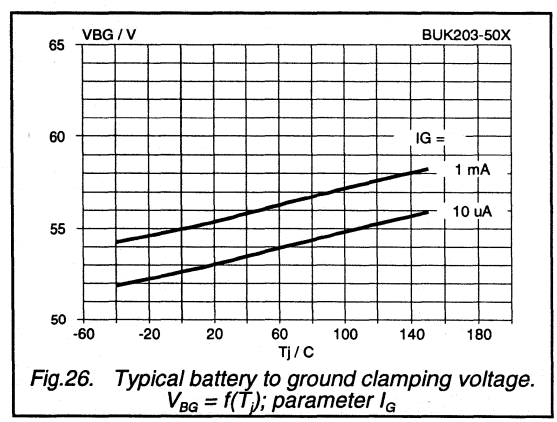


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

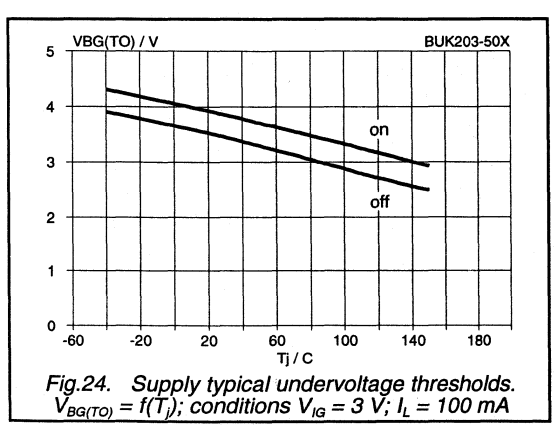


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 100\ mA$

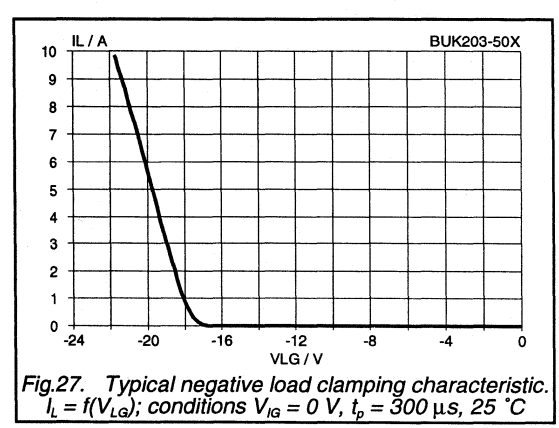


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

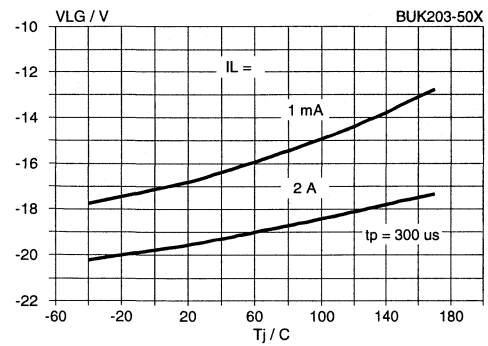


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

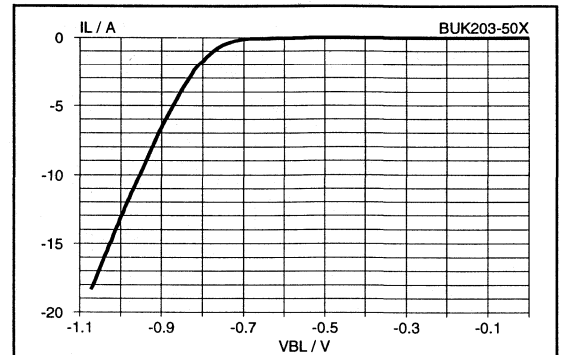


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

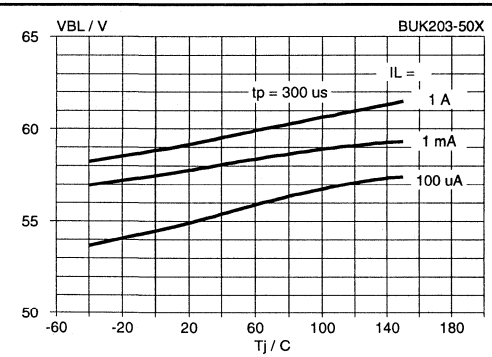


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

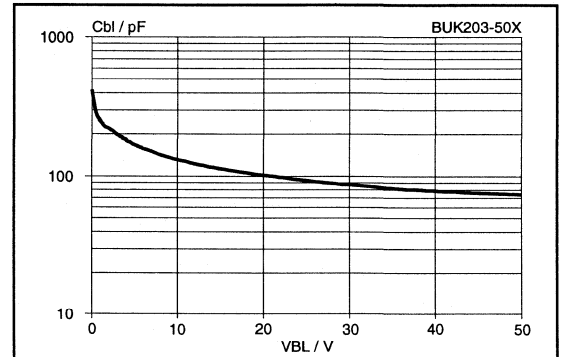


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions $f = 1$ MHz, $V_{IG} = 0$ V

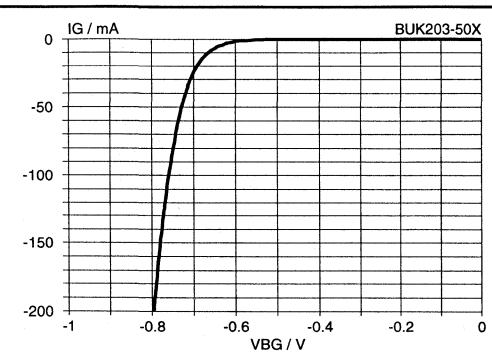


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

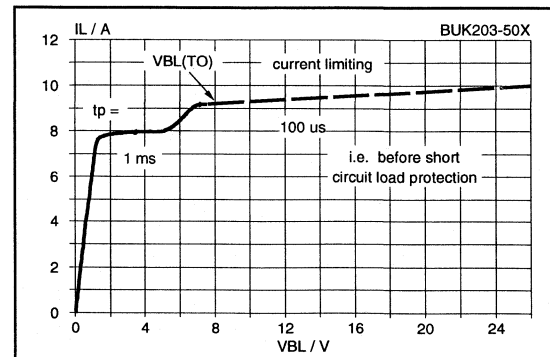


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

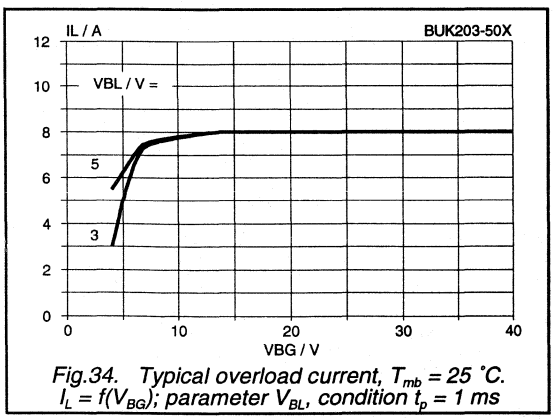


Fig.34. Typical overload current, T_{mb} = 25 °C. $I_L = f(V_{BG})$; parameter V_{BL}, condition t_p = 1 ms

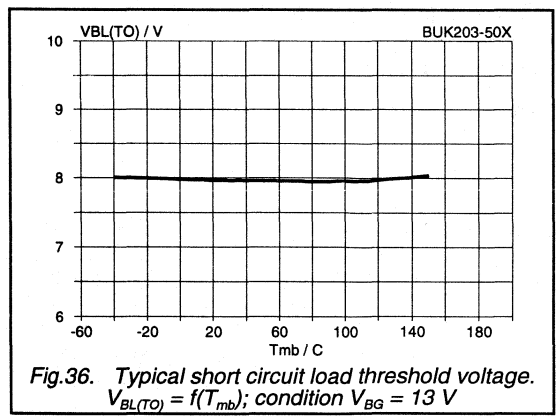


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

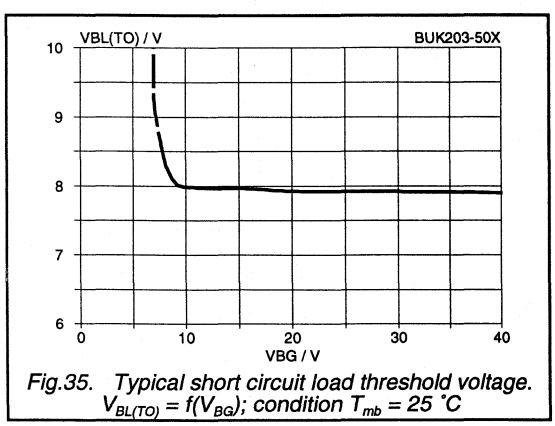


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

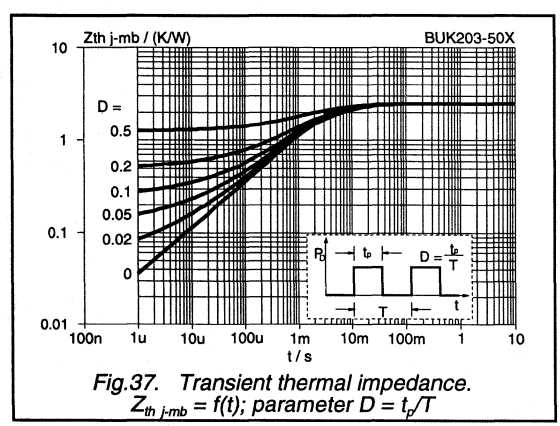
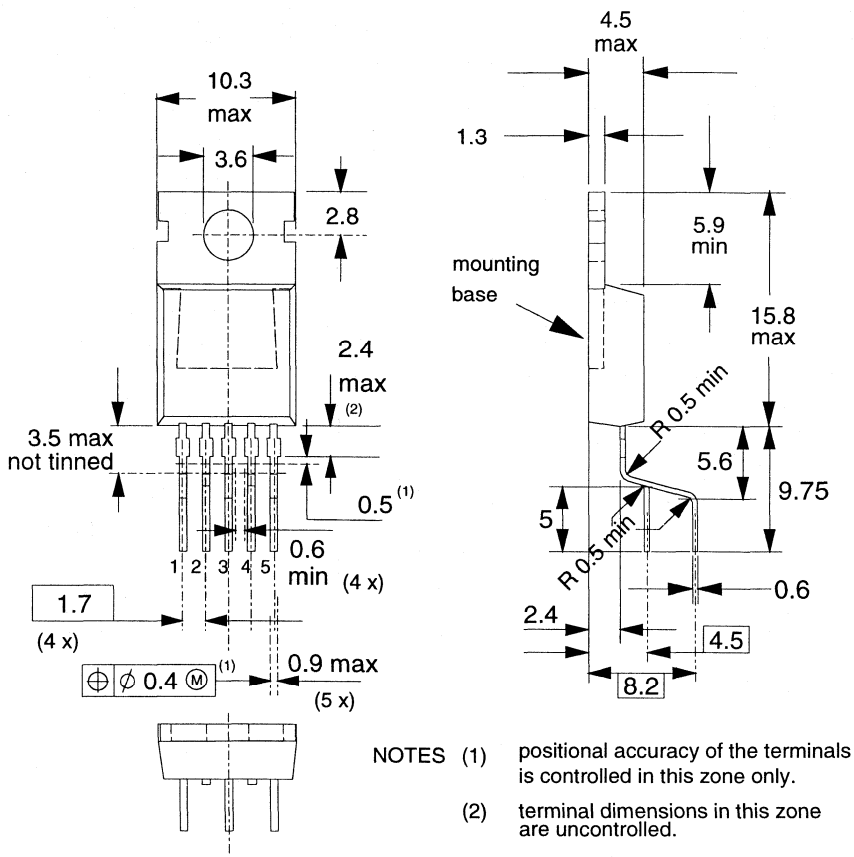


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g



NOTES (1) positional accuracy of the terminals is controlled in this zone only.

(2) terminal dimensions in this zone are uncontrolled.

Fig.38. SOT263 standard lead-form;

pin 3 connected to mounting base.

Note

1. Accessories supplied on request: refer to mounting instructions for TO220 envelopes.

PowerMOS transistor TOPFET high side switch

BUK203-50Y

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	1.6	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	4	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	220	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

FUNCTIONAL BLOCK DIAGRAM

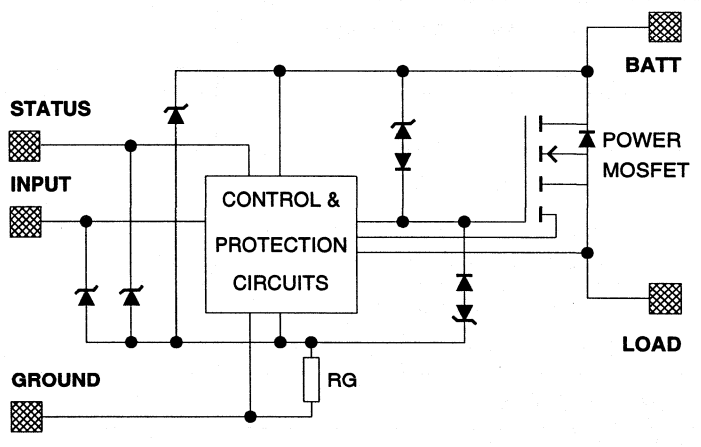


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT263

PIN	DESCRIPTION
1	Ground
2	Input
3	Battery (+ve supply)
4	Status
5	Load
tab	connected to pin 3

PIN CONFIGURATION

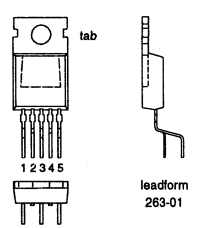


Fig. 2.

SYMBOL

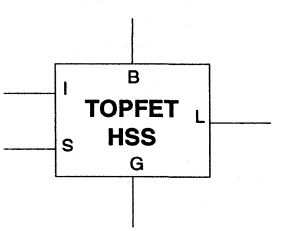


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 110$ °C	-	4	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	50	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150$ °C prior to turn-off	-	1.4	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2	2.5	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	75	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	1.6	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[9]	V_{BG} = 13 V; I_L = 2 A; t_p = 300 µs	-	160	220	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 0.5 A; t_p = 300 µs	-	225	320	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	30	90	150	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	6	8	10	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 25 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.7 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.3 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 2 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq 10$ mΩ				
$t_{d\,sc}$	Response time		-	160	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	11	-	A
	Overload protection[3]	eg $R_L \approx 1$ Ω				
$I_{L(lim)}$	Load current limiting	V_{BL} = 6 V; t_p = 1 ms	4	11	18	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1.3	3	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	20	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.6	3	V/µs
t_{off}	Total switching time	to 10% V_L	-	35	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	120	170	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

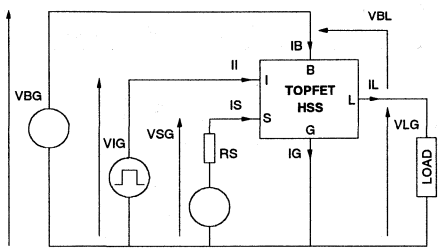


Fig.4. High side switch measurements schematic. (current and voltage conventions)

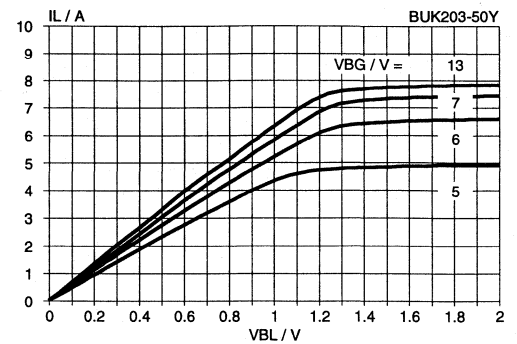


Fig.7. Typical on-state characteristics, T_j = 25 ˚C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

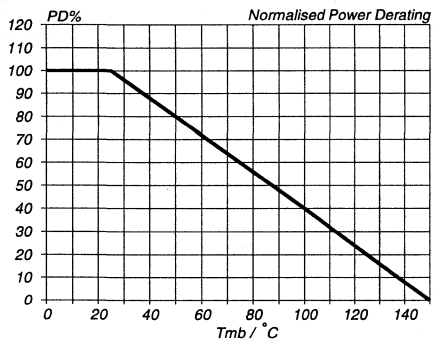


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

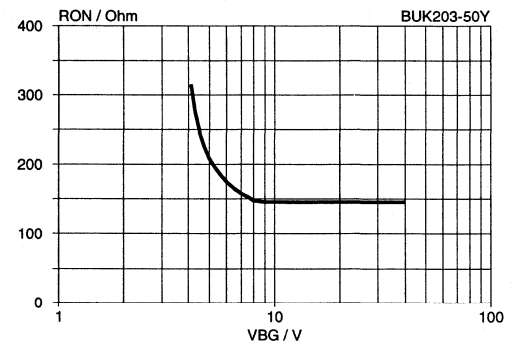


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{ON} = f(V_{BG})$; conditions: I_L = 2 A; t_p = 300 µs

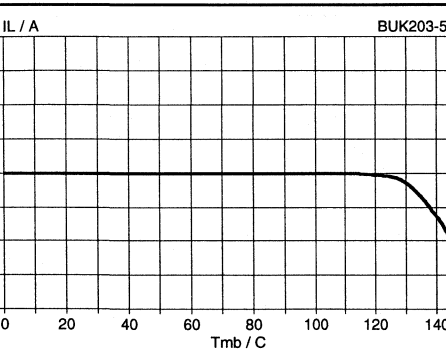


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

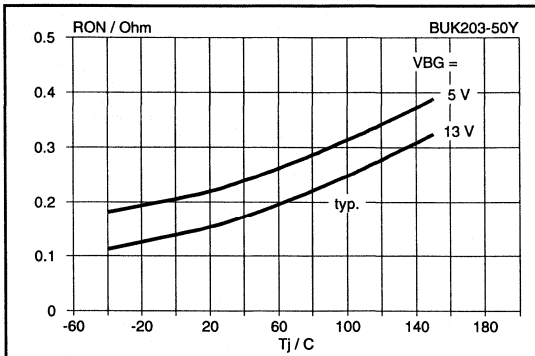


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 0.5 A

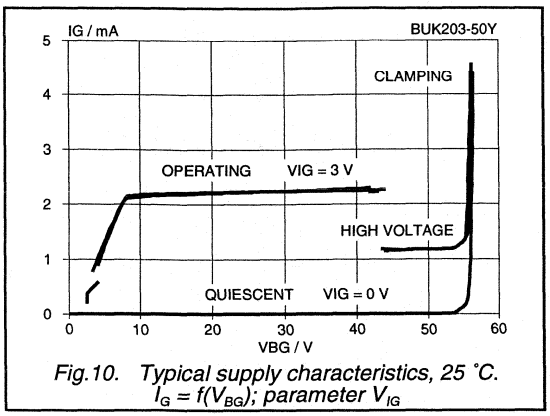


Fig.10. Typical supply characteristics, 25 °C. $I_G = f(V_{BG})$; parameter V_{IG}

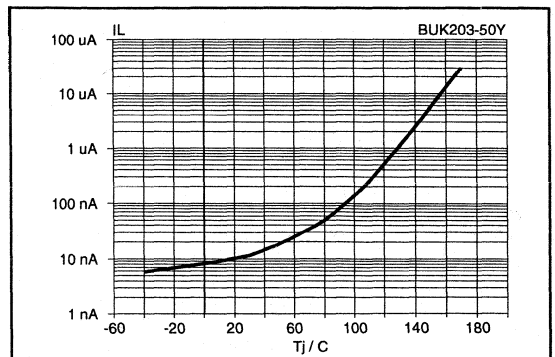


Fig.13. Typical off-state leakage current. $I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

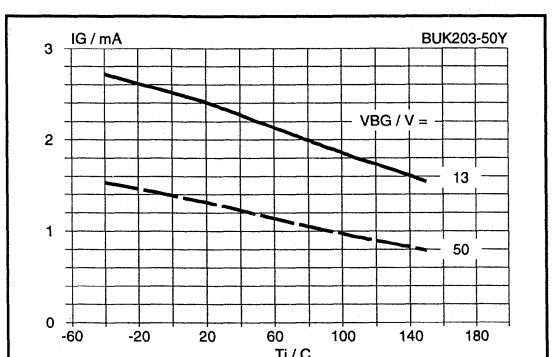


Fig.11. Typical operating supply current. $I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

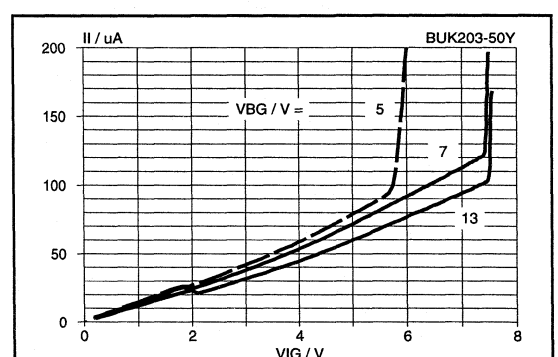


Fig.14. Typical input characteristics, T_j = 25 °C. $I_I = f(V_{IG})$; parameter V_{BG}

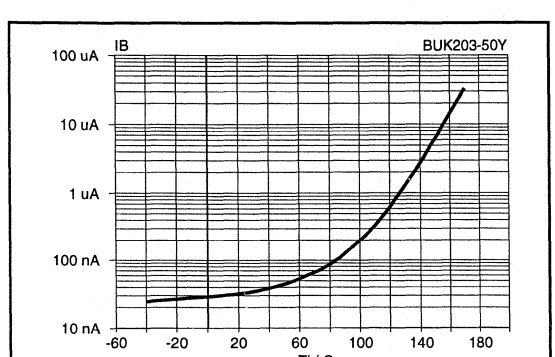


Fig.12. Typical supply quiescent current. $I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

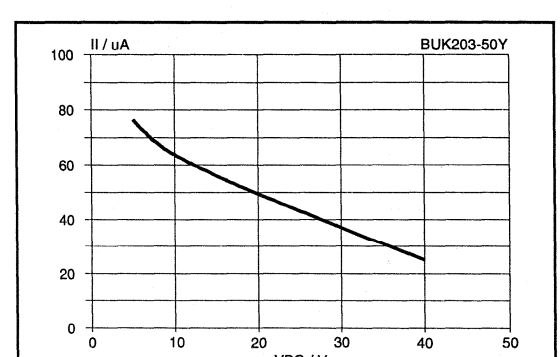


Fig.15. Typical input current, T_j = 25 °C. $I_I = f(V_{BG})$; condition V_{IG} = 5 V

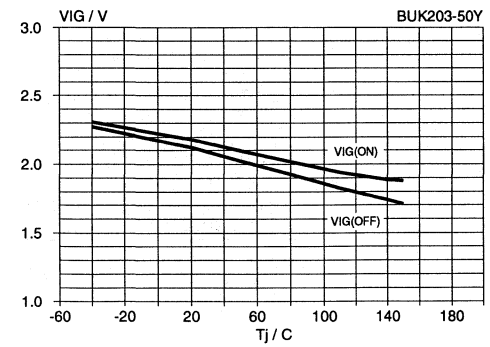


Fig.16. Typical input threshold voltages.
$V_{IG} = f(T_j)$; conditions V_{BG} = 13 V, I_L = 100 mA

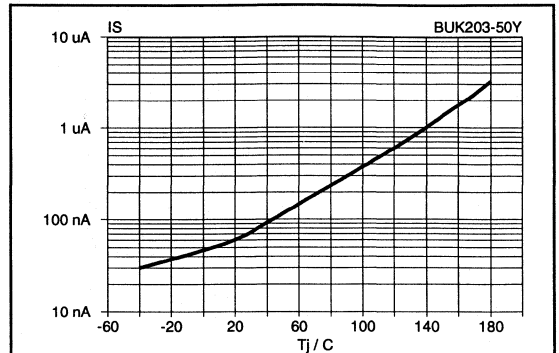


Fig.19. Typical status leakage current.
$I_S = f(T_j)$; conditions V_{SG} = 5 V, $V_{IG} = V_{BG}$ = 0 V

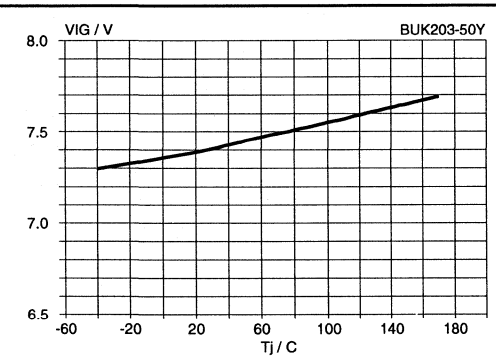


Fig.17. Typical input clamping voltage.
$V_{IG} = f(T_j)$; conditions I_I = 200 µA, V_{BG} = 13 V

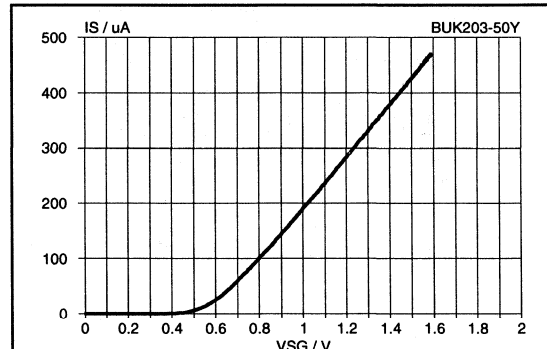


Fig.20. Typical status low characteristic, T_j = 25 °C.
$I_S = f(V_{SG})$; conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

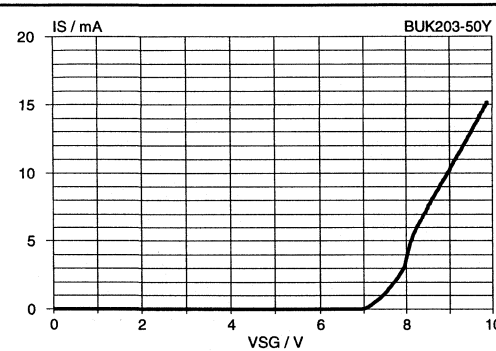


Fig.18. Typical status characteristic, T_j = 25 °C.
$I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG}$ = 0 V

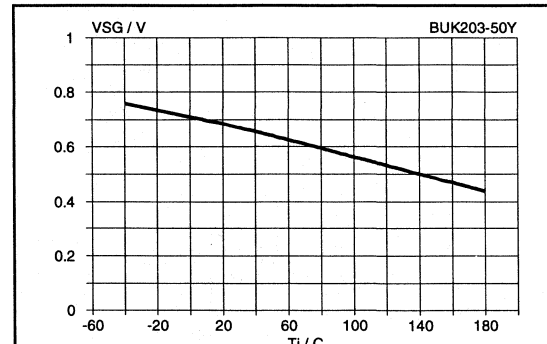


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$.
conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

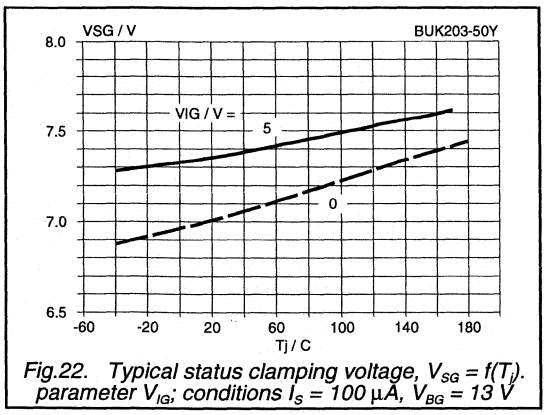


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

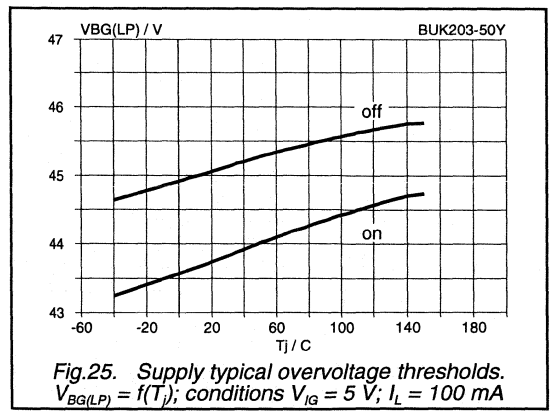


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 100\ mA$

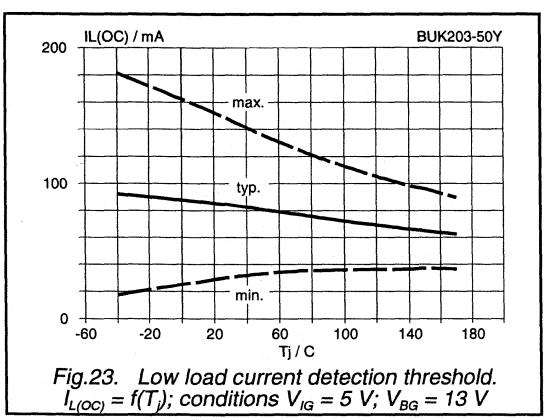


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

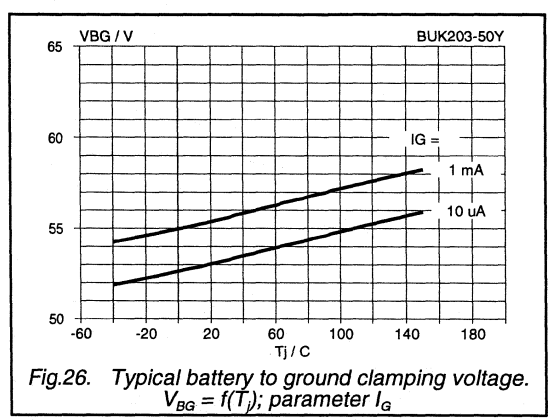


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

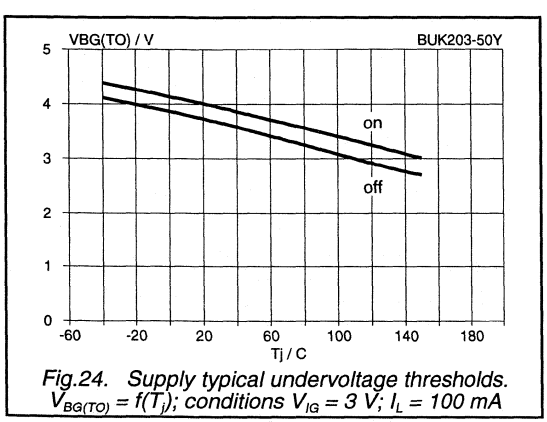


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 100\ mA$

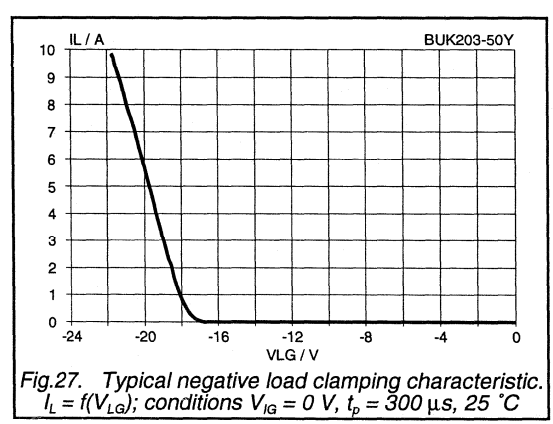


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

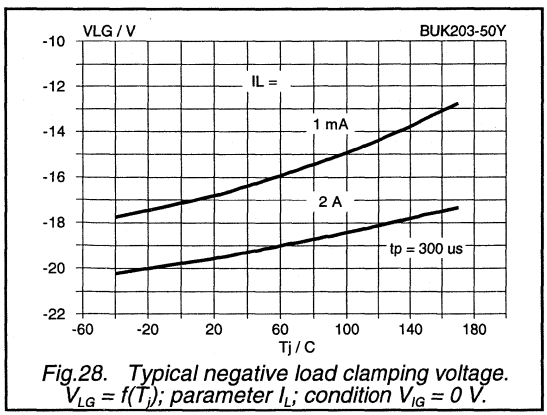


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

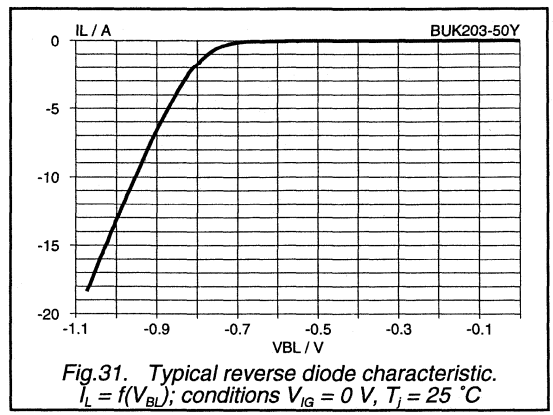


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

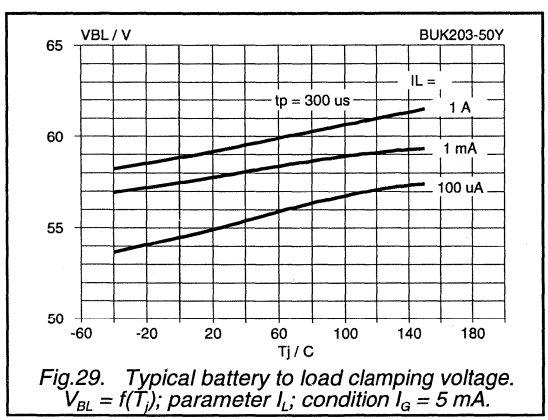


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

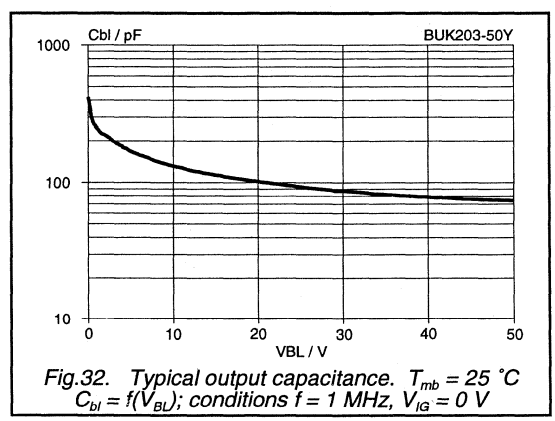


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions f = 1 MHz, $V_{IG} = 0$ V

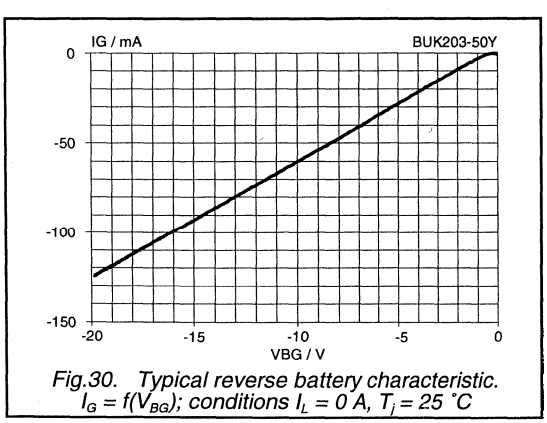


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

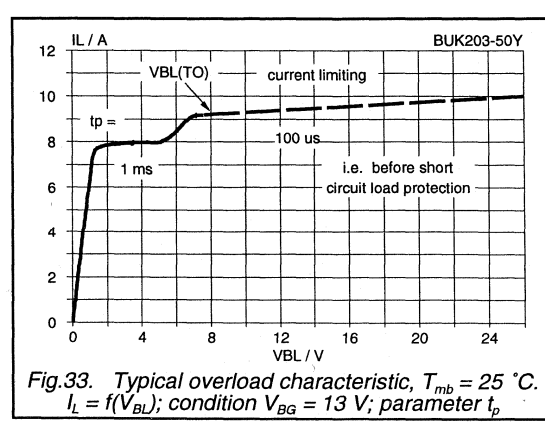


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

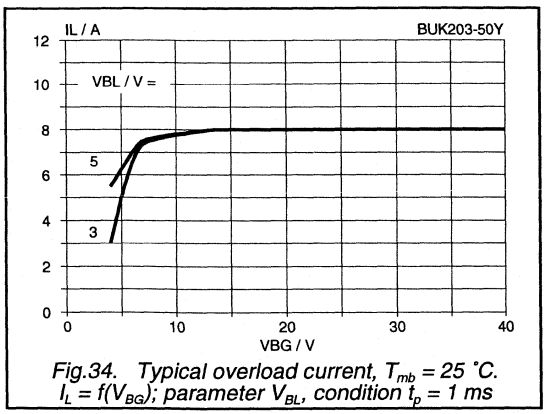


Fig.34. Typical overload current, T_{mb} = 25 ˚C. $I_L = f(V_{BG})$; parameter V_{BL}, condition t_p = 1 ms

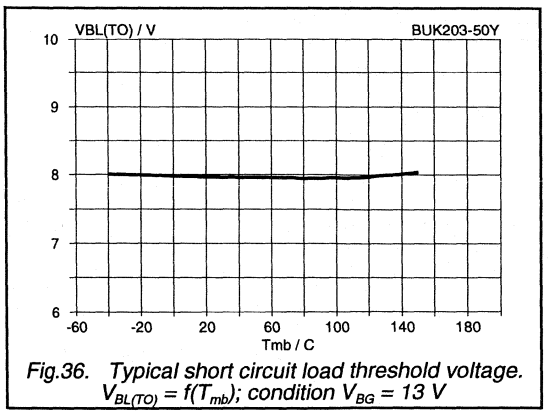


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

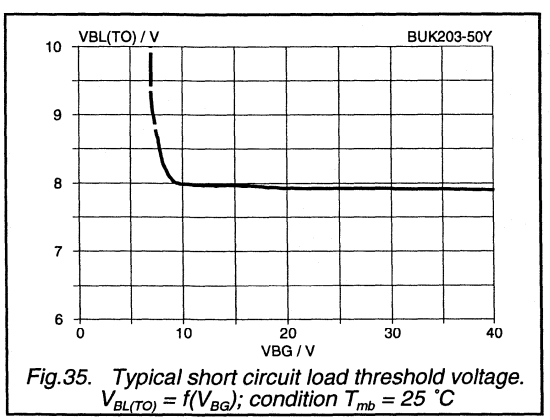


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 ˚C

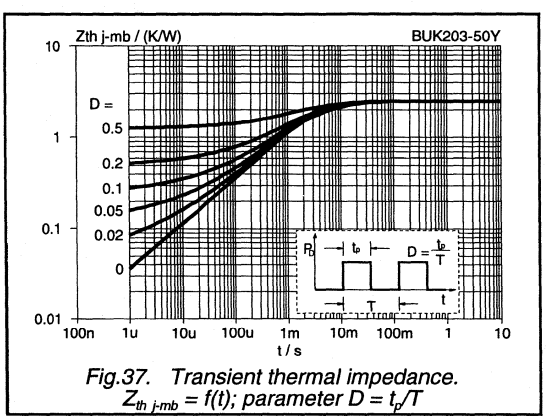
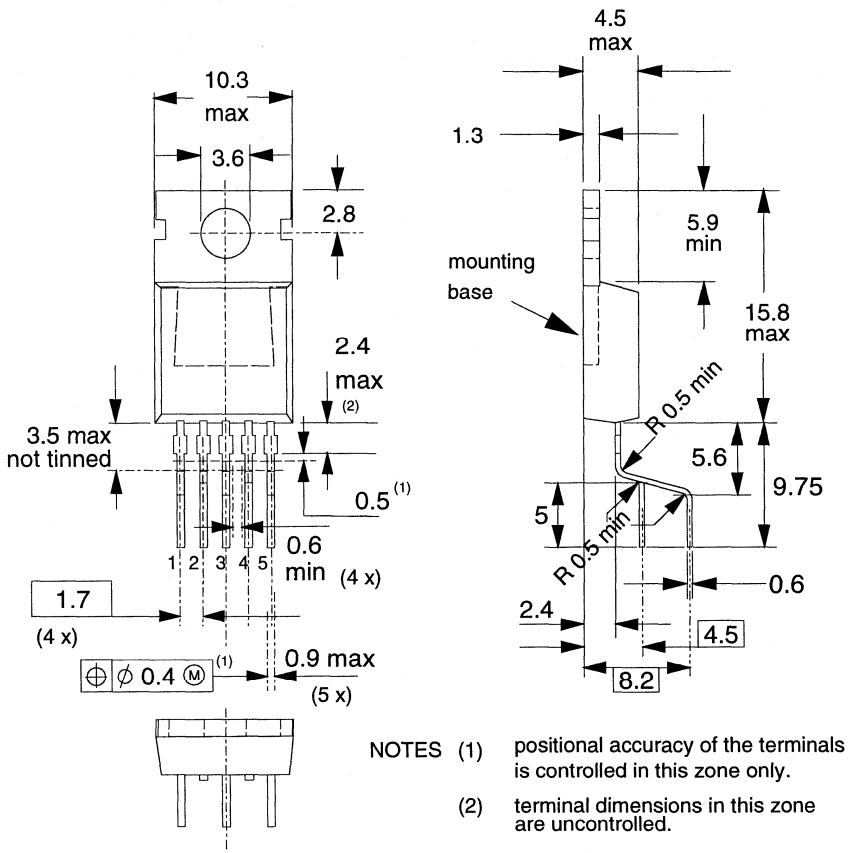


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g



NOTES (1) positional accuracy of the terminals is controlled in this zone only.

(2) terminal dimensions in this zone are uncontrolled.

Fig.38. SOT263 standard lead-form;

pin 3 connected to mounting base.

Note

1. Accessories supplied on request: refer to mounting instructions for TO220 envelopes.

An introduction to electronic automotive ignition

Application report

The function of an automotive ignition circuit is to provide a spark of sufficient energy to ignite the compressed air-fuel mixture at the appropriate time. Increasingly, electronics is being used to optimise the ignition event. This is now necessary to ensure conformance with emission regulations and to achieve maximum engine performance, fuel economy and engine efficiency. This section will look at some important aspects of the power stage of an electronic ignition system. Other sections in this chapter will look more closely at the power devices for this application.

Electronic ignition circuit

There are several different configurations for electronic ignition. Some are still being studied and there are several already in use. But by far the most common configuration for the power stage is that shown in Fig. 1. With this arrangement there is no distributor. The circuit shown is for a four cylinder engine and has two separate power circuits each feeding two cylinders. Extra power stages can be added for 6 and 8 cylinder engines. When one power stage fires, both plugs will spark but, by choosing pairs of cylinders which are 360° out of phase in the 4-stroke cycle, only one will have a mixture that can be ignited - the other will be approaching tdc at the end of the exhaust stroke.

Operation

During normal operation the transistor will be turned on some time before the spark is needed (t1 in Fig. 2). Current will now rise at a rate given by the equation

$$rate\,of\,rise = \frac{di}{dt} = \frac{V}{L} \qquad (1)$$

where V is the voltage across the primary of the coil. When the spark is needed (t3), the transistor is turned off. The current in the inductance will try to stop flowing but it can only change at the rate given by (1). This means that voltage on the primary is forced to become large and negative. Transformer action increases the secondary voltage until it reaches the voltage needed to create a spark at the plugs - minimum 5 kV but may be 10 to 30 kV. Current now flows through the spark and the secondary winding, the voltage now falls back to that necessary to maintain the current in the spark, t5. When all the coil energy has been delivered, t6, the voltage at the collector falls to the battery voltage.

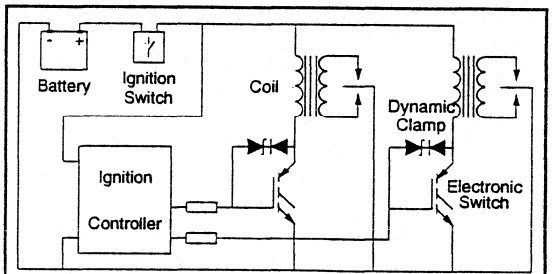


Fig. 1 Typical automotive ignition circuit

Spark energy

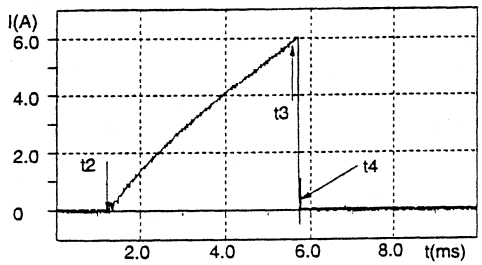
Under ideal conditions the mixture can be ignited with a spark energy of 0.3 mJ but, for reliable ignition under all possible engine conditions, spark energies in the range 60mJ to 150mJ are needed. The energy comes from the coil and is the energy stored as flux generated by the current that was allowed to build up in the primary. The energy stored in the magnetic field of the coil is:

$$E_{prim} = \frac{1}{2} L_{prim} i^2 \qquad (2)$$

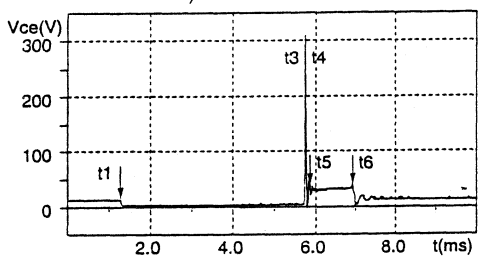
Timing

The timing of the spark is one of the most critical factors in achieving optimum engine performance. The controller uses information about engine speed, temperature, fuel etc. to decide how far before tdc the spark is needed. It then uses data from crankshaft position sensors to decide when to signal for a spark.

One factor which the controller cannot control is the delay between it issuing the command to spark and the spark being generated. Part of this delay is the time it takes the transistor to start turning off together with the rate at which the transistor voltage rises. The controller can make allowance for this delay but in many systems this is no more than a fixed offset. In practice the delay will vary with variations in the drive circuit, temperature and between devices - with some transistor types being more susceptible to variation than others.



a) Coil current



b) Transistor collector voltage

Fig. 2 Ignition circuit waveforms

Dwell

As mentioned earlier, proper ignition means there must be enough energy stored in the coil when the spark is needed, so the transistor must be turned on soon enough to allow time for the current to reach the required level. However, turning on too soon will mean that the current is higher than it needs to be. Although proper spark timing and energy is more important, optimum coil current is also significant. Higher currents create higher loss which reduces efficiency and increases the problems of thermal management. They can also reduce the life and reliability of the coil and create major difficulties when designing for survival under fault conditions like open circuit secondary.

The time to turn on the transistor is governed by (1). Coil inductance is an attribute of the coil but the primary voltage depends on battery voltage and the voltage drop across the transistor. Battery voltage can vary widely and can be very low particularly during engine cranking. Ensuring that the circuit operates reasonably well at these low voltages means keeping the transistor voltage drop as low as possible.

Fault conditions

Automotive systems must be reliable. Achieving high reliability means designing systems that can survive all the operating environments that the automobile can produce. Some of the harshest conditions are the fault conditions.

Open circuit secondary

Disconnection of a spark plug lead means that the stored coil energy cannot be dissipated in the spark. Unless steps are taken to prevent it, the voltage will be forced higher until it reaches the breakdown voltage of the transistor. The combination of high current and voltage would probably destroy the device. The solution to this problem is to operate the transistor in dynamic clamping. This can be achieved either by connecting a network between collector and the gate/base or by using a device with the network already integrated into it. With this arrangement the voltage rises to the clamping voltage, the transistor then turns on partially, with enough drive to allow the coil current to flow at a collector emitter voltage equal to the clamping voltage. The clamping voltage is set higher than the voltage normally needed to generate the spark.

Reverse Battery

Another condition which must be survived is when the battery connections are reversed. Ideally no current should flow and this can be achieved with some transistors which have a reverse blocking voltage greater than the battery voltage. With many transistors, however, reverse blocking is not guaranteed and to block the current means adding a diode in series. This is rarely acceptable because the diode forward voltage drop adds too much to the effective voltage drop. The alternatives are to allow the current to flow either by using a transistor which is rated to operate with reverse current or by fitting a diode in anti-parallel with the transistor.

IGBTs for automotive ignition — Application report

This publication describes a range of power transistors for automotive ignition applications from Philips Semiconductors. This range of IGBTs has been specifically optimised for the demanding conditions of ignition circuits. The IGBT is a voltage controlled, low loss, high power transistor which gives the ease of drive and low conduction losses that are required in automotive ignition circuits. The Philips range of ignition IGBTs includes conventional IGBT devices with standard gate drive input. It also includes a range of standard and logic level input protected IGBTs with integral gate drain and gate source clamping diodes.

Introduction to the IGBT

The structure of an IGBT is similar to that of a Power MOSFET, both being created by the parallel connection of many thousands of identical cells. Figure 1 shows the cross section of one IGBT cell. The only difference between this drawing and one for a MOSFET would be the polarity of the substrate - the MOSFET would be n+ rather than the p+ of the IGBT. Since the gate structures are identical the IGBT like the MOSFET is a voltage driven device with an extremely high input impedance.

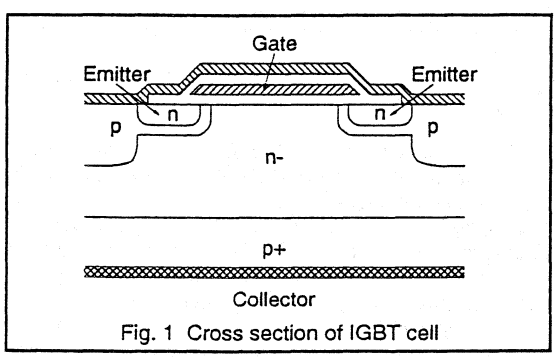


Fig. 1 Cross section of IGBT cell

Bipolar operation

Where the IGBT differs is in the characteristics of the output device. Conduction in a MOSFET is by majority carriers only but the p substrate silicon used for IGBTs promotes injection and gives bipolar conduction with both majority and minority carriers. The effect of this is to make the on state voltage drop of a high voltage IGBT much lower than that of the same size and voltage MOSFET. This feature is particularly useful in automotive ignition where high voltage devices are needed which can operate from low voltage supplies. In recognition of its combination of MOSFET input and bipolar output, the terminals of an IGBT are called Collector, Emitter and Gate.

Input Voltage

IGBTs, like MOSFETs, can have standard or logic level gate sensitivity. A standard device has a threshold voltage of typically 3.5 V - the threshold voltage is the gate voltage needed to allow the IGBT to conduct 1 mA, i.e just started to turn on. To be fully on, with an acceptable low V_{CE}, the gate voltage needs to be 8.5 V. In some situations, such as engine cranking, the battery voltage falls to less than 6 V and achieving adequate drive may be a problem.

An alternative would be to use a logic level IGBT which has a threshold of typically 1.5 V and is fully on with 5 V.

Another factor in the choice between standard or logic level, is that of noise immunity. In this application it can be very important that the IGBT is fully off, in a very low leakage state, when the driver stage output is LOW. Unfortunately, the LOW that a driver produces may not create a gate to emitter voltage of 0 V.

The threshold voltage of an IGBT falls as temperature rises. So the gate emitter voltage of a logic level IGBT (at $T_j = 120°C$) needs to be < 0.7V to ensure that it is off. A standard level part, with its higher threshold, has more immunity and it would still be off if the voltage was < 1.4 V.

Turn off control

The time between the gate signal arriving at the IGBT and the collector voltage rising is known as the delay time, t_d. An ignition system produces a spark when the collector voltage rises. Since the timing of the spark is critical, it is advantageous to have good control of t_d. With the IGBT, unlike some other ignition switches, t_d is dominated by gate charge and so can be very low and is easily controlled by the resistance of the driver circuit.

Safe Operating Area

One of the worst situations for creating IGBT latch up is inductive turn off. Such a turn off takes place in electronic ignition. IGBTs, for ignition applications, are specified with a safe operating area (SOA) and limiting value of collector current that can be safely switched under clamped inductive load conditions (I_{CLM}). Providing that the device is operated within its safe operating area (SOA) dynamic latch-up (or SOA failure) cannot occur. Philips ignition IGBTs have a large turn-off SOA and a large energy handling capability making them easy to use in ignition circuits.

Feature	Advantage
IGBTs	
•Voltage driven	-Low gate drive power -Simple gate circuit
•Logic level capability	-Low battery operation
•Bipolar operation	-Low conduction loss -Small device size
•PowerMOS/bipolar structure	-Negligible Storage time -Reverse blocking -Energy handling
•Large SOA	-No snubber required -Design flexibility
Clamped IGBTs	
•Integral clamp diodes	-Design simplicity -Overvoltage protection -Clamp voltage control -Improved reliability -ESD protection

Table 1. Advantages of IGBTs

Reverse Battery

The n- p+ junction, see Fig. 1, which is inherent in the structure of the IGBT, creates a reverse blocking junction. This junction, although unable to support very high reverse voltages, is able to block voltages in excess of a battery voltage. This gives the IGBT a reverse battery blocking capability which ensures that reverse battery fault conditions will not give rise to high currents which could damage the IGBT or any other components in the ignition circuit.

Clamped IGBT

A refinement of the conventional IGBT is the clamped or protected IGBT. This is produced by adding extra processing stages which allows polysilicon diodes, of known breakdown voltage, to be integrated with the IGBT structure. A short chain of diodes is connected between the gate and the emitter. This gives ESD protection by clamping the voltage, which can be applied across the gate emitter oxide, to a safe value.

A much longer chain, with a combined breakdown voltage of several hundreds of volts, is connected between the collector and the gate. This chain makes the IGBT into a dynamic clamp - possibly the best way of ensuring survival during ignition faults like open circuit secondary. The position of the diode chains is shown in the circuit symbol, see Fig. 2.

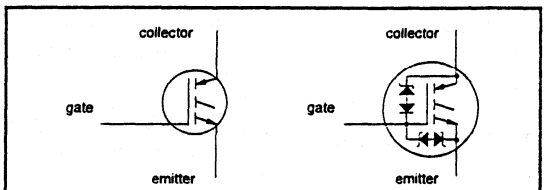


Fig. 2 IGBT circuit symbols

Conclusions

The Philips Semiconductors BUK854-500IS ignition IGBTs and clamped IGBTs BUK856-400IZ and BUK856-450IX are specifically designed to give a low loss, easy to drive and rugged solution to the demanding applications of automotive ignition circuits. IGBTs require the minimum of external components in the gate drive circuit and give negligible drive losses. The energy handling and reverse blocking capabilities of the device make it suitable for use in automotive environments - even under fault conditions. Voltage clamping and ESD protection give ease of design and use, improved reliability and performance in the ignition controller circuit.

Electronic switches for automotive ignition

Application report

Earlier sections in this chapter have discussed the nature of automotive electronic ignition and looked at a range of IGBTs which have been optimised for use in this type of application. This section will compare ignition IGBTs with ignition darlington transistors and come to the conclusions that IGBTs have several advantages which would be useful to the automotive designer.

Darlington transistors

In the past, the darlington transistor has been the favoured power transistor for ignition applications. The darlington connection is, in fact, a cascade of two separate bipolar transistors. The combination increases the gain allowing the high voltage device to be controlled by a relatively low power driver stage.

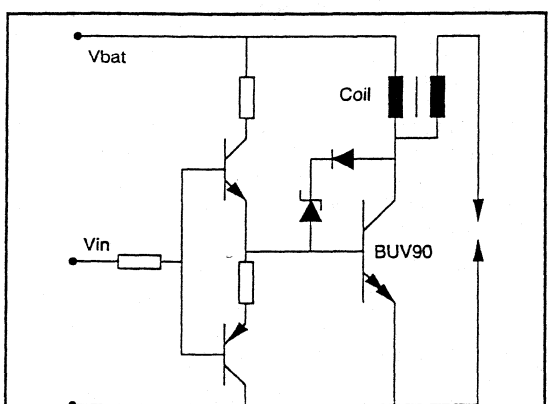


Fig. 1 Typical ignition circuit with darlington switch

As the darlington is a bipolar device it has a relatively low on-state voltage drop even though it can block a high voltage. The low voltage drop keeps conduction losses low and allows the ignition circuit to function at low battery voltages.

The disadvantage of a darlington is the complexity and cost of the base drive. Even though the gain is improved, by the darlington connection, a large gate current is still needed (approx. 100 mA) a circuit similar to that shown in Fig. 1 will be needed. It would be inefficient and costly to supply a current this large from the stabilised 5 V rail, so the supply could be the battery. This means that the drive dissipation when the transistor is on, is about 1.2 W and the average dissipation about 0.5 W. This level of dissipation requires a special driver IC or a circuit using discretes. All of this adds to the cost complexity and thermal problems of the ignition system.

The low on-state voltage drop of a bipolar device is the result of minority carrier injection. However, the minority carrier injection also introduces 'stored charge' into the device which must be removed at turn-off. The charge is extracted, at least partially, as negative base current during the period known as the storage time, t_s. How long this takes, depends on the amount of stored charge and the rate it is extracted. The amount of charge varies from device to device, with the level of the current and with temperature. The rate of extraction depends on the drive circuit and whether a 'simple' circuit like that of Fig. 1 is used or one which uses negative drive to remove the charge more quickly.

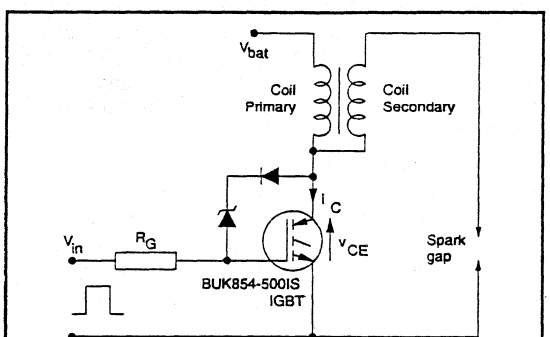


Fig. 2 Ignition IGBT circuit

Storage time adds to the delay between the input changing state and the spark being produced and the uncertainty in storage time, which results from the large number of variables, adds to the inaccuracy of the ignition timing.

Typical ignition darlingtons often include an internal antiparallel diode connected across the main emitter-collector terminals as shown in Fig. 1. This diode is not necessary for the normal operation of the ignition circuit and its function is simply to protect the darlington from reverse battery faults. However, during this condition, the diode does allow large reverse currents to flow through the ignition circuit.

IGBTs

The IGBT is a combination of bipolar transistor and Power MOSFET technologies. It has the advantage of the low on-state voltage drop of a bipolar darlington and can also be voltage driven in the same way as a Power MOSFET. This gives a highly efficient, easy to drive, minimum loss solution for the switching transistor in an ignition circuit.

A typical ignition circuit using the Philips BUK854-500IS IGBT is shown in Fig. 2; the saving in gate drive components is self evident. The need for a special driver stage is eliminated because drive dissipation for an IGBT will be approximately 10 μW which can be easily supplied by standard ICs. The BUK854-500IS has a voltage rating of 500V and standard gate threshold voltage, and is assembled in the TO220 package.

Clamped IGBTs

One of the most exciting features of IGBT technology is the ability to integrate protection functions into the IGBT to give significant advantages to the designer of power circuits. The BUK856-400IZ and BUK856-450IX are two such devices which have been specifically designed for automotive ignition circuits. The BUK856-400IZ is a logic level device, the BUK856-450IX has a standard gate threshold. The nominal clamp voltages are 400V and 450V respectively.

In these devices the dynamic clamp network shown in Fig. 2 is fabricated directly onto the IGBT. This gives guaranteed clamping of the IGBT at a fixed clamp voltage without the need for an external circuit. The clamp voltage is held to very tight tolerances over the full temperature range (-40°C to +150°C) required in automotive applications.

In both these devices gate-source protection diodes have also been incorporated into the structure of the devices to give full protection against ESD damage during handling and assembly of the device into engine management units.

IGBTs and darlingtons - A performance comparison

The performance of the BUK856-400IZ ignition IGBT has been compared with that of a typical ignition darlington in the ignition circuit of Fig. 1.

At turn-off the darlington switched considerably slower than the IGBT. The time between the input going low and the spark was 32 μs for the darlington and only 19 μs for the IGBT.

Table 1 shows a breakdown of the ignition system losses and demonstrates that whilst the device losses are slightly higher in the IGBT, the overall losses are higher in the darlington circuit due to extra loss in the base drive.

Power loss (W)	V_{clamp}=400V, I_{Cmax}=6.0A	
100Hz, (3000rpm)	IGBT	darlington
Conduction	1.37	1.16
Switching	0.71	0.79
Drive	0.00001	0.5
Total	2.08	2.45

Table 1. IGBT and darlington ignition circuit losses

Conclusion

Table 2 summarises the comparison between the IGBT and the darlington as the power switch in automotive ignition. The comparison shows that the darlington is good in the application but that the IGBT has some clear advantages making it significantly better.

	IGBT	darlington
Driver component count	Low	High
Speed of response, 'time to spark'	Fast	Slow
Total loss	Better	Good
Drive power	Low	High
Logic level operation	Yes	Yes
Open circuit load	Yes	Yes
Reverse blocking	Yes	No
Package size	Small	Large
Inbuilt voltage clamp	Possible	Possible
Inbuilt protection	Yes	No

Table 2. Performance comparison

Insulated Gate Bipolar Transistor Protected IGBT

BUK856-450IX

GENERAL DESCRIPTION

Protected N-channel insulated gate bipolar power transistor in a plastic envelope, intended for automotive ignition applications. The device has built-in zener diodes providing active collector voltage clamping and ESD protection up to 2 kV.

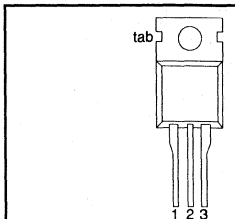
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{(CL)CER}$	Collector-emitter clamp voltage	400	450	500	V
V_{CEsat}	Collector-emitter on-state voltage			1.8	V
I_C	Collector current (DC)			15	A
P_{tot}	Total power dissipation			125	W
E_{CERS}	Clamped energy dissipation			300	mJ

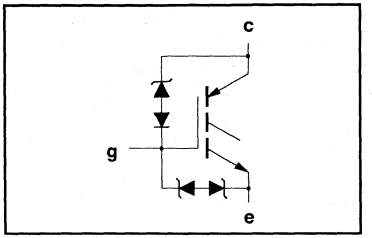
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	collector
3	emitter
tab	collector

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CE}	Collecter-emitter voltage	$t_p \leq 500\ \mu s$	-	500	V
V_{CE}	Collector-emitter voltage	Continuous	-20	50	V
$\pm V_{GE}$	Gate-emitter voltage	-	-	12	V
I_C	Collector current (DC)	$T_{mb} = 100\ ^\circ C$	-	8	A
I_C	Collector current (DC)	$T_{mb} = 25\ ^\circ C$	-	15	A
I_{CM}	Collector current (pulsed peak value, on-state)	-	-	25	A
I_{CLM}	Collector current (clamped inductive load)	$1\ k\Omega \leq R_G \leq 10k\Omega$; see Figs. 20,21			
		$T_j \leq 150^\circ C$	-	15	A
		$T_j \leq 175^\circ C$	-	10	A
E_{CERS}	Clamped turn-off energy (non-repetitive)	$T_{mb} = 25\ ^\circ C$; $I_C = 10$ A; see Figs.23,24	-	300	mJ
E_{ECR}	Reverse avalanche energy (repetitive)	$I_E = 1$ A	-	5	mJ
P_{tot}	Total power dissipation	$T_{mb} = 25\ ^\circ C$	-	125	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Operating Junction Temperature	-	-40	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	In free air	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CG}$	Collector-gate zener breakdown voltage	2 mA ≤ -I_G ≤ 5 mA; -40 ≤ T_j ≤175°C	400	450	500	V
$V_{(BR)EC}$	Reverse collector-emitter breakdown voltage	I_E = 50 mA -40 ≤ T_j ≤175°C	20	30	50	V
±$V_{(BR)GES}$	Gate-emitter breakdown voltage	I_G = ± 1 mA	12	15	20	V
$V_{GE(TO)}$	Gate threshold voltage	V_{CE} = V_{GE}; I_C = 1 mA;	2.0	3.5	4.5	V
$V_{GE(TO)}$		T_j = 175 °C	1.1	-	-	
I_{CER}	Collector current	V_{CE} = 50 V; R_{GE} = 1 kΩ	-	0.2	10	µA
I_{CER}		T_j = 125 °C	-	0.05	1	mA
I_{EC}	Reverse collector current	V_{CE} = -20 V	-	0.2	5	mA
I_{EC}		T_j = 125°C	-	2	10	mA
I_{GES}	Gate emitter leakage current	V_{GE} = 8.5 V	-	-	1	µA
I_{GES}		T_j =175°C	-	-	15	µA
V_{CEsat}	Collector-emitter on-state voltage	V_{GE} = 8.5 V; I_C = 8 A -40 ≤ T_j ≤175°C	-	1.3	1.8	V
V_{CEsat}		V_{GE} = 8.5 V; I_C = 2 A; T_j = 175°C	-	0.8	1.2	V
V_{CEsat}		V_{GE} = 8.5 V; I_C = 2 A; T_j = -40°C	-	1.0	1.4	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)CER}$	Collector-emitter clamp voltage	4 A≤ I_C ≤ 8 A; R_G = 1 kΩ; -40 ≤ T_j ≤ 175°C; Inductive load; see figs. 23,24	400	450	500	V
g_{fe}	Forward transconductance	V_{CE} = 15 V; I_C = 4 A	-	6.5	-	S
C_{ies}	Input capacitance	V_{GE} = 0 V; V_{CE} = 25 V; f = 1 MHz	-	720	900	pF
C_{oes}	Output capacitance		-	90	110	pF
C_{res}	Feedback capacitance		-	22	35	pF
$t_{d\ off}$	Turn-off delay time	I_C = 8 A; V_{CL} = 300 V; R_G = 1 kΩ;	-	5.5	8	µs
t_f	Fall time	V_{GE} = 10 V; T_j = 125°C;	-	5	8	µs
t_c	Crossover Time	Inductive load (externally clamped)	-	6	-	µs
E_{off}	Turn-off Energy loss	See Figs. 20,21.	-	7	-	mJ

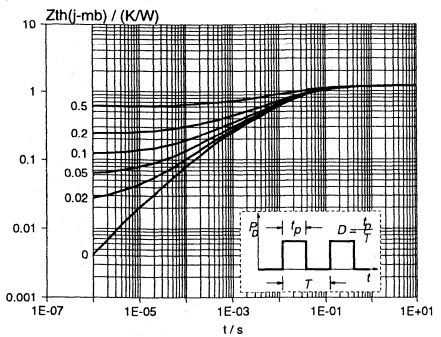


Fig.1. Transient thermal impedance
$Z_{th\ j\text{-}mb} = f(t)$; *parameter* $D = t_p/T$

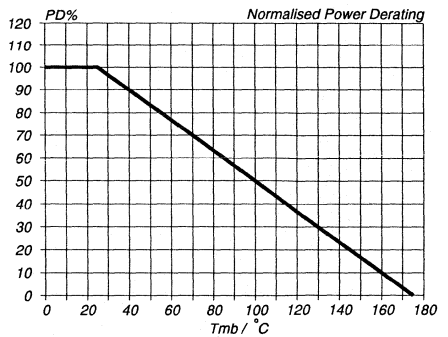


Fig.4. Normalised power dissipation.
$PD\% = 100.P_D/P_{D\ 25°C} = f(T_{mb})$

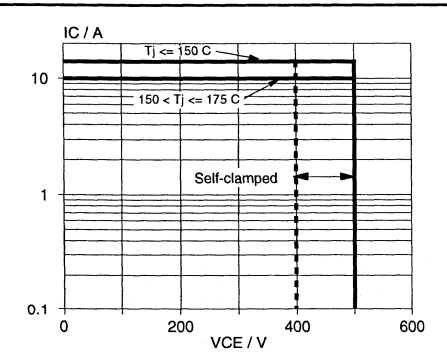


Fig.2. Turn-off safe operating area
conditions: $R_G \geq 1\ k\Omega$

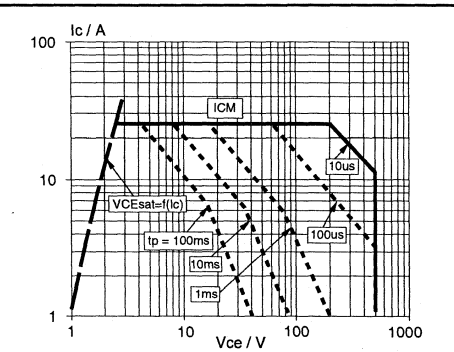


Fig.5. Pulsed on-state safe operating area
(non-repetitive). conditions : $T_{mb} = 125°C$

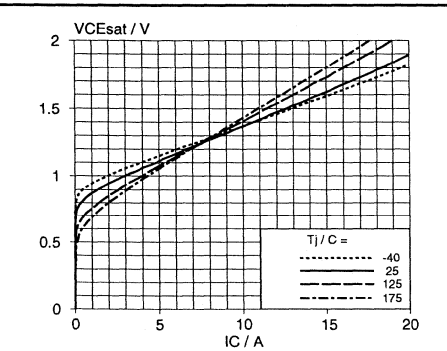


Fig.3. Typical on-state voltage
$V_{CEsat} = f(I_C)$; *parameter* T_j; *conditions:* $V_{GE} = 8.5\ V$

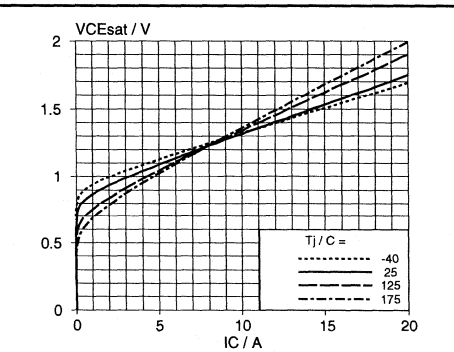


Fig.6. Typical on-state voltage
$V_{CEsat} = f(I_C)$; *parameter* T_j; *conditions:* $V_{GE} = 10\ V$

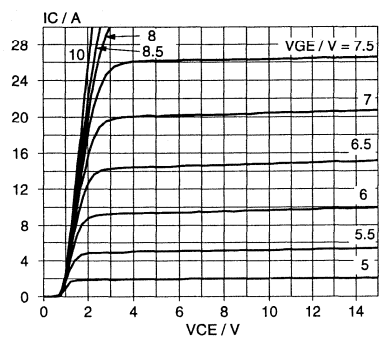


Fig.7. Typical output characteristics
I_C=f(V_{CE}); parameter V_{GE}; conditions: T_j=25°C

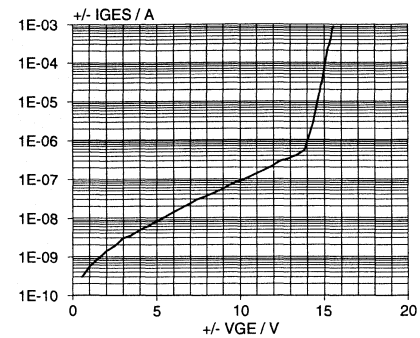


Fig.10. Typical gate-emitter charcteristics
I_{GES} = f(V_{GE}); conditions: V_{CE} = 0 V; T_j = 25°C

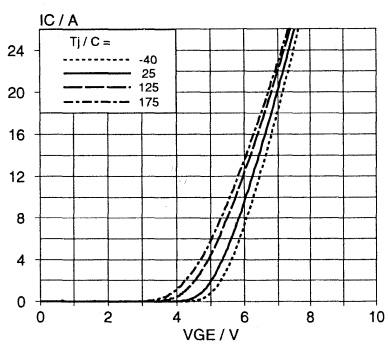


Fig.8. Typical transfer characteristics
I_C = f(V_{GE}), parameter T_j; conditions: V_{CE} = 15 V

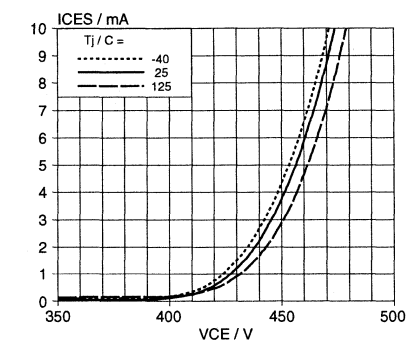


Fig.11. Typical collector clamp characteristics
I_{CES} = f(V_{CE}); parameter T_j; conditions: V_{GE} = 0 V

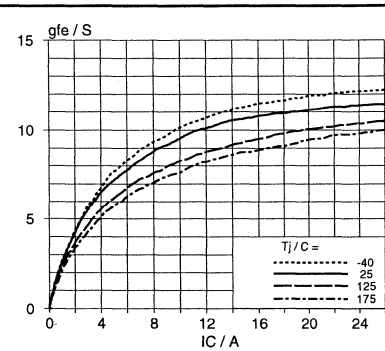


Fig.9. Typical forward transconductance
g_{fe} = f(I_C); parameter T_j; conditions: V_{CE} = 15 V

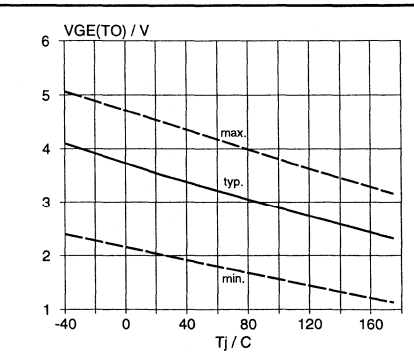


Fig.12. Gate threshold voltage
$V_{GE(TO)}$ = f(T_j); conditions: I_C = 1 mA; V_{CE} = V_{GE}

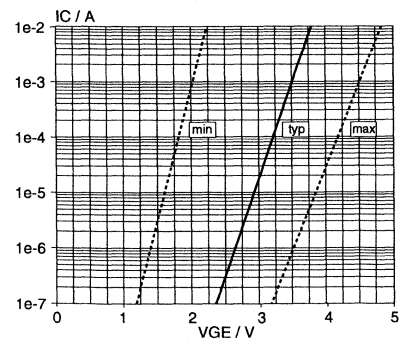


Fig.13. Sub-threshold collector current $I_C = f(V_{GE})$; $T_j = 25°C$; $V_{CE} = V_{GE}$

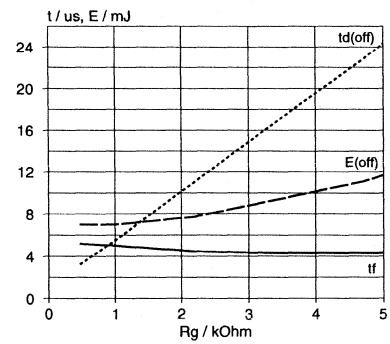


Fig.16. Typical switching characteristics vs. R_G conditions: T_j=125 °C; I_C=8 A; V_{CL}=300 V; L_C=5 mH.

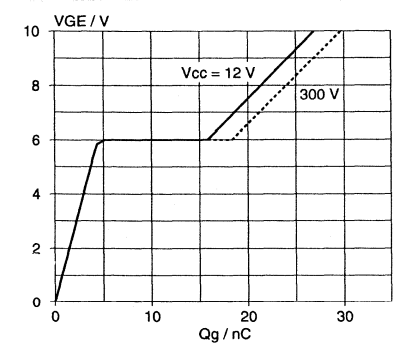


Fig.14. Typical turn-on gate charge characteristics $V_{GE} = f(Q_G)$; conditions: I_C = 8 A.

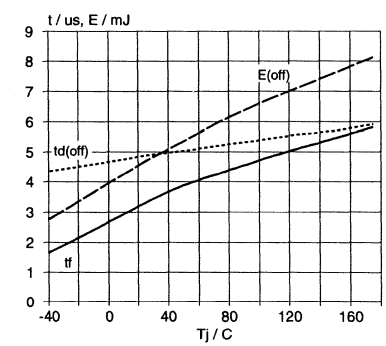


Fig.17. Typical switching characteristics vs. T_j conditions: I_C=8 A; V_{CL}=300 V; R_G=1 kΩ; L_C=5 mH.

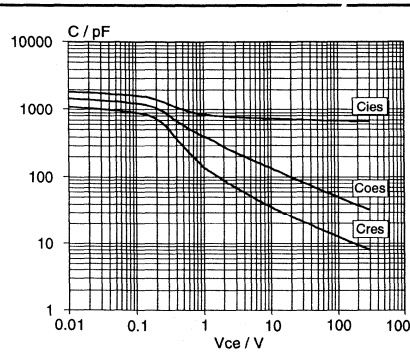


Fig.15. Typical capacitances C_{ies}, C_{oes}, C_{res} $C = f(V_{CE})$; conditions: V_{GE} = 0 V; f = 1 MHz

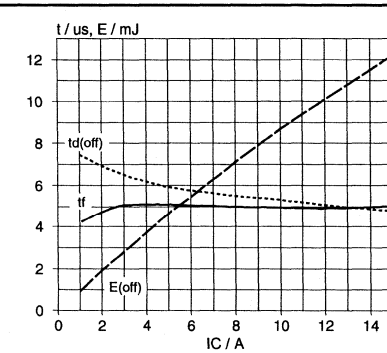


Fig.18. Typical switching characteristics vs. I_C conditions: T_j=125 °C V_{CL}=300 V; R_G=1 kΩ; L_C=5 mH.

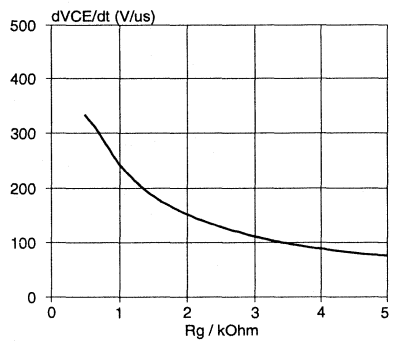


Fig.19. Typical turn-off dV_{CE}/dt vs. R_G. conditions: T_j = 125°C; I_C = 8 A; V_{CL} = 300 V.

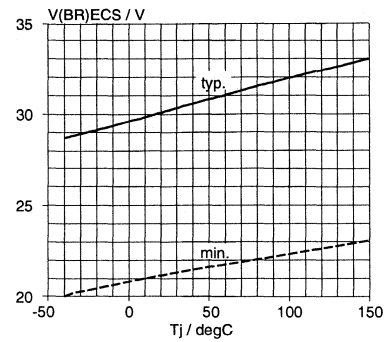


Fig.22. Reverse breakdown voltage $V_{(BR)ECS} = f(T_j)$; conditions: I_{EC} = 50 mA

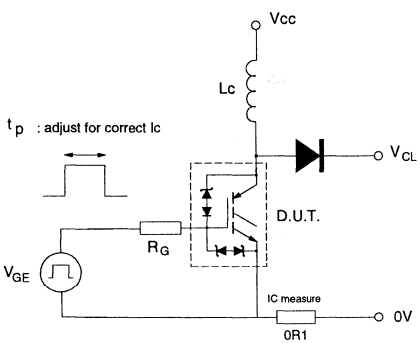


Fig.20. Test circuit for inductive load switching times.

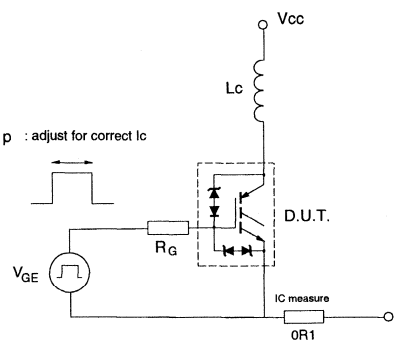


Fig.23. Test circuit for clamped inductive turn-off.

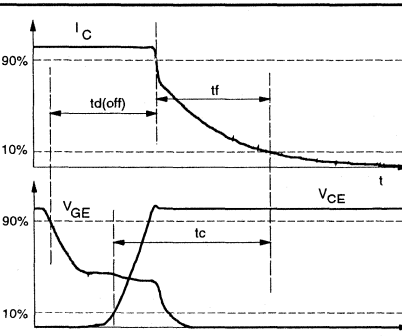


Fig.21. Definitions of inductive load switching times.

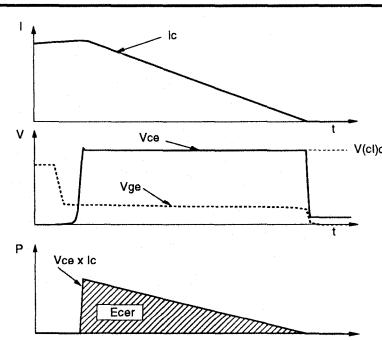


Fig.24. Definition of clamped turn-off energy E_{CER}

Insulated Gate Bipolar Transistor Protected Logic-Level IGBT

BUK856-400 IZ

GENERAL DESCRIPTION

Protected N-channel logic-level insulated gate bipolar power transistor in a plastic envelope, intended for automotive ignition applications. The device has built-in zener diodes providing active collector voltage clamping and ESD protection up to 2 kV.

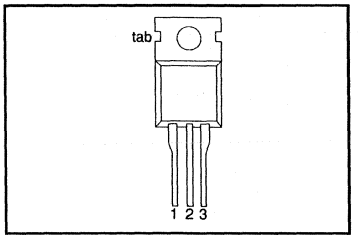
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{(CL)CER}$	Collector-emitter clamp voltage	350	400	500	V
V_{CEsat}	Collector-emitter on-state voltage			2.2	V
I_C	Collector current (DC)			20	A
P_{tot}	Total power dissipation			100	W
E_{CERS}	Clamped energy dissipation			300	mJ

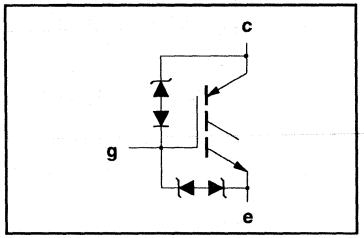
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	collector
3	emitter
tab	collector

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CE}	Collecter-emitter voltage	$t_p \leq 500\ \mu s$	-	500	V
V_{CE}	Collector-emitter voltage	Continuous	-20	50	V
$\pm V_{GE}$	Gate-emitter voltage	-	-	12	V
I_C	Collector current (DC)	$T_{mb} = 100\ °C$	-	10	A
I_C	Collector current (DC)	$T_{mb} = 25\ °C$	-	20	A
I_{CM}	Collector current (pulsed peak value, on-state)	$T_{mb} = 25\ °C$; $t_p \leq 10$ ms; $V_{CE} \leq 15$ V	-	25	A
I_{CLM}	Collector current (clamped inductive load)	$1\ k\Omega \leq R_G \leq 10\ k\Omega$	-	10	A
E_{CERS}	Clamped turn-off energy (non-repetitive)	$T_{mb} = 25\ °C$; $I_C = 10$ A; $R_G = 1\ k\Omega$; see Figs. 23,24	-	300	mJ
E_{CERR} [1]	Clamped turn-off energy (repetitive)	$T_{mb} = 100\ °C$; $I_C = 8$ A; $R_G = 1\ k\Omega$; f = 50 Hz	-	125	mJ
E_{ECR} [1]	Reverse avalanche energy (repetitive)	$I_E = 1$ A; f = 50 Hz	-	5	mJ
P_{tot}	Total power dissipation	$T_{mb} = 25\ °C$	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Operating Junction Temperature	-	-40	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

1 This applies to short-term operation in ignition circuits with open-secondary ignition coil.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Junction to mounting base		-	1.0	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	In free air	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CG}$	Collector-gate zener breakdown voltage	5 mA ≤ $-I_G$ ≤ 2 mA; -40 ≤ T_j ≤150°C	350	400	500	V
$V_{(BR)EC}$	Reverse collector-emitter breakdown voltage	I_E = 10 mA	20	30	50	V
$\pm V_{(BR)GES}$	Gate-emitter breakdown voltage	I_G = ± 1 mA	12	16	20	V
$V_{GE(TO)}$	Gate threshold voltage	V_{CE} = V_{GE}; I_C = 1 mA	1	1.5	2	V
$V_{GE(TO)}$	Gate threshold voltage	V_{CE} = V_{GE}; I_C = 1 mA; -40 ≤ T_j ≤150°C	0.6	-	2.4	V
I_{CES}	Zero gate voltage collector current	V_{CE} = 50 V; V_{GE} = 0 V; T_j = 25 °C	-	0.01	10	µA
I_{CES}	Zero gate voltage collector current	T_j = 125 °C	-	0.01	1	mA
I_{EC}	Reverse collector current	V_{CE} = -20 V	-	0.2	5	mA
I_{EC}	Reverse collector current	V_{CE} = -20 V; T_j = 125°C	-	2	20	mA
I_{GES}	Gate emitter leakage current	V_{GE} = ±6 V	-	0.1	1	µA
		T_j = 150°C	-	5	100	µA
V_{CEsat}	Collector-emitter on-state voltage	V_{GE} = 4.5 V; I_C = 8 A	-	1.2	2.2	V
		V_{GE} = 3.5 V; I_C = 6 A; -40 ≤ T_j ≤150°C	-	1.2	2.2	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)CER}$	Collector-emitter clamp voltage (peak value)	R_G = 1 kΩ; I_C = 10 A; -40 ≤ T_j ≤150°C; Inductive load; see Figs. 23,24	350	400	500	V
g_{fe}	Forward transconductance	V_{CE} = 15 V; I_C = 4 A	5.5	15	20	S
C_{ies}	Input capacitance	V_{GE} = 0 V; V_{CE} = 25 V; f = 1 MHz	-	940	1200	pF
C_{oes}	Output capacitance		-	95	130	pF
C_{res}	Feedback capacitance		-	30	50	pF
$t_{d\ off}$	Turn-off delay time	I_C = 8 A; V_{CL} = 300 V; R_G = 1 kΩ;	-	13	18	µs
t_f	Fall time	V_{GE} = 5 V; T_j = 125°C;	-	6	10	µs
t_c	Crossover Time	Inductive load; see Figs. 20,21	-	12	-	µs
E_{off}	Turn-off Energy loss		-	13	-	mJ

Insulated Gate Bipolar Transistor
Protected Logic-Level IGBT

BUK856-400 IZ

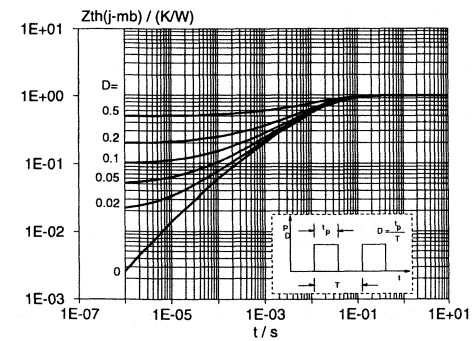


Fig.1. Transient thermal impedance
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

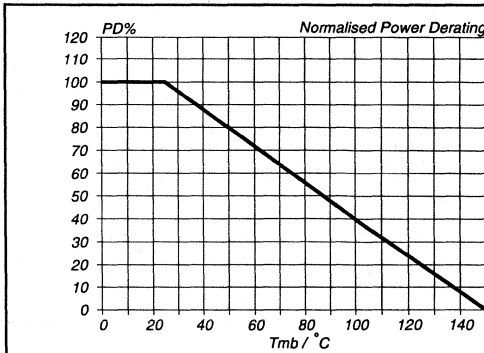


Fig.4. Normalised power dissipation.
PD% = 100.$P_D/P_{D\ 25°C}$ = f(T_{mb})

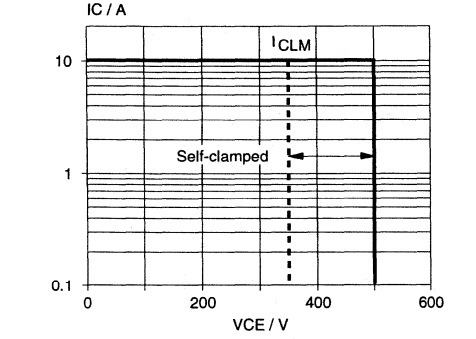


Fig.2. Turn-off Safe Operating Area
conditions: $T_j \leq T_{jmax.}$; $R_G \geq 1$ kΩ

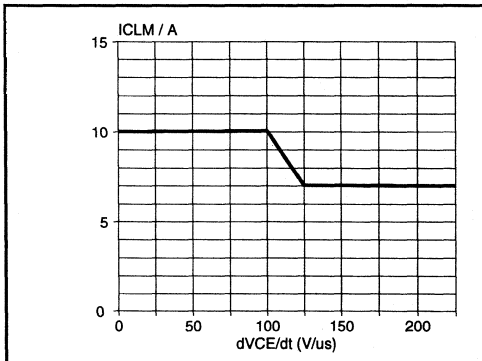


Fig.5. Derating of I_{CLM} with turn-off dV_{CE}/dt
conditions: $V_{CE} \leq 500$ V; $T_j \leq T_{jmax.}$

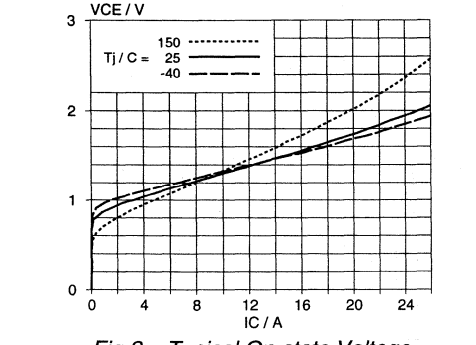


Fig.3. Typical On-state Voltage
$V_{CEsat} = f(I_C)$; parameter T_j; conditions: $V_{GE} = 3.5$ V

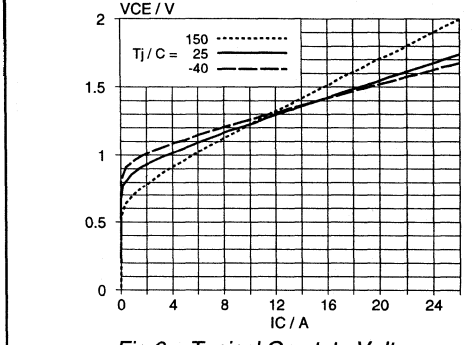


Fig.6. Typical On-state Voltage
$V_{CEsat} = f(I_C)$; parameter T_j; conditions: $V_{GE} = 5$ V

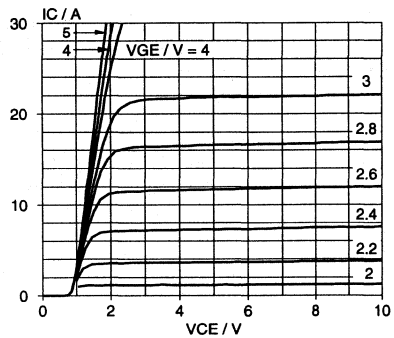


Fig.7. Typical Output Characteristics
$I_C = f(V_{CE})$; parameter V_{GE}; conditions: $T_j = 25°C$

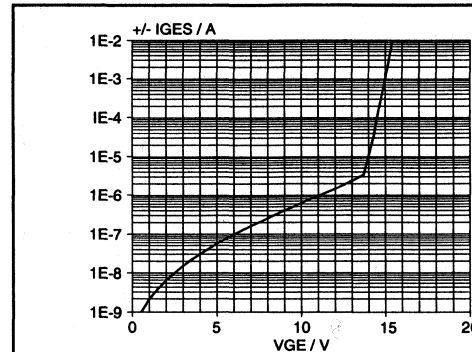


Fig.10. Typical gate-emitter charcteristics
$I_{GES} = f(V_{GE})$; conditions: $V_{CE} = 0$ V; $T_j = 25°C$

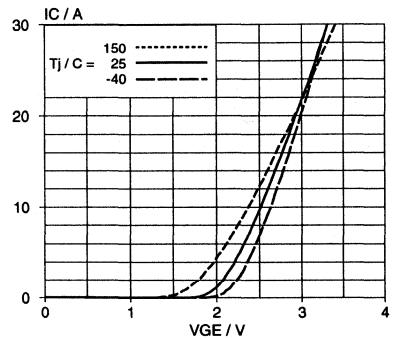


Fig.8. Typical Transfer Characteristics
$I_C = f(V_{GE})$, parameter T_j; conditions: $V_{CE} = 10$ V

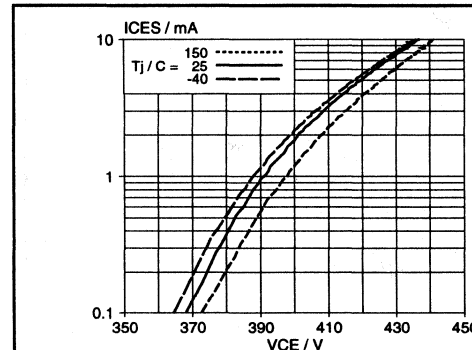


Fig.11. Typical collector clamp characteristics
$I_{CES} = f(V_{CE})$; parameter T_j; conditions: $V_{GE} = 0$ V

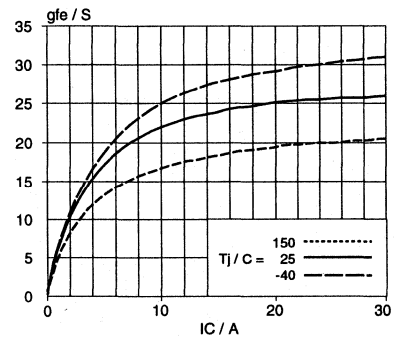


Fig.9. Typical Forward Transconductance
$g_{fe} = f(I_C)$; parameter T_j; conditions: $V_{CE} = 10$ V

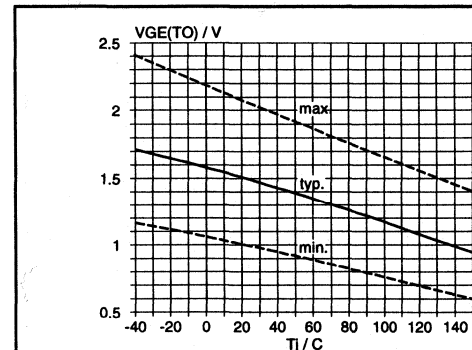


Fig.12. Gate Threshold Voltage
$V_{GE(TO)} = f(T_j)$; conditions: $I_C = 1$ mA; $V_{CE} = V_{GE}$

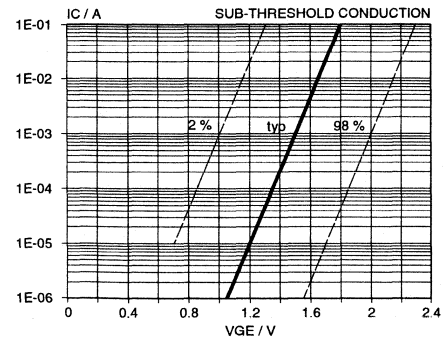


Fig.13. Sub-threshold collector current $I_C = f(V_{GE})$; $T_j = 25°C$; $V_{CE} = V_{GE}$

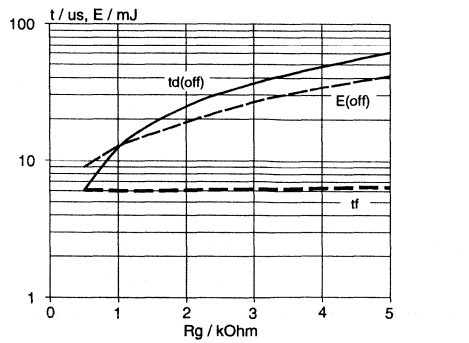


Fig.16. Typical Switching Characteristics vs. R_G conditions: T_j=125 °C; I_C=8 A; V_{CL}=300 V; L_C=5 mH.

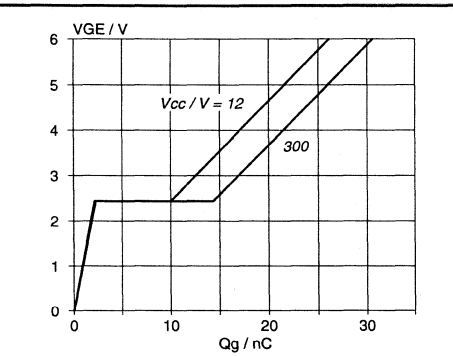


Fig.14. Typical Turn-on Gate Charge Characteristics $V_{GE} = f(Q_G)$; conditions: I_C = 8 A.

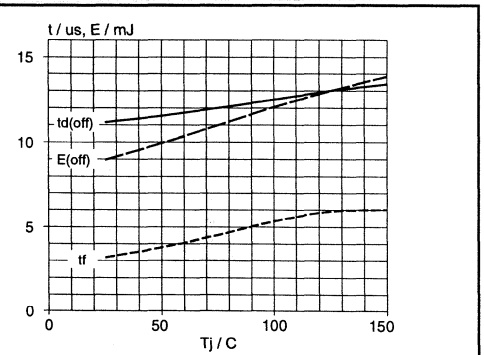


Fig.17. Typical Switching Characteristics vs. T_j conditions: I_C=8 A; V_{CL}=300 V; R_G=1 kΩ; L_C=5 mH.

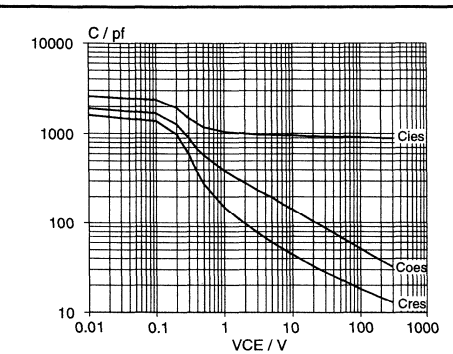


Fig.15. Typical Capacitances C_{ies}, C_{oes}, C_{res} $C = f(V_{CE})$; conditions: V_{GE} = 0 V; f = 1 MHz

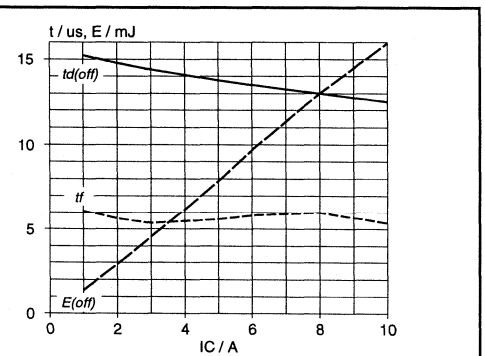


Fig.18. Typical Switching Characteristics vs. I_C conditions: T_j=125 °C V_{CL}=300 V; R_G=1 kΩ; L_C=5 mH.

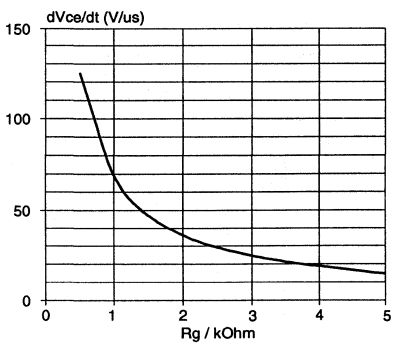


Fig.19. Typical Turn-off dV_{CE}/dt vs. R_G conditions: T_j=125 °C; I_C=8 A; V_{CL}=300 V; L_C=5 mH.

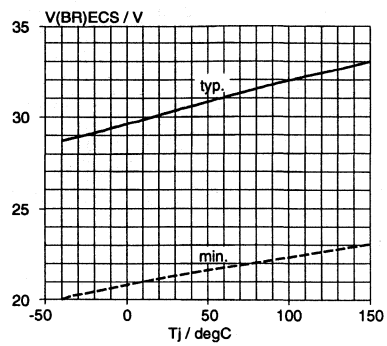


Fig.22. Reverse Breakdown Voltage $V_{(BR)ECS} = f(T_j)$; conditions: I_{EC} = 50 mA

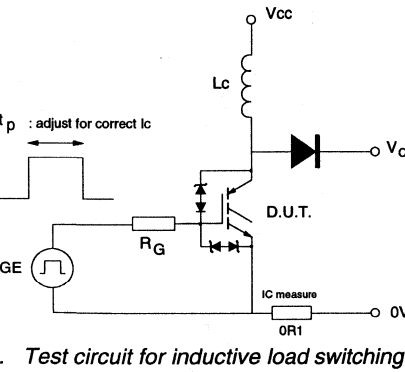


Fig.20. Test circuit for inductive load switching times.

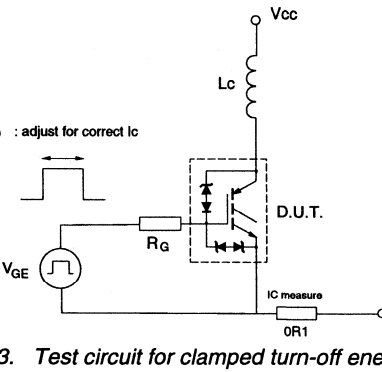


Fig.23. Test circuit for clamped turn-off energy test

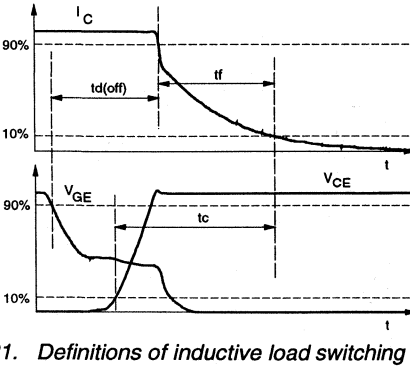


Fig.21. Definitions of inductive load switching times.

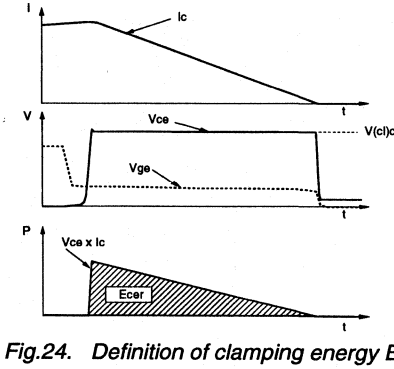


Fig.24. Definition of clamping energy E_{CER}

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

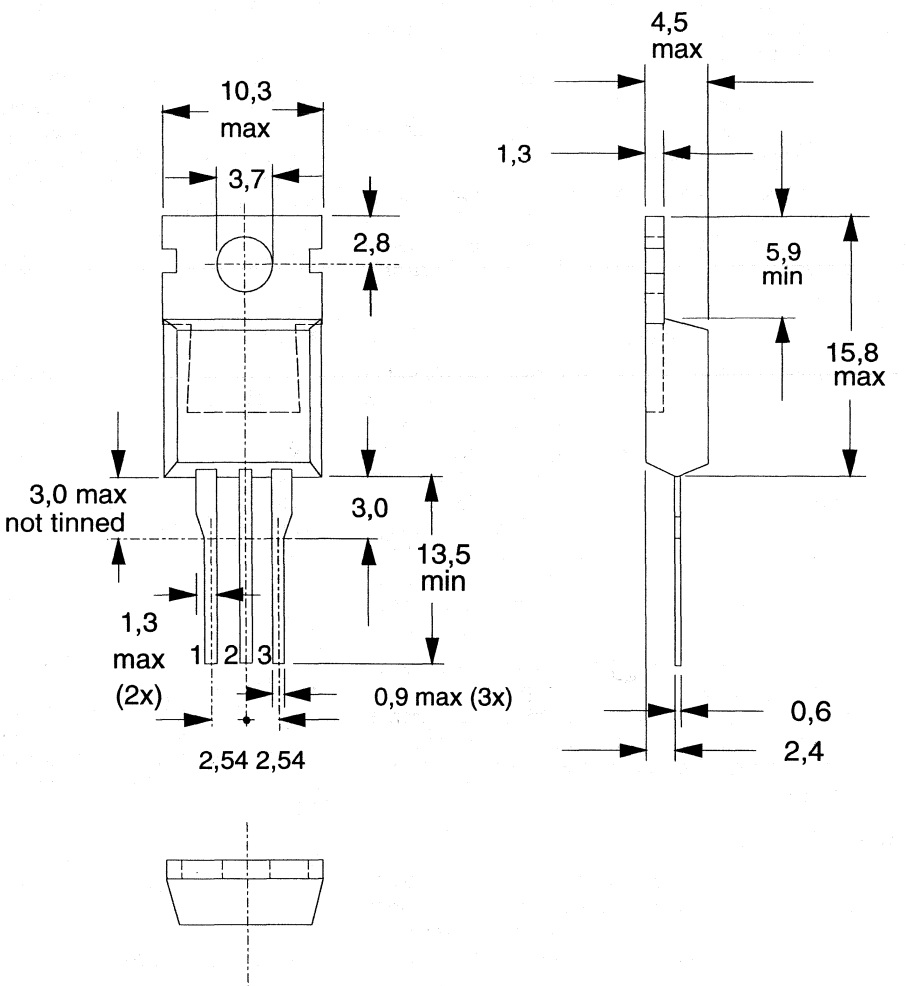


Fig.25. TO220AB; pin 2 connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to mounting instructions for TO220 envelopes.

Although the pulse width modulation, PWM, method of motor speed control is often preferred over the linear method it is not without problems. Some of these are totally eliminated in linear controllers. However, linear control techniques have their own limitations. By using a Philips TOPFET as the power device some of the disadvantages are removed giving a fully protected, linear control system.

This note will compare linear and PWM controllers. It will then give details of a circuit based around a BUK105-50S which shows that, with a TOPFET, it is simple to produce a fully protected, linear controller for adjusting the speed of a car heater fan.

Linear and PWM Control

PWM is often selected as the method of controlling the speed of a brush motor because it is more efficient than linear control. The reduction in energy loss results from a reduction in the loss in the controlling power device. The loss is lower because the device is only transiently in the high dissipation state of being partially ON. To keep the loss as low as possible, the transition time needs to be kept short, implying fast switching and high values of dV/dt and dI/dt. It is these fast switching rates which create the electrical noise that can be such a problem in automotive applications.

Linear control does not create this noise because it holds the output at a steady value. The power device is continuously in the partially ON state and its dissipation is high. If, however, this heat can be handled and the inefficiency is acceptable then linear control may be the better choice.

Device Selection Factors

In PWM control, on-state dissipation is the major energy loss, so $R_{DS(ON)}$ is the main selection criterion. In linear control, maximum dissipation occurs when half the supply voltage is being dropped across the device. In this state $R_{DS(ON)}$ is not relevant as dissipation is being controlled by the load and the supply. The limiting factor in this case is the need to dissipate the energy and keep the junction temperature to a safe value. The selection, therefore, is based on junction to mounting base and mounting base to heatsink thermal resistance. $R_{DS(ON)}$ cannot be ignored, however, because it sets the residual voltage loss at maximum speed which can be important.

TOPFET in Linear Control

The circuit shown in Fig. 10. is a linear controller for a car heater fan based around a BUK105-50S. TOPFET is well suited to this application because it is a real power device in a real power package giving it good thermal characteristics and low $R_{DS(ON)}$. The 5-pin TOPFET is used because the protection circuits need to be supplied independently from the input. The on-chip overtemperature protection feature of TOPFET is precisely the protection strategy needed in this type of high dissipation application.

Input Pin

In this circuit the input of the TOPFET is connected, via R1 and D1, to the output of an operational amplifier. The TOPFET drain voltage is attenuated by R2/R3 and fed to the positive input of the amplifier. The negative input is connected to the wiper of the speed setting potentiometer. This TOPFET/op-amp arrangement creates a non-inverting amplifier with a gain of

$$gain = \frac{(R2 + R3)}{R3}$$

In such a low frequency system the presence of R1 at 2.2 kΩ will not have a significant effect on normal operation. However, if TOPFET is tripped, its internal gate source transistor will be turned on and, because R1 is greater than the 2 kΩ needed for self protection (see R_I in the data sheet), the MOSFET gate will be pulled down and the TOPFET will be OFF.

Diode D1 prevents the input of the TOPFET being pulled negative with respect to the source.

Protection Supply

To ensure that the overtemperature and shorted load protection circuits work, the protection supply pin needs to be connected to an adequate supply. To allow TOPFET to be reset, provision has to be made to switch this so it can fall below the minimum reset voltage, V_{PSR}. Possibly the easiest way to achieve this is by feeding the protection supply from a CMOS gate.

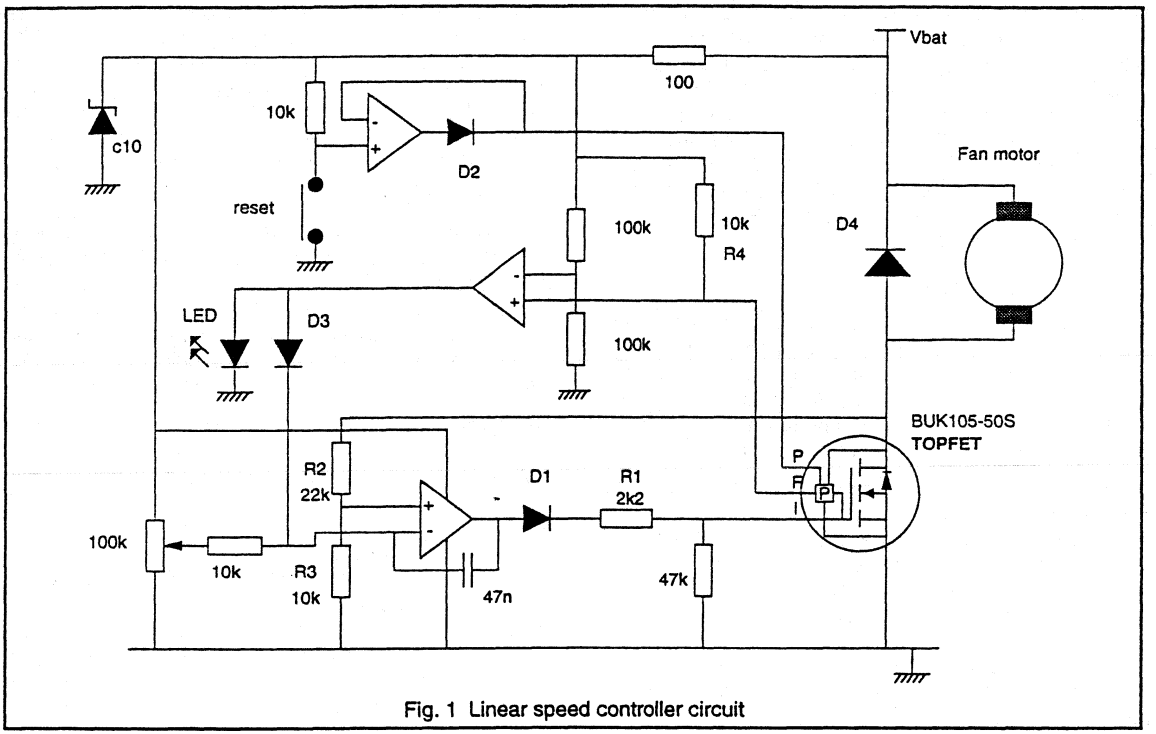


Fig. 1 Linear speed controller circuit

Two version of BUK105-50 are available, 'S' and 'L'. They differ in their protection supply requirements. L devices are designed to operate from a nominal 5 V. This makes them compatible with 5 V logic families like the 74HC and HCT series. L types can be driven at 10 V but as curves in the data show the protection characteristics are affected. On the other hand, S devices are designed to work with a nominal 10 V such as is available from HEF4000 logic gates.

If this circuit were part of a larger system then it is likely that such a gate would be available. In the circuit given here the protection pin is connected to the output of an op-amp wired as a non-inverting buffer. The buffer input is pulled up to the +ve rail with 10 kΩ. The protection supply can be taken low - to reset the TOPFET - by a pushbutton which grounds the input of the buffer.

Flag pin

In this circuit the flag pin is connected to a 10 kΩ pull-up resistor, R4. In a more sophisticated system this signal could then be fed to the input of a logic gate and used to inform the system controller of a fault condition. The controller could use this information to initiate a reset sequence or perhaps shut down the circuit and record the fact in a maintenance record store.

In this simpler system the flag output feeds the input of an op-amp wired as a comparator which in turn indicates a fault by lighting a LED. The output is also fed via D3 to the input of the speed controller op-amp. This overrides the signal from the speed adjusting potentiometer and takes the TOPFET input low. This arrangement has been used - even though the circuit has been designed to allow the TOPFET to self protect - to prevent the TOPFET from turning back on when there is no protection supply, for example during reset.

Drain pin

Freewheel diode D4 is needed if the energy stored in the motor inductance exceeds the TOPFET's non-repetitive inductive turn-off energy rating at the designed operating junction temperature. The overvoltage clamping of the TOPFET is still needed, however, to protect against supply line transients.

PWM control with TOPFET

Application report

Speed control of permanent magnet dc motors is required in many automotive and industrial applications, such as blower fan drives. The need for protected load outputs in such systems can be met by using a TOPFET with its inherent protection against short circuit, overtemperature, overvoltage and ESD. In section 5.3.7 the two basic methods for speed control, linear and PWM, are compared and discussed and a circuit example for linear control is given. This section gives an example of a PWM drive circuit using a 5-pin TOPFET.

Circuit Description

The circuit shown in Fig. 1 contains all the elements needed to produce a PWM circuit which can control the speed of a heater fan motor. The power device, because it is a TOPFET, can survive if the load is partially or completed shorted, if overvoltage transients appear on the supply lines or if the cooling is, or becomes, insufficient.

In a PWM control system the supply to the motor has to be switched periodically at a frequency significantly above its mechanical time constant. The net armature voltage and thus the motor speed is controlled by the duty cycle, i.e. on-time/period, of the control signal. With the component values shown, the circuit operates at a frequency of 20kHz. This means that any mechanical noise created by the switching is ultrasonic. The main building blocks of the circuit are the PWM generator, the power driver and the interface between the two.

PWM Generator

In Fig. 1, OP1 together with T1 and T2 form a saw-tooth generator, whose frequency is determined by R1 and C1. OP2 compares the saw-tooth voltage waveform at its inverting input with the voltage determined by the potentiometer P1. The output of OP2 is high as long as the saw-tooth voltage is less than the P1 voltage. As a result, the higher the voltage at P1, the longer the positive pulse width and thus the higher the duty cycle of the signal at the output of OP2.

Interface PWM Generator - TOPFET

The output signal of OP2 is fed to emitter-followers T4 and T5. These act as a low impedance driver for the input of the TOPFET. The drive is needed to achieve the short switching times which keep the dynamic switching losses of the TOPFET below the on-state losses.

Resistor R15 is included between the driver T4/T5 and the TOPFET input to ensure proper function of the TOPFET's internal overvoltage protection. This overvoltage protection is an active clamp circuit that will try to pull up the gate of the TOPFET's power MOSFET (i.e. the input pin) if the drain-source voltage exceeds 50V. A minimum resistance of 100Ω between input and ground is needed for the active clamp to succeed.

If the load is shorted or the TOPFET's junction temperature is too high, the internal sensors of the TOPFET will detect it and inform the protection logic which will turn off the internal flag transistor. The flag pin, which is connected to the drain of this transistor, will be pulled high by resistor R16. This will turn on transistor T3 pulling the input to the driver stage, T4/T5, low and hence turning the TOPFET off.

The TOPFET will remain in this state - even if the error condition disappears - until a reset is applied. The 5-pin TOPFETs are reset by taking the protection SUPPLY pin below V_{PSR}. In this circuit this is done by closing the reset switch, pulling the protection pin to ground. In this state there is no protection supply so the TOPFET is unprotected. However, the TOPFET indicates the absence of a protection supply by the flag transistor remaining off. In this circuit this causes the drive to the TOPFET to be low hence the TOPFET will stay off. The TOPFET will resume normal operation when the reset switch is opened and the protection supply is re-established.

Power Stage

In this circuit, the main power switch is a BUK105-50L which has an $R_{DS(ON)}$ of 60 mΩ @ V_{IS} = 5 V. The L version of the BUK105 has been chosen so that the protection supply can be fed from the available 5 V supply. The maximum protection supply current, I_{PS}, is 350 µA, the voltage drop across R17 could be 0.42 V. Even if the voltage is regulated as low as 4.5 V, the protection supply will still be > 4 V, the minimum V_{PSP} for valid protection with a V_{IS} of 5 V.

If a lower $R_{DS(ON)}$ were needed this could be achieved by modifying the circuit to give a higher V_{IS} on the TOPFET. A V_{IS} = 7 V would give an $R_{DS(ON)}$ = 50 mΩ. An input voltage as high as 10 V could be used but any increase must be accompanied by an increase in the protection supply voltage. A curve showing the required V_{PSP} for the full range of input voltage is given in the data sheet.

PWM control with TOPFET

Application report

The given circuit can be used in both 12V and 24V systems because, with an input voltage of 5V, the TOPFET is short circuit protected up to a supply voltage of 35V. However, if a supply this high is expected then the dissipation and voltage rating of the regulator would need to be studied.

D1 is a freewheel diode across the motor load which must be present even though the TOPFET has an internal clamp circuit. This is because the dissipation resulting from repetitively clamping at 20 kHz is very high, much higher than any power switch of this size would be able to handle. R18/C4 are optional devices that slow down switching, reducing dV/dt and hence RF noise emission.

Capacitor C5 helps to decouple the circuit from the supply and prevents excessive dI/dt on the power lines and the excessive voltage spikes it would produce.

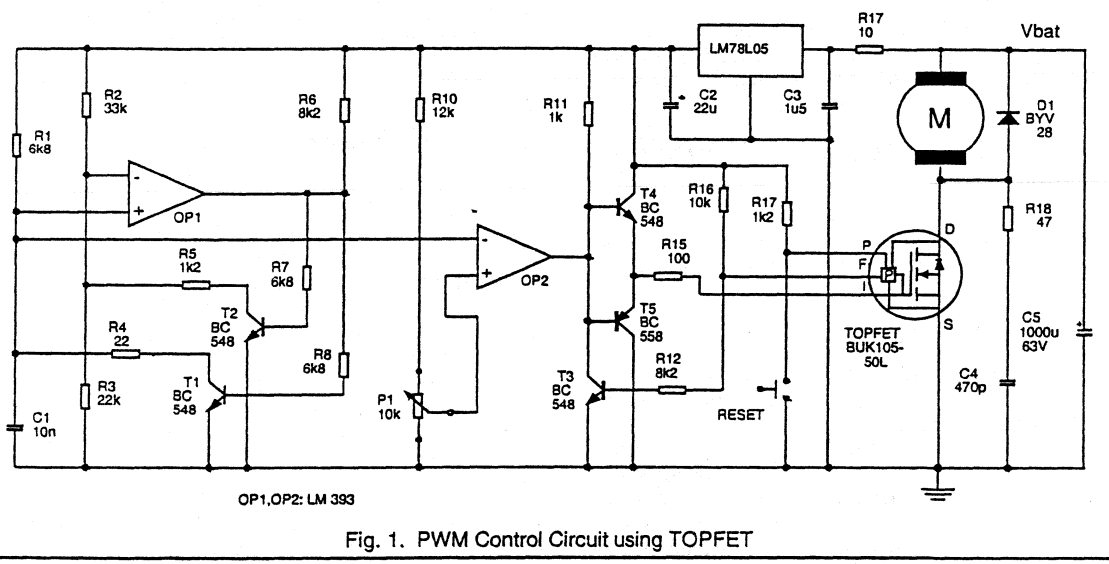


Fig. 1. PWM Control Circuit using TOPFET

Isolated drive for TOPFET

Application report

An isolated drive for a power transistor is required if an electronic replacement of an electromechanical relay is to be realised. By using a TOPFET, with its integrated protection functions, in combination with an isolated input drive, the following advantages over an electromechanical relay can be achieved:

- o Permanent short circuit protection
- o Over temperature protection
- o Active clamping at inductive turn-off
- o Logic level control
- o Higher switching frequency

This section presents a complete circuit example of a transformer isolated drive. It also discusses other isolation techniques particularly in relation to meeting TOPFET's specific requirements.

Basic Methods for Isolated INPUT Drives

Opto-Isolated Drives

For this method a light emitter (e.g. LED or lamp) and a photo-device is needed. The latter can be subdivided into two groups:

Photo Resistors/Transistors

With these devices a 'switch' can be built to control the input voltage of a TOPFET. They cannot provide the power needed to drive the input so a separate supply is needed. In low side configurations this can be the main supply directly. In high side configurations an input voltage above main supply level is needed which could be generated by a charge pump. However, the supply connection needed for this type of opto-isolated drive is not needed with an electromechanical relay. So an opto-isolated drive with photo resistors/transistors cannot serve as a universal relay replacement.

Photo Cells

The drive energy from a control pin can be transferred to the input pin of a power device by means of photo cells. This would eliminate the need for the additional supply connection. Integrated devices exist that combine an LED and a chain of photo-cells. They are designed to drive ordinary power MOSFETs so their output current, due to the low efficiency of the photo-cells, is only a few μA. This is not enough to supply the protection circuits of a TOPFET so this method cannot be used to provide isolated drive for a TOPFET.

Transformer Isolated Drives

As with photo-cells, pulse transformers provide a means of transferring energy from the control pin to the input of the power device. However, the transfer efficiency of a pulse transformer is much higher, so the protection circuits of a TOPFET can be supplied satisfactorily.

Extremely small pulse transformers are now available, and some outlines are suitable for surface mount. It is, therefore, realistic and practical to use this method to create a relay replacement for high and low side configurations.

Circuit Description

Figure 1 shows a transformer-isolated drive circuit for TOPFET. As discussed above, a TOPFET in combination with this drive circuit can be employed either in high side or low side configuration without modifications on the driver side. The drive signal on the transformer's primary side is a pulse train that is rectified on the secondary side to provide a continuous input voltage V_{IS} for the TOPFET. For the given dimensioning, a pulse rate in the range of 100kHz is well suited. A high pulse rate is advantageous as it allows the dimensions of the transformer and smoothing capacitor, C2, to be minimised.

On the primary side, a voltage is applied to the transformer when T1 is on. The positive pulse amplitude is limited by D7 on the secondary side. The drain current of T1 and the transformer current are limited by R1.

During the off period of T1, the transformer's primary current freewheels through D1 and D2. Thus the absolute maximum value for the negative pulse amplitude on the primary winding is equal to the sum of breakdown voltage of zener diode D2 and forward diode drop across D1. At a duty cycle of 50%, this value should be at least as high as the positive pulse amplitude. This allows the primary current to reach zero and thus the magnetic flux in the core to be reset while T1 is off. The maximum off-state drain-source voltage of T1 occurs if the secondary winding of the transformer is left open. It is the sum of supply voltage VP, zener voltage of D2 and forward voltage drop across D1.

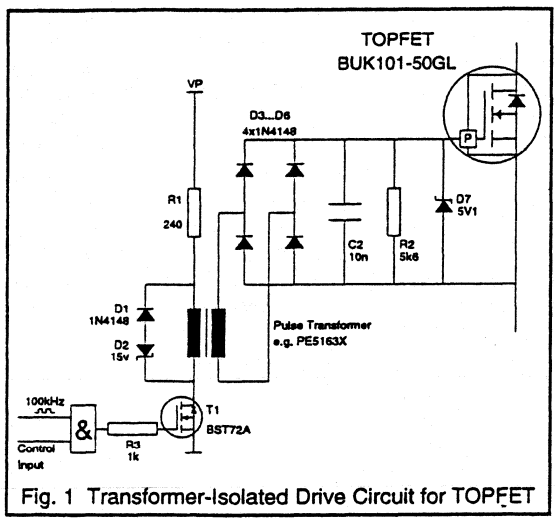


Fig. 1 Transformer-Isolated Drive Circuit for TOPFET

Using a bridge rectifier on the secondary side makes use of both positive and negative pulses to generate the input-to-source voltage V_{IS} for driving the TOPFET. This increases the efficiency. It also reduces the ripple on V_{IS}, therefore the ripple on the load current and hence the electromagnetic noise emission.

The minimum value for V_{IS} is set by the need to have enough voltage for correct operation of the TOPFET's overload protection circuits. The maximum is determined by the breakdown voltage of the ESD protection diode at the input pin. Taking this into account, V_{IS} should be within the range of 4V-6V in the case of the TOPFET type BUK101-50GL. In the given circuit the lower limit of V_{IS} is determined by the minimum supply voltage VP on the primary side, the transformer ratio, and the diode voltage drops at the bridge rectifier. Zener diode D7 ensures that V_{IS} cannot exceed the upper voltage limit.

The time constant of R2 and smoothing capacitor C2 determine the fall time of V_{IS} after the control input at the primary side goes low. A fall time significantly longer than that chosen here should be avoided for the following reason.

After a TOPFET has turned off to protect itself, it is latched off so it stays in the off-state as long as V_{IS} is high. To reset the TOPFET, V_{IS} must go low. In this circuit this happens when the control input at the primary side goes low, disconnecting the drive pulses from the gate of T1. On the secondary side, this allows C2 to be discharged by R2 and hence V_{IS} to decrease. When V_{IS} has fallen below the protection reset voltage level V_{ISR}, the fault latch will reset and an internal transistor, which holds the gate low, will turn off. The gate voltage will now rise to the C2 voltage and the TOPFET's output MOSFET will conduct again. The MOSFET will be fully off when V_{IS} falls below the TOPFET threshold voltage $V_{IS(TO)}$. In the range between V_{ISR} and $V_{IS(TO)}$ (max. 3.5V-1V for the BUK101-50GL) the output MOSFET may conduct while the protection circuits are non-active. For safe reset of a latched TOPFET with a shorted load, this V_{IS}-range must be passed through within a limited time interval. With the dimensioning of R2 and C2 shown in Fig. 1, this time interval is approximately 130 µs. The BUK101-50GL is guaranteed to withstand a hard short circuit for > 300 µs at a battery voltage of 35V and V_{IS}=5V. So the chosen values of R2 and C2 ensure safe turn-off of the TOPFET.

3-pin and 5-pin TOPFET leadforms

Application report

The TOPFET (Temperature and Overload Protected MOSFET) range of devices from Philips Semiconductors is based on conventional vertical power MOSFET technology with the advantages of on-chip protection circuitry. Using this approach the devices are able to achieve the very low values of RDS(on) which are required in applications for automotive and other power circuits. TOPFET devices are currently available in two topologies for maximum compatibility with the requirements of circuit designers.

3-pin TOPFETs TO220	$R_{th j\text{-}mb}$ (K/W)	5-pin TOPFETs SOT263	$R_{th j\text{-}mb}$ (K/W)
BUK100-50GL	3.1	BUK104-50L	3.1
BUK100-50GS	3.1	BUK104-50S	3.1
BUK101-50GL	1.67	BUK105-50L	1.67
BUK101-50GS	1.67	BUK105-50S	1.67
BUK102-50GL	1.0	BUK106-50L	1.0
BUK102-50GS	1.0	BUK106-50S	1.0

Table 1. 3-pin and 5-pin TOPFET type ranges

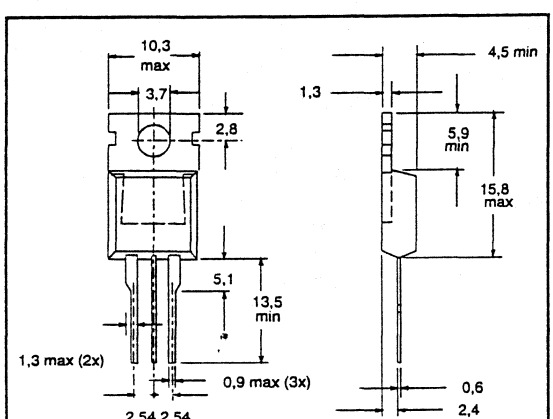


Fig. 1 TO220AB

The 3-pin TOPFETs are assembled in the standard TO220-AB package (Fig. 1), which is also sometimes known as SOT78. The 5-pin versions are assembled in the SOT263 PENTAWATT package (Fig. 2). Depending upon the load and the application the devices can be operated in free air or attached to a heatsink. When using a heatsink the advantage of these outlines lies in the very low thermal impedance which can be achieved. Table 1 shows the thermal resistances for the range of TOPFET devices.

Although these outlines are industry standards, on occasions users have the need to form the leads of the devices to accommodate a variety of assembly requirements. Philips Semiconductors can offer a number of standard pre-formed leadbend options to make the purchase and specification of leadformed devices easier.

These pre-forms satisfy the basic rules concerning the bending and forming of copper leads and ensure that, for example, the bend radius is not less than the thickness of the lead and that there is sufficient material at the base of the plastic moulding to enable the act of pre-forming to take place without damage to the crystal or its die attach and wire-bonding.

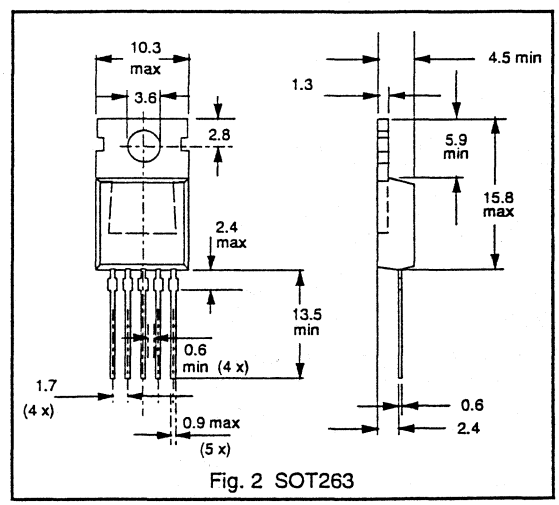


Fig. 2 SOT263

Figure 3 shows leadform option L02 for a TO220 type. A device with this standard leadbend can be ordered by specifying /L02 as the suffix for the device type. For example, a BUK101-50GL with this leadbend is specified by ordering type BUK101-50GL/L02.

In addition to this, there is often the necessity to crop the tab off the device to make a low profile version, when height above the pcb is restricted. Again, without control, there is a risk of fracturing the crystal during this process but Philips Semiconductors can offer this option (SOT226), shown in Fig. 4, which can be ordered by specifying the suffix /CR to the device type number, eg. BUK102-50GS/CR.

For surface mountable TOPFETs, the leadbend option L06 means that the device can be used in applications where a low profile is required. With this option an electrical contact

from the pcb to the tab of the device is possible. The device is shown in Fig. 5 and, for the BUK100-50GS would be specified as the BUK-100-50GS/CRL06.

For 5-pin TOPFET the device is available in the leadbent SOT263 outline as standard (Fig. 6). For the leadform option the device type number is modified by the addition of the suffix P to the SOT263 type name, eg BUK104-50L (SOT263) becomes BUK104-50LP (leadbent SOT263).

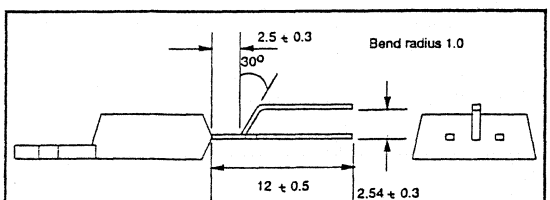


Fig. 3 TO220, L02 leadbend

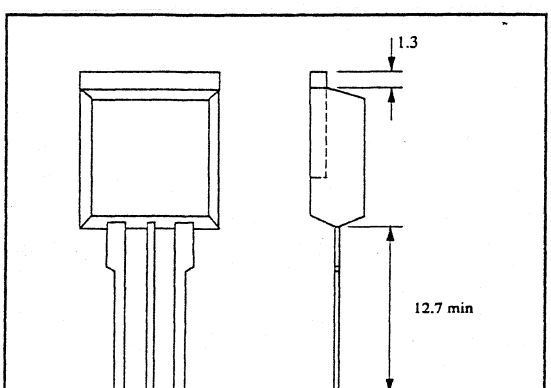


Fig. 4 SOT226

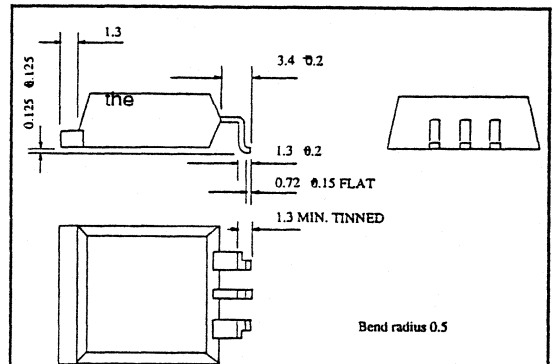


Fig. 5 SOT226, L06 leadbend

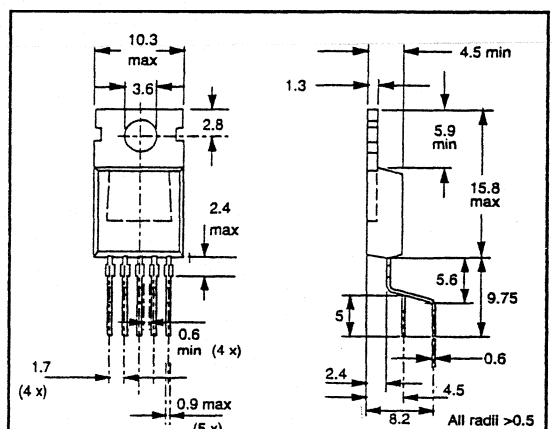


Fig. 6 SOT263, leadbend

TOPFET input voltage

Application report

Low side TOPFET data sheets specify that the voltage between the input and source pins should not be less than 0 V, in other words should not go negative. In many circumstances, sound layout using normal logic gates will ensure that this condition is always satisfied. However, in some situations it is difficult to design a circuit in which this condition is met under all conditions. This section explains the reason for the quoted rating and shows that it is a limit in only a few circumstances. The paper will also illustrate how negative inputs can be generated. Section 5.1.12 shows how negative inputs can be prevented and recommends a simple method of stopping a TOPFET being damaged if negative inputs do occur.

Reason for specification limit

All the pins of a low side TOPFET are protected against ESD. The input pin - the most sensitive pin of a normal MOSFET - is protected by a special diode connected between the input and the source. In the presence of an ESD pulse, this diode conducts and clamps the voltage on the input pin to a safe level.

The diode is formed by an area of n++ in a p+ region which is diffused into the n- epi layer, see Fig. 1. The input pin is connected to the n++ region and then to the rest of the circuits. The p+ region is connected by the metalisation to the source area of the power MOSFET part of the TOPFET. However, the p+ region also connects to the n- epi layer and hence to the drain via the n+ substrate. The ESD diode is formed by the n++ / p+ junction. However, the n++ and p+ diffusions in the n- epi also create a parasitic npn transistor. It is the presence of this transistor which makes the negative input rating necessary.

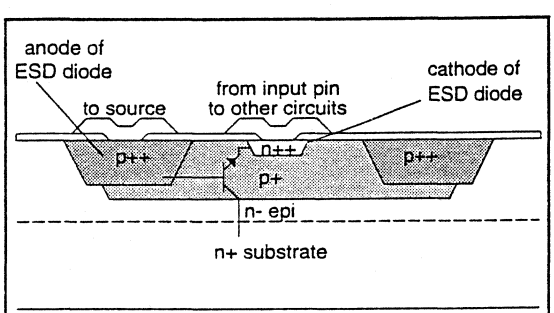


Fig. 1 Cross section of TOPFET ESD diode

With an input potential lower than the source potential, the input acts as an emitter, the drain as a collector and the source as a base, so the potential difference will act as bias for the parasitic transistor. The diffusion concentrations used to create a good ESD protection diode create a transistor with a limited forward SOA. The characteristics of the transistor mean that it can be damaged if its V_{CE} is greater than 30 V when its base is forward biased. For the TOPFET this means that damage could be caused only if the input goes negative while the drain voltage is > 30 V.

It should be noted that the conditions which may damage the transistor assume the impedance of the bias supply is low. If the bias is restricted the limits of SOA are different so the drain voltage needed for damage will be different. In any event at drain voltages < 30 V, a negative input will cause the parasitic transistor to conduct but will not cause damage.

Conditions creating negative input

The most obvious effect of the minimum V_{IS} is to preclude the use of negative drive to speed up turn off. However, this technique is only justifiable in very high frequency circuits and TOPFET is intended for use in DC or low frequency applications, so it is unlikely that this type of drive will be under consideration. The typical TOPFET driver stage will be unipolar using gates or discrete transistors from positive supply rails only. These drivers will turn the TOPFET off either by removing the drive and allowing TOPFET to turn itself off, via its internal pull down resistor, or by pulling the input to zero volts. It would appear, therefore, that negative inputs should not occur, but in some situations and with some circuit configurations they can.

High side circuits

A negative input can be created if an overvoltage transient is applied to an off-state TOPFET being used as a high side switch. A TOPFET will start to conduct if a supply line voltage transient exceeds its clamping voltage. The current now flowing through the TOPFET will also flow through the low side load, raising the source potential above ground. The driver stage may be designed to turn the TOPFET off by pulling the input to ground as in Fig. 2. If it is, then the conditions for harmful negative input have been created - the drain voltage is > 30 V, the input is at ground and the source potential is higher, so the input is negative.

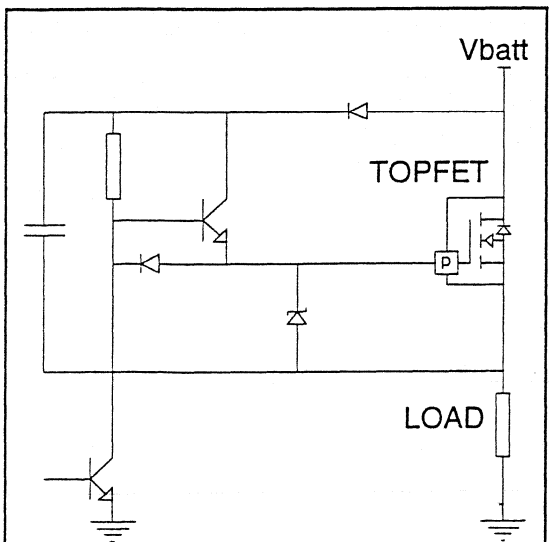


Fig. 2 Driver taking input to ground - high side

Low side circuits

In some circumstances it is possible to create negative input in a low side configuration. In the previous example it was a small current in relatively large resistance that raised the source above ground. The same effect can be created by a large current in the low, but not negligible, resistance of the wiring between the source pin and ground.

Systems are often configured with separate power and signal grounds and it is possible that the driver will be referenced to signal ground, see Fig. 3. In this case the TOPFET input will be pulled to signal ground potential when it is being turned off. The source will be connected to power ground and the common connection between the grounds may a considerable distance from the TOPFET. The resistance of the wiring will be low but even 20 mΩ may be significant if the current is high.

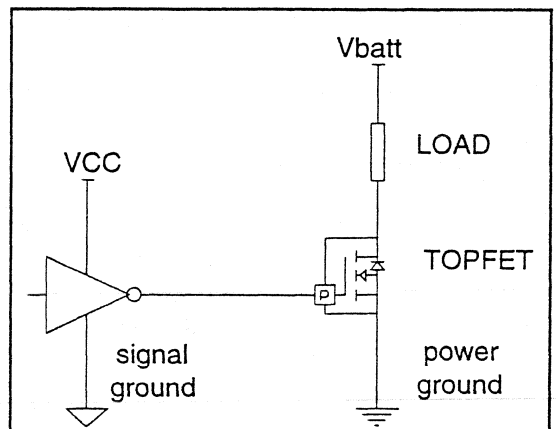


Fig. 3 Low side switch - separate grounds

There are two occasions when a large enough current could be flowing. The first is during the turn-on of a load with a high inrush current, for example a cold incandescent lamp. The second is when the load is shorted out. If the TOPFET turns off while this current is flowing, the energy in the inductance of the wiring from the load to the TOPFET drain would raise the drain voltage, possibly to greater than 30 V. The high current, as high as 60 A, in the source to ground wiring, say 20 mΩ, would raise the source 1.2 V above ground. So, the combination of conditions which may damage a TOPFET have been created.

The circuits and circumstances mentioned in this paper are only examples and other hazardous negative input situations will exist. Methods of preventing negative input and of stopping a TOPFET being damaged, if negative inputs do occur, is presented in section 5.1.12.

Negative input and TOPFET

Application report

Low side TOPFET data sheets specify that the voltage between the input and source pins should not be less than 0 V, ie. should not go negative. This limit is needed to prevent the parasitic transistor, formed by the input ESD protection diode in the n- epi, being damaged in some circumstances. The reason for the limit and the causes of potentially damaging conditions are discussed more fully in section 5.3.11. This section will show how damaging negative inputs can be prevented and recommend a simple method of stopping low side TOPFETs being damaged if negative inputs do occur.

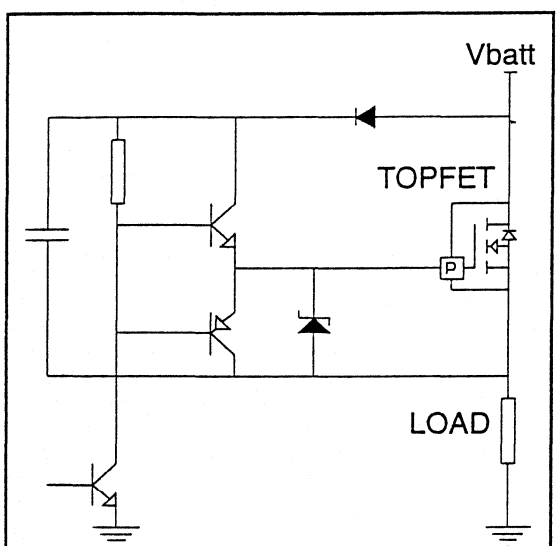


Fig. 1 High side driver taking input to source

Avoiding negative input

Section 5.3.11 gave examples of high and low side drive configurations which could, in some circumstances, generate a potentially damaging negative input. There are two ways to prevent the input from being taken too low. The first is to fit a diode in series with the input pin. The cathode of the diode would be connected to the TOPFET. The diode would conduct while the driver output was high but would turn off and isolate the input pin when the driver tried to pull the input low. The driver would now not be driving the TOPFET off but would be allowing it to turn itself off via its internal input - source resistor.

The second method is to arrange the drive so that it turns the TOPFET off by pulling the input to the source rather than to ground. The circuit shown in Fig. 1 shows a high side drive in which this has been achieved. The TOPFET is turned off by a pnp transistor being turned on and pulling the input to the source.

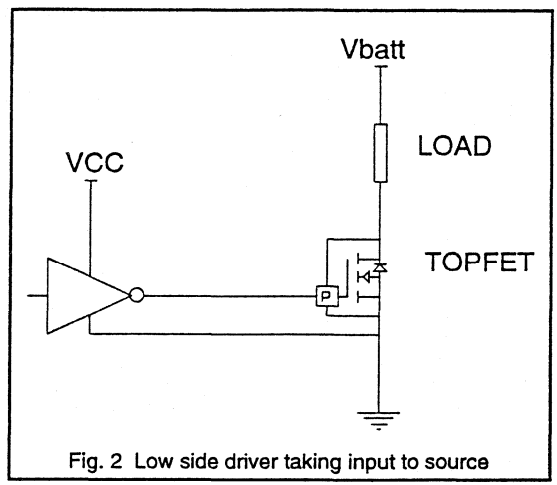


Fig. 2 Low side driver taking input to source

Figure 2 shows a low side drive where the GND pin of the cmos gate is connected as close as possible to the TOPFET source pin. Once more the effect is to turn off the TOPFET by pulling the input to source.

If negative inputs cannot be avoided

The technique of referencing drivers to the source pin helps prevent negative inputs being generated. It is used in most power MOSFET switching situations and should be used with TOPFET wherever possible. If negative inputs cannot be eliminated there are ways of preventing them from causing damage to a TOPFET.

Although published data gives 0 V as the lower limit of V_{IS}, lower values can be acceptable. The V_{IS} limit of 0 V ensures that the SOA of the parasitic transistor associated with the ESD diode is never exceeded. The arrangement shown in Fig. 3. can be used to ensure this. This shows the parasitic npn transistor of the TOPFET and two additional anti-parallel diodes in series with the input.

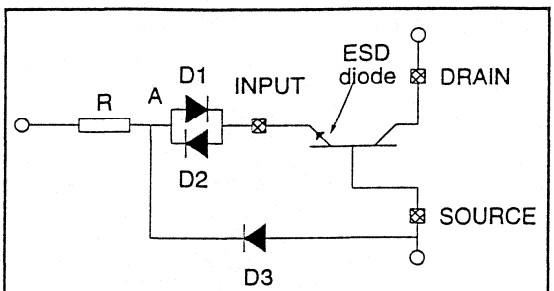


Fig. 3 Equivalent circuit of protected TOPFET input

If the drive voltage goes negative, the diode D1 (see fig. 3) is reverse biased and diodes D2 and D3 are forward biased. The voltage between Source and point A is limited by D3 and the current is limited by R. This voltage is divided between D2 and the base-emitter junction of the ESD diode. The current flowing through the ESD diode's base-emitter junction is therefore negligible and so the SOA of this transistor is not exceeded. This means that all the conditions needed to damage the device can be avoided and the TOPFET is protected against negative input.

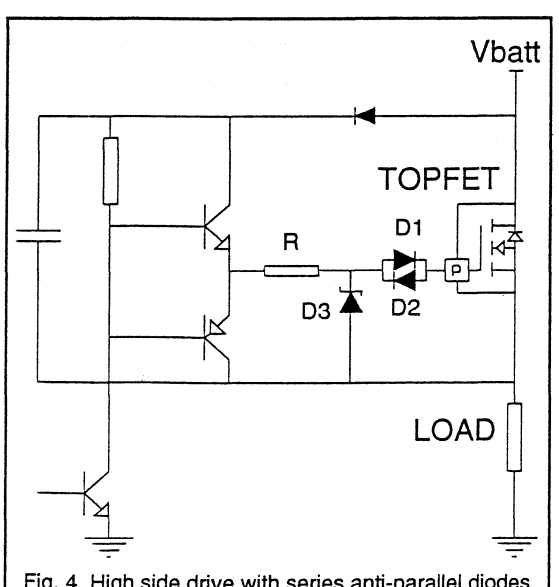


Fig. 4 High side drive with series anti-parallel diodes

In the normal on state, D1 will be forward biased but it will create a voltage drop of about 0.5 V between point A and the TOPFET input. To enable a 3 pin TOPFET to protect itself, its input must be >4.0 V so the designer needs to ensure that the voltage at A is >4.5 V.

During a normal turn-off the gate discharge current will flow through the forward biased D2. No special measures are needed to cope with D2's voltage drop because 0.5 V is well below the TOPFET's threshold voltage so it will be properly turned off if point A is taken to 0 V.

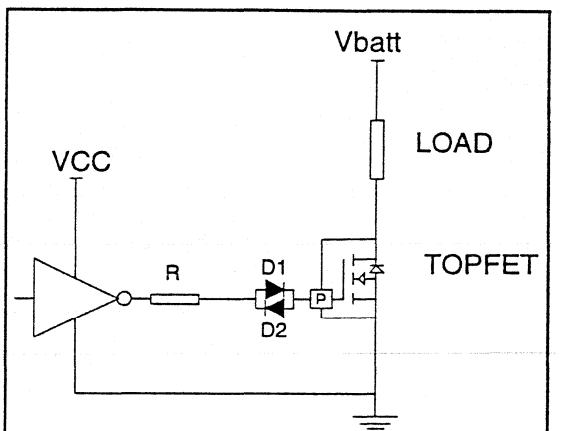


Fig. 5 Low side drive with series anti-parallel diodes

Figure 4 shows the high side drive of Fig. 1 modified to include the series anti-parallel diodes, D1 and D2. D3 is already present in the form of the input voltage limiting zener so the only extra components are the series anti-parallel diodes. A modified low side drive is shown in Fig. 5. Here D1 and D2 are fitted between the output of a cmos gate and the TOPFET input pin. In this circuit, diode limiting is provided by the bipolar parasitic diode inherent in cmos output stages.

Series resistor values

The recommended minimum resistor values are,

Types	Over-voltage transient	Minimum series resistor
3-Pin	< 200 V for 2 ms	50 Ω
3-Pin	< 300 V for 2 ms	300 Ω
5-Pin	< 100 V for 2 ms	200 Ω
5-Pin	< 200 V for 2 ms	1000 Ω
5-Pin	< 300 V for 2 ms	2000 Ω

If the negative voltage between point A and the source is present for a longer period of time than 2 ms then a larger value of series resistor may be required.

Switching inductive leads with TOPFET

Application report

If there is current flowing in the coil of a solenoid or a relay then there is energy stored in the inductance. At turn-off this energy has to be removed from the coil and dissipated somewhere. During this process, an extremely high voltage will be generated unless measures are taken to limit it. This voltage can lead to breakdown and, beyond a certain energy level, damage to the switching transistor. Common methods of controlling this voltage are a freewheel diode in parallel with the inductor or a suppressor diode in parallel with the switching transistor.

A TOPFET with its overvoltage clamping feature can save these extra elements, provided that its limiting values are not exceeded during the turn-off procedure. This section shows a simplified method of estimating the dissipated energy and the junction temperature rise in a TOPFET at inductive turn-off. The equations given here are first order approximations. They act as an aid in determining the need for an external freewheel or suppressor element.

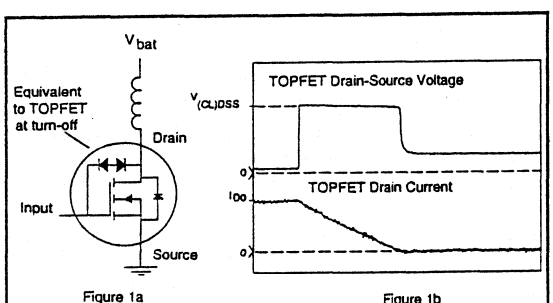


Fig. 1 TOPFET. Switching an inductive load

TOPFET behaviour

Figure 1 shows an equivalent circuit diagram and the shapes of drain current I_D and drain-source voltage V_{DS} versus time for a TOPFET switching an inductor. The overvoltage clamp feature of TOPFET is represented by a zener diode that drives the output power MOSFET into conduction if V_{DS} rises too high. In this state the TOPFET acts as an active clamp element, limiting its own V_{DS} to typically 60V.

Saving of external overvoltage protection

The TOPFET clamp feature is the only voltage limiting required if the energy associated with turn-off, E_{clamp}, does not increase the TOPFET's junction temperature too far. The following section shows how to estimate E_{clamp}. Limiting values for the energies E_{DSM} for non-repetitive clamping and E_{DRM} for repetitive clamping are stated in the data sheet. E_{DSM} relates to a peak junction temperature of 225°C reached during clamping which is acceptable if it occurs only a few times in the lifetime of a device. Thus E_{DSM} should only be used when deciding on the necessity for external protection against overvoltage transients that occur extremely rarely.

However, when switching inductive loads, absorbing E_{clamp} is a normal condition. So to achieve the best longterm reliability, the peak junction temperature should not exceed 150°C. A method for estimating the peak junction temperature is given later.

In this type of repetitive clamping application, the E_{DRM} rating in the data sheet can be compared with E_{clamp} to give an initial indication of need for external voltage limiting. This initial assessment should be followed by a temperature calculation to find the maximum allowable mounting base temperature and thus the heatsink requirements.

Estimation of clamping energy

The energy stored in the coil of a solenoid valve or a relay with the inductance L at a current I is:

$$E_L = \frac{1}{2} L I^2 \qquad (1)$$

The clamping energy E_{clamp} in the TOPFET during an inductive turn-off follows from equation (1) and the fact that, during clamping, the battery also delivers energy to the TOPFET:

$$E_{clamp} = \frac{1}{2} L I_{DO}^2 \frac{V_{(CL)DSS}}{V_{(CL)DSS} - V_{bat}} \qquad (2)$$

In (2) I_{DO} is the drain current at start of turn-off, $V_{(CL)DSS}$ the TOPFET's typical drain-source clamping voltage, V_{bat} the battery voltage and L the load inductance. Equation (2) assumes an inductor with no resistance. In practice, there will be some resistance, which will dissipate a fraction of E_{clamp}. Therefore, (2) represents a worst case situation.

Estimation of junction temperature

The peak junction temperature during clamping can be estimated by adding the maximum temperature rise ΔT_j to the average junction temperature, T_{j0}.

$$T_{j,pk} = T_{j0} + \Delta T_j \quad (3)$$

Measurements have shown that ΔT_j can be approximated by

$$\Delta T_j = \frac{5}{6} V_{(CL)DSS} \cdot I_{D0} \cdot Z_{th} \quad (4)$$

Where Z_{th} is the transient thermal impedance for a pulse width of $\frac{1}{3}$ of the time in clamping, which, for a coil resistance of zero Ohms, is:

$$t_{clamp} = \frac{L \cdot I_{D0}}{V_{(CL)DSS} - V_{bat}} \quad (5)$$

Average dissipation will make T_{j0} higher than the mounting base temperature T_{mb}, which can be assumed as constant, if the TOPFET is mounted on a heatsink. In repetitive switching applications, both on-state losses and turn-off losses contribute to the average dissipation. So T_{j0} will be:

$$T_{j0} = T_{mb} + \left(E_{clamp} \cdot f + I_{RMS}^2 \cdot R_{DS(ON)}\right) \cdot R_{th,j-mb} \quad (6)$$

In (6) I_{RMS} is the root mean square value of the load current and $R_{DS(ON)}$ is the on-state resistance of the TOPFET. In non repetitive applications, the average dissipation is the on state dissipation so T_{j0} is:

$$T_{j0} = T_{mb} + I_{D0}^2 \cdot R_{DS(ON)} \cdot R_{th,j-mb} \quad (7)$$

If these calculations indicate that the peak junction temperature is less than $T_{j\,max}$, then external voltage limiting is not needed.

Calculation examples

Both examples are carried out for V_{bat}=13 V and a BUK101-50GS with a clamping voltage of 60 V. For calculation of on-state losses, the maximum $R_{DS(ON)}$ at T_j=150°C of 87.5 mΩ is taken.

Example 1: An inductor with L=10 mH is switched off non-repetitively at a dc current I_{D0}=7 A.

(5) gives t_{clamp} = 1.5 ms. The BUK101 data curve indicates a Z_{th} of about 0.28 K/W at $t_{clamp}/3$ = 500 µs. (4) then gives a ΔT_j of about 100 K. It is a non repetitive application so use (7) to find T_{j0}, which indicates that T_j is about 7°C above T_{mb} due to on-state losses. From the ΔT_j and T_{j0} figures it can be inferred:
$T_{j,pk}$ < 150°C for T_{mb} < (150-100-7)°C = 43°C.

Example 2: An inductor with L=3 mH is switched at I_{D0}=4 A and a frequency of 100Hz and a duty cycle of 0.5.

(2) yields a clamp energy of 31 mJ, which is less than the E_{DRM} rating of the BUK101 of 40 mJ so repetitive clamping is allowed. (6) yields that T_{j0} will be about 8 K above T_{mb}. From (4) and (5), ΔT_j can be estimated to be < 30 K. These figures imply that this load can be safely driven if the T_{mb} of the BUK101-50GS is < 112°C.

High side linear drive with TOPFET

Application report

This section describes a complete high side linear drive circuit using a TOPFET. A low side linear TOPFET drive circuit is described in section 5.3.7 and the principal pros and cons of linear versus PWM drivers are discussed there. The most important differences between high and low side linear drives are:

- The high side drive needs a charge pump circuit to provide an input voltage higher than the battery voltage.
- In the high side drive the load provides negative feedback for the output transistor. Therefore, the control loop circuit needed to maintain stability in a low side drive can be saved.

The circuit described in this paper was designed for and tested with a 200W fan motor for cars.

Circuit description

The complete high side linear drive circuit can be split up into two blocks:

- The drive circuit
- The charge pump

Drive circuit

Figure 1 shows the drive circuit. Motor speed is controlled by changing the TOPFET's input voltage and therefore its voltage drop. A 5-pin TOPFET is used because this type allows the protection circuit to be supplied independently of the input. This is necessary because in this application the input-source voltage may become too low to supply the protection circuit of a 3-pin TOPFET.

The TOPFET's input voltage and therefore the speed of the fan motor is determined by potentiometer R5. The TOPFET is operating as a source follower. The inherent negative feedback of this configuration will automatically ensure that the source potential will equal the input potential (minus the gate-source voltage) no matter what current is flowing in the motor.

An increase in motor load will tend to slow the motor reducing its back EMF and creating a demand for extra current. The extra current would increase the voltage drop across the TOPFET, lowering the source potential. Since the input potential has been set, the lower source potential increases the gate-source voltage turning the TOPFET on harder. The voltage drop will now reduce, returning the source - hence motor voltage - to its original value but at a higher current level. All of this means that even without an external feedback network, motor speed is inherently stable, although not absolutely constant, under the full range of motor loads.

Transistor T2 works as a current generator and supplies the protection circuit of the TOPFET. T2 is switchable via transistor T1 and Schottky diode D3. If the potentiometer is in position A, transistors T1 and T2 are switched off allowing R11 to pull the protection supply voltage to 0 V. This feature means the TOPFET, if it has tripped due to over temperature or overload, can be reset by turning the potentiometer to position A.

Position A is also the standby mode. With both transistors switched off, the drive circuit has a very small current consumption. This means that in standby the current consumption of the whole circuit (drive and charge pump) is about 0.3mA.

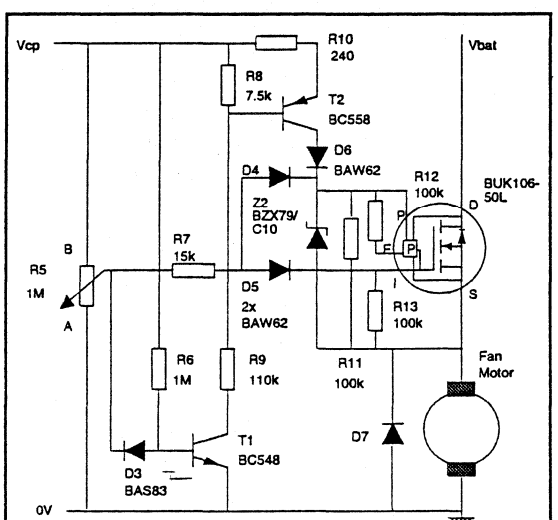


Fig. 1 Drive circuit

TOPFET interface

Negative potentials are not permitted between a TOPFET's protection supply (P), input (I) or flag (F) and its source. This must be considered, especially when designing high side drivers, where the source potential is determined by the load voltage.

If an overvoltage pulse occurs at the supply terminal while the TOPFET is off, the source potential will rise with the overvoltage as soon as the TOPFET's clamp voltage is exceeded. At this time the P,F and I pins should not be clamped with reference to ground, but should be allowed to rise with the source potential. In this circuit this is achieved by diodes D5 and D6 in the feeds to the I,P and F pins.

Zener diode Z2 limits the maximum protection supply and flag voltages to about 10 V and, via D4, the input-source voltage to about 10.6 V. Resistor R7 has a value high enough to allow the TOPFET's internal protection circuits to turn off the device in the event of an over temperature or short circuit load.

Charge pump

Figure 2 shows the charge pump circuit. IC1 works as an astable pulse generator at a frequency of 20 kHz which, together with D1, D2, C4, C5 produces a voltage doubler. The ICM7555 is a type with low current consumption. This is an important feature because the circuit consumes current, even when the driver circuit is in standby mode.

In its normal operating mode, the drive circuit has a typical current consumption of 1.5mA which determines the values of C4 and C5. R4 is included to limit the output current of IC1. The charge pump generates an output voltage of about 22V at a battery voltage of 12.6V. Z1, R1 and C1 will smooth and limit the supply to the circuit and provide protection from voltage spikes.

For correct operation of TOPFET's active protection circuits, sufficient voltage has to be applied to its protection pin. The minimum protection supply voltage for the BUK106-50L is 4V for input voltages Vis up to 6.5V (see data sheet Fig. 17). For the circuit presented and the component values given, this requirement is met with a battery voltage as low as 8 V. If operation at a lower battery voltage is needed then a voltage tripler charge pump could be used in place of the voltage doubler proposed in this paper.

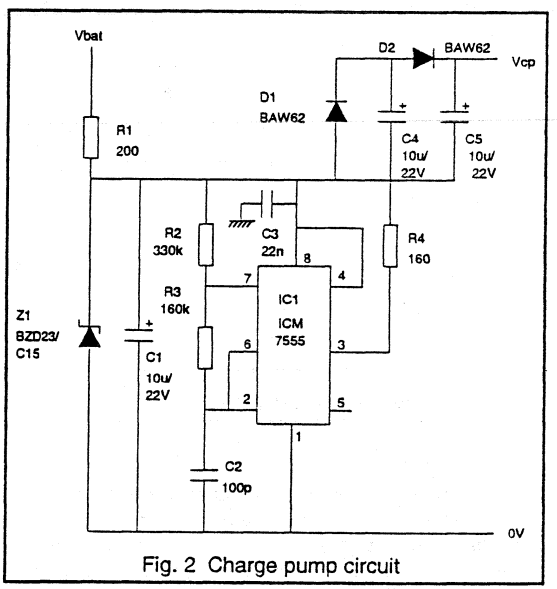


Fig. 2 Charge pump circuit

Driving DC motors with TOPFET

Application report

Examples for motor drive circuits using low side TOPFET have already been given in section 5.3.7: "Linear Control with TOPFET", and section 5.3.8: "PWM Control with TOPFET". This section discusses the characteristics of DC motors that have to be considered when designing a drive circuit with low side TOPFET and gives examples of some basic drive circuits.

Important motor characteristics

The permanent magnet motor is the most common type of motor for driving a wide range of applications including small industrial drives, cooling fans and model cars. Therefore, the following discussions are based on this type. The equivalent circuit of these motors is shown in Fig. 1, where R_A and L_A represent the resistance and inductance of the armature.

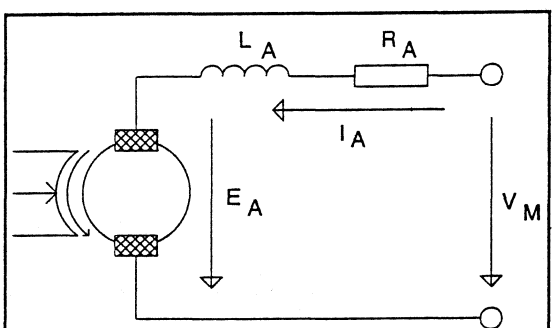


Fig. 1 Equivalent circuit for PM DC motor

Inrush current

Correct operation of some mechanical loads creates a special starting torque requirement for the motor. Since motor torque is proportional to motor current, high starting torque can only be achieved if the inrush current is allowed to be high. The TOPFETs BUK100...BUK106 do not use current limiting techniques to provide overload protection, so the inrush current they can deliver to a motor is limited only by the forward transconductance g_{fs}. To meet extreme starting torque requirements, an 'S'type with 10 V control is to be preferred over an 'L' type with 5 V control because 'S' types can deliver approximately twice the current of 'L' types. Typical currents can be judged from the data sheet $I_{D(SC)}$ in the section TRANSFER CHARACTERISTICS.

Stall current

The stall current of a dc motor is limited by the armature resistance, R_A in Fig. 1, and can reach values of 5-8 times the nominal current. This current will cause overheating in the motor which may damage the winding insulation or demagnetize the stator magnets.

The current would also cause extra dissipation in the driver but a TOPFET, with its over temperature protection, would survive a permanent stall condition. In addition, with careful thermal design, the TOPFET can also be used to prevent damage to the motor.

Inductive kick back at turn-off

The energy stored in the armature inductance, L_A, has to be removed when the motor is turning off. As in the case of inductive loads such as solenoid valves and relay coils, this is usually done by a freewheel diode. Provided that the energy is within its E_{DRM} rating, a TOPFET's overvoltage protection feature can be used instead of a freewheel diode. Section 5.3.13: "Switching Inductive Loads with TOPFET", covers this topic in more detail and gives a simple calculation method to assess the need for a freewheel diode. If overtemperature shutdown due to a stalled motor can occur, a freewheel diode is generally recommended. Without freewheel diode the TOPFET would have to absorb a very high energy at a junction temperature of at least 150 °C.

In the case of pulsed operation of the motor (e.g. pulse width modulation for speed control), the use of a freewheel diode is advisable. Without it, motor current ripple would be higher and the loss in the switching device could be as high as it would be in a linear control circuit.

Special effects of back EMF

Effects at running out

The back EMF, E_A, of a motor is proportional to the rotational speed. When the TOPFET is turned off, the motor acts as a generator and E_A can serve as the feedback signal in a PWM control system.

Although the back EMF voltage of many motors is, during normal running, below its terminal voltage, in some situations and with some motors the peak back EMF can exceed the terminal voltage. Shortly after turn-off these EMF peaks may even exceed the battery voltage plus one diode drop. In this case the EMF can supply current into the battery circuit by forward biasing the TOPFET's Source-Drain diode (see Fig. 2a). As a result of the internal structure of a low side TOPFET, the Source-Drain diode current will create a conduction path from the Input to the Drain. The current through this path can be limited to a safe

value by including a series resistance R_I as shown in Fig. 2a. Recommended values for R_I are 100Ω for 5V drivers and 220Ω for drivers above 6V.

For 5 pin TOPFETs a path is also created from the Protection Supply and Flag pins. In this case, sufficient current limiting is often provided by the resistors that are fitted to connect the Flag and Protection Supply pins to Vcc (see Fig. 2c). The actual resistor values must be determined from consideration of the TOPFET and control circuit data sheets.

Effects of intermittent short circuit

When a TOPFET's short circuit protection has tripped due to a short circuited motor, the motor will continue to turn. In this situation the motor acts as a generator and its current is reversed. The motor will lose rotational energy and, if the short circuit remains long enough, will stop. In practice however, contact sparking can cause intermittent short circuits. In this case the short circuit may be interrupted before the motor has stopped. After the interruption the generator current will continue to flow, forced by the armature inductance L_A. A path for this negative current into the battery is provided via TOPFET's Source-Drain diode. As described in the above section, currents into Input, Protection Supply and Flag terminals should then be limited by means of series resistances.

Besides this, TOPFET's internal circuits are non-active while its Source-Drain diode is forward biased and a previous overload shutdown will not stay latched. As a consequence, a TOPFET that has turned off due to a short circuit across its motor load may turn on again if the short circuit opens before the motor has stopped. This behaviour will not damage the TOPFET. However, Figs 2b and 2c show ways of avoiding it if it is not acceptable.

The first method (Fig. 2b) is to avoid forward biasing of TOPFET's Source-Drain diode by means of a series diode D1. An alternative path for the generator current is provided by zener diode D2. (It is worth noting that interruption of the current path with D1 will be required in applications where reverse battery must not activate the motor.) If the inclusion of a power diode into the motor circuit is not acceptable the alternative shown in Fig. 2c can be used. In this approach the flag signal sets an external latch when the TOPFET is tripped by the short circuit. In this way the TOPFET status is stored even when its Source-Drain diode is forward biased. If the TOPFET is being driven from a microcontroller, the 'latch' function could be implemented in software.

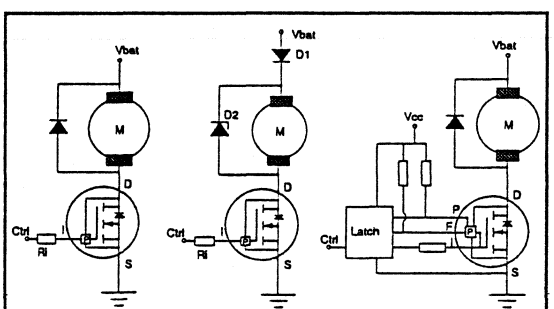


Fig. 2 Basic motor drive circuits with TOPFET

PROTECTION DEVICES

VOLTAGE REGULATOR DIODES

Silicon planar diodes in DO-35 envelopes intended for use as low voltage stabilizers or voltage references. They are available in four series; each series having a different tolerance rating, one series is to the international standardized E24 (± 5%) range, the other three have tolerances of 1%, 2% and 3% on working voltage. Each series consists of 37 types with nominal working voltages ranging from 2,4 V to 75 V.

QUICK REFERENCE DATA

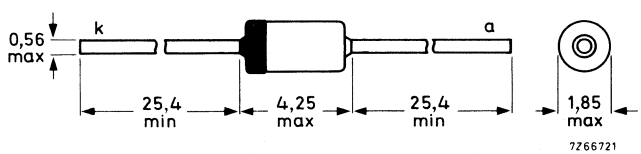
Working voltage range	V_Z	nom.	2,4 to 75 V
Total power dissipation	P_{tot}	max.	500 mW *
Non-repetitive peak reverse power dissipation	P_{ZSM}	max.	30 W
Junction temperature	T_j	max.	200 °C
Thermal resistance from junction to tie-point	$R_{th\ j\text{-}tp}$	=	0,30 K/mW *

* If leads are kept at T_{tp} = 50 °C at 8 mm from body.

MECHANICAL DATA

Dimensions in mm

Fig.1 DO-35 (SOD27).



Cathode indicated by coloured band.
The diodes are type-branded.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Average forward current (averaged over any 20 ms period)	$I_{F(AV)}$	max.	250	mA
Repetitive peak forward current	I_{FRM}	max.	250	mA
Total power dissipation	P_{tot}	max.	500	mW *
		max.	400	mW **
Non-repetitive peak reverse power dissipation $t = 100\ \mu s$; $T_j = 150\ ^oC$	P_{ZSM}	max.	30	W
Storage temperature	T_{stg}	−65 to +	200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to tie-point	$R_{th\ j\text{-}tp}$	=	0,30	K/mW*
From junction to ambient	$R_{th\ j\text{-}a}$	=	0,38	K/mW**

CHARACTERISTICS

$T_j = 25\ ^oC$

Forward voltage $I_F = 10$ mA		V_F	<	0,9	V
Reverse current					
BZX79-.2V4	$V_R = 1$ V	I_R	<	50	μA
.2V7	$V_R = 1$ V	I_R	<	20	μA
.3V0	$V_R = 1$ V	I_R	<	10	μA
.3V3	$V_R = 1$ V	I_R	<	5	μA
.3V6	$V_R = 1$ V	I_R	<	5	μA
.3V9	$V_R = 1$ V	I_R	<	3	μA
.4V3	$V_R = 1$ V	I_R	<	3	μA
.4V7	$V_R = 2$ V	I_R	<	3	μA
.5V1	$V_R = 2$ V	I_R	<	2	μA
.5V6	$V_R = 2$ V	I_R	<	1	μA
.6V2	$V_R = 4$ V	I_R	<	3	μA
.6V8	$V_R = 4$ V	I_R	<	2	μA
.7V5	$V_R = 5$ V	I_R	<	1	μA
.8V2	$V_R = 5$ V	I_R	<	700	nA
.9V1	$V_R = 6$ V	I_R	<	500	nA
.10	$V_R = 7$ V	I_R	<	200	nA
.11 to .13	$V_R = 8$ V	I_R	<	100	nA
.15 to .75	$V_R = 0{,}7\ V_{Znom}$	I_R	<	50	nA

. = A for 1% tolerance range
. = B for 2% tolerance range
. = F for 3% tolerance range
. = C for E24 (± 5%) tolerance range

* If leads are kept at $T_{tp} = 50\ ^oC$ at 8 mm from body.
** In still air at maximum lead length up to $T_{amb} = 50\ ^oC$.

T_j = 25 °C
± 1% tolerance range

BZX79A	working voltage V_Z (V) at I_{Ztest} = 5 mA		differential resistance r_{diff} (Ω) at I_{Ztest} = 5 mA		temperature coefficient S_Z (mV/K) at I_{Ztest} = 5 mA			differential resistance r_{diff} (Ω) at I_Z = 1 mA	
	min.	max.	typ.	max.	min.	typ.	max.	typ.	max.
A2V4	2,37	2,43	70	100	−3,5	−1,6	0	275	600
A2V7	2,67	2,73	75	100	−3,5	−2,0	0	300	600
A3V0	2,97	3,03	80	95	−3,5	−2,1	0	325	600
A3V3	3,26	3,34	85	95	−3,5	−2,4	0	350	600
A3V6	3,56	3,64	85	90	−3,5	−2,4	0	375	600
A3V9	3,86	3,94	85	90	−3,5	−2,5	0	400	600
A4V3	4,25	4,35	80	90	−3,5	−2,5	0	410	600
A4V7	4,65	4,75	50	80	−3,5	−1,4	0,2	425	500
A5V1	5,04	5,16	40	60	−2,7	−0,8	1,2	400	480
A5V6	5,54	5,66	15	40	−2,0	1,2	2,5	80	400
A6V2	6,13	6,27	6	10	0,4	2,3	3,7	40	150
A6V8	6,73	6,87	6	15	1,2	3,0	4,5	30	80
A7V5	7,42	7,58	6	15	2,5	4,0	5,3	30	80
A8V2	8,11	8,29	6	15	3,2	4,6	6,2	40	80
A9V1	9,00	9,20	6	15	3,8	5,5	7,0	40	100
A10	9,90	10,10	8	20	4,5	6,4	8,0	50	150
A11	10,89	11,11	10	20	5,4	7,4	9,0	50	150
A12	11,88	12,12	10	25	6,0	8,4	10,0	50	150
A13	12,87	13,13	10	30	7,0	9,4	11,0	50	170
A15	14,85	15,15	10	30	9,2	11,4	13,0	50	200
A16	15,84	16,16	10	40	10,4	12,4	14,0	50	200
A18	17,82	18,18	10	45	12,4	14,4	16,0	50	225
A20	19,80	20,20	15	55	14,4	16,4	18,0	60	225
A22	21,78	22,22	20	55	16,4	18,4	20,0	60	250
A24	23,76	24,24	25	70	18,4	20,4	22,0	60	250
	at I_{Ztest} = 2 mA		at I_{Ztest} = 2 mA		at I_{Ztest} = 2 mA			at I_Z = 0,5 mA	
A27	26,73	27,27	25	80	21,4	23,4	25,3	65	300
A30	29,70	30,30	30	80	24,4	26,6	29,4	70	300
A33	32,67	33,33	35	80	27,4	29,7	33,4	75	325
A36	35,64	36,36	35	90	30,4	33,0	37,4	80	350
A39	38,61	39,39	40	130	33,4	36,4	41,2	80	350
A43	42,57	43,43	45	150	37,6	41,2	46,6	85	375
A47	46,53	47,47	50	170	42,0	46,1	51,8	85	375
A51	50,49	51,51	60	180	46,6	51,0	57,2	90	400
A56	55,44	56,56	70	200	52,2	57,0	63,8	100	425
A62	61,38	62,62	80	215	58,8	64,4	71,6	120	450
A68	67,32	68,68	90	240	65,6	71,7	79,8	150	475
A75	74,25	75,75	95	255	73,4	80,2	88,6	170	500

T_j = 25 °C

± 2% tolerance range.

BZX79-...	working voltage V_Z (V) at I_{Ztest} = 5 mA		differential resistance r_{diff} (Ω) at I_{Ztest} = 5 mA		temperature coefficient S_Z (mV/K) at I_{Ztest} = 5 mA			differential resistance r_{diff} (Ω) at I_Z = 1 mA	
	min.*	max.*	typ.	max.	min.	typ.	max.	typ.	max.
B2V4	2,35	2,45	70	100	−3,5	−1,6	0	275	600
B2V7	2,65	2,75	75	100	−3,5	−2,0	0	300	600
B3V0	2,94	3,06	80	95	−3,5	−2,1	0	325	600
B3V3	3,23	3,37	85	95	−3,5	−2,4	0	350	600
B3V6	3,53	3,67	85	90	−3,5	−2,4	0	375	600
B3V9	3,82	3,98	85	90	−3,5	−2,5	0	400	600
B4V3	4,21	4,39	80	90	−3,5	−2,5	0	410	600
B4V7	4,61	4,79	50	80	−3,5	−1,4	0,2	425	500
B5V1	5,00	5,20	40	60	−2,7	−0,8	1,2	400	480
B5V6	5,49	5,71	15	40	−2,0	1,2	2,5	80	400
B6V2	6,08	6,32	6	10	0,4	2,3	3,7	40	150
B6V8	6,66	6,94	6	15	1,2	3,0	4,5	30	80
B7V5	7,35	7,65	6	15	2,5	4,0	5,3	30	80
B8V2	8,04	8,36	6	15	3,2	4,6	6,2	40	80
B9V1	8,92	9,28	6	15	3,8	5,5	7,0	40	100
B10	9,80	10,20	8	20	4,5	6,4	8,0	50	150
B11	10,80	11,20	10	20	5,4	7,4	9,0	50	150
B12	11,80	12,20	10	25	6,0	8,4	10,0	50	150
B13	12,70	13,30	10	30	7,0	9,4	11,0	50	170
B15	14,70	15,30	10	30	9,2	11,4	13,0	50	200
B16	15,70	16,30	10	40	10,4	12,4	14,0	50	200
B18	17,60	18,40	10	45	12,4	14,4	16,0	50	225
B20	19,60	20,40	15	55	14,4	16,4	18,0	60	225
B22	21,60	22,40	20	55	16,4	18,4	20,0	60	250
B24	23,50	24,50	25	70	18,4	20,4	22,0	60	250
	at I_{Ztest} = 2 mA		at I_{Ztest} = 2 mA		at I_{Ztest} = 2 mA			at I_Z = 0,5 mA	
B27	26,50	27,50	25	80	21,4	23,4	25,3	65	300
B30	29,40	30,60	30	80	24,4	26,6	29,4	70	300
B33	32,30	33,70	35	80	27,4	29,7	33,4	75	325
B36	35,30	36,70	35	90	30,4	33,0	37,4	80	350
B39	38,20	39,80	40	130	33,4	36,4	41,2	80	350
B43	42,10	43,90	45	150	37,6	41,2	46,6	85	375
B47	46,10	47,90	50	170	42,0	46,1	51,8	85	375
B51	50,00	52,00	60	180	46,6	51,0	57,2	90	400
B56	54,90	57,10	70	200	52,2	57,0	63,8	100	425
B62	60,80	63,20	80	215	58,8	64,4	71,6	120	450
B68	66,60	69,40	90	240	65,6	71,7	79,8	150	475
B75	73,50	76,50	95	255	73,4	80,2	88,6	170	500

*When the real value is beyond this limit it is regulated as acceptable when it is within the 2% tolerance range.

T_j = 25 °C
± 3% tolerance range

BZX79	working voltage V_Z (V) at I_{Ztest} = 5 mA		differential resistance r_{diff} (Ω) at I_{Ztest} = 5 mA		temperature coefficient S_Z (mV/K) at I_{Ztest} = 5 mA	leakage current I_R at V_R	
	min.	max.	typ.	max.	typ.	μA	V
F2V4	2,33	2,47	70	100	−1,6	50	1
F2V7	2,62	2,78	75	100	−2,0	20	1
F3V0	2,91	3,09	80	100	−2,1	10	1
F3V3	3,20	3,40	85	100	−2,4	5	1
F3V6	3,49	3,71	85	100	−2,4	5	1
F3V9	3,78	4,02	85	100	−2,5	3	1
F4V3	4,17	4,43	80	100	−2,5	3	1
F4V7	4,56	4,84	50	100	−1,4	3	2
F5V1	4,95	5,25	40	80	−0,8	2	2
F5V6	5,43	5,77	15	40	1,2	1	2
F6V2	6,01	6,39	6	30	2,3	3	4
F6V8	6,60	7,00	6	20	3,0	2	4
F7V5	7,28	7,72	6	20	4,0	1	5
F8V2	7,95	8,45	6	20	4,6	0,7	5
F9V1	8,83	9,37	6	20	5,5	0,5	6
F10	9,70	10,30	8	25	6,4	0,2	7
F11	10,67	11,33	10	25	7,4	0,1	8
F12	11,64	12,36	10	25	8,4	0,1	8
F13	12,61	13,39	10	35	9,4	0,1	8
F15	14,55	15,45	10	40	11,4	0,05	10
F16	15,50	16,50	10	45	12,4	0,05	
F18	17,50	18,50	10	50	14,4	0,05	
F20	19,40	20,60	15	60	16,4	0,05	
F22	21,30	22,70	20	70	18,4	0,05	
F24	23,30	24,70	25	80	20,4	0,05	
	at I_{Ztest} = 2 mA		at I_{Ztest} = 2 mA		at I_{Ztest} = 2 mA	at I_Z = 0,5 mA	
F27	26,20	27,80	25	80	23,4	0,05	0,7
F30	29,10	30,90	30	100	26,6	0,05	0,7
F33	32,00	34,00	35	120	29,7	0,05	0,7
F36	34,90	37,10	35	140	33,0	0,05	0,7
F39	37,80	40,20	40	150	36,4	0,05	0,7
F43	41,70	44,30	45	160	41,2	0,05	0,7
F47	45,60	48,40	50	170	46,1	0,05	0,7
F51	49,50	52,50	60	180	51,0	0,05	0,7
F56	54,30	57,70	70	200	57,0	0,05	0,7
F62	60,10	63,90	80	220	64,4	0,05	0,7
F68	66,00	70,00	90	240	71,7	0,05	0,7
F75	72,80	77,20	95	255	80,2	0,05	0,7

T_j = 25 °C

E24 (± 5%) logarithmic range

BZX79-...	working voltage V_Z (V) at I_{Ztest} = 5 mA		differential resistance r_{diff} (Ω) at I_{Ztest} = 5 mA		temperature coefficient S_Z (mV/K) at I_{Ztest} = 5 mA			differential resistance r_{diff} (Ω) at I_Z = 1 mA	
	min.	max.	typ.	max.	min.	typ.	max.	typ.	max.
C2V4	2,2	2,6	70	100	−3,5	−1,6	0	275	600
C2V7	2,5	2,9	75	100	−3,5	−2,0	0	300	600
C3V0	2,8	3,2	80	95	−3,5	−2,1	0	325	600
C3V3	3,1	3,5	85	95	−3,5	−2,4	0	350	600
C3V6	3,4	3,8	85	90	−3,5	−2,4	0	375	600
C3V9	3,7	4,1	85	90	−3,5	−2,5	0	400	600
C4V3	4,0	4,6	80	90	−3,5	−2,5	0	410	600
C4V7	4,4	5,0	50	80	−3,5	−1,4	0,2	425	500
C5V1	4,8	5,4	40	60	−2,7	−0,8	1,2	400	480
C5V6	5,2	6,0	15	40	−2,0	1,2	2,5	80	400
C6V2	5,8	6,6	6	10	0,4	2,3	3,7	40	150
C6V8	6,4	7,2	6	15	1,2	3,0	4,5	30	80
C7V5	7,0	7,9	6	15	2,5	4,0	5,3	30	80
C8V2	7,7	8,7	6	15	3,2	4,6	6,2	40	80
C9V1	8,5	9,6	6	15	3,8	5,5	7,0	40	100
C10	9,4	10,6	8	20	4,5	6,4	8,0	50	150
C11	10,4	11,6	10	20	5,4	7,4	9,0	50	150
C12	11,4	12,7	10	25	6,0	8,4	10,0	50	150
C13	12,4	14,1	10	30	7,0	9,4	11,0	50	170
C15	13,8	15,6	10	30	9,2	11,4	13,0	50	200
C16	15,3	17,1	10	40	10,4	12,4	14,0	50	200
C18	16,8	19,1	10	45	12,4	14,4	16,0	50	225
C20	18,8	21,2	15	55	14,4	16,4	18,0	60	225
C22	20,8	23,3	20	55	16,4	18,4	20,0	60	250
C24	22,8	25,6	25	70	18,4	20,4	22,0	60	250
	at I_{Ztest} = 2 mA		at I_{Ztest} = 2 mA		at I_{Ztest} = 2 mA			at I_Z = 0,5 mA	
C27	25,1	28,9	25	80	21,4	23,4	25,3	65	300
C30	28,0	32,0	30	80	24,4	26,6	29,4	70	300
C33	31,0	35,0	35	80	27,4	29,7	33,4	75	325
C36	34,0	38,0	35	90	30,4	33,0	37,4	80	350
C39	37,0	41,0	40	130	33,4	36,4	41,2	80	350
C43	40,0	46,0	45	150	37,6	41,2	46,6	85	375
C47	44,0	50,0	50	170	42,0	46,1	51,8	85	375
C51	48,0	54,0	60	180	46,6	51,0	57,2	90	400
C56	52,0	60,0	70	200	52,2	57,0	63,8	100	425
C62	58,0	66,0	80	215	58,8	64,4	71,6	120	450
C68	64,0	72,0	90	240	65,6	71,7	79,8	150	475
C75	70,0	79,0	95	255	73,4	80,2	88,6	170	500

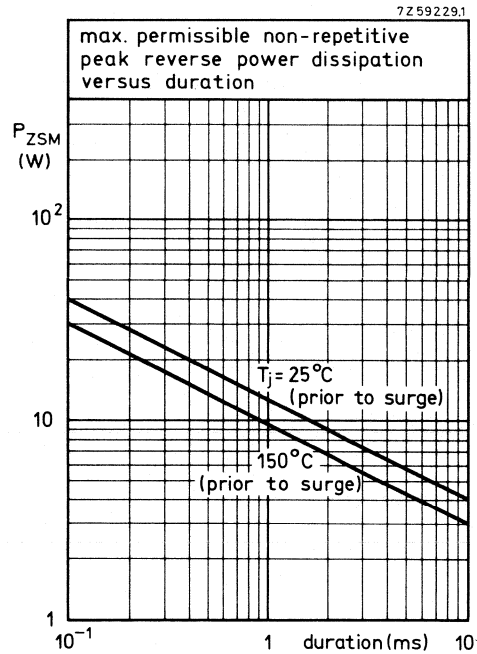

7Z59229.1
max. permissible non-repetitive peak reverse power dissipation versus duration
P_{ZSM} (W)
10^2
10
1
10^{-1}
1
duration (ms)
10
T_j = 25 °C (prior to surge)
150 °C (prior to surge)

Fig. 2.

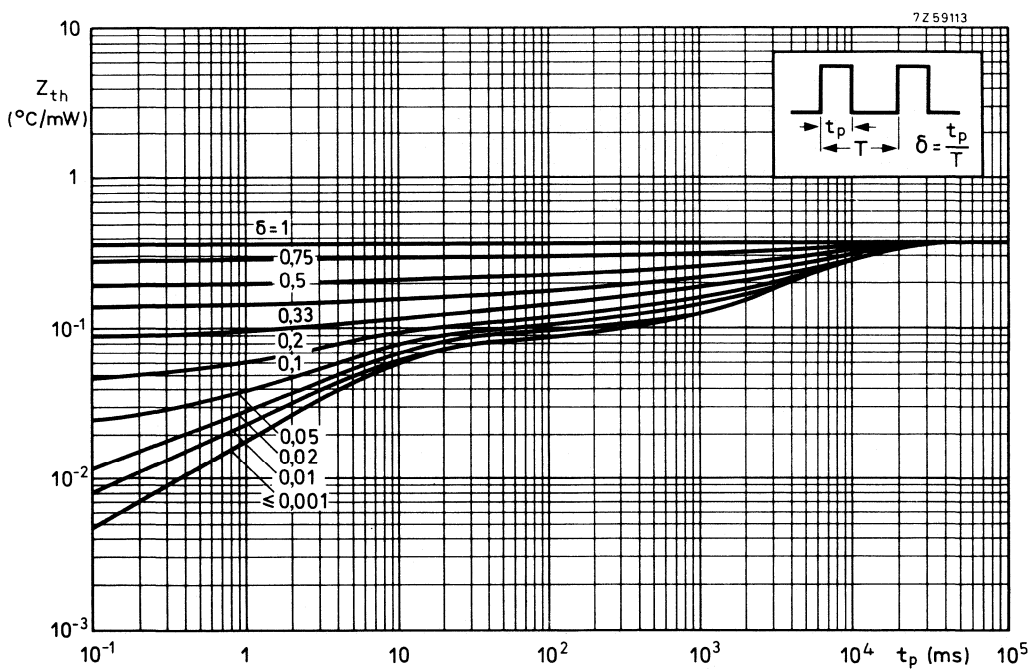

7Z59113
Z_{th} (°C/mW)
10
1
10^{-1}
10^{-2}
10^{-3}
t_p
T
$\delta = \frac{t_p}{T}$
δ = 1
0,75
0,5
0,33
0,2
0,1
0,05
0,02
0,01
≤ 0,001
10^{-1}
1
10
10^2
10^3
10^4
t_p (ms)
10^5

Fig. 3.

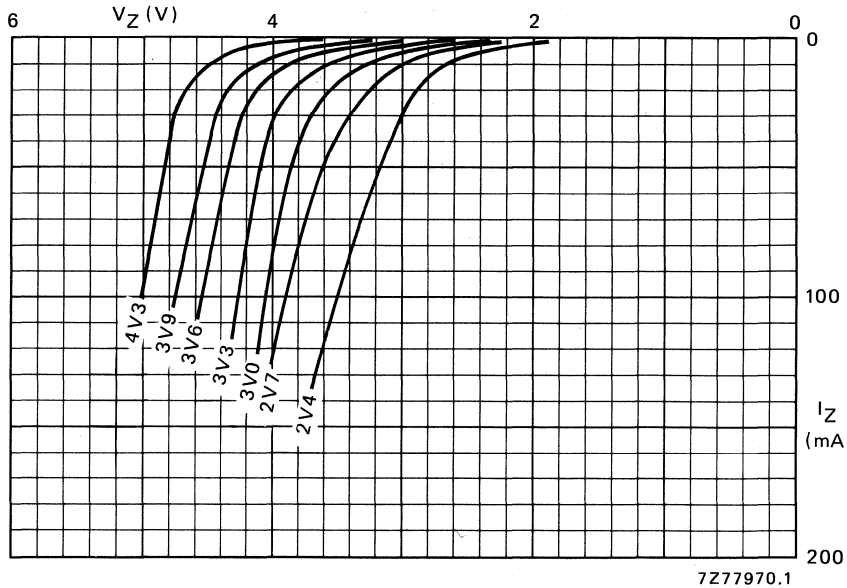


Fig. 4 Static characteristics; typical values; T_{amb} = 25 °C.

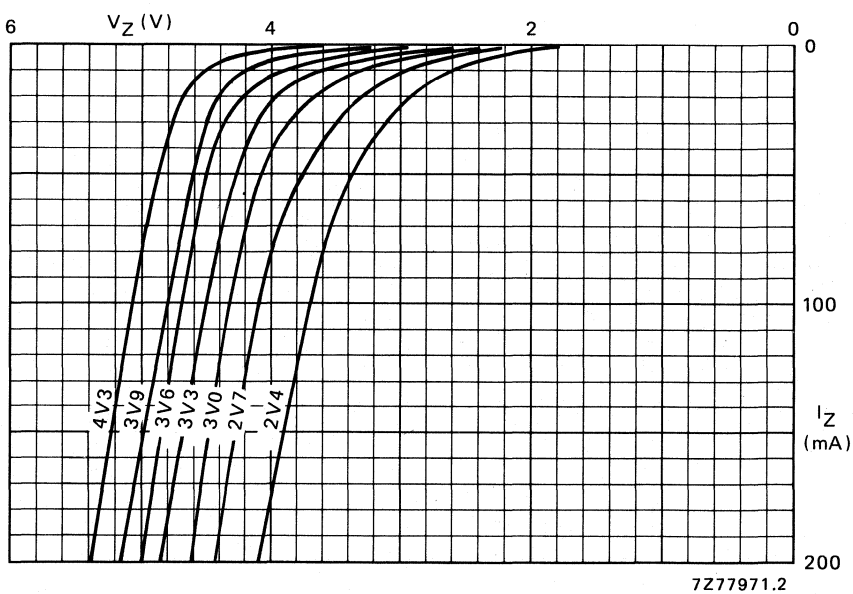


Fig. 5 Dynamic characteristics; typical values; T_j = 25 °C.

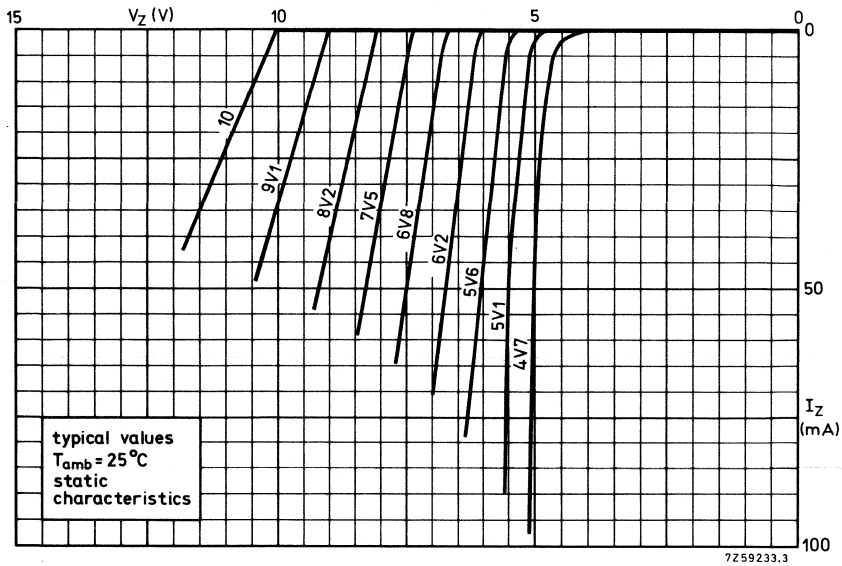

15
V_Z (V)
10
5
0
0
10
9V1
8V2
7V5
6V8
6V2
5V6
5V1
4V7
50
I_Z
(mA)
typical values
T_{amb} = 25°C
static
characteristics
100
7Z59233.3

Fig. 6.

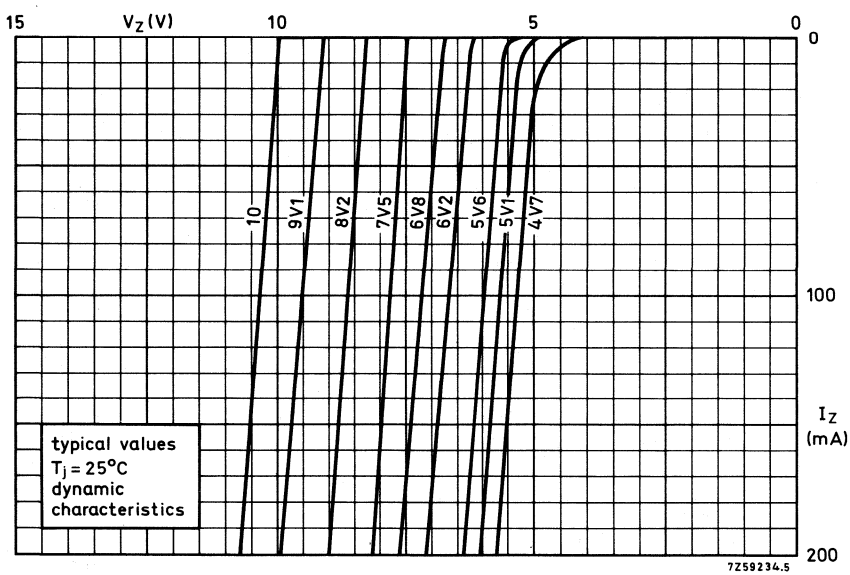

15
V_Z (V)
10
5
0
0
10
9V1
8V2
7V5
6V8
6V2
5V6
5V1
4V7
100
I_Z
(mA)
typical values
T_j = 25°C
dynamic
characteristics
200
7Z59234.5

Fig. 7.

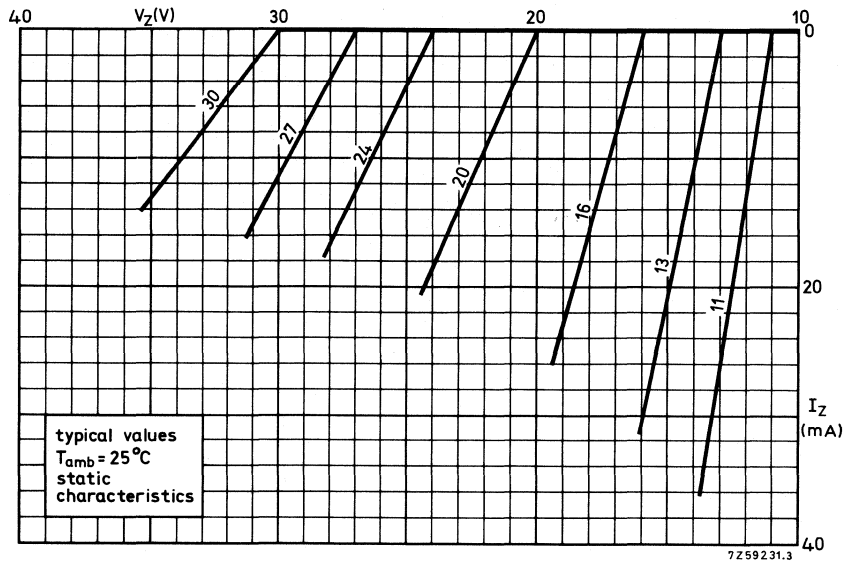

40
V_Z(V)
30
20
10
0
30
27
24
20
16
13
11
20
I_Z
(mA)
typical values
T_{amb} = 25°C
static
characteristics
40
7Z59231.3

Fig. 8.

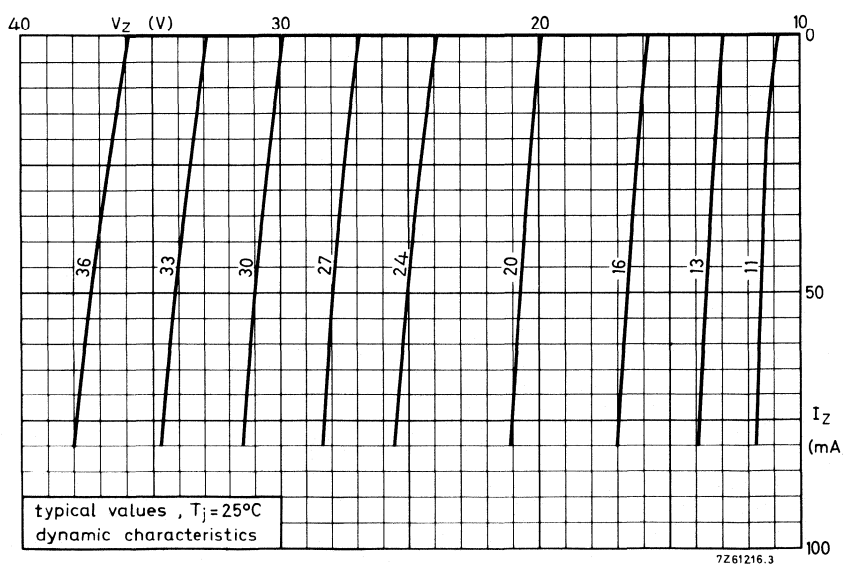

40
V_Z (V)
30
20
10
0
36
33
30
27
24
20
16
13
11
50
I_Z
(mA)
typical values , T_j = 25°C
dynamic characteristics
100
7Z61216.3

Fig. 9.

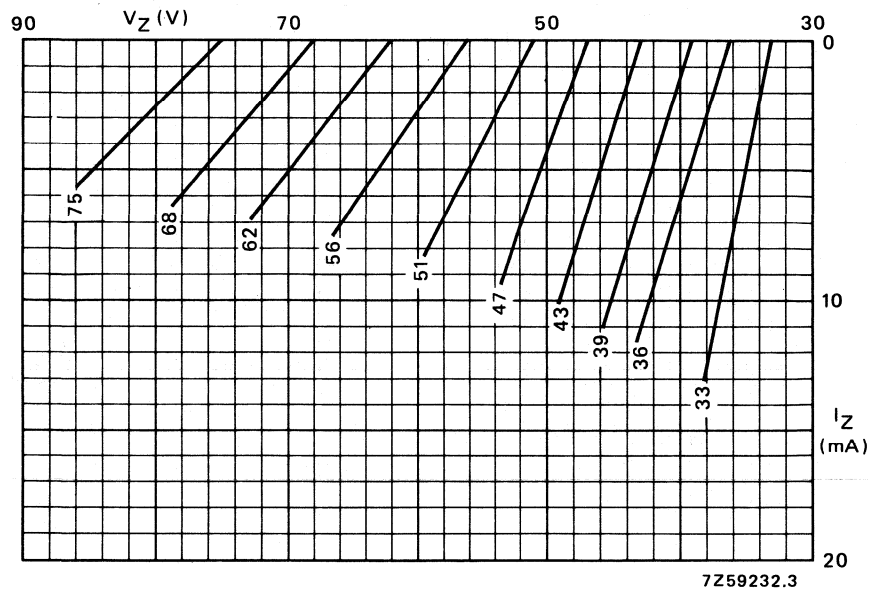


Fig. 10 Static characteristics; typical values; T_{amb} = 25 °C.

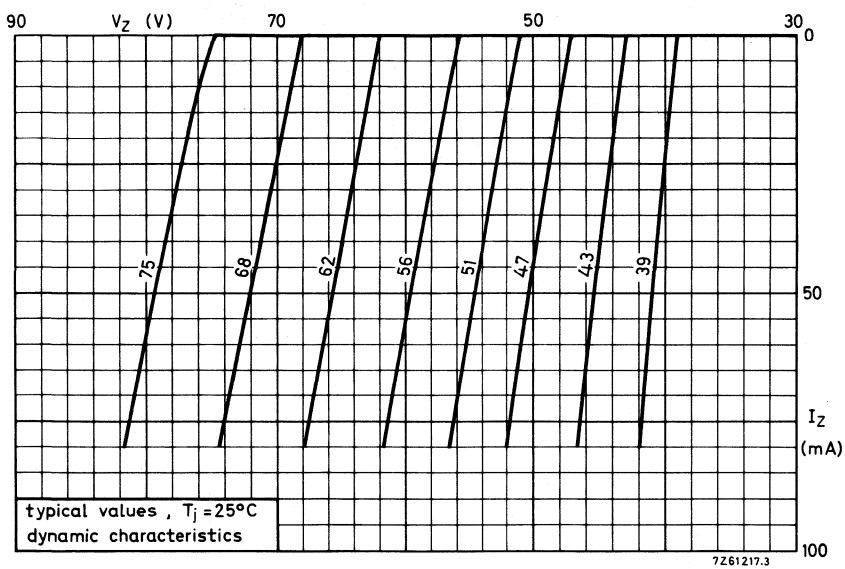


Fig. 11.

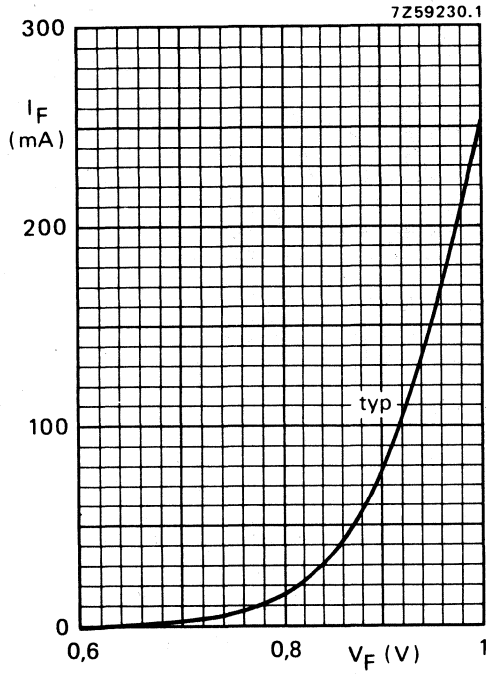


Fig. 12 T_j = 25 °C.

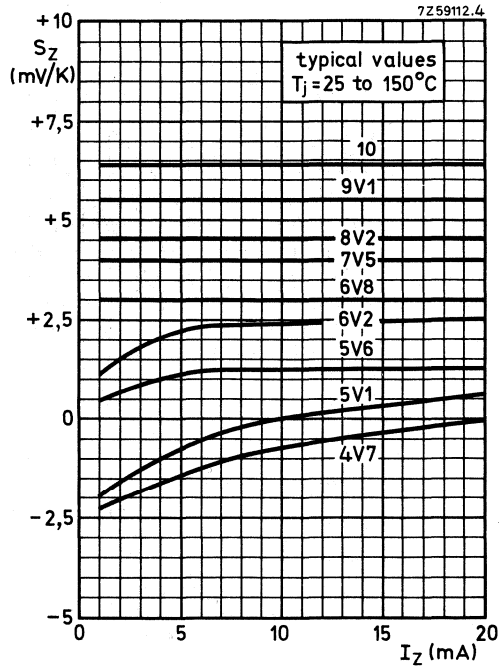


Fig. 13.

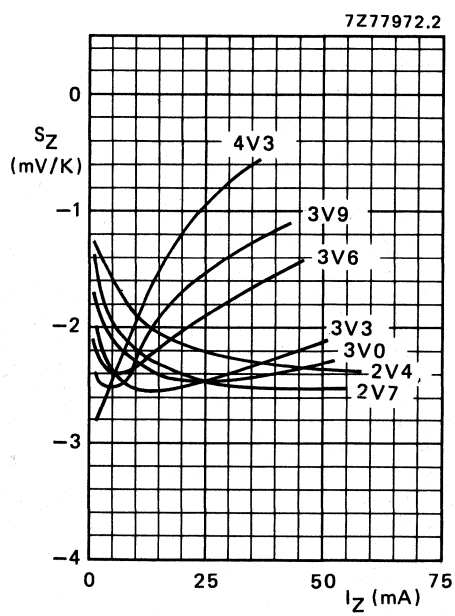


Fig. 14 Typical values; T_j = 25 to 150 °C.

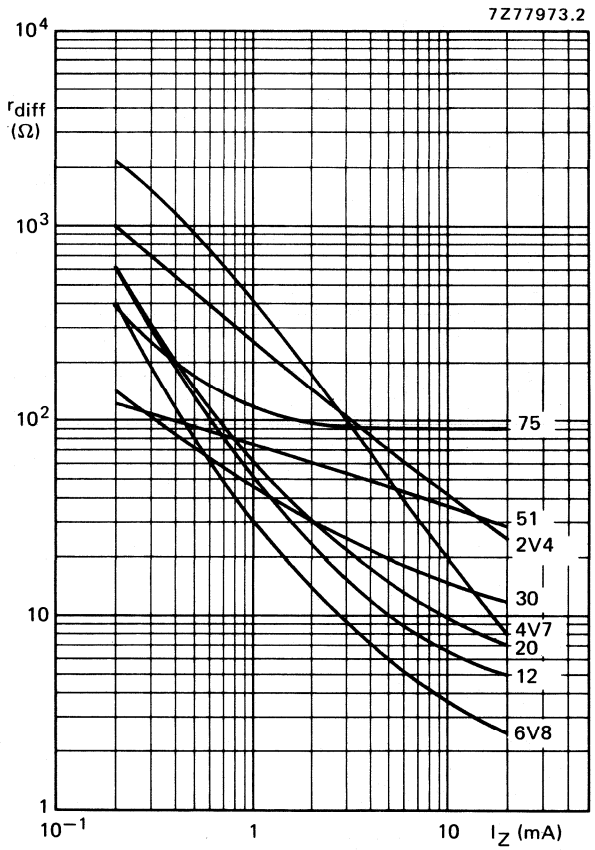


Fig. 15 Typical values; T_j = 25 °C; f = 1 kHz.

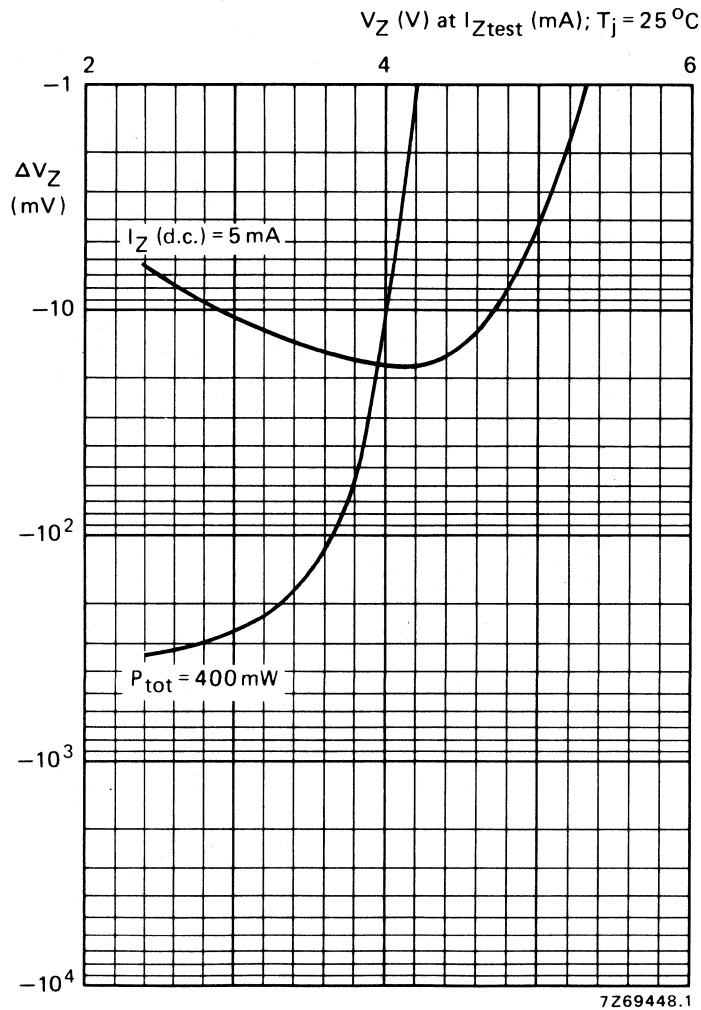


Fig. 16 Typical change of working voltage under operating conditions at T_{amb} = 25 °C.

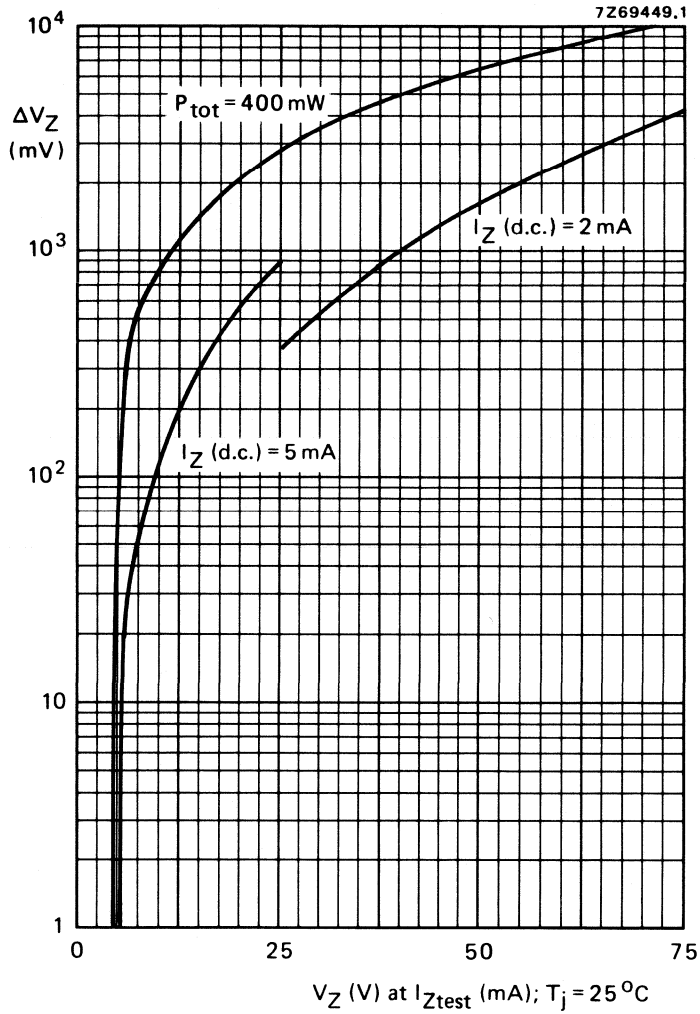


Fig. 17 Typical change of working voltage under operating conditions at T_{amb} = 25 °C.

VOLTAGE REGULATOR DIODES

Silicon planar voltage regulator diodes in hermetically sealed DO-41 glass envelopes intended for stabilization purposes. The series covers the normalized E24 (± 5%) range of nominal working voltages ranging from 3,6 V to 75 V.

QUICK REFERENCE DATA

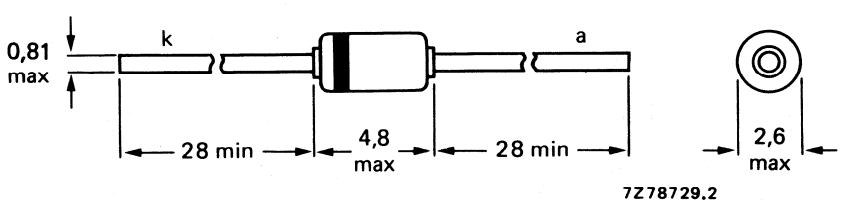
Working voltage range	V_Z	nom.	3,6 to 75 V
Total power dissipation	P_{tot}	max.	1,3 W*
Non-repetitive peak reverse power dissipation t_p = 100 μs; T_j = 25 °C	P_{ZSM}	max.	60 W
Junction temperature	T_j	max.	200 °C
Thermal resistance from junction to tie-point	$R_{th\ j\text{-}tp}$	=	110 K/W*

* If leads are kept at T_{tp} = 55 °C at 4 mm from body.

MECHANICAL DATA

Dimensions in mm

Fig. 1 DO-41 (SOD-66).



Cathode indicated by coloured band.
The diodes are type-branded.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Working current (d.c.)	I_Z	limited by $P_{tot\,max}$	
Non-repetitive peak reverse current t_p = 10 ms; half sine-wave; T_{amb} = 25 °C	I_{ZSM}	see table below	
Repetitive peak forward current	I_{FRM}	max. 250	mA
Total power dissipation (see also Fig. 2)	P_{tot}	max. 1,30 max. 1	W* W**
Non-repetitive peak reverse power dissipation t_p = 100 μs; T_j = 25 °C	P_{ZSM}	max. 60	W
Storage temperature	T_{stg}	−65 to + 200	°C
Junction temperature	T_j	max. 200	°C

THERMAL RESISTANCE

From junction to tie-point	$R_{th\,j\text{-}tp}$	=	110	K/W*
From junction to ambient mounted on a printed-circuit board	$R_{th\,j\text{-}a}$	=	175	K/W**

BZV85–. . . .	Non-repetitive peak reverse current I_{ZSM} (mA) max.
C3V6	2000
C3V9	1950
C4V3	1850
C4V7	1800
C5V1	1750
C5V6	1700
C6V2	1620
C6V8	1550
C7V5	1500
C8V2	1400
C9V1	1340
C10	1200
C11	1100
C12	1000
C13	900
C15	760
C16	700

BZV85–. . .	Non-repetitive peak reverse current I_{ZSM} (mA) max.
C18	600
C20	540
C22	500
C24	450
C27	400
C30	380
C33	350
C36	320
C39	296
C43	270
C47	246
C51	226
C56	208
C62	186
C68	171
C75	161

* If the temperature of the leads at 4 mm from the body are kept up to T_{tp} = 55 °C.

** Measured in still air up to T_{amb} = 25 °C and mounted on printed-circuit board with lead length of 10 mm and print copper area of 1 cm^2 per lead.

CHARACTERISTICS

T_j = 25 °C

Forward voltage at I_F = 50 mA V_F < 1,0 V

	working voltage E24 (± 5%) V_Z (V) at I_{Ztest}			test current I_{Ztest} (mA)	differential resistance r_{diff} (Ω) at I_{Ztest}	temperature coefficient S_Z(mV/K) at I_{Ztest}		reverse current I_R (μA) at V_R	test voltage V_R (V)
BZV85–. . . .	min.	nom.	max.		max.	min.	max.	max.	
C3V6	3,4	3,6	3,8	60	15	−3,5	−1,0	50	1,0
C3V9	3,7	3,9	4,1	60	15	−3,5	−1,0	10	1,0
C4V3	4,0	4,3	4,6	50	13	−2,7	0	5	1,0
C4V7	4,4	4,7	5,0	45	13	−2,0	0,7	3	1,0
C5V1	4,8	5,1	5,4	45	10	−0,5	2,2	3	2,0
C5V6	5,2	5,6	6,0	45	7	0	2,7	2	2,0
C6V2	5,8	6,2	6,6	35	4	0,6	3,6	2	3,0
C6V8	6,4	6,8	7,2	35	3,5	1,3	4,3	2	4,0
C7V5	7,0	7,5	7,9	35	3	2,5	5,5	1	4,5
C8V2	7,7	8,2	8,7	25	5	3,1	6,1	0,7	5,0
C9V1	8,5	9,1	9,6	25	5	3,8	7,2	0,7	6,5
C10	9,4	10	10,6	25	8	4,7	8,5	0,2	7,0
C11	10,4	11	11,6	20	10	5,3	9,3	0,2	7,7
C12	11,4	12	12,7	20	10	6,3	10,8	0,2	8,4
C13	12,4	13	14,1	20	10	7,4	12,0	0,2	9,1
C15	13,8	15	15,6	15	15	8,9	13,6	0,05	10,5
C16	15,3	16	17,1	15	15	10,7	15,4	0,05	11,0
C18	16,8	18	19,1	15	20	11,8	17,1	0,05	12,5
C20	18,8	20	21,2	10	24	13,6	19,1	0,05	14,0
C22	20,8	22	23,3	10	25	16,6	22,1	0,05	15,5
C24	22,8	24	25,6	10	30	18,3	24,3	0,05	17
C27	25,1	27	28,9	8	40	20,1	27,5	0,05	19
C30	28	30	32	8	45	22,4	32,0	0,05	21
C33	31	33	35	8	45	24,8	35,0	0,05	23
C36	34	36	38	8	50	27,2	39,9	0,05	25
C39	37	39	41	6	60	29,6	43,0	0,05	27
C43	40	43	46	6	75	34,0	48,3	0,05	30
C47	44	47	50	4	100	37,4	52,5	0,05	33
C51	48	51	54	4	125	40,8	56,5	0,05	36
C56	52	56	60	4	150	46,8	63,0	0,05	39
C62	58	62	66	4	175	52,2	72,5	0,05	43
C68	64	68	72	4	200	60,5	81,0	0,05	48
C75	70	75	80	4	225	66,5	88,0	0,05	53

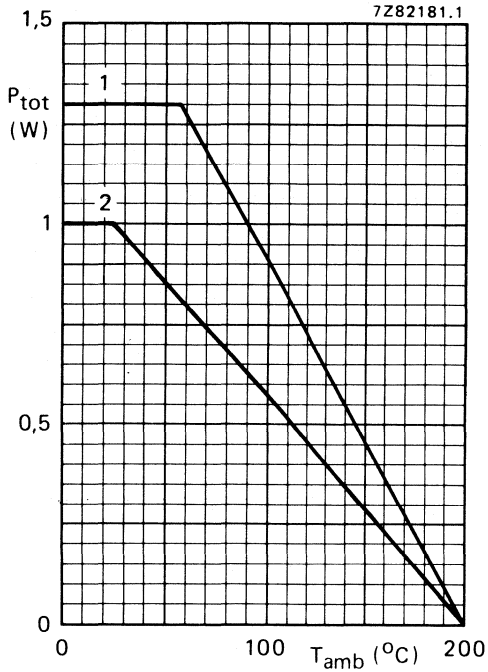


Fig. 2 Maximum permissible power dissipation versus ambient temperature.

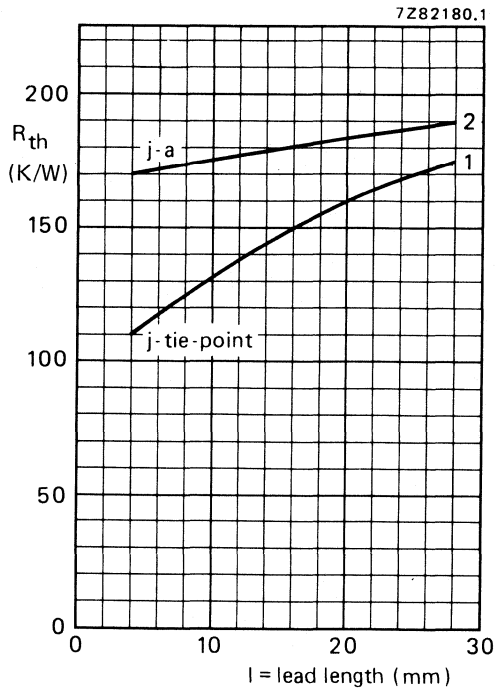
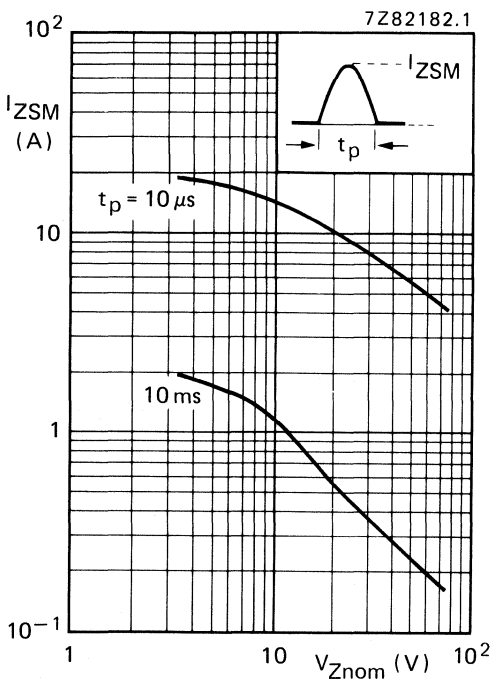


Fig. 3 Thermal resistance versus lead length.



Mounting methods (see Figs 2 and 3)

1. To tie-points (lead length = 4 mm in Fig. 2).
2. Mounted on a printed-circuit board (with lead length of 10 mm in Fig. 2) and print copper area of 1 cm^2 per lead.

Fig. 4 Half sine-wave; T_{amb} = 25 °C.

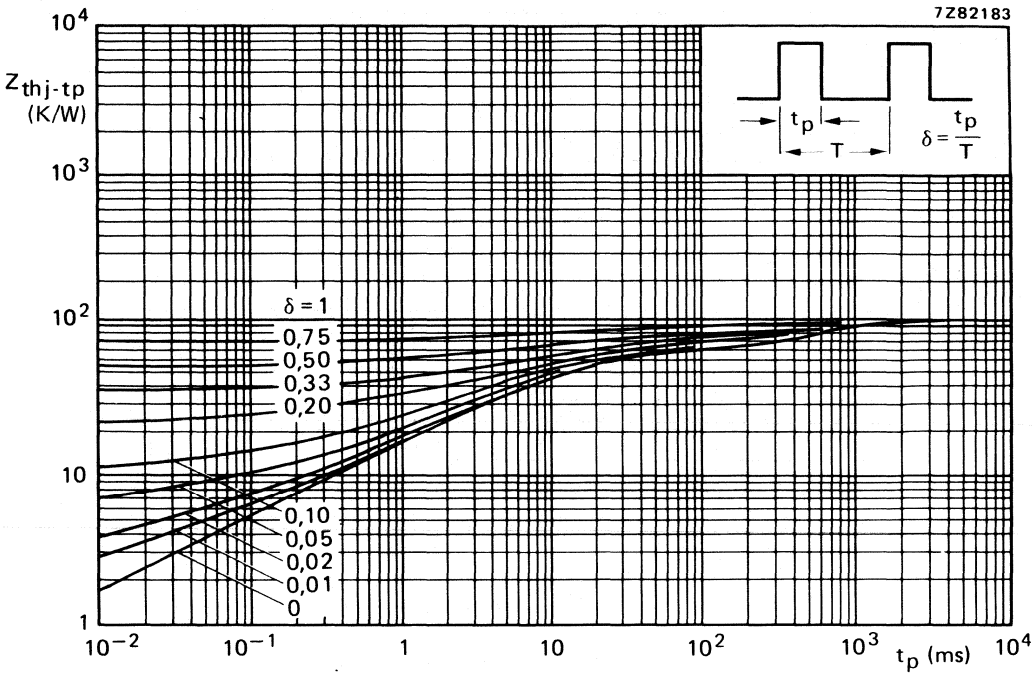


Fig. 5 Thermal impedance from junction to tie-point with a lead length of 4 mm.

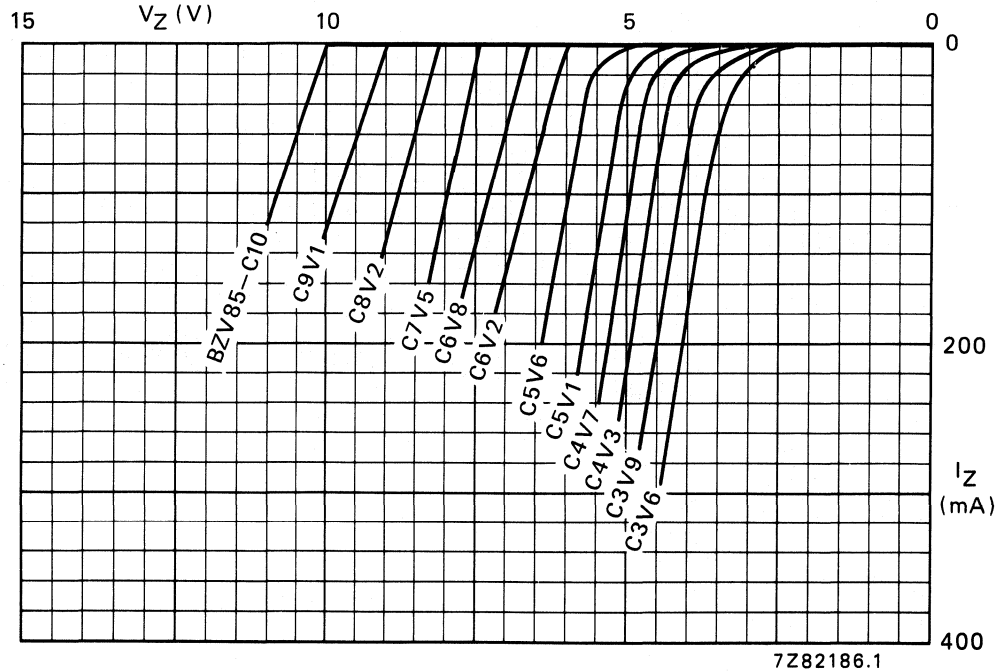


Fig. 6 Static characteristics; typical values; T_{amb} = 25 °C.

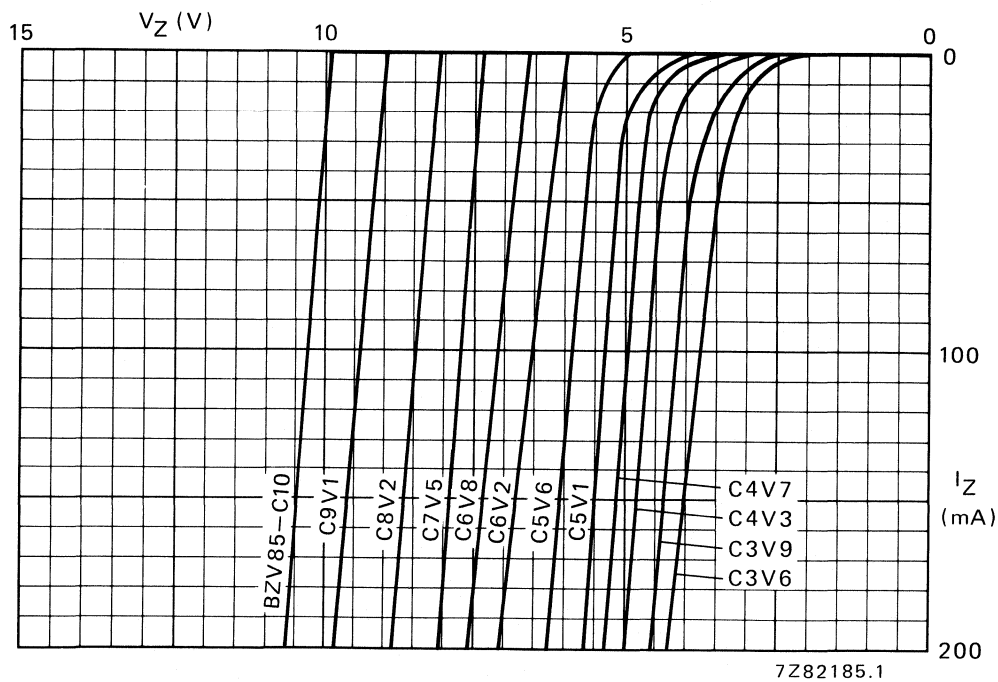


Fig. 7 Dynamic characteristics; typical values; T_j = 25 °C.

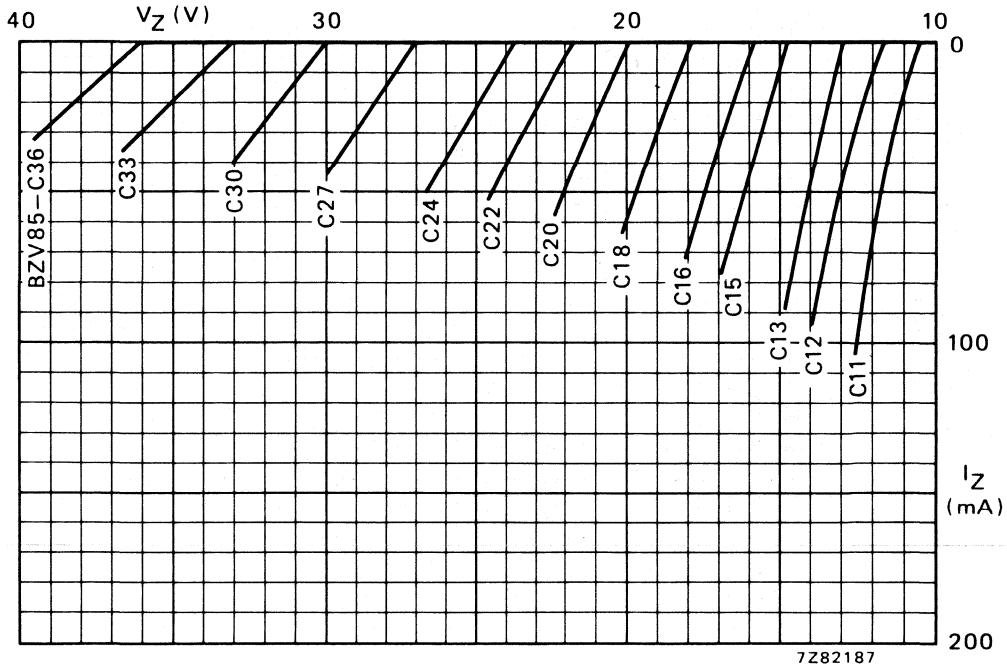


Fig. 8 Static characteristics; typical values; T_{amb} = 25 °C.

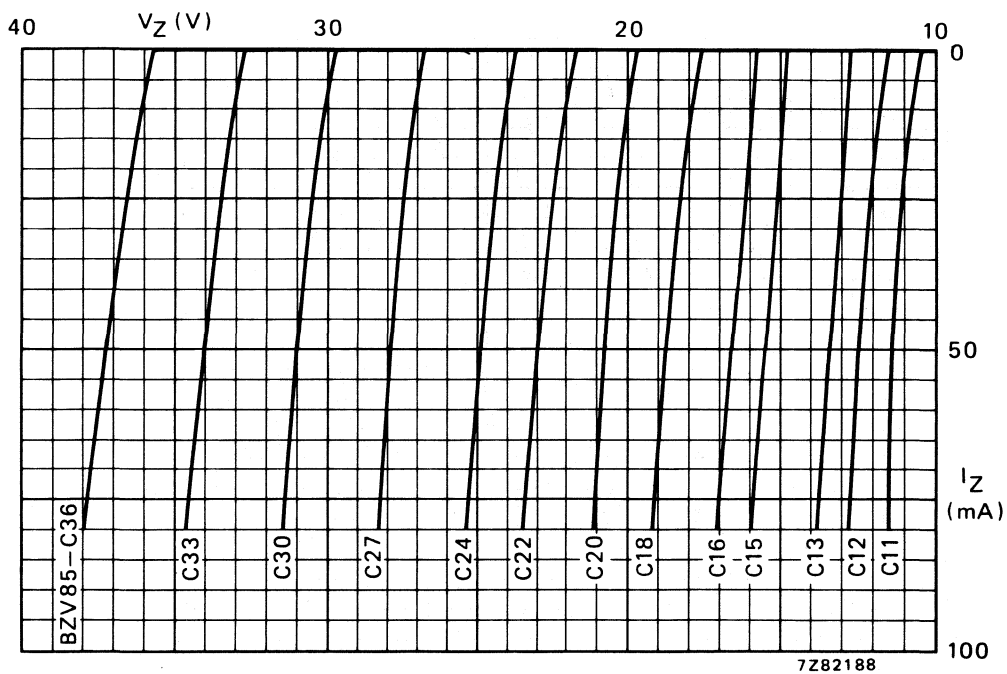


Fig. 9 Dynamic characteristics; typical values; T_j = 25 °C.

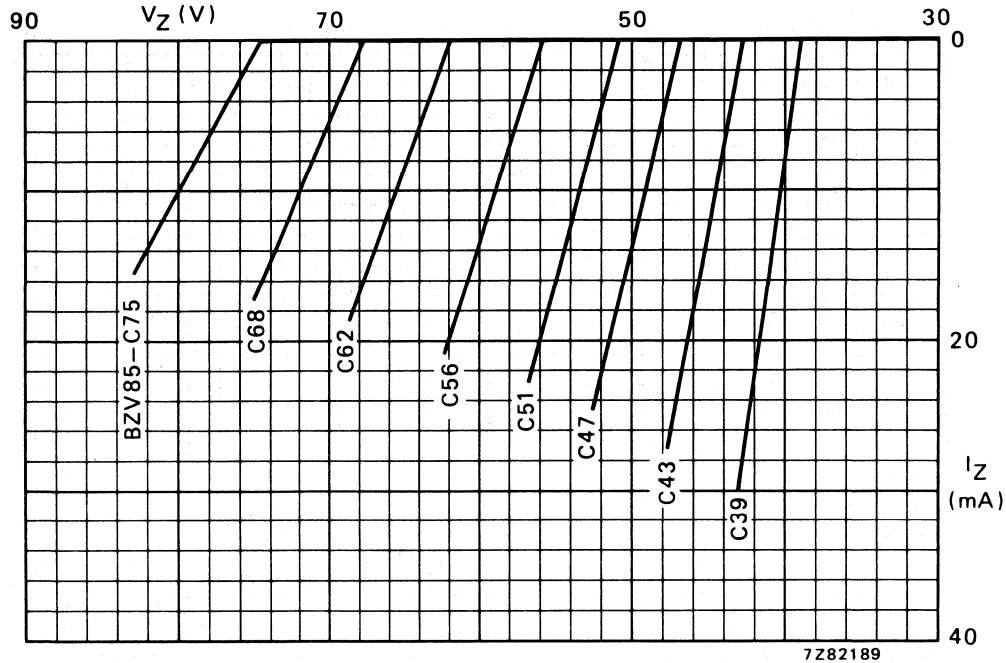


Fig. 10 Static characteristics; typical values; T_{amb} = 25 °C.

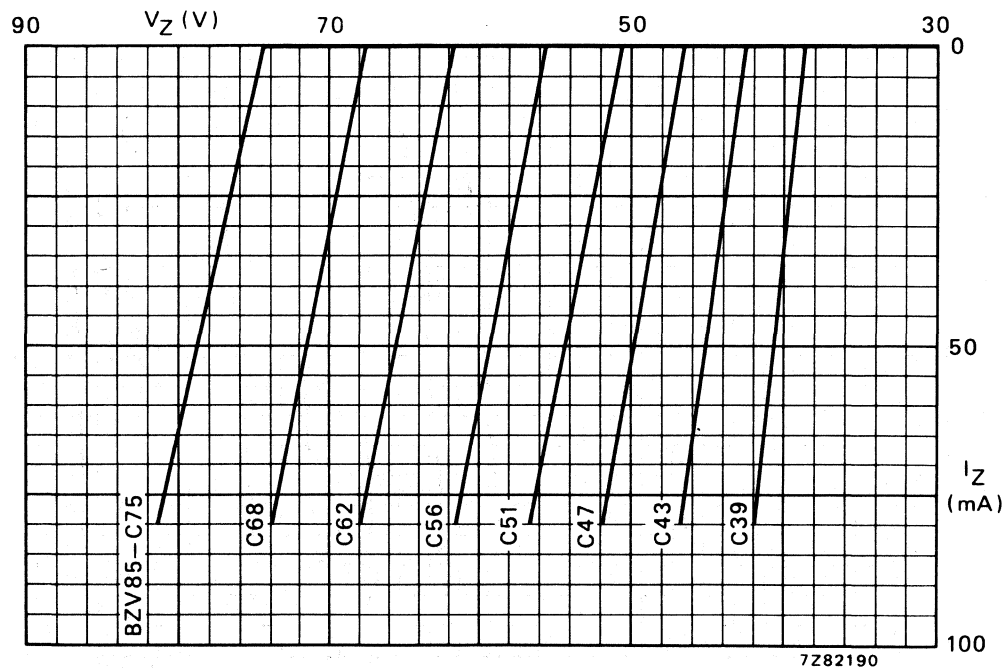


Fig. 11 Dynamic characteristics; typical values; T_j = 25 °C.

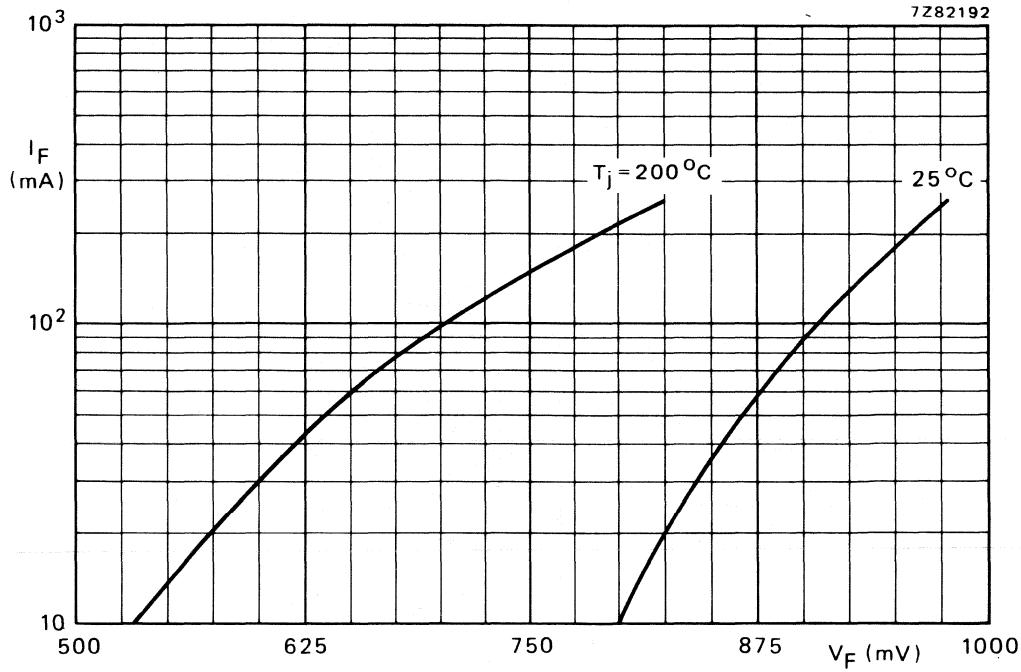


Fig. 12 Typical values.

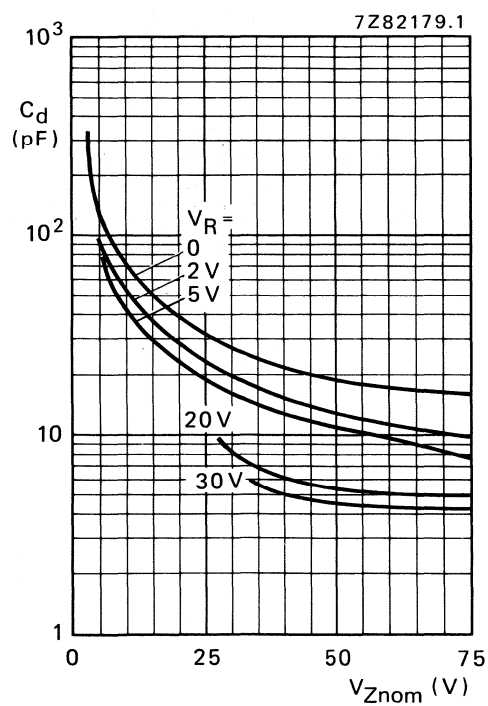


Fig. 13 f = 1 MHz; T_j = 25 °C; typical values.

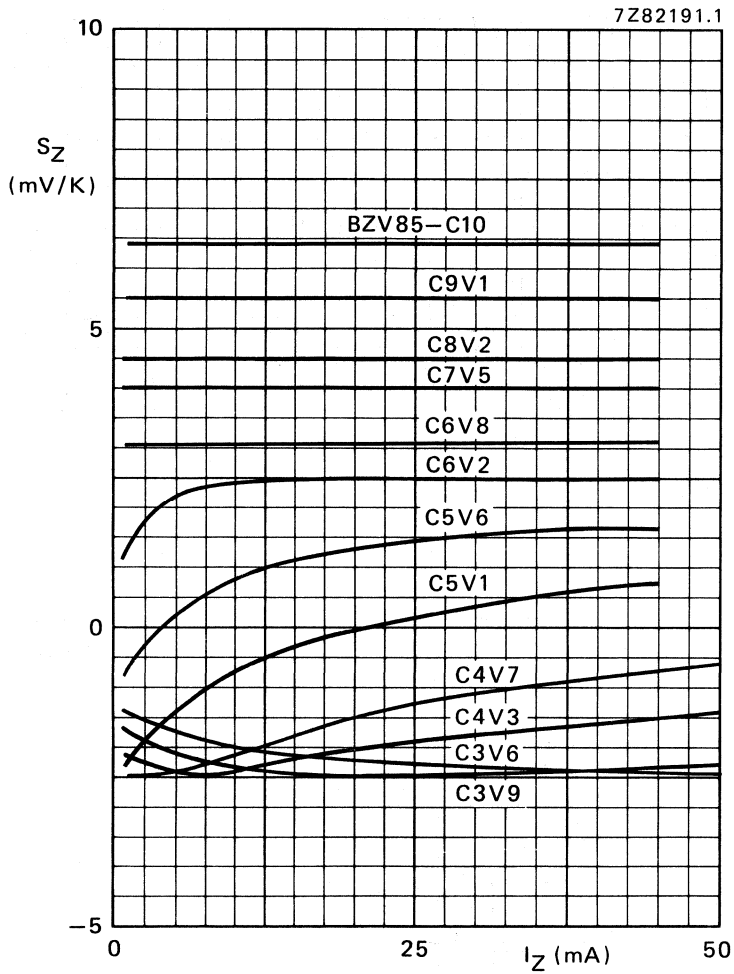


Fig. 14 T_j = 25 °C to 150 °C; typical values.

For types above 7,5 V the temperature coefficient is independent of current and can be read from the CHARACTERISTICS.

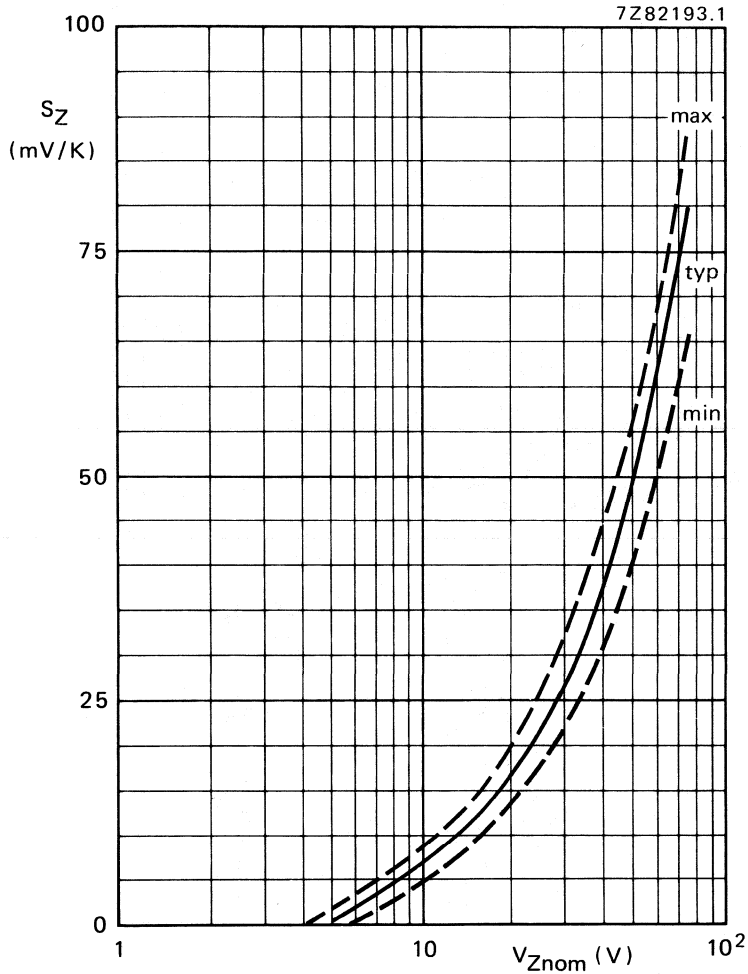


Fig. 15 $I_Z = I_{Ztest}$; T_j = 25 °C to 150 °C.

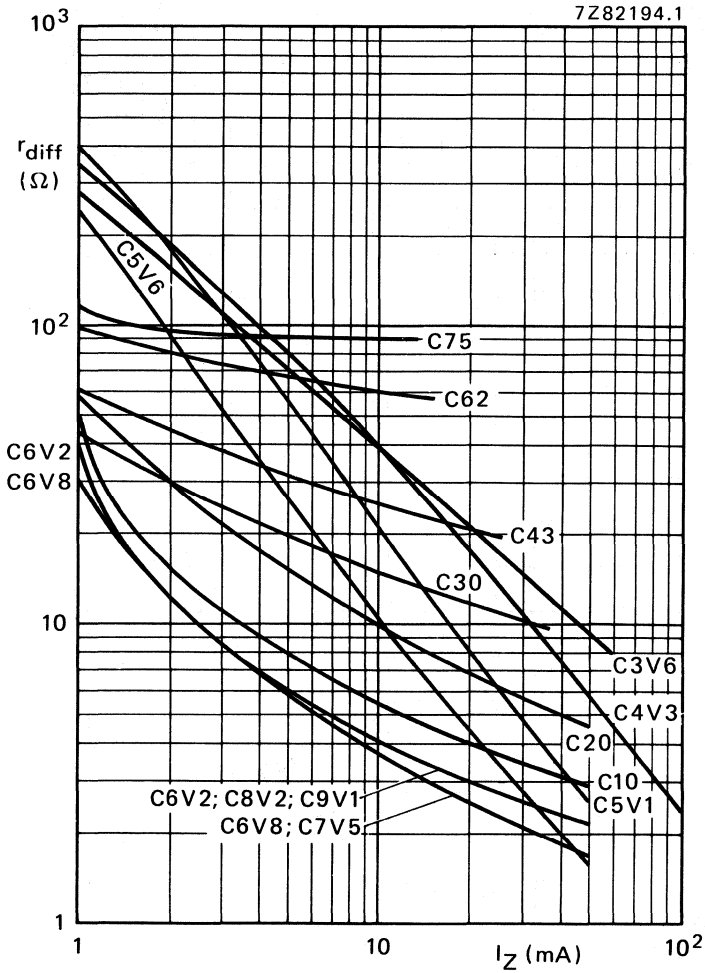


Fig. 16 f = 1 kHz; T_j = 25 °C; typical values.

Voltage regulator diodes BZD23 series

DESCRIPTION

Glass-passivated diodes in hermetically sealed axial-leaded implosion diode (ID) glass envelopes. They are intended for use as voltage regulator and transient suppressor diodes in medium power regulation and transient suppression circuits.

The series consists of BZD23-C3V6 to C6V8 and BZD23-C7V5 to C510, in the normalized E24 range.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	NOM.	MAX.	UNIT
V_Z	voltage regulator working voltage range			
	C3V6 - C6V8	3.6 to 6.8	–	V
	C7V5 - C270	7.5 to 270	–	V
P_{tot}	total power dissipation			
	C3V6 - C6V8	–	2	W
	C7V5 - C510	–	2.5	W
V_R	transient suppressor stand-off voltage			
	C7V5 - C510	6.2 to 430	–	V
P_{RSM}	non-repetitive peak reverse power dissipation	–	300	W

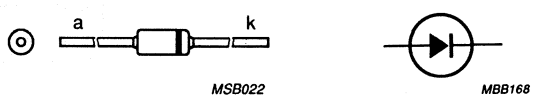


Fig.1 Simplified outline (SOD81) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

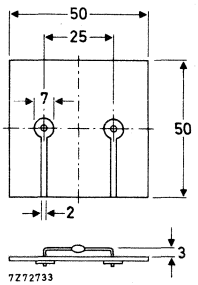
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
P_{tot}	total power dissipation	T_{tp} = 25 °C; lead length 10 mm			
	C3V6 - C6V8		–	2	W
	C7V5 - C510		–	2.5	W
		T_{amb} = 55 °C; PCB mounting; see Fig.2			
	C3V6 - C6V8		–	1	W
	C7V5 - C510		–	1	W
P_{RSM}	non-repetitive peak reverse power dissipation	t_p = 100 µs, square pulse; T_j = 25 °C (prior to surge); see also Fig.7			
	C3V6 - C6V8	see also Fig.8	–	300	W
	C7V5 - C510		–	300	W
		T_j = 25 °C (prior to surge); waveform 10/1000 exponential pulse; see Fig.3			
	C7V5 - C510		–	150	W
T_{stg}	storage temperature range				
	C3V6 - C6V8		–65	200	°C
	C7V5 - C510		–65	175	°C
T_j	junction temperature				
	C3V6 - C6V8		–	200	°C
	C7V5 - C510		–	175	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}tp}$	from junction to tie-point	note 1	
	C3V6 - C6V8		87 K/W
	C7V5 - C510		60 K/W
$R_{th\ j\text{-}a}$	from junction to ambient	note 2	
	C3V6 - C6V8		145 K/W
	C7V5 - C510		120 K/W

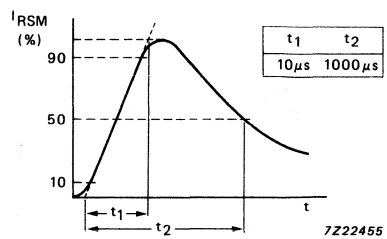
Notes

1. Lead length 10 mm.
2. Mounted on a 1.5 mm thick epoxy-glass printed circuit board; thickness of copper ≥ 40 µm; see Fig.2.



Dimensions in mm.

Fig.2 Printed circuit board mounting.



t_1 = 10 μs.

t_2 = 1000 μs.

Fig.3 Current pulse (in accordance with IEC 60-2, section 6).

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_F	forward voltage	I_F = 0.2 A; note 1		
	C3V6 - C6V8		1.2	V
	C7V5 - C510		1.2	V

Note

1. Measured under pulse conditions to avoid excessive dissipation.

CHARACTERISTICS

When used as voltage regulator diodes.

BZD23 XXXXX	WORKING VOLTAGE			DIFFERENTIAL RESISTANCE		TEMPERATURE COEFFICIENT		TEST CURRENT	REVERSE CURRENT at REVERSE VOLTAGE	
	V_Z (V)			r_{diff} (Ω)		S_Z (%/K)		I_Z (mA)	I_R (μA)	V_R (V)
	MIN.	NOM.	MAX.	TYP.	MAX.	MIN.	MAX.		MAX.	
C3V6	3.4	3.6	3.8	4	8	−0.14	−0.04	100	100	1
C3V9	3.7	3.9	4.1	4	8	−0.14	−0.04	100	50	1
C4V3	4.0	4.3	4.6	4	7	−0.12	−0.02	100	25	1
C4V7	4.4	4.7	5	3	7	−0.10	0	100	10	1
C5V1	4.8	5.1	5.4	3	6	−0.08	−0.02	100	5	1
C5V6	5.2	5.6	6	2	4	−0.04	0.04	100	10	2
C6V2	5.8	6.2	6.6	2	3	−0.01	0.06	100	5	2
C6V8	6.4	6.8	7.2	1	3	0	0.07	100	10	3
C7V5	7	7.5	7.9	1	2	0	0.07	100	50	3
C8V2	7.7	8.2	8.7	1	2	0.03	0.08	100	10	3
C9V1	8.5	9.1	9.6	2	4	0.03	0.08	50	10	5
C10	9.4	10	10.6	2	4	0.05	0.09	50	7	7.5
C11	10.4	11	11.6	4	7	0.05	0.10	50	3	8.2
C12	11.4	12	12.7	4	7	0.05	0.10	50	2	9.1
C13	12.4	13	14.1	5	10	0.05	0.10	50	1	10
C15	13.8	15	15.6	5	10	0.05	0.10	50	1	11
C16	15.3	16	17.1	6	15	0.06	0.11	25	1	12
C18	16.8	18	19.1	6	15	0.06	0.11	25	1	13
C20	18.8	20	21.2	6	15	0.06	0.11	25	1	15
C22	20.8	22	23.3	6	15	0.06	0.11	25	1	16
C24	22.8	24	25.6	7	15	0.06	0.11	25	1	18
C27	25.1	27	28.9	7	15	0.06	0.11	25	1	20
C30	28	30	32	8	15	0.06	0.11	25	1	22
C33	31	33	35	8	15	0.06	0.11	25	1	24
C36	34	36	38	21	40	0.06	0.11	10	1	27
C39	37	39	41	21	40	0.06	0.11	10	1	30
C43	40	43	46	24	45	0.07	0.12	10	1	33
C47	44	47	50	24	45	0.07	0.12	10	1	36
C51	48	51	54	25	60	0.07	0.12	10	1	39
C56	52	56	60	25	60	0.07	0.12	10	1	43
C62	58	62	66	25	80	0.08	0.13	10	1	47
C68	64	68	72	25	80	0.08	0.13	10	1	51
C75	70	75	79	30	100	0.08	0.13	10	1	56
C82	77	82	87	30	100	0.08	0.13	10	1	62

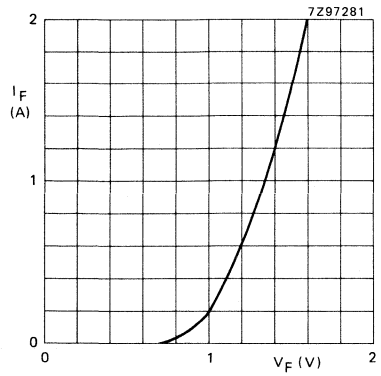
BZD23 XXXXX	WORKING VOLTAGE			DIFFERENTIAL RESISTANCE		TEMPERATURE COEFFICIENT		TEST CURRENT	REVERSE CURRENT at REVERSE VOLTAGE	
	V_Z (V)			r_{diff} (Ω)		S_Z (%/K)		I_Z (mA)	I_R (μA)	V_R (V)
	MIN.	NOM.	MAX.	TYP.	MAX.	MIN.	MAX.		MAX.	
C91	85	91	96	60	200	0.09	0.13	5	1	68
C100	94	100	106	60	200	0.09	0.13	5	1	75
C110	104	110	116	80	250	0.09	0.13	5	1	82
C120	114	120	127	80	250	0.09	0.13	5	1	91
C130	124	130	141	110	300	0.09	0.13	5	1	100
C150	138	150	156	130	300	0.09	0.13	5	1	110
C160	153	160	171	150	350	0.09	0.13	5	1	120
C180	168	180	191	180	400	0.09	0.13	5	1	130
C200	188	200	212	200	500	0.09	0.13	5	1	150
C220	208	220	233	350	750	0.09	0.13	2	1	160
C240	228	240	256	400	850	0.09	0.13	2	1	180
C270	251	270	289	450	1000	0.09	0.13	2	1	200

CHARACTERISTICS

When used as transient suppressor diodes; T_j = 25 °C.

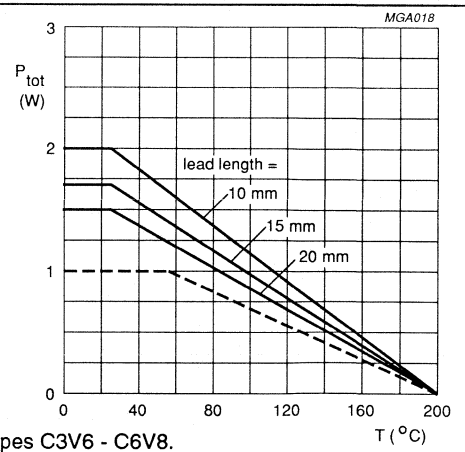
BZD23 XXXXX	CLAMPING VOLTAGE at NON-REPETITIVE PEAK (10/1000 PULSE) REVERSE CURRENT		REVERSE CURRENT AT RECOMMENDED STAND-OFF VOLTAGE	
	$V_{(CL)R}$ (V)	I_{RSM} (A)	I_R (μA)	V_R (V)
	MAX.		MAX.	
C7V5	11.3	13.3	1500	6.2
C8V2	12.3	12.2	1200	6.8
C9V1	13.3	11.3	100	7.5
C10	14.8	10.1	20	8.2
C11	15.7	9.6	5	9.1
C12	17	8.8	5	10
C13	18.9	7.9	5	11
C15	20.9	7.2	5	12
C16	22.9	6.6	5	13
C18	25.6	5.9	5	15
C20	28.4	5.3	5	16
C22	31	4.8	5	18
C24	33.8	4.4	5	20
C27	38.1	3.9	5	22
C30	42.2	3.6	5	24

BZD23 XXXXX	CLAMPING VOLTAGE at NON-REPETITIVE PEAK (10/1000 PULSE) REVERSE CURRENT		REVERSE CURRENT AT RECOMMENDED STAND-OFF VOLTAGE	
	$V_{(CL)R}$ (V)	I_{RSM} (A)	I_R (μA)	V_R (V)
	MAX.		MAX.	
C33	46.2	3.2	5	27
C36	50.1	3	5	30
C39	54.1	2.8	5	33
C43	60.7	2.5	5	36
C47	65.5	2.3	5	39
C51	70.8	2.1	5	43
C56	78.6	1.9	5	47
C62	86.5	1.7	5	51
C68	94.4	1.6	5	56
C75	103.5	1.5	5	62
C82	114	1.3	5	68
C91	126	1.2	5	75
C100	139	1.1	5	82
C110	152	1	5	91
C120	167	0.90	5	100
C130	185	0.81	5	110
C150	204	0.73	5	120
C160	224	0.67	5	130
C180	249	0.60	5	150
C200	276	0.54	5	160
C220	305	0.50	5	180
C240	336	0.45	5	200
C270	380	0.40	5	220
C300	419	0.36	5	240
C330	459	0.33	5	270
C360	498	0.30	5	300
C390	537	0.28	5	330
C430	603	0.25	5	360
C470	655	0.23	5	390
C510	707	0.21	5	430



T_j = 25 °C.

Fig.4 Forward current as a function of forward voltage, typical values.

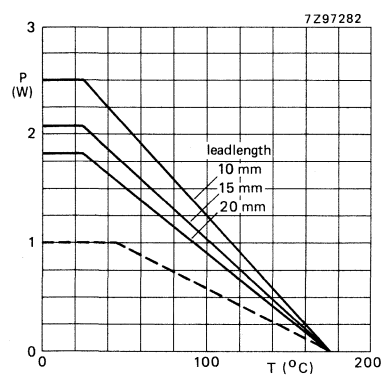


Types C3V6 - C6V8.

Solid line = tie-point temperature.

Dotted line = ambient temperature with device mounted as shown in Fig.2.

Fig.5 Maximum total power dissipation as a function of temperature.

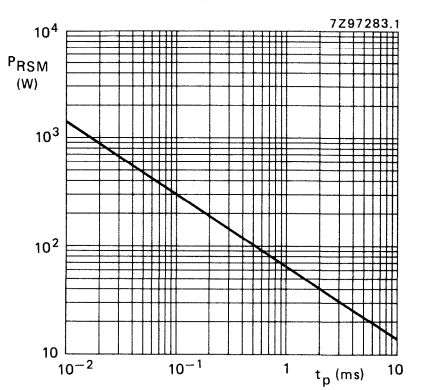


Types C7V5 - C270.

Solid line = tie-point temperature.

Dotted line = ambient temperature with device mounted as shown in Fig.2.

Fig.6 Maximum total power dissipation as a function of temperature.



T_j = 25 °C.

Fig.7 Maximum non-repetitive peak reverse power dissipation (square pulse), prior to surge.

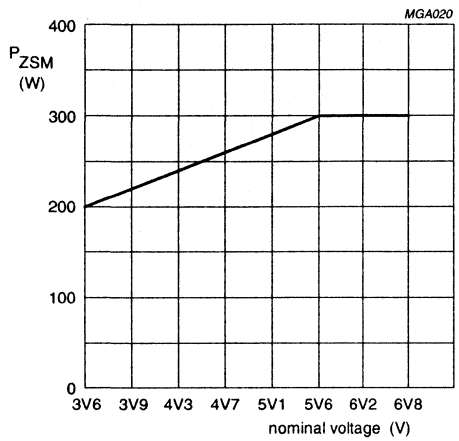
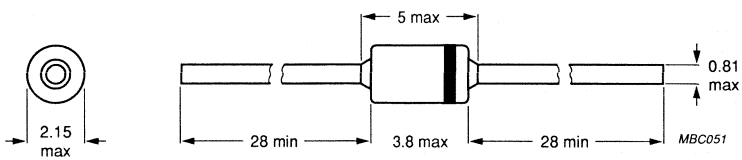


Fig.8 Non-repetitive peak reverse power dissipation as a function of nominal voltage.

PACKAGE OUTLINE



Dimensions in mm.

Marking band indicates the cathode.

Fig.9 SOD81.

Voltage regulator diodes BZD27 series

DESCRIPTION

Glass-passivated diodes in hermetically sealed leadless surface mounted implosion diode (SMID) glass envelopes. They are intended for use as voltage regulator and transient suppressor diodes in medium power regulation and transient suppression circuits.

The series consists of BZD27-C3V6 to C6V8 and BZD27-C7V5 to C510, in the normalized E24 range.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	NOM.	MAX.	UNIT
V_Z	voltage regulator working voltage range			
	C3V6 - C6V8	3.6 to 6.8	–	V
	C7V5 - C270	7.5 to 270	–	V
P_{tot}	total power dissipation			
	C3V6 - C6V8	–	1.7	W
	C7V5 - C510	–	2.3	W
V_R	transient suppressor stand-off voltage			
	C7V5 - C510	6.2 to 430	–	V
P_{RSM}	non-repetitive peak reverse power dissipation	–	300	W

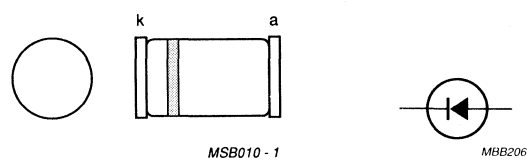


Fig.1 Simplified outline (SOD87) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

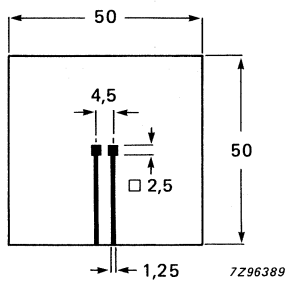
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
P_{tot}	total power dissipation	T_{tp} = 105 °C			
	C3V6 - C6V8		–	1.7	W
	C7V5 - C510		–	2.3	W
		PCB mounting; see Fig.2			
	C3V6 - C6V8	T_{amb} = 60 °C	–	0.8	W
	C7V5 - C510	T_{amb} = 55 °C	–	0.8	W
P_{RSM}	non-repetitive peak reverse power dissipation	t_p = 100 µs, square pulse; T_j = 25 °C (prior to surge); see also Fig.7			
	C3V6 - C6V8	see also Fig.8	–	300	W
	C7V5 - C510		–	300	W
		T_j = 25 °C (prior to surge); waveform 10/1000 exponential pulse; see Fig.3			
	C7V5 - C510		–	150	W
T_{stg}	storage temperature range				
	C3V6 - C6V8		–65	200	°C
	C7V5 - C510		–65	175	°C
T_j	junction temperature				
	C3V6 - C6V8		–	200	°C
	C7V5 - C510		–	175	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}tp}$	from junction to tie-point		
	C3V6 - C6V8		55 K/W
	C7V5 - C510		30 K/W
$R_{th\ j\text{-}a}$	from junction to ambient		
	C3V6 - C6V8	note 1	175 K/W
	C7V5 - C510		150 K/W

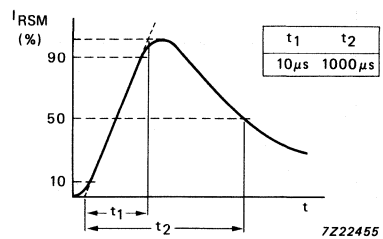
Note

1. Mounted on a 1.5 mm thick epoxy-glass printed circuit board; thickness of copper ≥ 40 µm; see Fig.2.



Dimensions in mm.

Fig.2 Printed circuit board mounting.



t_1 = 10 μs.

t_2 = 1000 μs.

Fig.3 Current pulse (in accordance with IEC 60-2, section 6).

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_F	forward voltage	I_F = 0.2 A; note 1		
	C3V6 - C6V8		1.2	V
	C7V5 - C510		1.2	V

Note

1. Measured under pulse conditions to avoid excessive dissipation.

CHARACTERISTICS

When used as voltage regulator diodes.

BZD27 XXXXX	WORKING VOLTAGE			DIFFERENTIAL RESISTANCE		TEMPERATURE COEFFICIENT		TEST CURRENT	REVERSE CURRENT at REVERSE VOLTAGE	
	V_Z (V)			r_{diff} (Ω)		S_Z (%/K)		I_Z (mA)	I_R (μA)	V_R (V)
	MIN.	NOM.	MAX.	TYP.	MAX.	MIN.	MAX.		MAX.	
C3V6	3.4	3.6	3.8	4	8	−0.14	−0.04	100	100	1
C3V9	3.7	3.9	4.1	4	8	−0.14	−0.04	100	50	1
C4V3	4.0	4.3	4.6	4	7	−0.12	−0.02	100	25	1
C4V7	4.4	4.7	5	3	7	−0.10	0	100	10	–
C5V1	4.8	5.1	5.4	3	6	−0.08	−0.02	100	5	1
C5V6	5.2	5.6	6	2	4	−0.04	0.04	100	10	2
C6V2	5.8	6.2	6.6	2	3	−0.01	0.06	100	5	2
C6V8	6.4	6.8	7.2	1	3	0	0.07	100	10	3
C7V5	7	7.5	7.9	1	2	0	0.07	100	50	3
C8V2	7.7	8.2	8.7	1	2	0.03	0.08	100	10	3
C9V1	8.5	9.1	9.6	2	4	0.03	0.08	50	10	5
C10	9.4	10	10.6	2	4	0.05	0.09	50	7	7.5
C11	10.4	11	11.6	4	7	0.05	0.10	50	3	8.2
C12	11.4	12	12.7	4	7	0.05	0.10	50	2	9.1
C13	12.4	13	14.1	5	10	0.05	0.10	50	1	10
C15	13.8	15	15.6	5	10	0.05	0.10	50	1	11
C16	15.3	16	17.1	6	15	0.06	0.11	25	1	12
C18	16.8	18	19.1	6	15	0.06	0.11	25	1	13
C20	18.8	20	21.2	6	15	0.06	0.11	25	1	15
C22	20.8	22	23.3	6	15	0.06	0.11	25	1	16
C24	22.8	24	25.6	7	15	0.06	0.11	25	1	18
C27	25.1	27	28.9	7	15	0.06	0.11	25	1	20
C30	28	30	32	8	15	0.06	0.11	25	1	22
C33	31	33	35	8	15	0.06	0.11	25	1	24
C36	34	36	38	21	40	0.06	0.11	10	1	27
C39	37	39	41	21	40	0.06	0.11	10	1	30
C43	40	43	46	24	45	0.07	0.12	10	1	33
C47	44	47	50	24	45	0.07	0.12	10	1	36
C51	48	51	54	25	60	0.07	0.12	10	1	39
C56	52	56	60	25	60	0.07	0.12	10	1	43
C62	58	62	66	25	80	0.08	0.13	10	1	47
C68	64	68	72	25	80	0.08	0.13	10	1	51
C75	70	75	79	30	100	0.08	0.13	10	1	56

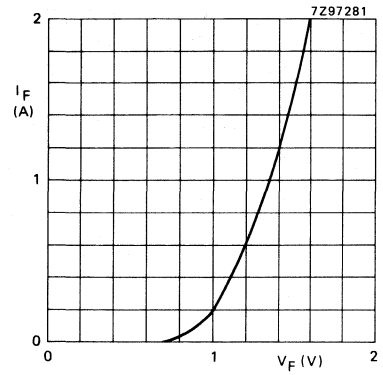
BZD27 XXXXX	WORKING VOLTAGE			DIFFERENTIAL RESISTANCE		TEMPERATURE COEFFICIENT		TEST CURRENT	REVERSE CURRENT at REVERSE VOLTAGE	
	V_Z (V)			r_{diff} (Ω)		S_Z (%/K)		I_Z (mA)	I_R (μA)	V_R (V)
	MIN.	NOM.	MAX.	TYP.	MAX.	MIN.	MAX.		MAX.	
C82	77	82	87	30	100	0.08	0.13	10	1	62
C91	85	91	96	60	200	0.09	0.13	5	1	68
C100	94	100	106	60	200	0.09	0.13	5	1	75
C110	104	110	116	80	250	0.09	0.13	5	1	82
C120	114	120	127	80	250	0.09	0.13	5	1	91
C130	124	130	141	110	300	0.09	0.13	5	1	100
C150	138	150	156	130	300	0.09	0.13	5	1	110
C160	153	160	171	150	350	0.09	0.13	5	1	120
C180	168	180	191	180	400	0.09	0.13	5	1	130
C200	188	200	212	200	500	0.09	0.13	5	1	150
C220	208	220	233	350	750	0.09	0.13	2	1	160
C240	228	240	256	400	850	0.09	0.13	2	1	180
C270	251	270	289	450	1000	0.09	0.13	2	1	200

CHARACTERISTICS

When used as transient suppressor diodes; T_j = 25 °C.

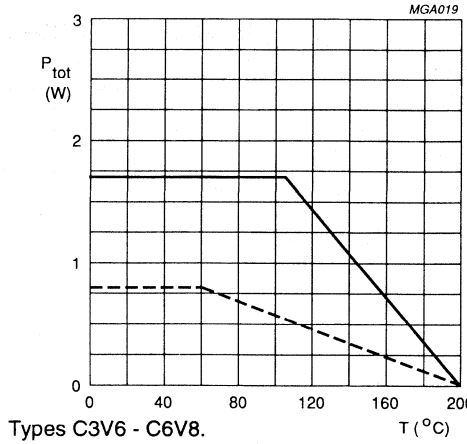
BZD27 XXXXX	CLAMPING VOLTAGE at NON-REPETITIVE PEAK REVERSE CURRENT (10/1000 PULSE)		REVERSE CURRENT AT RECOMMENDED STAND-OFF VOLTAGE	
	$V_{(CL)R}$ (V)	I_{RSM} (A)	I_R (μA)	V_R (V)
	MAX.		MAX.	
C7V5	11.3	13.3	1500	6.2
C8V2	12.3	12.2	1200	6.8
C9V1	13.3	11.3	100	7.5
C10	14.8	10.1	20	8.2
C11	15.7	9.6	5	9.1
C12	17	8.8	5	10
C13	18.9	7.9	5	11
C15	20.9	7.2	5	12
C16	22.9	6.6	5	13
C18	25.6	5.9	5	15
C20	28.4	5.3	5	16
C22	31	4.8	5	18
C24	33.8	4.4	5	20
C27	38.1	3.9	5	22

BZD27 XXXXX	CLAMPING VOLTAGE at NON-REPETITIVE PEAK REVERSE CURRENT (10/1000 PULSE)		REVERSE CURRENT AT RECOMMENDED STAND-OFF VOLTAGE	
	$V_{(CL)R}$ (V) MAX.	I_{RSM} (A)	I_R (μA) MAX.	V_R (V)
C30	42.2	3.6	5	24
C33	46.2	3.2	5	27
C36	50.1	3	5	30
C39	54.1	2.8	5	33
C43	60.7	2.5	5	36
C47	65.5	2.3	5	39
C51	70.8	2.1	5	43
C56	78.6	1.9	5	47
C62	86.5	1.7	5	51
C68	94.4	1.6	5	56
C75	103.5	1.5	5	62
C82	114	1.3	5	68
C91	126	1.2	5	75
C100	139	1.1	5	82
C110	152	1	5	91
C120	167	0.90	5	100
C130	185	0.81	5	110
C150	204	0.73	5	120
C160	224	0.67	5	130
C180	249	0.60	5	150
C200	276	0.54	5	160
C220	305	0.50	5	180
C240	336	0.45	5	200
C270	380	0.40	5	220
C300	419	0.36	5	240
C330	459	0.33	5	270
C360	498	0.30	5	300
C390	537	0.28	5	330
C430	603	0.25	5	360
C470	655	0.23	5	390
C510	707	0.21	5	430



T_j = 25 °C.

Fig.4 Forward current as a function of forward voltage, typical values.

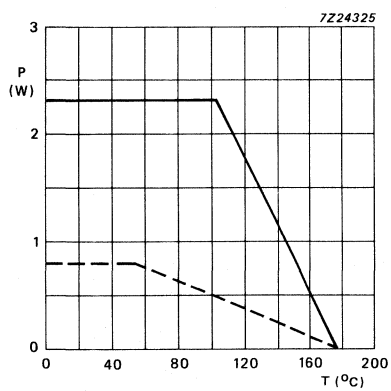


Types C3V6 - C6V8.

Solid line = tie-point temperature.

Dotted line = ambient temperature with device mounted as shown in Fig.2.

Fig.5 Maximum total power dissipation as a function of temperature.

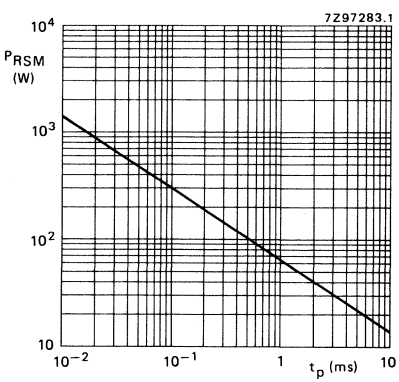


Types C7V5 - C270.

Solid line = tie-point temperature.

Dotted line = ambient temperature with device mounted as shown in Fig.2.

Fig.6 Maximum total power dissipation as a function of temperature.



T_j = 25 °C.

Fig.7 Maximum non-repetitive peak reverse power dissipation (square pulse), prior to surge.

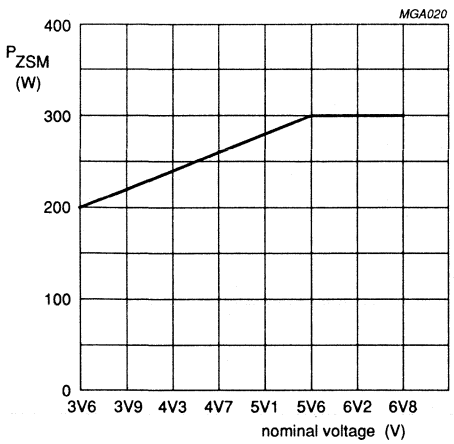
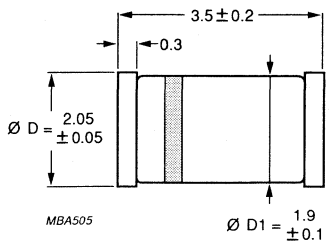


Fig.8 Non-repetitive peak reverse power dissipation as a function of nominal voltage.

PACKAGE OUTLINE



Dimensions in mm.

Marking band indicates the cathode.

Fig.9 SOD87.

REGULATOR DIODES

Glass passivated diodes in hermetically sealed axial-leaded glass envelopes. They are intended for use as voltage regulator and transient suppressor diode in medium power regulation and transient suppression circuits.

The series consists of BZT03-C7V5 to BZT03-C510 in the normalized E24 range.

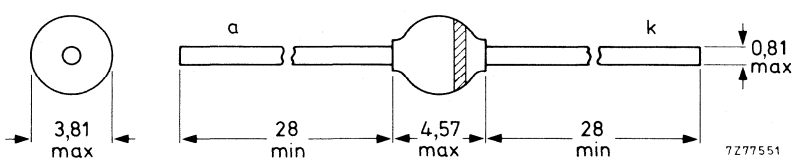
QUICK REFERENCE DATA

			voltage regulator	transient suppressor	
Working voltage range	V_Z	nom.	7.5 to 270		V
Stand-off voltage	V_R			6.2 to 430	V
Total power dissipation	P_{tot}	max.	3.25		W
Non-repetitive peak reverse power dissipation T_j = 25 °C; t_p = 100 μs	P_{RSM}	max.		600	W

MECHANICAL DATA

Dimensions in mm

Fig.1 SOD-57.



The marking band indicates the cathode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Total power dissipation			
T_{tp} = 25 °C; lead length 10 mm	P_{tot}	max.	3,25 W
T_{amb} = 45 °C; p.c.b. mounting (Fig. 2)	P_{tot}	max.	1,3 W
Repetitive peak reverse power dissipation	P_{ZRM}	max.	10 W
Non-repetitive peak reverse power dissipation;			
t_p = 100 μs, square pulse; T_j = 25 °C (prior to surge)	P_{RSM}	max.	600 W
waveform 10/1000 exponential pulse (Fig. 3);			
T_j = 25 °C (prior to surge)	P_{RSM}	max.	300 W
Storage temperature	T_{stg}	−65 to + 175	°C
Junction temperature	T_j	max.	175 °C

THERMAL RESISTANCE

Influence of mounting method

1. Thermal resistance from junction to tie-point at a lead length of 10 mm	$R_{th\ j\text{-}tp}$	=	46 K/W
2. Thermal resistance from junction to ambient when mounted on a 1,5 mm thick epoxy-glass printed-circuit board; Cu-thickness ⩾ 40 μm; Fig. 2 (see "Thermal model")	$R_{th\ j\text{-}a}$	=	100 K/W

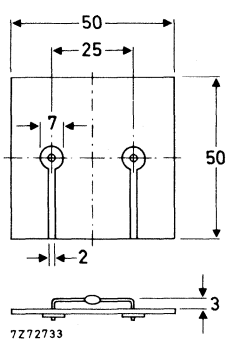


Fig. 2 Mounted on a printed-circuit board.

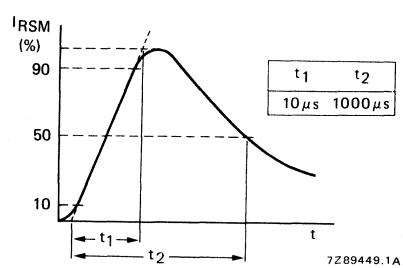


Fig. 3 Current pulse according to IEC 60-2, Section 6.

CHARACTERISTICS

Forward voltage			
I_F = 0,5 A; T_j = 25 °C	V_F	<	1,2 V

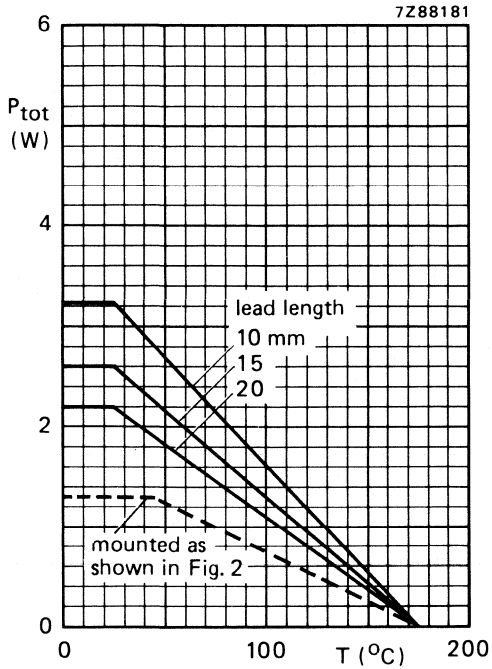


Fig. 4 Maximum total power dissipation as a function of temperature.
——— = T_{tp}; – – – – = T_{amb}; Fig. 2.

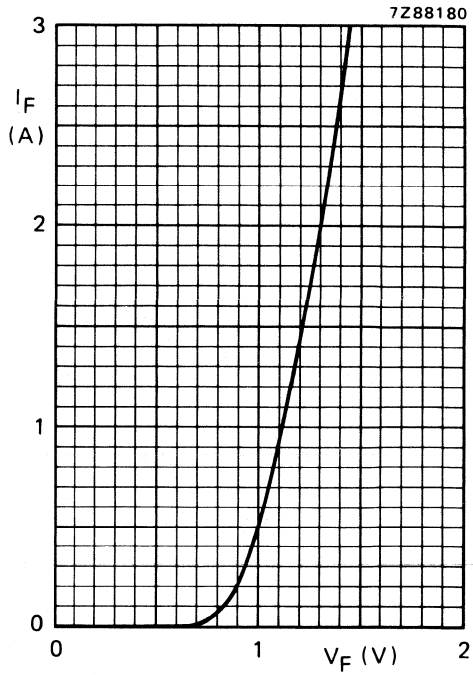


Fig. 5 Typical forward voltage drop T_j = 25 °C.

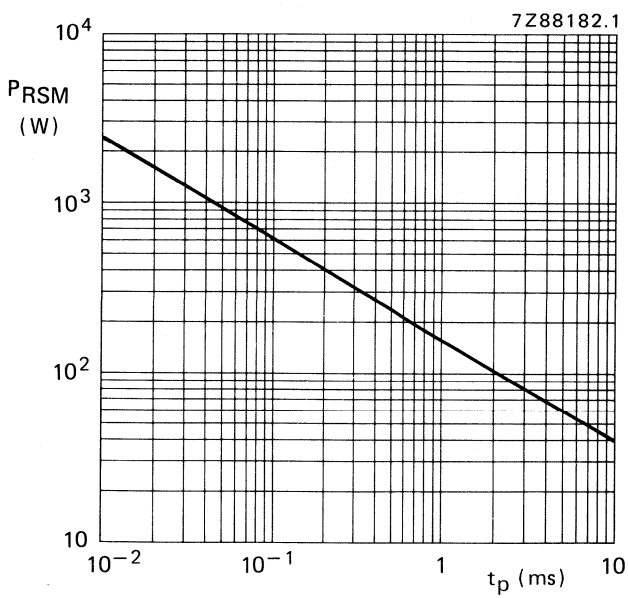


Fig. 6 Maximum non-repetitive peak reverse power dissipation; square current pulse; T_j = 25 °C prior to surge.

CHARACTERISTICS when used as voltage regulator diodes; T_j = 25 °C

BZT03-XXXX	working voltage V_Z V			differential resistance r_{diff} Ω		temperature coefficient S_Z %/K		test current I_Z mA	reverse current at I_R μA	reverse voltage V_R V
	min.	typ.	max.	typ.	max.	min.	max.		max.	
C7V5	7,0	7,5	7,9	1	2	0	0,07	100	750	5,6
C8V2	7,7	8,2	8,7	1	2	0,03	0,08	100	600	6,2
C9V1	8,5	9,1	9,6	2	4	0,03	0,08	50	20	6,8
C10	9,4	10,0	10,6	2	4	0,05	0,09	50	10	7,5
C11	10,4	11,0	11,6	4	7	0,05	0,10	50	4	8,2
C12	11,4	12,0	12,7	4	7	0,05	0,10	50	3	9,1
C13	12,4	13,0	14,1	5	10	0,05	0,10	50	2	10
C15	13,8	15,0	15,6	5	10	0,05	0,10	50	1	11
C16	15,3	16,0	17,1	6	15	0,06	0,11	25	1	12
C18	16,8	18,0	19,1	6	15	0,06	0,11	25	1	13
C20	18,8	20,0	21,2	6	15	0,06	0,11	25	1	15
C22	20,8	22,0	23,3	6	15	0,06	0,11	25	1	16
C24	22,8	24,0	25,6	7	15	0,06	0,11	25	1	18
C27	25,1	27,0	28,9	7	15	0,06	0,11	25	1	20
C30	28	30	32	8	15	0,06	0,11	25	1	22
C33	31	33	35	8	15	0,06	0,11	25	1	24
C36	34	36	38	21	40	0,06	0,11	10	1	27
C39	37	39	41	21	40	0,06	0,11	10	1	30
C43	40	43	46	24	45	0,07	0,12	10	1	33
C47	44	47	50	24	45	0,07	0,12	10	1	36
C51	48	51	54	25	60	0,07	0,12	10	1	39
C56	52	56	60	25	60	0,07	0,12	10	1	43
C62	58	62	66	25	80	0,08	0,13	10	1	47
C68	64	68	72	25	80	0,08	0,13	10	1	51
C75	70	75	79	30	100	0,08	0,13	10	1	56
C82	77	82	87	30	100	0,08	0,13	10	1	62
C91	85	91	96	60	200	0,09	0,13	5	1	68
C100	94	100	106	60	200	0,09	0,13	5	1	75
C110	104	110	116	80	250	0,09	0,13	5	1	82
C120	114	120	127	80	250	0,09	0,13	5	1	91
C130	124	130	141	110	300	0,09	0,13	5	1	100
C150	138	150	156	130	300	0,09	0,13	5	1	110
C160	153	160	171	150	350	0,09	0,13	5	1	120
C180	168	180	191	180	400	0,09	0,13	5	1	130
C200	188	200	212	200	500	0,09	0,13	5	1	150
C220	208	220	233	350	750	0,09	0,13	2	1	160
C240	228	240	256	400	850	0,09	0,13	2	1	180
C270	251	270	289	450	1000	0,09	0,13	2	1	200

CHARACTERISTICS when used as transient suppressor diodes; T_j = 25 °C

	breakdown voltage at test current		clamping voltage at non-repetitive peak reverse current (10/1000 pulse)		reverse current at recommended stand-off voltage	
	$V_{(BR)R}$	I_R	$V_{(CL)R}$	I_{RSM}	I_R	V_R
	V	mA	V	A	μA	V
BZT03-	min.		max.		max.	
C7V5	7.0	100	11.3	26.5	1500	6.2
C8V2	7.7	100	12.3	24.4	1200	6.8
C9V1	8.5	50	13.3	22.7	50	7.5
C10	9.4	50	14.8	20.3	20	8.2
C11	10.4	50	15.7	19.1	5	9.1
C12	11.4	50	17.0	17.7	5	10
C13	12.4	50	18.9	15.9	5	11
C15	13.8	50	20.9	14.4	5	12
C16	15.3	25	22.9	13.1	5	13
C18	16.8	25	25.6	11.7	5	15
C20	18.8	25	28.4	10.6	5	16
C22	20.8	25	31.0	9.7	5	18
C24	22.8	25	33.8	8.9	5	20
C27	25.1	25	38.1	7.9	5	22
C30	28	25	42.2	7.1	5	24
C33	31	25	46.2	6.5	5	27
C36	34	10	50.1	6.0	5	30
C39	37	10	54.1	5.5	5	33
C43	40	10	60.7	4.9	5	36
C47	44	10	65.5	4.6	5	39
C51	48	10	70.8	4.2	5	43
C56	52	10	78.6	3.8	5	47
C62	58	10	86.5	3.5	5	51
C68	64	10	94.4	3.2	5	56
C75	70	10	103.5	2.9	5	62
C82	77	10	114.0	2.6	5	68
C91	85	5	126	2.4	5	75
C100	94	5	139	2.2	5	82
C110	104	5	152	2.0	5	91
C120	114	5	167	1.8	5	100
C130	124	5	185	1.6	5	110
C150	138	5	204	1.5	5	120
C160	153	5	224	1.3	5	130
C180	168	5	249	1.2	5	150
C200	188	5	276	1.1	5	160
C220	208	2	305	1.0	5	180
C240	228	2	336	0.9	5	200
C270	251	2	380	0.8	5	220
C300	280	2	419	0.72	5	240
C330	310	2	459	0.65	5	270
C360	340	1	498	0.60	5	300
C390	370	1	537	0.56	5	330
C430	400	1	603	0.50	5	360
C470	440	1	655	0.45	5	390
C510	480	1	707	0.42	5	430

Voltage regulator diodes BZG03 series

DESCRIPTION

High reliability glass-passivated diodes in a small rectangular SMD SOD106A envelope. The envelope dimensions meet JEDEC DO-214AC envelope specification. They are intended for use as medium power voltage regulator diodes, especially in automotive applications.

The series consists of BZG03-C10 to BZG03-C270 in the normalized E24 range.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	NOM.	MAX.	UNIT
V_Z	working voltage range	10 to 270	–	V
P_{tot}	total power dissipation	–	3	W
P_{ZSM}	non-repetitive peak reverse power dissipation	–	600	W

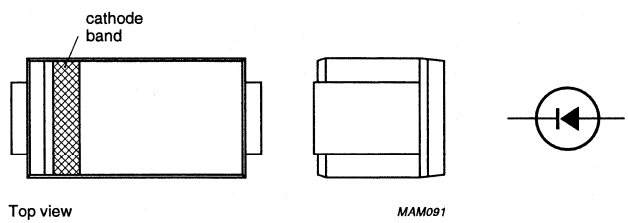


Fig.1 Simplified outline (SOD106A) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
P_{tot}	total power dissipation	T_{tp} = 100 °C	–	3	W
		T_{amb} = 50 °C; PCB mounted; see Fig 2	–	1.25	W
P_{ZSM}	non-repetitive peak reverse power dissipation	t_p = 100 µs, square pulse; T_j = 25 °C prior to surge	–	600	W
T_{stg}	storage temperature		–65	+175	°C
T_j	junction temperature		–65	+175	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}tp}$	thermal resistance from junction to tie-point		25 K/W
$R_{th\ j\text{-}amb}$	thermal resistance from junction to ambient	note (1)	100 K/W
		note (2)	150 K/W

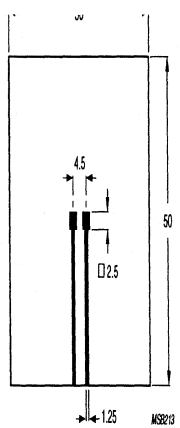
Notes

1. Device mounted on a 0.7 mm thick Al_2O_3 printed-circuit board; thickness of copper ≥ 35 μm; see Fig 2.
2. Device mounted on a 1.5 mm thick epoxy glass printed-circuit board; thickness of copper ≥ 40 μm ; see Fig 2

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

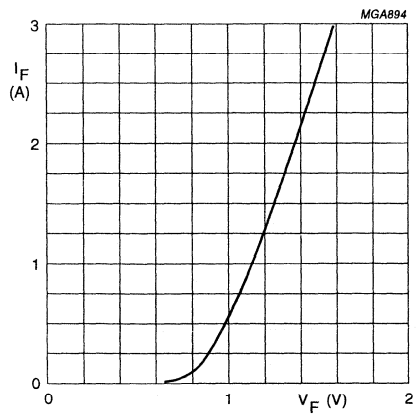
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_F	forward voltage	I_F = 0.5 A	–	1.2	V



Dimensions in mm.

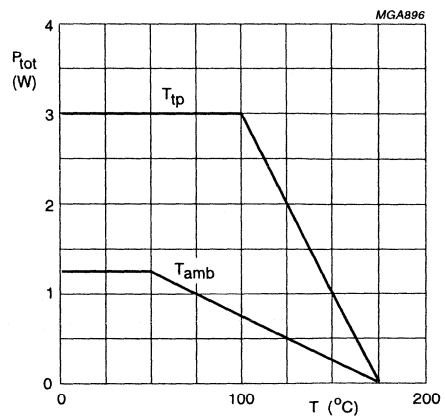
Fig.2 Printed-circuit board for surface mounting.

BZG03 -XXXX	WORKING VOLTAGE			DIFFERENTIAL RESISTANCE		TEMPERATURE COEFFICIENT		TEST CURRENT	REVERSE CURRENT at REVERSE VOLTAGE	
	V_Z (V) at I_Z			r_{dif} (Ω) at I_Z		S_Z (%/K) at I_Z		I_Z (mA)	I_R (μA)	V_R (V)
	MIN.	NOM.	MAX.	TYP.	MAX.	MIN.	MAX.		MAX.	
C10	9.4	10	10.6	2	4	0.05	0.09	50	10	7.5
C11	10.4	11	11.6	4	7	0.05	0.10	50	4	8.2
C12	11.4	12	12.7	4	7	0.05	0.10	50	3	9.1
C13	12.4	13	14.1	5	10	0.05	0.10	50	2	10
C15	13.8	15	15.6	5	10	0.05	0.10	50	1	11
C16	15.3	16	17.1	6	15	0.06	0.11	25	1	12
C18	16.8	18	19.1	6	15	0.06	0.11	25	1	13
C20	18.8	20	21.2	6	15	0.06	0.11	25	1	15
C22	20.8	22	23.3	6	15	0.06	0.11	25	1	16
C24	22.8	24	25.6	7	15	0.06	0.11	25	1	18
C27	25.1	27	28.9	7	15	0.06	0.11	25	1	20
C30	28	30	32	8	15	0.06	0.11	25	1	22
C33	31	33	35	8	15	0.06	0.11	25	1	24
C36	34	36	38	21	40	0.06	0.11	10	1	27
C39	37	39	41	21	40	0.06	0.11	10	1	30
C43	40	43	46	24	45	0.07	0.12	10	1	33
C47	44	47	50	24	45	0.07	0.12	10	1	36
C51	48	51	54	25	60	0.07	0.12	10	1	39
C56	52	56	60	25	60	0.07	0.12	10	1	43
C62	58	62	66	25	80	0.08	0.13	10	1	47
C68	64	68	72	25	80	0.08	0.13	10	1	51
C75	70	75	79	30	100	0.08	0.13	10	1	56
C82	77	82	87	30	100	0.08	0.13	10	1	62
C91	85	91	96	60	200	0.09	0.13	5	1	68
C100	94	100	106	60	200	0.09	0.13	5	1	75
C110	104	110	116	80	250	0.09	0.13	5	1	82
C120	114	120	127	80	250	0.09	0.13	5	1	91
C130	124	130	141	110	300	0.09	0.13	5	1	100
C150	138	150	156	130	300	0.09	0.13	5	1	110
C160	153	160	171	150	350	0.09	0.13	5	1	120
C180	168	180	191	180	400	0.09	0.13	5	1	130
C200	188	200	212	200	500	0.09	0.13	5	1	150
C220	208	220	233	350	750	0.09	0.13	2	1	160
C240	228	240	256	400	850	0.09	0.13	2	1	180
C270	251	270	289	450	1000	0.09	0.13	2	1	200



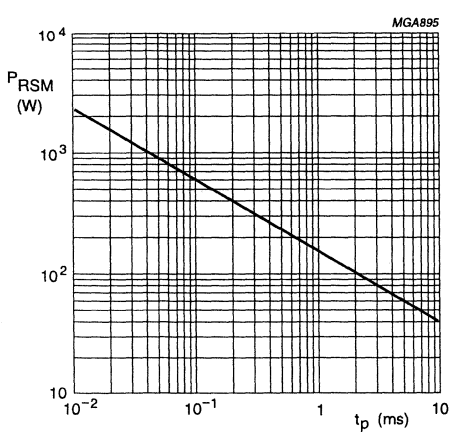
T_j = 25 °C.

Fig.3 Forward current as a function of forward voltage; typical values.



Device mounted as shown in Fig.2.

Fig.4 Maximum total power dissipation as a function of temperature.



T_j = 25 °C prior to surge.

Fig.5 Maximum non-repetitive peak reverse power dissipation (square pulse).

PACKAGE OUTLINE

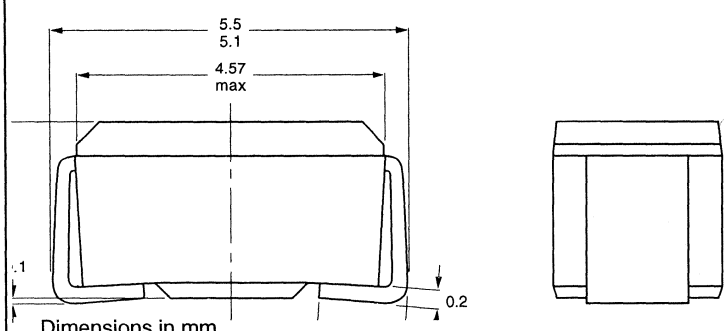


Fig.8 SOD106A.

REGULATOR DIODES

Glass passivated diodes in hermetically sealed axial-leaded glass envelopes. They are intended for use as voltage regulator and transient suppressor diode in medium power regulation and transient suppression circuits.

The series consists of BZW03-C7V5 to BZW03-C510 in the normalized E24 range.

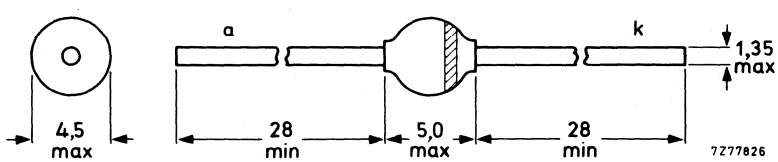
QUICK REFERENCE DATA

			voltage regulator	transient suppressor	
Working voltage range	V_Z	nom.	7,5 to 270		V
Stand-off voltage	V_R			6,2 to 430	V
Total power dissipation	P_{tot}	max.	6		W
Non-repetitive peak reverse power dissipation T_j = 25 °C; t_p = 100 μs	P_{RSM}			1000	W

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-64.



The marking band indicates the cathode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Total power dissipation			
T_{tp} = 25 °C; lead length 10 mm	P_{tot}	max.	6 W
T_{amb} = 45 °C; p.c.b. mounting (Fig. 2)	P_{tot}	max.	1,75 W
Repetitive peak reverse power dissipation	P_{ZRM}	max.	20 W
Non-repetitive peak reverse power dissipation			
t_p = 100 μs square pulse; T_j = 25 °C (prior to surge)	P_{RSM}	max.	1000 W
waveform 10/1000 exponential pulse (see Fig. 3), T_j = 25 °C (prior to surge)	P_{RSM}	max.	500 W
Storage temperature	T_{stg}		−65 to +175 °C
Junction temperature	T_j	max.	175 °C

THERMAL RESISTANCE

Influence of mounting method

1. Thermal resistance from junction to tie-point at a lead length of 10 mm	$R_{th\ j\text{-}tp}$	=	25 K/W
2. Thermal resistance from junction to ambient when mounted on a 1,5 mm thick epoxy-glass printed-circuit board; Cu-thickness ≥ 40 μm; Fig. 2 (see "Thermal model")	$R_{th\ j\text{-}a}$	=	75 K/W

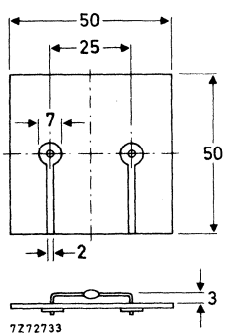


Fig. 2 Mounted on a printed-circuit board.

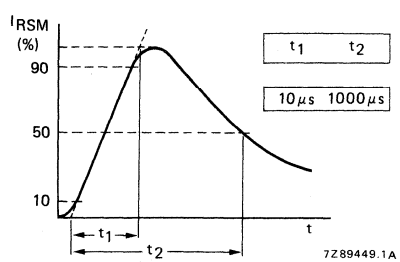


Fig. 3 Current pulse according to IEC 60-2, Section 6.

CHARACTERISTICS

Forward voltage			
I_F = 1 A; T_j = 25 °C	V_F	<	1,2 V

CHARACTERISTICS when used as voltage regulator diodes; T_j = 25 °C

	working voltage V_Z			differential resistance r_{diff}		temperature coefficient S_Z		test current I_Z	reverse current I_R at reverse voltage V_R	
	V			Ω		%/K		mA	μA	V
BZW03-	min.	nom.	max.	typ.	max.	min.	max.		max.	
C7V5	7,0	7,5	7,9	0,7	1,5	0	0,07	175	1500	5,6
C8V2	7,7	8,2	8,7	0,8	1,5	0,03	0,08	150	1200	6,2
C9V1	8,5	9,1	9,6	0,9	2,0	0,03	0,08	150	40	6,8
C10	9,4	10,0	10,6	1,0	2,0	0,05	0,09	125	20	7,5
C11	10,4	11,0	11,6	1,1	2,5	0,05	0,10	125	15	8,2
C12	11,4	12,0	12,7	1,1	2,5	0,05	0,10	100	10	9,1
C13	12,4	13,0	14,1	1,2	2,5	0,05	0,10	100	4	10
C15	13,8	15,0	15,6	1,2	2,5	0,05	0,10	75	2	11
C16	15,3	16,0	17,1	1,3	2,5	0,06	0,11	75	2	12
C18	16,8	18,0	19,1	1,3	2,5	0,06	0,11	65	2	13
C20	18,8	20,0	21,2	1,5	3	0,06	0,11	65	2	15
C22	20,8	22,0	23,3	1,6	3,5	0,06	0,11	50	2	16
C24	22,8	24,0	25,6	1,8	3,5	0,06	0,11	50	2	18
C27	25,1	27,0	28,9	2,5	5	0,06	0,11	50	2	20
C30	28	30	32	4	8	0,06	0,11	40	2	22
C33	31	33	35	5	10	0,06	0,11	40	2	24
C36	34	36	38	6	11	0,06	0,11	30	2	27
C39	37	39	41	7	14	0,06	0,11	30	2	30
C43	40	43	46	10	20	0,07	0,12	30	2	33
C47	44	47	50	12	25	0,07	0,12	25	2	36
C51	48	51	54	14	27	0,07	0,12	25	2	39
C56	52	56	60	18	35	0,07	0,12	20	2	43
C62	58	62	66	20	42	0,08	0,13	20	2	47
C68	64	68	72	22	44	0,08	0,13	20	2	51
C75	70	75	79	25	45	0,08	0,13	20	2	56
C82	77	82	87	30	65	0,08	0,13	15	2	62
C91	85	91	96	40	75	0,09	0,13	15	2	68
C100	94	100	106	45	90	0,09	0,13	12	2	75
C110	104	110	116	65	125	0,09	0,13	12	2	82
C120	114	120	127	90	170	0,09	0,13	10	2	91
C130	124	130	141	100	190	0,09	0,13	10	2	100
C150	138	150	156	150	330	0,09	0,13	8	2	110
C160	153	160	171	180	350	0,09	0,13	8	2	120
C180	168	180	191	210	430	0,09	0,13	5	2	130
C200	188	200	212	250	500	0,09	0,13	5	2	150
C220	208	220	233	350	700	0,09	0,13	5	2	160
C240	228	240	256	450	900	0,09	0,13	5	2	180
C270	251	270	289	600	1200	0,09	0,13	5	2	200

CHARACTERISTICS when used as transient suppressor diodes; T_j = 25 °C

clamping voltage at non-repetitive peak reverse current 10/1000 pulse		reverse current at recommended stand-off voltage		
$V_{(CL)R}$ V	I_{RSM} A	I_R μA	V_R V	
max.	max.	max.		BZW03-
11,3	44,2	3000	6,2	C7V5
12,3	40,6	2400	6,8	C8V2
13,3	37,6	100	7,5	C9V1
14,8	34,0	40	8,2	C10
15,7	31,8	30	9,1	C11
17,0	29,4	20	10	C12
18,9	26,4	10	11	C13
20,9	23,9	10	12	C15
22,9	21,8	10	13	C16
25,6	19,5	10	15	C18
28,4	17,6	10	16	C20
31	16,1	10	18	C22
33,8	14,8	10	20	C24
38,1	13,1	10	22	C27
42,2	11,8	10	24	C30
46,2	10,8	10	27	C33
50,1	10,0	10	30	C36
54,1	9,2	10	33	C39
60,7	8,2	10	36	C43
65,5	7,6	10	39	C47
70,8	7,0	10	43	C51
78,6	6,3	10	47	C56
86,5	5,8	10	51	C62
94,4	5,3	10	56	C68
103,5	4,8	10	62	C75
114,0	4,3	10	68	C82
126	3,9	10	75	C91
139	3,6	10	82	C100
152	3,3	10	91	C110
167	3,0	10	100	C120
185	2,7	10	110	C130
204	2,4	10	120	C150
224	2,2	10	130	C160
249	2,0	10	150	C180
276	1,8	10	160	C200
305	1,6	10	180	C220
336	1,5	10	200	C240
380	1,3	10	220	C270
419	1,2	10	240	C300
459	1,1	10	270	C330
498	1,0	10	300	C360
537	0,93	10	330	C390
603	0,83	10	360	C430
655	0,76	10	390	C470
707	0,71	10	430	C510

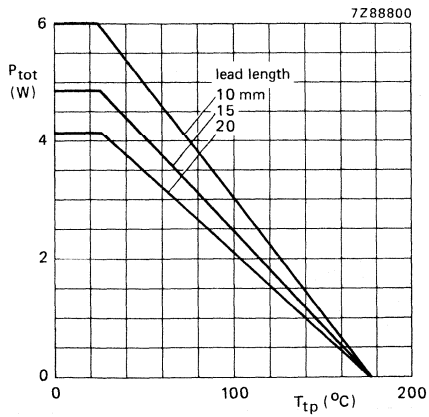


Fig. 4 Maximum total power dissipation as a function of tie-point temperature.

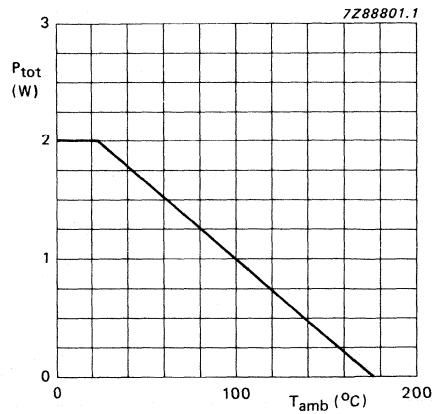


Fig. 5 Maximum total power dissipation as a function of ambient temperature, mounted as shown in Fig. 2.

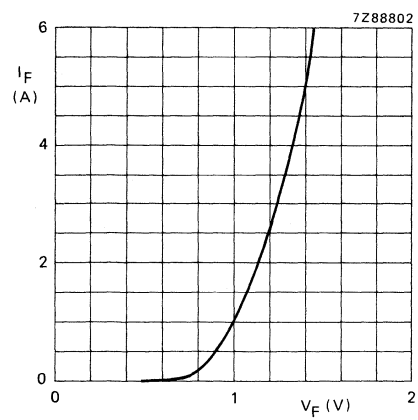


Fig. 6 Typical forward voltage drop at T_j = 25 °C.

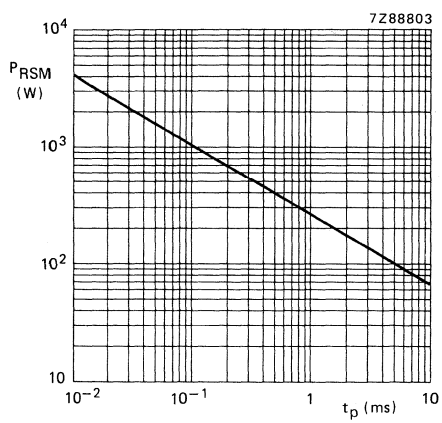


Fig. 7 Maximum non-repetitive peak reverse power dissipation; square current pulse; T_j = 25 °C prior to surge.

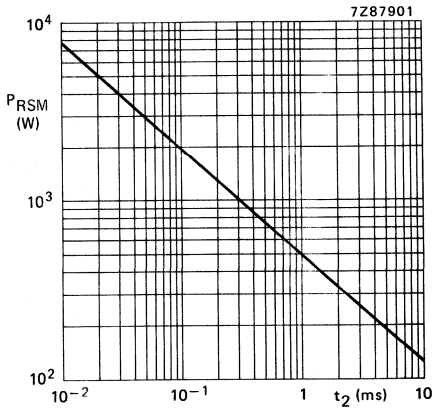


Fig. 8 Maximum non-repetitive peak reverse power dissipation; exponential pulse; T_j = 25 °C prior to surge.

Transient suppressor diodes BZG04 series

FEATURES

- High reliability
- SOD106A/JEDEC DO-214AC package
- Glass passivated.

APPLICATIONS

- As medium power transient suppressor diodes, especially in automotive applications.

DESCRIPTION

High reliability glass passivated diodes in a small rectangular SMD SOD106A plastic package. The package meets JEDEC DO-214AC package specification.

The series consists of BZG04-8V2 to BZG04-200 in the normalized E24 range.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	NOM.	MAX.	UNIT
V_R	stand-off voltage range	8.2 to 200	–	V
P_{RSM}	non-repetitive peak reverse power dissipation	–	300	W

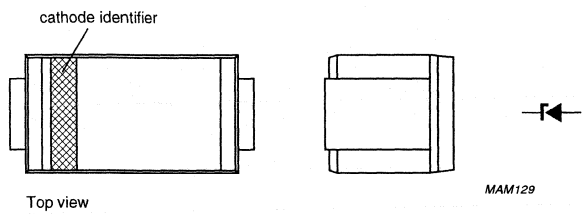


Fig.1 Simplified outline (SOD106A; DO-214AC) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

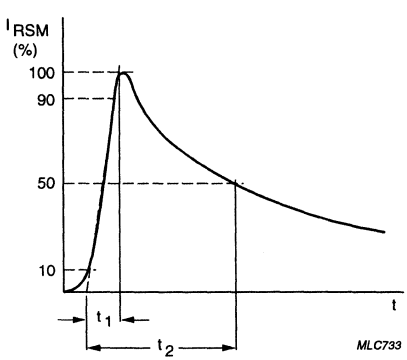
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
P_{RSM}	non-repetitive peak reverse power dissipation	$^{10}/_{1000}$ exponential pulse; T_j = 25 °C prior to surge; see Fig.2	–	300	W
T_{stg}	storage temperature		−65	+175	°C
T_j	junction temperature		−65	+175	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}tp}$	thermal resistance from junction to tie-point		25	K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	100	K/W
		note 2	150	K/W

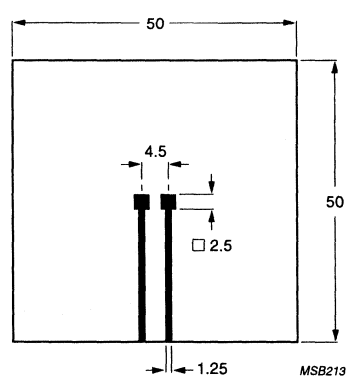
Notes

1. Device mounted on an Al_2O_3 printed-circuit board, 0.7 mm thick; thickness of Cu-layer ≥35 µm, see Fig.3.
2. Device mounted on an epoxy-glass printed-circuit board, 1.5 mm thick; thickness of Cu-layer ≥40 µm, see Fig.3.



t_1 = 10 µs; t_2 = 1000 µs.

Fig.2 Current pulse according to *"IEC 60-1, section 8"*.



Dimensions in mm.
Material: Al_2O_3 or epoxy-glass.

Fig.3 Printed-circuit board for surface mounting.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_F	continuous forward voltage	I_F = 0.5 A	1.2	V

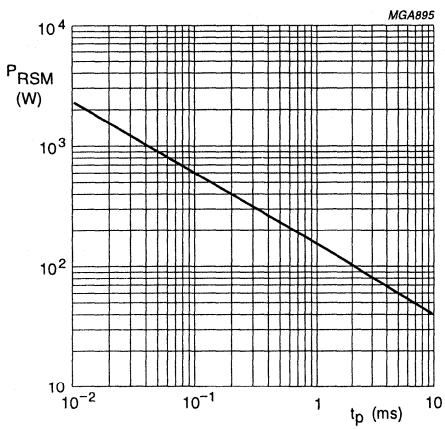
TRANSIENT SUPPRESSION CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

TYPE NUMBER	MIN. REVERSE BREAKDOWN VOLTAGE		MAX. CLAMPING VOLTAGE		MAX. REVERSE CURRENT	
	$V_{(BR)Rmin}$ (V)	at I_R (mA)	$V_{(CL)Rmax}$ (V)	at I_{RSM}[1] (A)	I_{Rmax} (A)	at V_R (V)
BZG04-8V2	9.4	50	14.8	20.3	20	8.2
BZG04-9V1	10.4	50	15.7	19.1	5	9.1
BZG04-10	11.4	50	17.0	17.7	5	10
BZG04-11	12.4	50	18.9	15.9	5	11
BZG04-12	13.8	50	20.9	14.4	5	12
BZG04-13	15.3	25	22.9	13.1	5	13
BZG04-15	16.8	25	25.6	11.7	5	15
BZG04-16	18.8	25	28.4	10.6	5	16
BZG04-18	20.8	25	31.0	9.7	5	18
BZG04-20	22.8	25	33.8	8.9	5	20
BZG04-22	25.1	25	38.1	7.9	5	22
BZG04-24	28	25	42.2	7.1	5	24
BZG04-27	31	25	46.2	6.5	5	27
BZG04-30	34	10	50.1	6.0	5	30
BZG04-33	37	10	54.1	5.5	5	33
BZG04-36	40	10	60.7	4.9	5	36
BZG04-39	44	10	65.5	4.6	5	39
BZG04-43	48	10	70.8	4.2	5	43
BZG04-47	52	10	78.6	3.8	5	47
BZG04-51	58	10	86.5	3.5	5	51
BZG04-56	64	10	94.4	3.2	5	56
BZG04-62	70	10	103.5	2.9	5	62
BZG04-68	77	10	114.0	2.6	5	68
BZG04-75	85	5	126	2.4	5	75
BZG04-82	94	5	139	2.2	5	82
BZG04-91	104	5	152	2.0	5	91
BZG04-100	114	5	167	1.8	5	100
BZG04-110	124	5	185	1.6	5	110
BZG04-120	138	5	204	1.5	5	120
BZG04-130	153	5	224	1.3	5	130
BZG04-150	168	5	249	1.2	5	150
BZG04-160	188	5	276	1.1	5	160
BZG04-180	208	2	305	1.0	5	180
BZG04-200	228	2	336	0.9	5	200

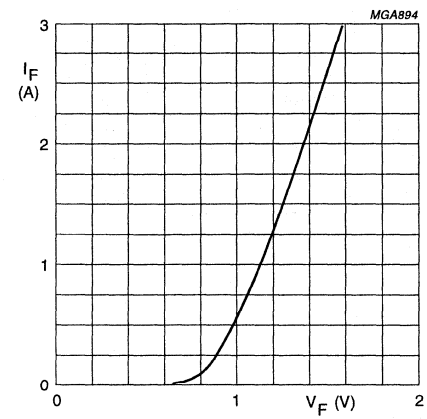
Note

1. In accordance with *"IEC 60-1, section 8"* ($^{10}/_{1000}$ pulse).



Square current pulse; T_j = 25 °C prior to surge.

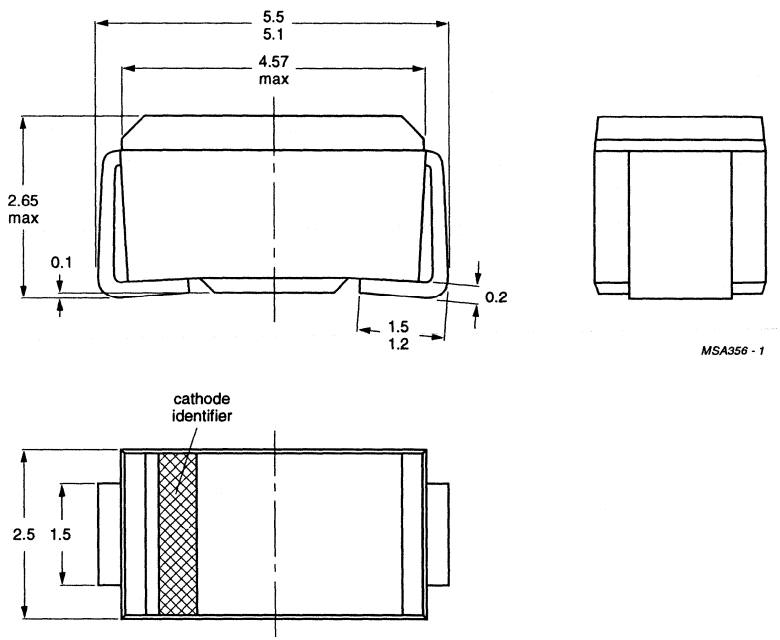
Fig.4 Maximum permissible non-repetitive peak reverse power dissipation as function of pulse time.



T_j = 25 °C.

Fig.5 Forward current as a function of forward voltage; typical values.

PACKAGE OUTLINE



Dimensions in mm.
The marking band indicates the cathode.

Fig.6 SOD106A.

VOLTAGE REGULATOR DIODES

Silicon planar diodes in DO-35 envelopes intended for use as low voltage stabilizers or voltage references. They are available in four series; each series having a different tolerance rating, one series is to the international standardized E24 (± 5%) range, the other three have tolerances of 1%, 2% and 3% on working voltage. Each series consists of 37 types with nominal working voltages ranging from 2,4 V to 75 V.

QUICK REFERENCE DATA

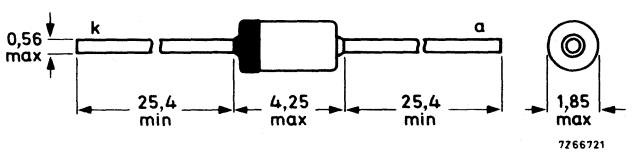
Working voltage range	V_Z	nom.	2,4 to 75	V
Total power dissipation	P_{tot}	max.	500	mW *
Non-repetitive peak reverse power dissipation	P_{ZSM}	max.	30	W
Junction temperature	T_j	max.	200	°C
Thermal resistance from junction to tie-point	$R_{th\ j\text{-}tp}$	=	0,30	K/mW *

* If leads are kept at T_{tp} = 50 °C at 8 mm from body.

MECHANICAL DATA

Dimensions in mm

Fig.1 DO-35 (SOD27).



Cathode indicated by coloured band.
The diodes are type-branded.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Average forward current (averaged over any 20 ms period)	$I_{F(AV)}$	max.	250	mA
Repetitive peak forward current	I_{FRM}	max.	250	mA
Total power dissipation	P_{tot}	max.	500	mW *
		max.	400	mW **
Non-repetitive peak reverse power dissipation $t = 100\ \mu s$; $T_j = 150\ ^oC$	P_{ZSM}	max.	30	W
Storage temperature	T_{stg}	−65 to +	200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to tie-point	$R_{th\ j\text{-}tp}$	=	0,30	K/mW*
From junction to ambient	$R_{th\ j\text{-}a}$	=	0,38	K/mW**

CHARACTERISTICS

$T_j = 25\ ^oC$

Forward voltage $I_F = 10$ mA		V_F	<	0,9	V
Reverse current					
BZX79-.2V4	$V_R = 1$ V	I_R	<	50	μA
.2V7	$V_R = 1$ V	I_R	<	20	μA
.3V0	$V_R = 1$ V	I_R	<	10	μA
.3V3	$V_R = 1$ V	I_R	<	5	μA
.3V6	$V_R = 1$ V	I_R	<	5	μA
.3V9	$V_R = 1$ V	I_R	<	3	μA
.4V3	$V_R = 1$ V	I_R	<	3	μA
.4V7	$V_R = 2$ V	I_R	<	3	μA
.5V1	$V_R = 2$ V	I_R	<	2	μA
.5V6	$V_R = 2$ V	I_R	<	1	μA
.6V2	$V_R = 4$ V	I_R	<	3	μA
.6V8	$V_R = 4$ V	I_R	<	2	μA
.7V5	$V_R = 5$ V	I_R	<	1	μA
.8V2	$V_R = 5$ V	I_R	<	700	nA
.9V1	$V_R = 6$ V	I_R	<	500	nA
.10	$V_R = 7$ V	I_R	<	200	nA
.11 to .13	$V_R = 8$ V	I_R	<	100	nA
.15 to .75	$V_R = 0{,}7\ V_{Znom}$	I_R	<	50	nA

. = A for 1% tolerance range
. = B for 2% tolerance range
. = F for 3% tolerance range
. = C for E24 (± 5%) tolerance range

* If leads are kept at $T_{tp} = 50\ ^oC$ at 8 mm from body.
** In still air at maximum lead length up to $T_{amb} = 50\ ^oC$.

T_j = 25 °C
± 1% tolerance range

BZX79A	working voltage V_Z (V) at I_{Ztest} = 5 mA		differential resistance r_{diff} (Ω) at I_{Ztest} = 5 mA		temperature coefficient S_Z (mV/K) at I_{Ztest} = 5 mA			differential resistance r_{diff} (Ω) at I_Z = 1 mA	
	min.	max.	typ.	max.	min.	typ.	max.	typ.	max.
A2V4	2,37	2,43	70	100	−3,5	−1,6	0	275	600
A2V7	2,67	2,73	75	100	−3,5	−2,0	0	300	600
A3V0	2,97	3,03	80	95	−3,5	−2,1	0	325	600
A3V3	3,26	3,34	85	95	−3,5	−2,4	0	350	600
A3V6	3,56	3,64	85	90	−3,5	−2,4	0	375	600
A3V9	3,86	3,94	85	90	−3,5	−2,5	0	400	600
A4V3	4,25	4,35	80	90	−3,5	−2,5	0	410	600
A4V7	4,65	4,75	50	80	−3,5	−1,4	0,2	425	500
A5V1	5,04	5,16	40	60	−2,7	−0,8	1,2	400	480
A5V6	5,54	5,66	15	40	−2,0	1,2	2,5	80	400
A6V2	6,13	6,27	6	10	0,4	2,3	3,7	40	150
A6V8	6,73	6,87	6	15	1,2	3,0	4,5	30	80
A7V5	7,42	7,58	6	15	2,5	4,0	5,3	30	80
A8V2	8,11	8,29	6	15	3,2	4,6	6,2	40	80
A9V1	9,00	9,20	6	15	3,8	5,5	7,0	40	100
A10	9,90	10,10	8	20	4,5	6,4	8,0	50	150
A11	10,89	11,11	10	20	5,4	7,4	9,0	50	150
A12	11,88	12,12	10	25	6,0	8,4	10,0	50	150
A13	12,87	13,13	10	30	7,0	9,4	11,0	50	170
A15	14,85	15,15	10	30	9,2	11,4	13,0	50	200
A16	15,84	16,16	10	40	10,4	12,4	14,0	50	200
A18	17,82	18,18	10	45	12,4	14,4	16,0	50	225
A20	19,80	20,20	15	55	14,4	16,4	18,0	60	225
A22	21,78	22,22	20	55	16,4	18,4	20,0	60	250
A24	23,76	24,24	25	70	18,4	20,4	22,0	60	250
	at I_{Ztest} = 2 mA		at I_{Ztest} = 2 mA		at I_{Ztest} = 2 mA			at I_Z = 0,5 mA	
A27	26,73	27,27	25	80	21,4	23,4	25,3	65	300
A30	29,70	30,30	30	80	24,4	26,6	29,4	70	300
A33	32,67	33,33	35	80	27,4	29,7	33,4	75	325
A36	35,64	36,36	35	90	30,4	33,0	37,4	80	350
A39	38,61	39,39	40	130	33,4	36,4	41,2	80	350
A43	42,57	43,43	45	150	37,6	41,2	46,6	85	375
A47	46,53	47,47	50	170	42,0	46,1	51,8	85	375
A51	50,49	51,51	60	180	46,6	51,0	57,2	90	400
A56	55,44	56,56	70	200	52,2	57,0	63,8	100	425
A62	61,38	62,62	80	215	58,8	64,4	71,6	120	450
A68	67,32	68,68	90	240	65,6	71,7	79,8	150	475
A75	74,25	75,75	95	255	73,4	80,2	88,6	170	500

T_j = 25 °C

± 2% tolerance range.

BZX79-...	working voltage V_Z (V) at I_{Ztest} = 5 mA		differential resistance r_{diff} (Ω) at I_{Ztest} = 5 mA		temperature coefficient S_Z (mV/K) at I_{Ztest} = 5 mA			differential resistance r_{diff} (Ω) at I_Z = 1 mA	
	min.*	max.*	typ.	max.	min.	typ.	max.	typ.	max.
B2V4	2,35	2,45	70	100	−3,5	−1,6	0	275	600
B2V7	2,65	2,75	75	100	−3,5	−2,0	0	300	600
B3V0	2,94	3,06	80	95	−3,5	−2,1	0	325	600
B3V3	3,23	3,37	85	95	−3,5	−2,4	0	350	600
B3V6	3,53	3,67	85	90	−3,5	−2,4	0	375	600
B3V9	3,82	3,98	85	90	−3,5	−2,5	0	400	600
B4V3	4,21	4,39	80	90	−3,5	−2,5	0	410	600
B4V7	4,61	4,79	50	80	−3,5	−1,4	0,2	425	500
B5V1	5,00	5,20	40	60	−2,7	−0,8	1,2	400	480
B5V6	5,49	5,71	15	40	−2,0	1,2	2,5	80	400
B6V2	6,08	6,32	6	10	0,4	2,3	3,7	40	150
B6V8	6,66	6,94	6	15	1,2	3,0	4,5	30	80
B7V5	7,35	7,65	6	15	2,5	4,0	5,3	30	80
B8V2	8,04	8,36	6	15	3,2	4,6	6,2	40	80
B9V1	8,92	9,28	6	15	3,8	5,5	7,0	40	100
B10	9,80	10,20	8	20	4,5	6,4	8,0	50	150
B11	10,80	11,20	10	20	5,4	7,4	9,0	50	150
B12	11,80	12,20	10	25	6,0	8,4	10,0	50	150
B13	12,70	13,30	10	30	7,0	9,4	11,0	50	170
B15	14,70	15,30	10	30	9,2	11,4	13,0	50	200
B16	15,70	16,30	10	40	10,4	12,4	14,0	50	200
B18	17,60	18,40	10	45	12,4	14,4	16,0	50	225
B20	19,60	20,40	15	55	14,4	16,4	18,0	60	225
B22	21,60	22,40	20	55	16,4	18,4	20,0	60	250
B24	23,50	24,50	25	70	18,4	20,4	22,0	60	250
	at I_{Ztest} = 2 mA		at I_{Ztest} = 2 mA		at I_{Ztest} = 2 mA			at I_Z = 0,5 mA	
B27	26,50	27,50	25	80	21,4	23,4	25,3	65	300
B30	29,40	30,60	30	80	24,4	26,6	29,4	70	300
B33	32,30	33,70	35	80	27,4	29,7	33,4	75	325
B36	35,30	36,70	35	90	30,4	33,0	37,4	80	350
B39	38,20	39,80	40	130	33,4	36,4	41,2	80	350
B43	42,10	43,90	45	150	37,6	41,2	46,6	85	375
B47	46,10	47,90	50	170	42,0	46,1	51,8	85	375
B51	50,00	52,00	60	180	46,6	51,0	57,2	90	400
B56	54,90	57,10	70	200	52,2	57,0	63,8	100	425
B62	60,80	63,20	80	215	58,8	64,4	71,6	120	450
B68	66,60	69,40	90	240	65,6	71,7	79,8	150	475
B75	73,50	76,50	95	255	73,4	80,2	88,6	170	500

*When the real value is beyond this limit it is regulated as acceptable when it is within the 2% tolerance range.

T_j = 25 °C
± 3% tolerance range

BZX79	working voltage V_Z (V) at I_{Ztest} = 5 mA		differential resistance r_{diff} (Ω) at I_{Ztest} = 5 mA		temperature coefficient S_Z (mV/K) at I_{Ztest} = 5 mA	leakage current I_R at V_R	
	min.	max.	typ.	max.	typ.	μA	V
F2V4	2,33	2,47	70	100	−1,6	50	1
F2V7	2,62	2,78	75	100	−2,0	20	1
F3V0	2,91	3,09	80	100	−2,1	10	1
F3V3	3,20	3,40	85	100	−2,4	5	1
F3V6	3,49	3,71	85	100	−2,4	5	1
F3V9	3,78	4,02	85	100	−2,5	3	1
F4V3	4,17	4,43	80	100	−2,5	3	1
F4V7	4,56	4,84	50	100	−1,4	3	2
F5V1	4,95	5,25	40	80	−0,8	2	2
F5V6	5,43	5,77	15	40	1,2	1	2
F6V2	6,01	6,39	6	30	2,3	3	4
F6V8	6,60	7,00	6	20	3,0	2	4
F7V5	7,28	7,72	6	20	4,0	1	5
F8V2	7,95	8,45	6	20	4,6	0,7	5
F9V1	8,83	9,37	6	20	5,5	0,5	6
F10	9,70	10,30	8	25	6,4	0,2	7
F11	10,67	11,33	10	25	7,4	0,1	8
F12	11,64	12,36	10	25	8,4	0,1	8
F13	12,61	13,39	10	35	9,4	0,1	8
F15	14,55	15,45	10	40	11,4	0,05	10
F16	15,50	16,50	10	45	12,4	0,05	
F18	17,50	18,50	10	50	14,4	0,05	
F20	19,40	20,60	15	60	16,4	0,05	
F22	21,30	22,70	20	70	18,4	0,05	
F24	23,30	24,70	25	80	20,4	0,05	
	at I_{Ztest} = 2 mA		at I_{Ztest} = 2 mA		at I_{Ztest} = 2 mA	at I_Z = 0,5 mA	
F27	26,20	27,80	25	80	23,4	0,05	0,7
F30	29,10	30,90	30	100	26,6	0,05	0,7
F33	32,00	34,00	35	120	29,7	0,05	0,7
F36	34,90	37,10	35	140	33,0	0,05	0,7
F39	37,80	40,20	40	150	36,4	0,05	0,7
F43	41,70	44,30	45	160	41,2	0,05	0,7
F47	45,60	48,40	50	170	46,1	0,05	0,7
F51	49,50	52,50	60	180	51,0	0,05	0,7
F56	54,30	57,70	70	200	57,0	0,05	0,7
F62	60,10	63,90	80	220	64,4	0,05	0,7
F68	66,00	70,00	90	240	71,7	0,05	0,7
F75	72,80	77,20	95	255	80,2	0,05	0,7

T_j = 25 °C

E24 (± 5%) logarithmic range

BZX79-...	working voltage V_Z (V) at I_{Ztest} = 5 mA		differential resistance r_{diff} (Ω) at I_{Ztest} = 5 mA		temperature coefficient S_Z (mV/K) at I_{Ztest} = 5 mA			differential resistance r_{diff} (Ω) at I_Z = 1 mA	
	min.	max.	typ.	max.	min.	typ.	max.	typ.	max.
C2V4	2,2	2,6	70	100	−3,5	−1,6	0	275	600
C2V7	2,5	2,9	75	100	−3,5	−2,0	0	300	600
C3V0	2,8	3,2	80	95	−3,5	−2,1	0	325	600
C3V3	3,1	3,5	85	95	−3,5	−2,4	0	350	600
C3V6	3,4	3,8	85	90	−3,5	−2,4	0	375	600
C3V9	3,7	4,1	85	90	−3,5	−2,5	0	400	600
C4V3	4,0	4,6	80	90	−3,5	−2,5	0	410	600
C4V7	4,4	5,0	50	80	−3,5	−1,4	0,2	425	500
C5V1	4,8	5,4	40	60	−2,7	−0,8	1,2	400	480
C5V6	5,2	6,0	15	40	−2,0	1,2	2,5	80	400
C6V2	5,8	6,6	6	10	0,4	2,3	3,7	40	150
C6V8	6,4	7,2	6	15	1,2	3,0	4,5	30	80
C7V5	7,0	7,9	6	15	2,5	4,0	5,3	30	80
C8V2	7,7	8,7	6	15	3,2	4,6	6,2	40	80
C9V1	8,5	9,6	6	15	3,8	5,5	7,0	40	100
C10	9,4	10,6	8	20	4,5	6,4	8,0	50	150
C11	10,4	11,6	10	20	5,4	7,4	9,0	50	150
C12	11,4	12,7	10	25	6,0	8,4	10,0	50	150
C13	12,4	14,1	10	30	7,0	9,4	11,0	50	170
C15	13,8	15,6	10	30	9,2	11,4	13,0	50	200
C16	15,3	17,1	10	40	10,4	12,4	14,0	50	200
C18	16,8	19,1	10	45	12,4	14,4	16,0	50	225
C20	18,8	21,2	15	55	14,4	16,4	18,0	60	225
C22	20,8	23,3	20	55	16,4	18,4	20,0	60	250
C24	22,8	25,6	25	70	18,4	20,4	22,0	60	250
	at I_{Ztest} = 2 mA		at I_{Ztest} = 2 mA		at I_{Ztest} = 2 mA			at I_Z = 0,5 mA	
C27	25,1	28,9	25	80	21,4	23,4	25,3	65	300
C30	28,0	32,0	30	80	24,4	26,6	29,4	70	300
C33	31,0	35,0	35	80	27,4	29,7	33,4	75	325
C36	34,0	38,0	35	90	30,4	33,0	37,4	80	350
C39	37,0	41,0	40	130	33,4	36,4	41,2	80	350
C43	40,0	46,0	45	150	37,6	41,2	46,6	85	375
C47	44,0	50,0	50	170	42,0	46,1	51,8	85	375
C51	48,0	54,0	60	180	46,6	51,0	57,2	90	400
C56	52,0	60,0	70	200	52,2	57,0	63,8	100	425
C62	58,0	66,0	80	215	58,8	64,4	71,6	120	450
C68	64,0	72,0	90	240	65,6	71,7	79,8	150	475
C75	70,0	79,0	95	255	73,4	80,2	88,6	170	500

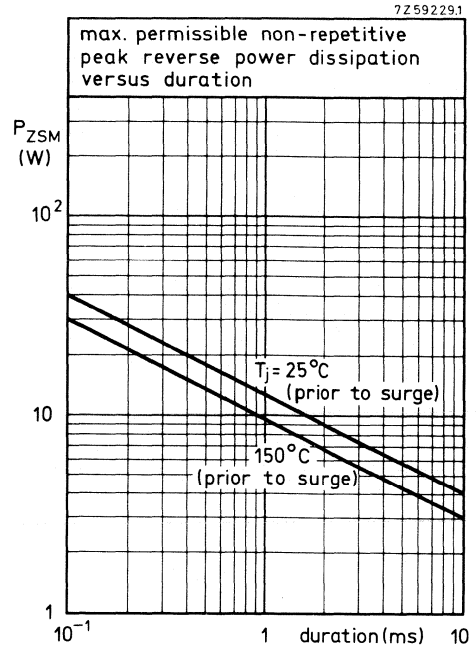

7Z59229.1
max. permissible non-repetitive peak reverse power dissipation versus duration
P_{ZSM} (W)
10^2
10
1
10^{-1}
1
duration (ms)
10
T_j = 25°C (prior to surge)
150°C (prior to surge)

Fig. 2.

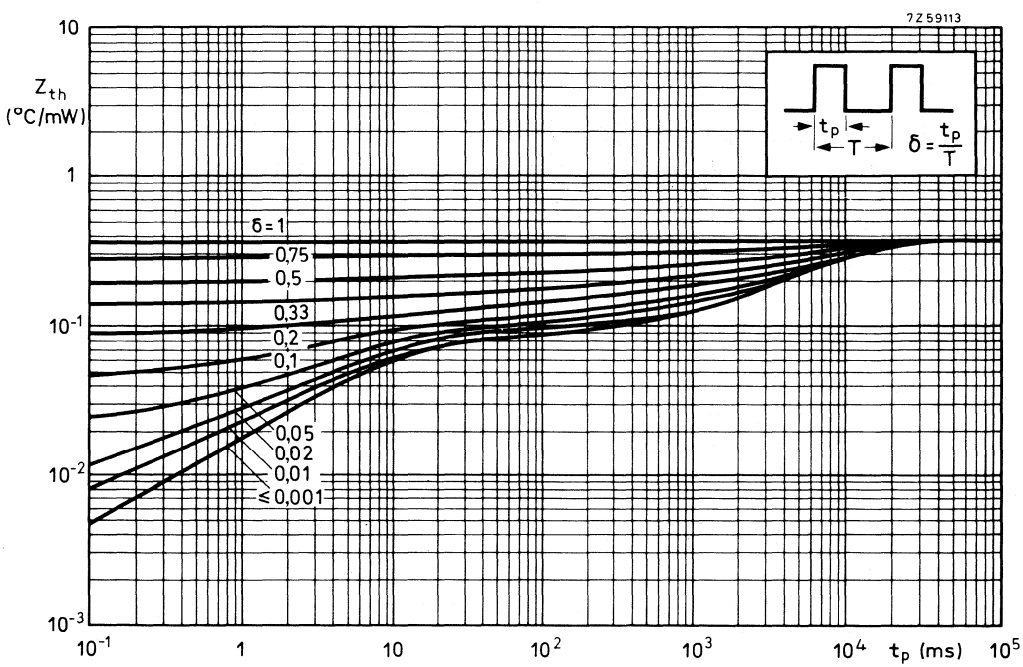

7Z59113
Z_{th} (°C/mW)
10
1
10^{-1}
10^{-2}
10^{-3}
10^{-1}
1
10
10^2
10^3
10^4
t_p (ms)
10^5
δ = 1
0,75
0,5
0,33
0,2
0,1
0,05
0,02
0,01
≤ 0,001
t_p
T
$\delta = \frac{t_p}{T}$

Fig. 3.

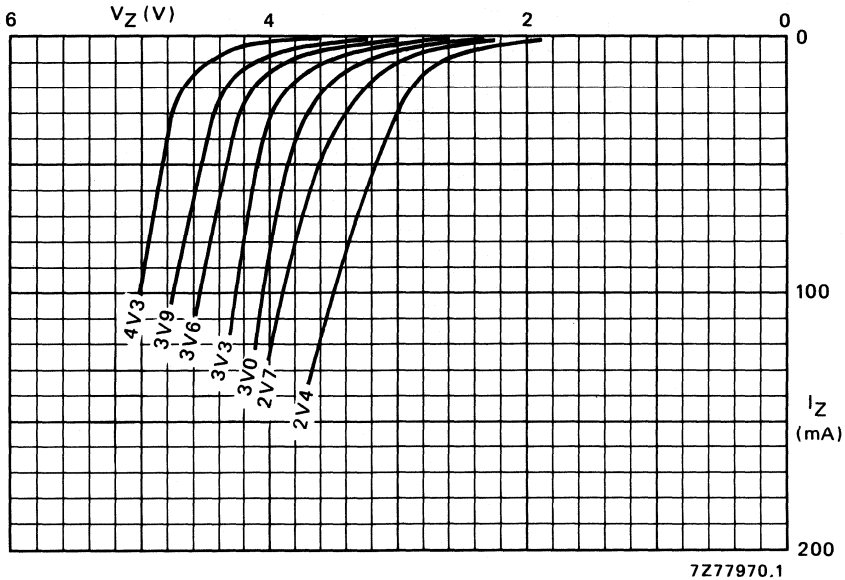


Fig. 4 Static characteristics; typical values; T_{amb} = 25 °C.

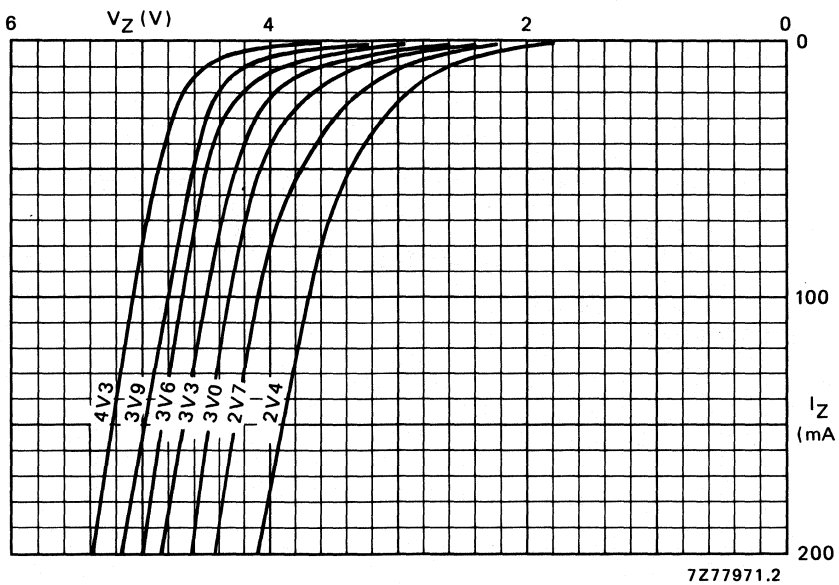


Fig. 5 Dynamic characteristics; typical values; T_j = 25 °C.

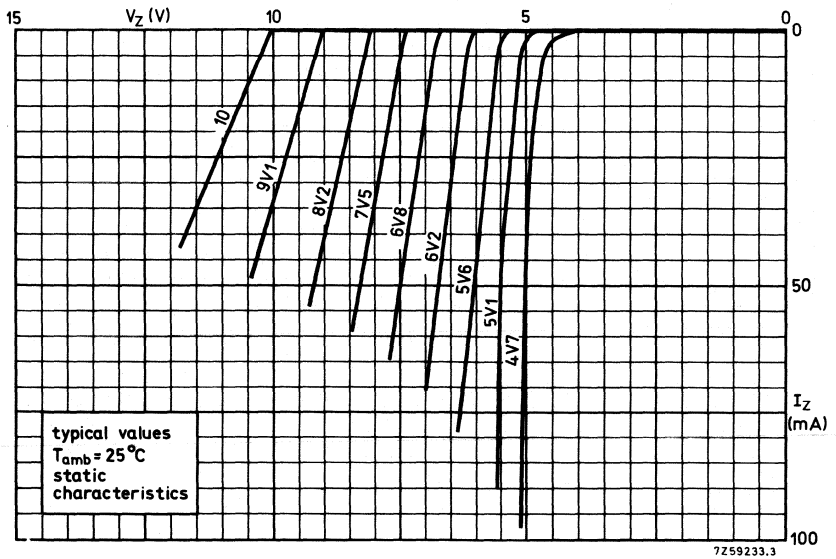

15
V_Z (V)
10
5
0
0
50
100
I_Z
(mA)
10
9V1
8V2
7V5
6V8
6V2
5V6
5V1
4V7
typical values
T_{amb} = 25°C
static
characteristics
7Z59233.3

Fig. 6.

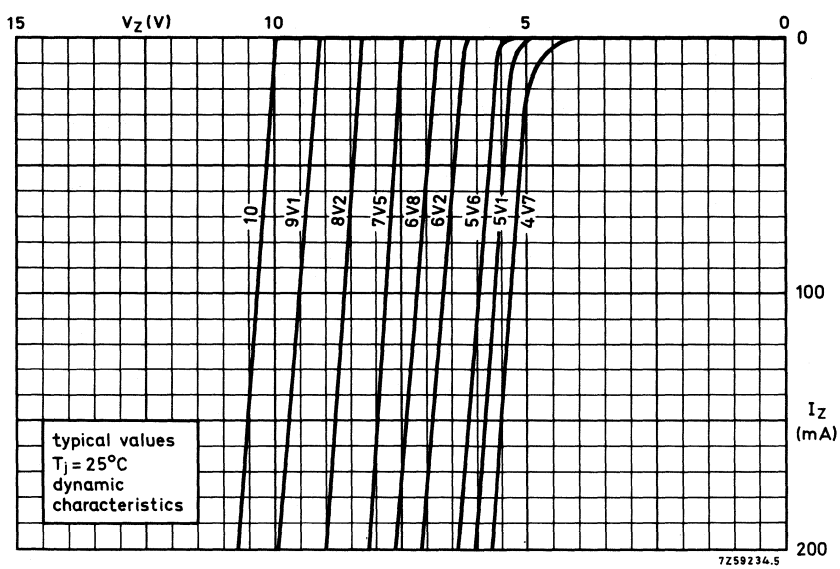

15
V_Z (V)
10
5
0
0
100
200
I_Z
(mA)
10
9V1
8V2
7V5
6V8
6V2
5V6
5V1
4V7
typical values
T_j = 25°C
dynamic
characteristics
7Z59234.5

Fig. 7.

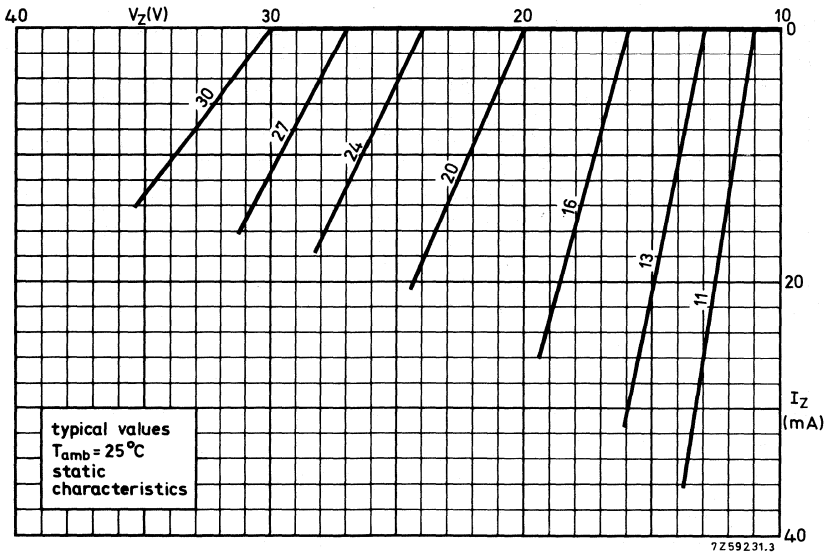

40
V_Z(V)
30
20
10
0
30
27
24
20
16
13
11
20
I_Z
(mA)
typical values
T_{amb} = 25°C
static
characteristics
40
7Z59231.3

Fig. 8.

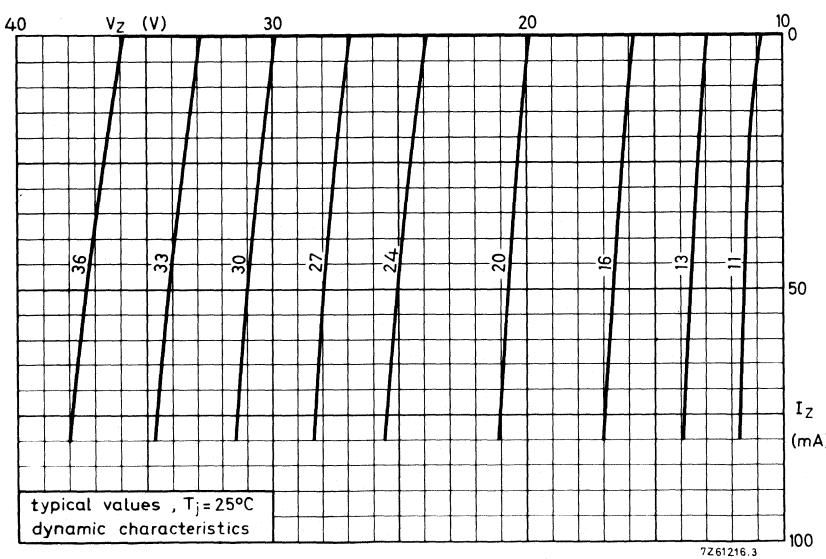

40
V_Z (V)
30
20
10
0
36
33
30
27
24
20
16
13
11
50
I_Z
(mA)
typical values , T_j = 25°C
dynamic characteristics
100
7Z61216.3

Fig. 9.

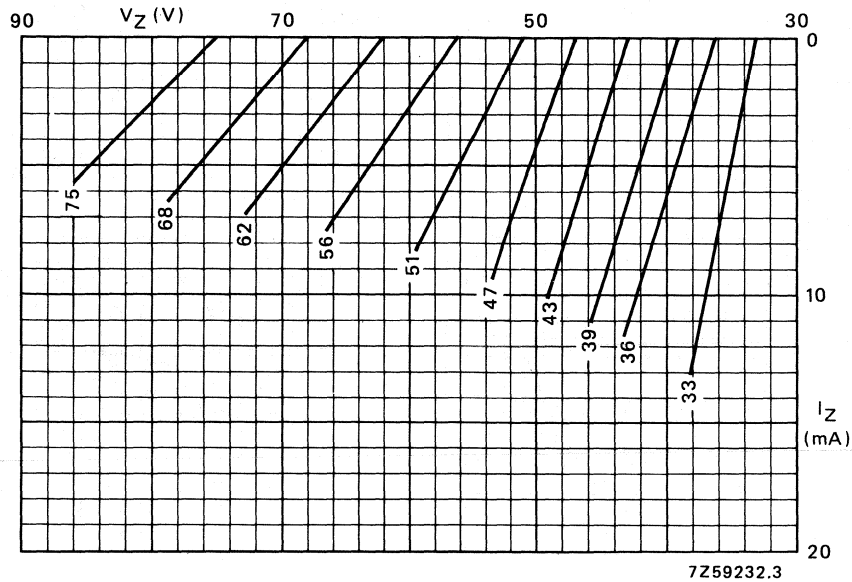


Fig. 10 Static characteristics; typical values; T_{amb} = 25 °C.

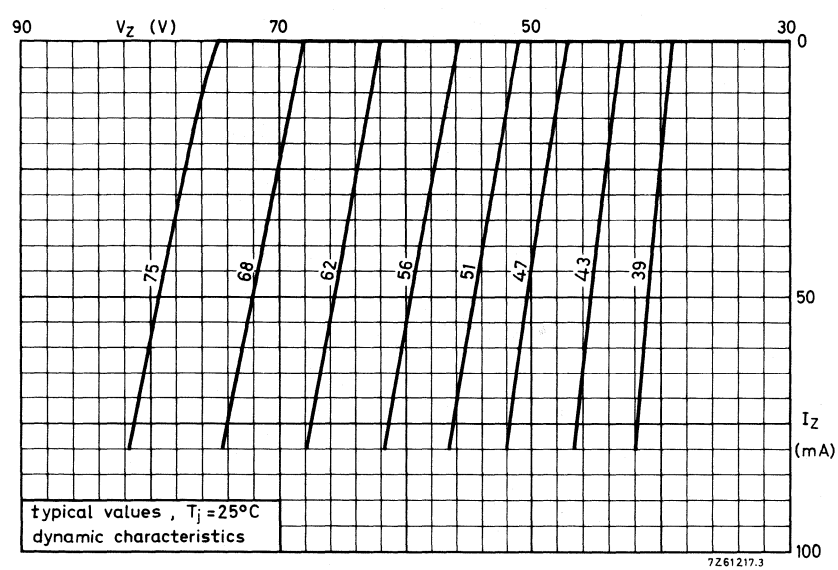


Fig. 11.

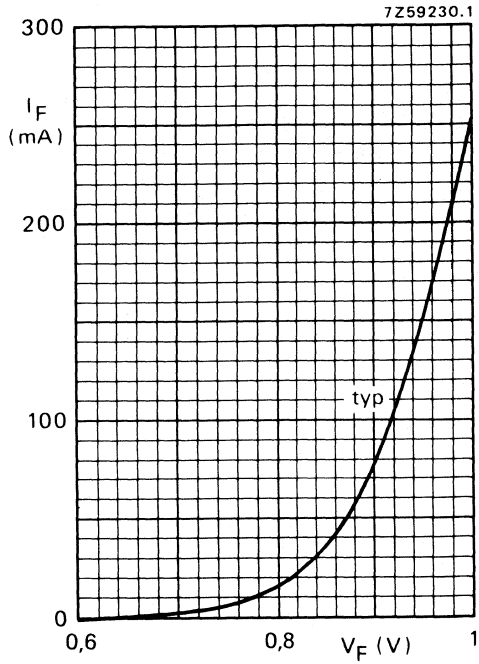


Fig. 12 T_j = 25 °C.

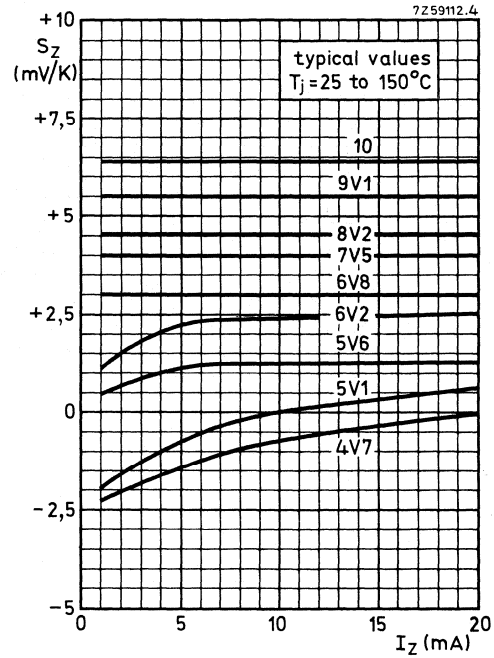


Fig. 13.

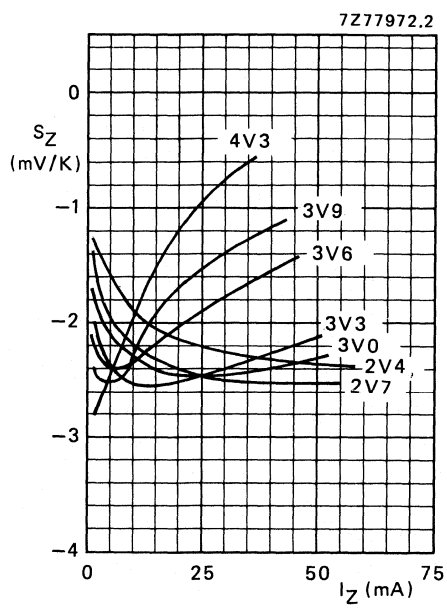


Fig. 14 Typical values; T_j = 25 to 150 °C.

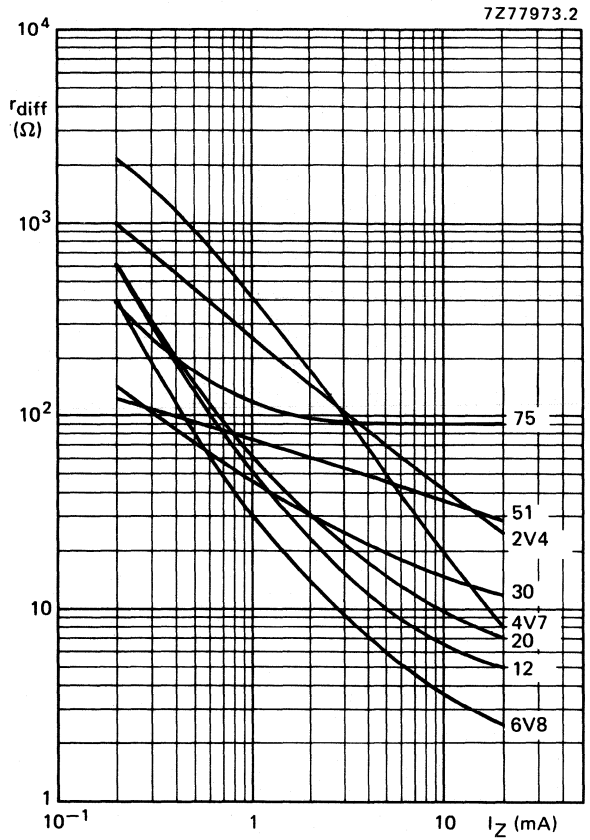


Fig. 15 Typical values; T_j = 25 °C; f = 1 kHz.

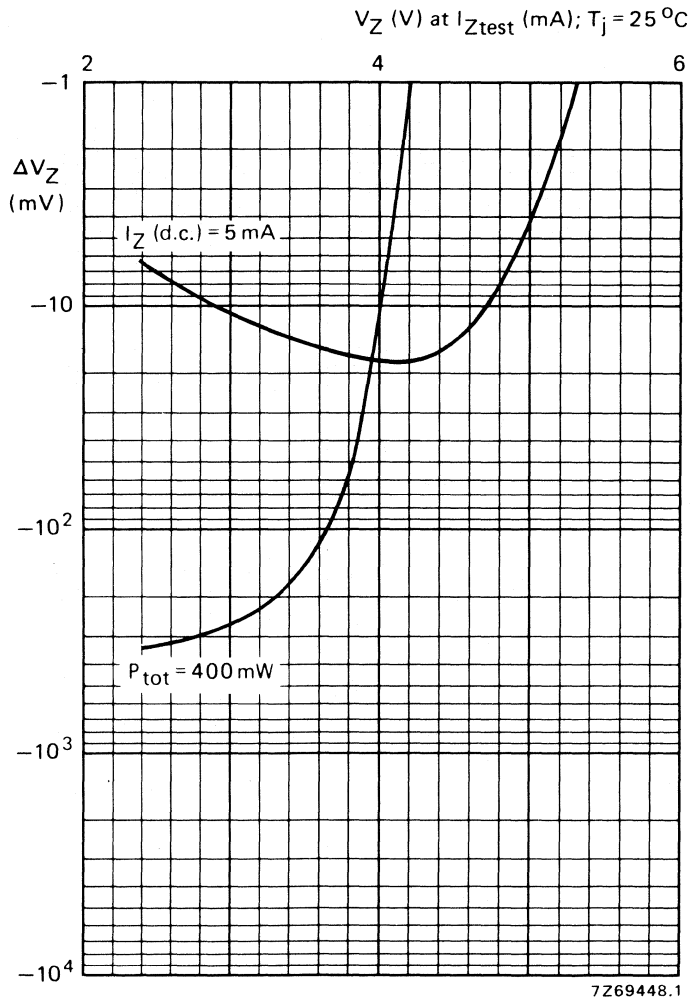


Fig. 16 Typical change of working voltage under operating conditions at T_{amb} = 25 °C.

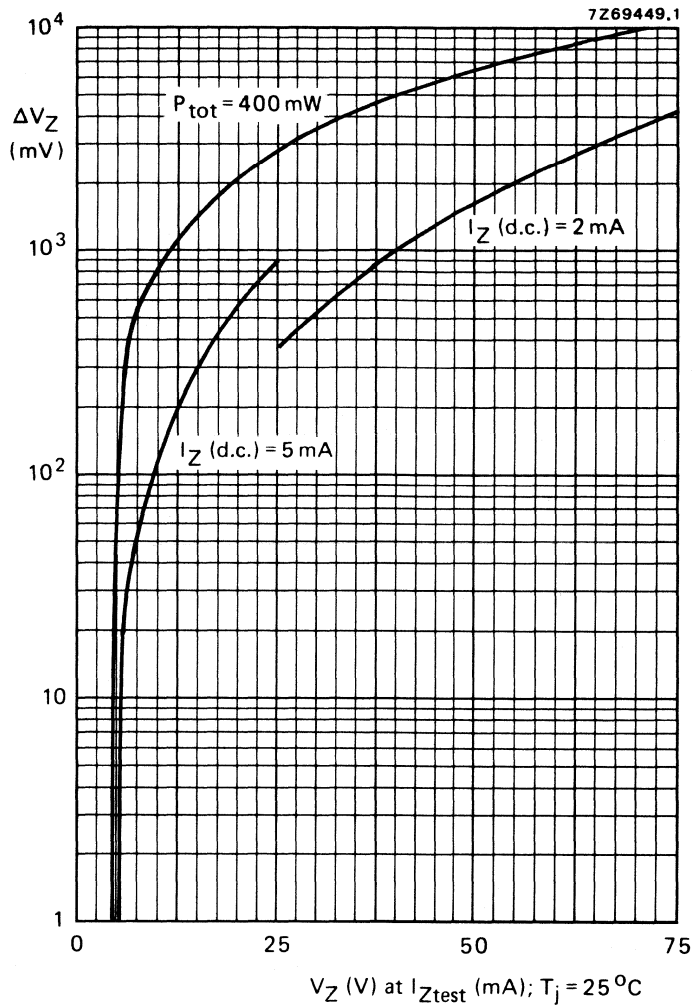


Fig. 17 Typical change of working voltage under operating conditions at T_{amb} = 25 °C.

VOLTAGE REGULATOR DIODES

Silicon planar voltage regulator diodes in hermetically sealed DO-41 glass envelopes intended for stabilization purposes. The series covers the normalized E24 (± 5%) range of nominal working voltages ranging from 3,6 V to 75 V.

QUICK REFERENCE DATA

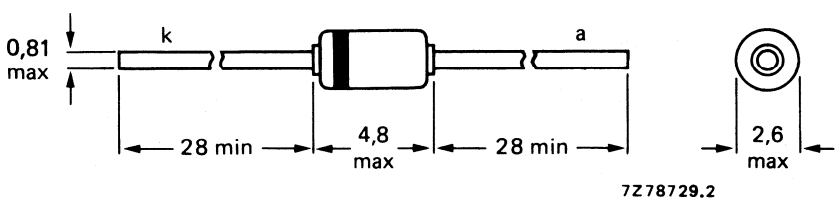
Working voltage range	V_Z	nom.	3,6 to 75 V
Total power dissipation	P_{tot}	max.	1,3 W*
Non-repetitive peak reverse power dissipation t_p = 100 μs; T_j = 25 °C	P_{ZSM}	max.	60 W
Junction temperature	T_j	max.	200 °C
Thermal resistance from junction to tie-point	$R_{th\ j\text{-}tp}$	=	110 K/W*

* If leads are kept at T_{tp} = 55 °C at 4 mm from body.

MECHANICAL DATA

Dimensions in mm

Fig. 1 DO-41 (SOD-66).



Cathode indicated by coloured band.
The diodes are type-branded.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Working current (d.c.)	I_Z	limited by $P_{tot\,max}$	
Non-repetitive peak reverse current t_p = 10 ms; half sine-wave; T_{amb} = 25 °C	I_{ZSM}	see table below	
Repetitive peak forward current	I_{FRM}	max.	250 mA
Total power dissipation (see also Fig. 2)	P_{tot}	max. max.	1,30 W* 1 W**
Non-repetitive peak reverse power dissipation t_p = 100 μs; T_j = 25 °C	P_{ZSM}	max.	60 W
Storage temperature	T_{stg}		−65 to + 200 °C
Junction temperature	T_j	max.	200 °C

THERMAL RESISTANCE

From junction to tie-point	$R_{th\,j\text{-}tp}$	=	110 K/W*
From junction to ambient mounted on a printed-circuit board	$R_{th\,j\text{-}a}$	=	175 K/W**

BZV85–. . . .	Non-repetitive peak reverse current I_{ZSM} (mA) max.
C3V6	2000
C3V9	1950
C4V3	1850
C4V7	1800
C5V1	1750
C5V6	1700
C6V2	1620
C6V8	1550
C7V5	1500
C8V2	1400
C9V1	1340
C10	1200
C11	1100
C12	1000
C13	900
C15	760
C16	700

BZV85–. . .	Non-repetitive peak reverse current I_{ZSM} (mA) max.
C18	600
C20	540
C22	500
C24	450
C27	400
C30	380
C33	350
C36	320
C39	296
C43	270
C47	246
C51	226
C56	208
C62	186
C68	171
C75	161

* If the temperature of the leads at 4 mm from the body are kept up to T_{tp} = 55 °C.

** Measured in still air up to T_{amb} = 25 °C and mounted on printed-circuit board with lead length of 10 mm and print copper area of 1 cm^2 per lead.

CHARACTERISTICS

T_j = 25 °C

Forward voltage at I_F = 50 mA V_F < 1,0 V

	working voltage E24 (± 5%) V_Z (V) at I_{Ztest}			test current I_{Ztest} (mA)	differential resistance r_{diff} (Ω) at I_{Ztest}	temperature coefficient S_Z(mV/K) at I_{Ztest}		reverse current I_R (μA) at V_R	test voltage V_R (V)
BZV85–. . . .	min.	nom.	max.		max.	min.	max.	max.	
C3V6	3,4	3,6	3,8	60	15	−3,5	−1,0	50	1,0
C3V9	3,7	3,9	4,1	60	15	−3,5	−1,0	10	1,0
C4V3	4,0	4,3	4,6	50	13	−2,7	0	5	1,0
C4V7	4,4	4,7	5,0	45	13	−2,0	0,7	3	1,0
C5V1	4,8	5,1	5,4	45	10	−0,5	2,2	3	2,0
C5V6	5,2	5,6	6,0	45	7	0	2,7	2	2,0
C6V2	5,8	6,2	6,6	35	4	0,6	3,6	2	3,0
C6V8	6,4	6,8	7,2	35	3,5	1,3	4,3	2	4,0
C7V5	7,0	7,5	7,9	35	3	2,5	5,5	1	4,5
C8V2	7,7	8,2	8,7	25	5	3,1	6,1	0,7	5,0
C9V1	8,5	9,1	9,6	25	5	3,8	7,2	0,7	6,5
C10	9,4	10	10,6	25	8	4,7	8,5	0,2	7,0
C11	10,4	11	11,6	20	10	5,3	9,3	0,2	7,7
C12	11,4	12	12,7	20	10	6,3	10,8	0,2	8,4
C13	12,4	13	14,1	20	10	7,4	12,0	0,2	9,1
C15	13,8	15	15,6	15	15	8,9	13,6	0,05	10,5
C16	15,3	16	17,1	15	15	10,7	15,4	0,05	11,0
C18	16,8	18	19,1	15	20	11,8	17,1	0,05	12,5
C20	18,8	20	21,2	10	24	13,6	19,1	0,05	14,0
C22	20,8	22	23,3	10	25	16,6	22,1	0,05	15,5
C24	22,8	24	25,6	10	30	18,3	24,3	0,05	17
C27	25,1	27	28,9	8	40	20,1	27,5	0,05	19
C30	28	30	32	8	45	22,4	32,0	0,05	21
C33	31	33	35	8	45	24,8	35,0	0,05	23
C36	34	36	38	8	50	27,2	39,9	0,05	25
C39	37	39	41	6	60	29,6	43,0	0,05	27
C43	40	43	46	6	75	34,0	48,3	0,05	30
C47	44	47	50	4	100	37,4	52,5	0,05	33
C51	48	51	54	4	125	40,8	56,5	0,05	36
C56	52	56	60	4	150	46,8	63,0	0,05	39
C62	58	62	66	4	175	52,2	72,5	0,05	43
C68	64	68	72	4	200	60,5	81,0	0,05	48
C75	70	75	80	4	225	66,5	88,0	0,05	53

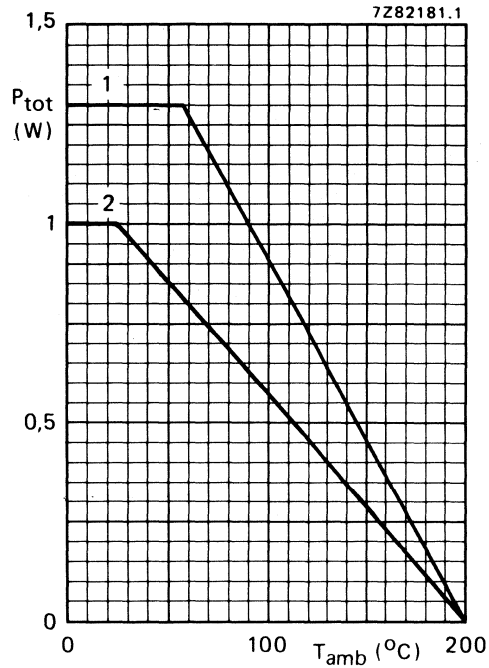


Fig. 2 Maximum permissible power dissipation versus ambient temperature.

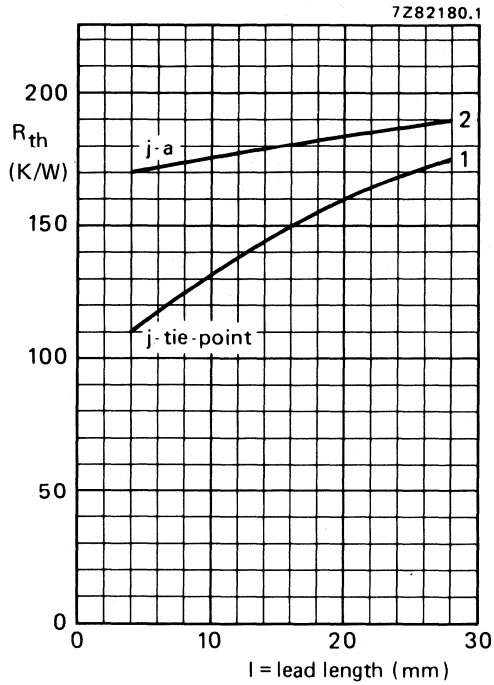


Fig. 3 Thermal resistance versus lead length.

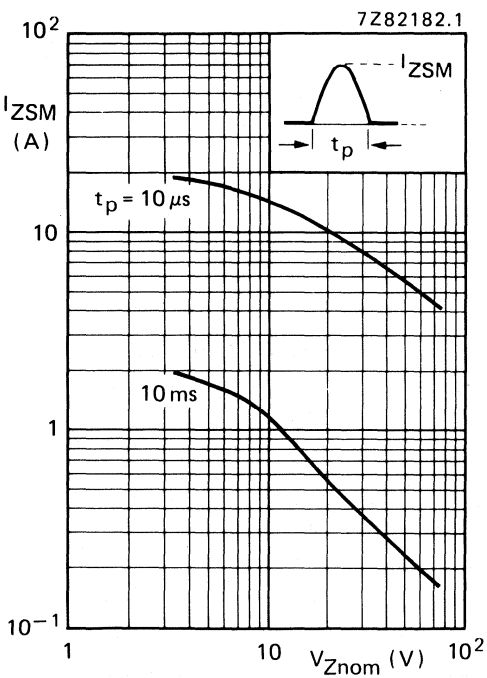


Fig. 4 Half sine-wave; T_{amb} = 25 °C.

Mounting methods (see Figs 2 and 3)

1. To tie-points (lead length = 4 mm in Fig. 2).
2. Mounted on a printed-circuit board (with lead length of 10 mm in Fig. 2) and print copper area of 1 cm² per lead.

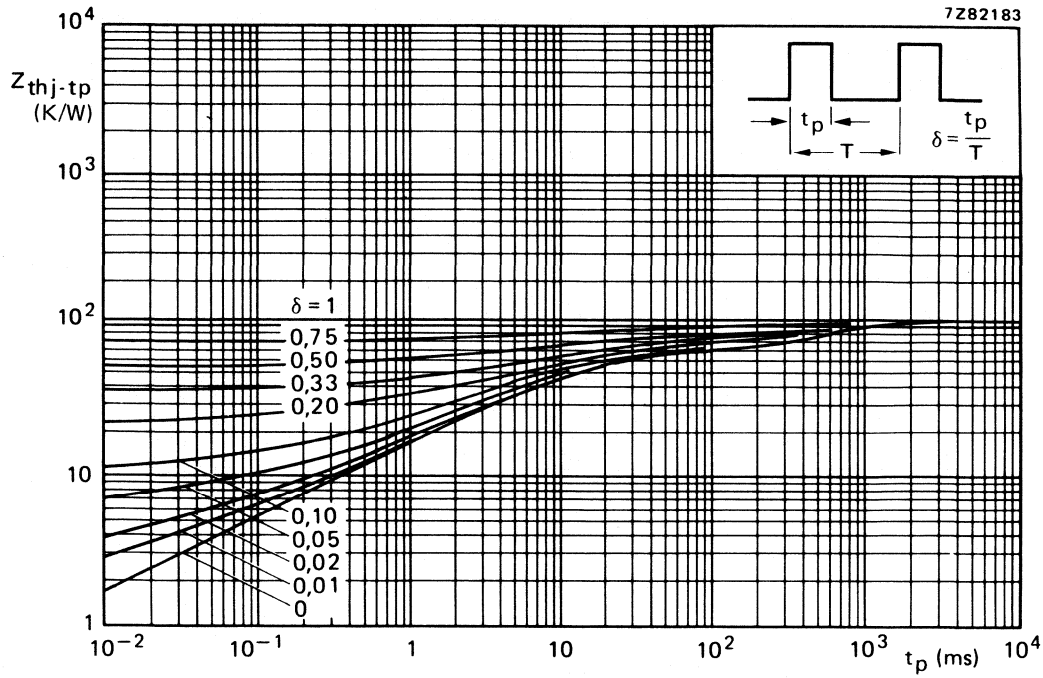


Fig. 5 Thermal impedance from junction to tie-point with a lead length of 4 mm.

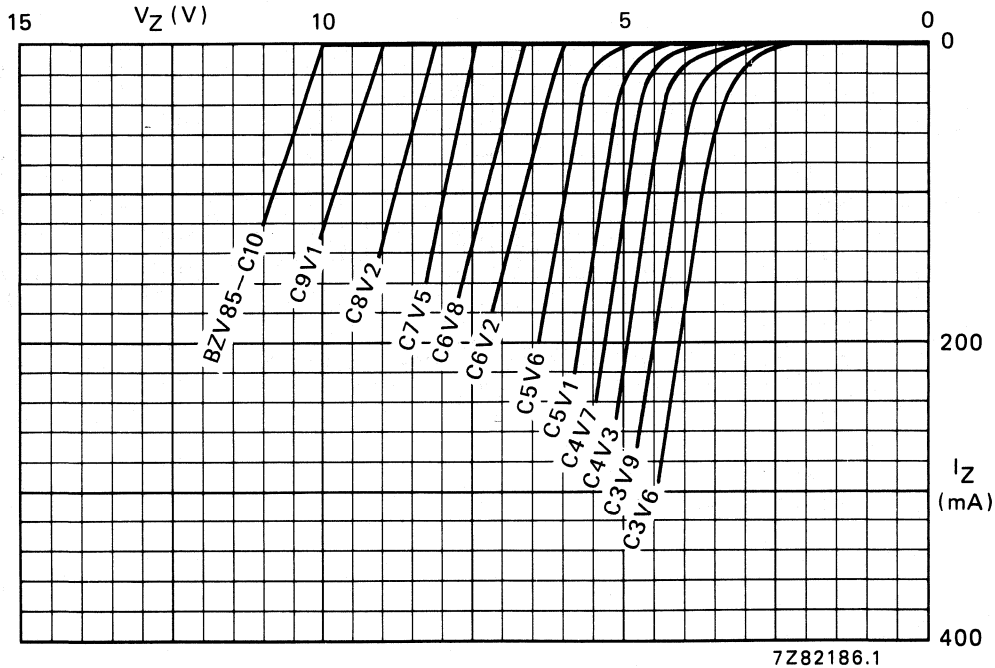


Fig. 6 Static characteristics; typical values; T_{amb} = 25 °C.

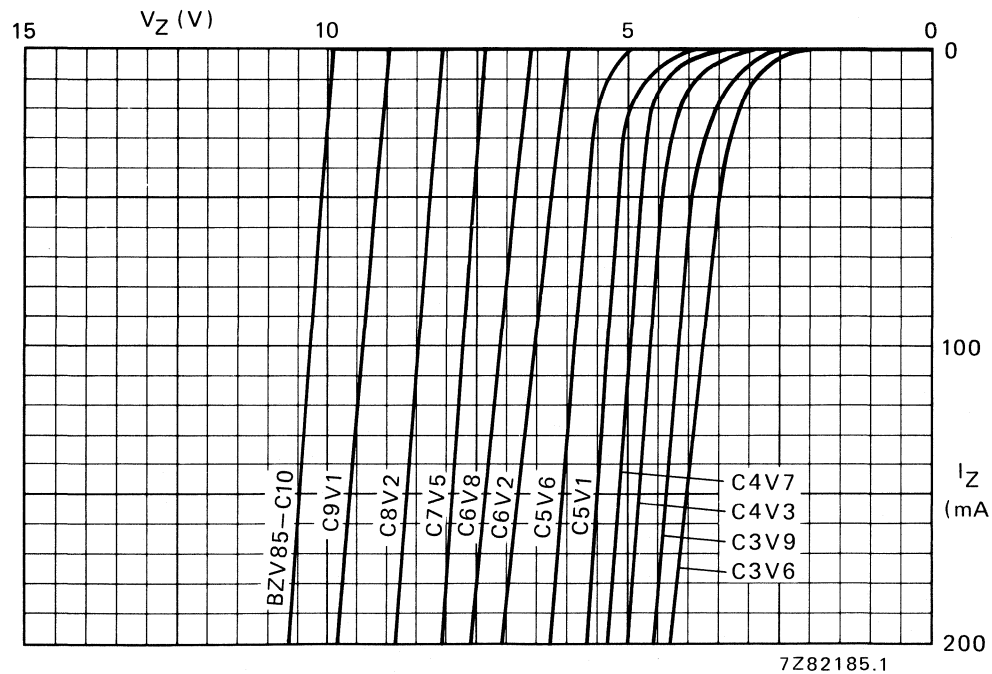


Fig. 7 Dynamic characteristics; typical values; T_j = 25 °C.

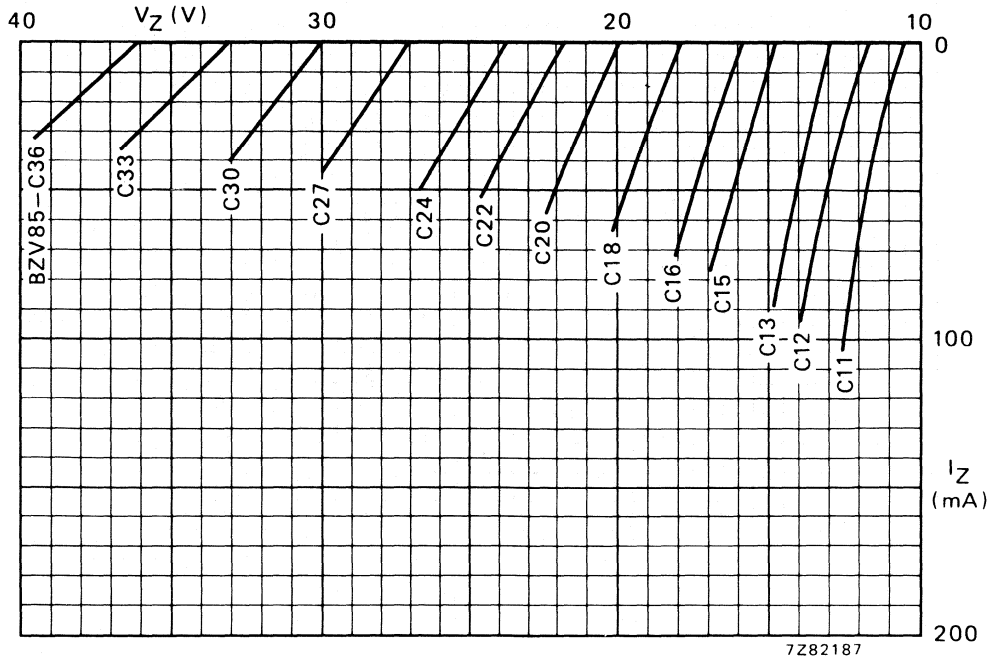


Fig. 8 Static characteristics; typical values; T_{amb} = 25 °C.

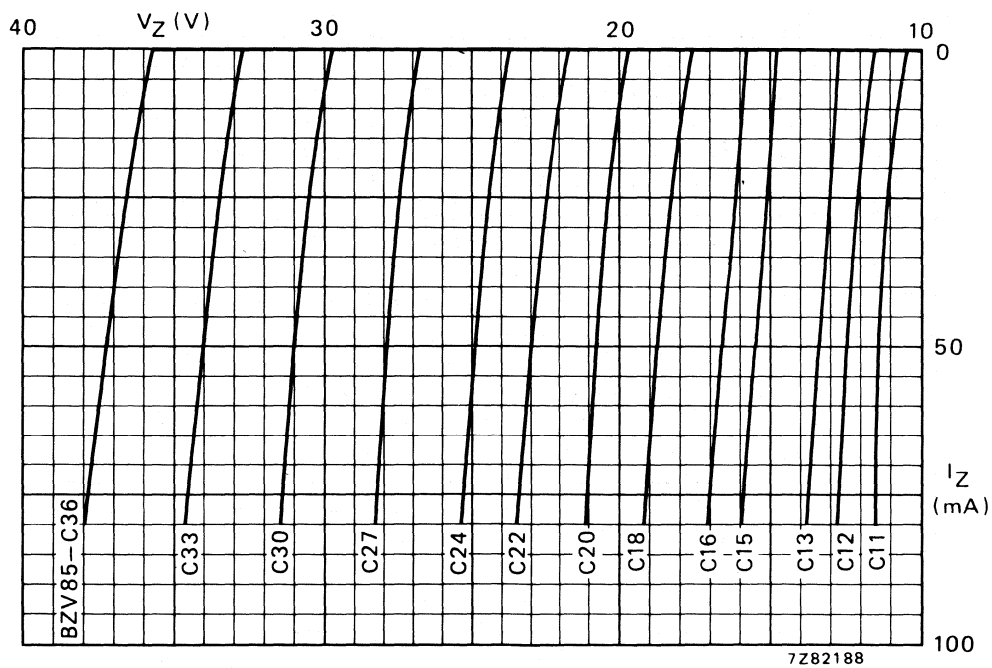


Fig. 9 Dynamic characteristics; typical values; T_j = 25 °C.

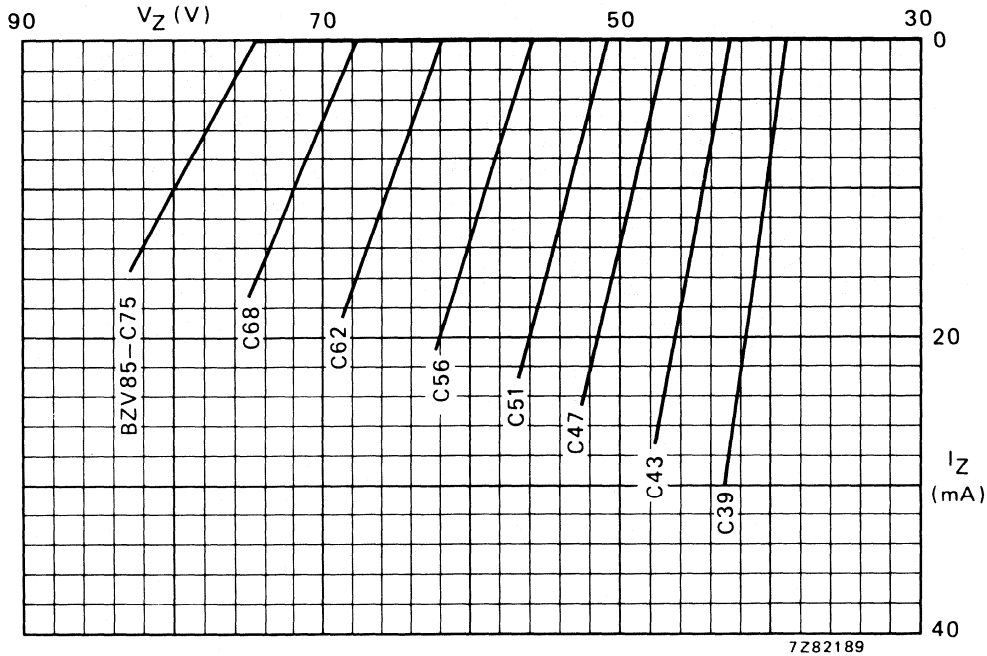


Fig. 10 Static characteristics; typical values; T_{amb} = 25 °C.

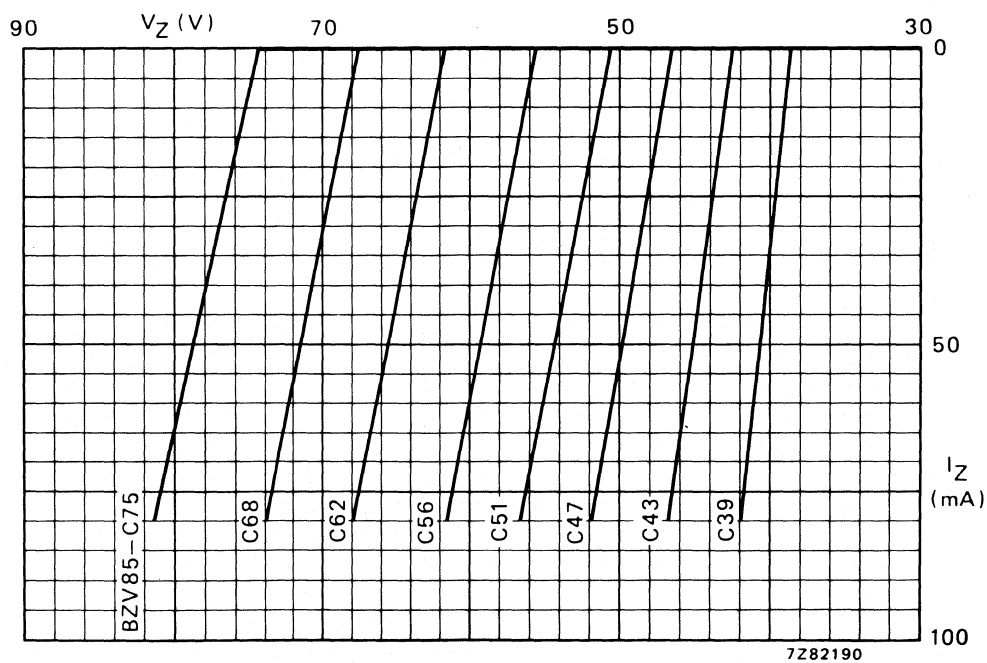


Fig. 11 Dynamic characteristics; typical values; T_j = 25 °C.

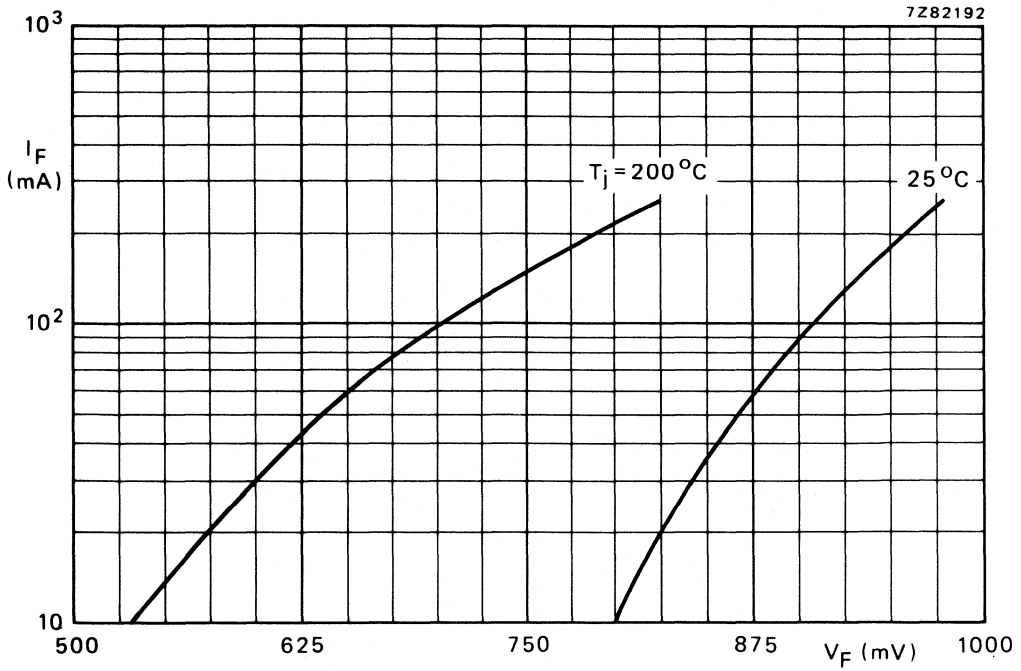


Fig. 12 Typical values.

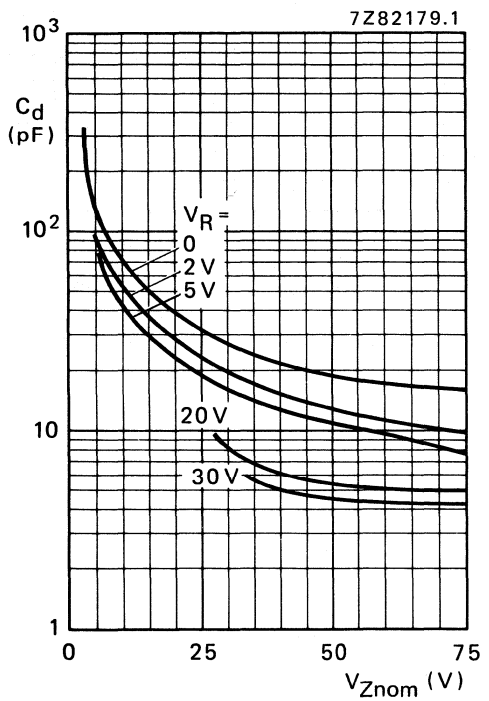


Fig. 13 f = 1 MHz; T_j = 25 °C; typical values.

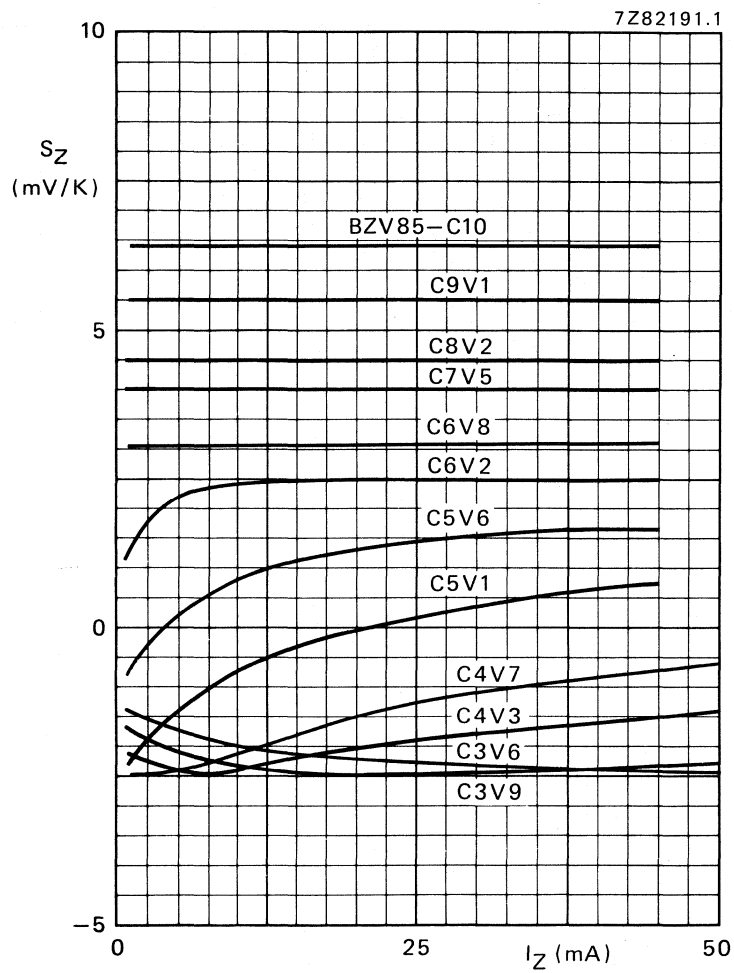


Fig. 14 T_j = 25 °C to 150 °C; typical values.

For types above 7,5 V the temperature coefficient is independent of current and can be read from the CHARACTERISTICS.

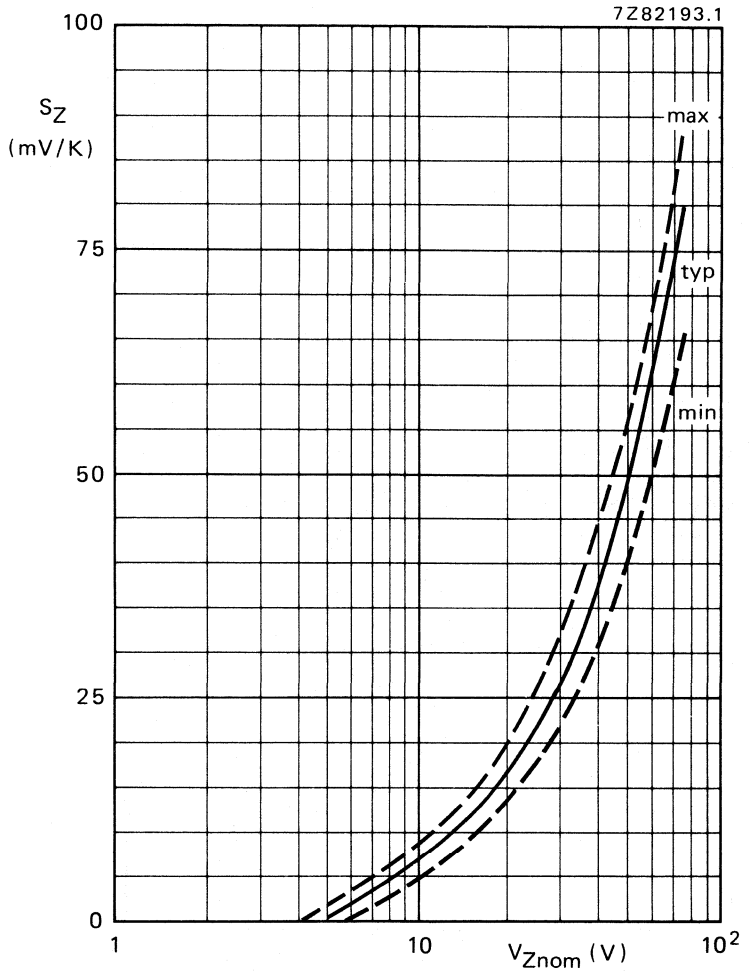


Fig. 15 $I_Z = I_{Ztest}$; T_j = 25 °C to 150 °C.

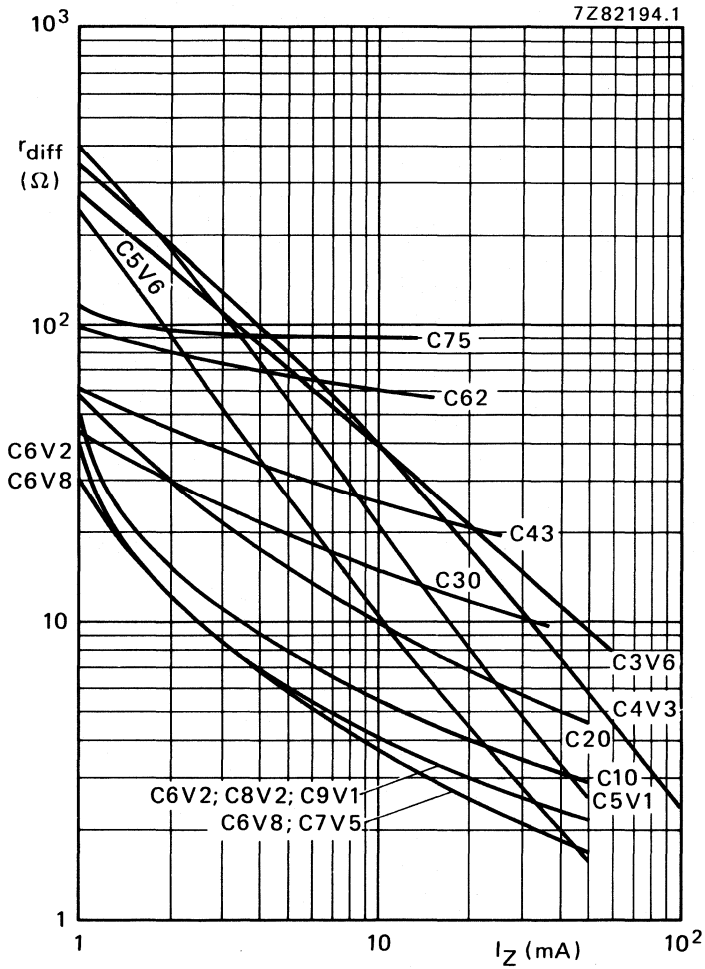


Fig. 16 f = 1 kHz; T_j = 25 °C; typical values.

Voltage regulator diodes BZD23 series

DESCRIPTION

Glass-passivated diodes in hermetically sealed axial-leaded implosion diode (ID) glass envelopes. They are intended for use as voltage regulator and transient suppressor diodes in medium power regulation and transient suppression circuits.

The series consists of BZD23-C3V6 to C6V8 and BZD23-C7V5 to C510, in the normalized E24 range.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	NOM.	MAX.	UNIT
V_Z	voltage regulator working voltage range			
	C3V6 - C6V8	3.6 to 6.8	–	V
	C7V5 - C270	7.5 to 270	–	V
P_{tot}	total power dissipation			
	C3V6 - C6V8	–	2	W
	C7V5 - C510	–	2.5	W
V_R	transient suppressor stand-off voltage			
	C7V5 - C510	6.2 to 430	–	V
P_{RSM}	non-repetitive peak reverse power dissipation	–	300	W

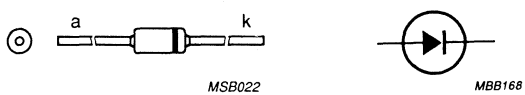


Fig.1 Simplified outline (SOD81) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

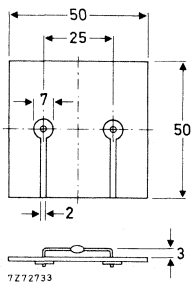
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
P_{tot}	total power dissipation	T_{tp} = 25 °C; lead length 10 mm			
	C3V6 - C6V8		–	2	W
	C7V5 - C510		–	2.5	W
		T_{amb} = 55 °C; PCB mounting; see Fig.2			
	C3V6 - C6V8		–	1	W
	C7V5 - C510		–	1	W
P_{RSM}	non-repetitive peak reverse power dissipation	t_p = 100 µs, square pulse; T_j = 25 °C (prior to surge); see also Fig.7			
	C3V6 - C6V8	see also Fig.8	–	300	W
	C7V5 - C510		–	300	W
		T_j = 25 °C (prior to surge); waveform 10/1000 exponential pulse; see Fig.3			
	C7V5 - C510		–	150	W
T_{stg}	storage temperature range				
	C3V6 - C6V8		–65	200	°C
	C7V5 - C510		–65	175	°C
T_j	junction temperature				
	C3V6 - C6V8		–	200	°C
	C7V5 - C510		–	175	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}tp}$	from junction to tie-point	note 1	
	C3V6 - C6V8		87 K/W
	C7V5 - C510		60 K/W
$R_{th\ j\text{-}a}$	from junction to ambient	note 2	
	C3V6 - C6V8		145 K/W
	C7V5 - C510		120 K/W

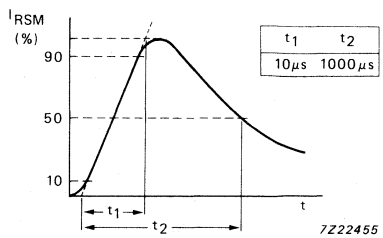
Notes

1. Lead length 10 mm.
2. Mounted on a 1.5 mm thick epoxy-glass printed circuit board; thickness of copper ≥ 40 µm; see Fig.2.



Dimensions in mm.

Fig.2 Printed circuit board mounting.



t_1 = 10 μs.

t_2 = 1000 μs.

Fig.3 Current pulse (in accordance with IEC 60-2, section 6).

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_F	forward voltage	I_F = 0.2 A; note 1		
	C3V6 - C6V8		1.2	V
	C7V5 - C510		1.2	V

Note

1. Measured under pulse conditions to avoid excessive dissipation.

CHARACTERISTICS

When used as voltage regulator diodes.

BZD23 XXXXX	WORKING VOLTAGE			DIFFERENTIAL RESISTANCE		TEMPERATURE COEFFICIENT		TEST CURRENT	REVERSE CURRENT at REVERSE VOLTAGE	
	V_Z (V)			r_{diff} (Ω)		S_Z (%/K)		I_Z (mA)	I_R (μA)	V_R (V)
	MIN.	NOM.	MAX.	TYP.	MAX.	MIN.	MAX.		MAX.	
C3V6	3.4	3.6	3.8	4	8	−0.14	−0.04	100	100	1
C3V9	3.7	3.9	4.1	4	8	−0.14	−0.04	100	50	1
C4V3	4.0	4.3	4.6	4	7	−0.12	−0.02	100	25	1
C4V7	4.4	4.7	5	3	7	−0.10	0	100	10	1
C5V1	4.8	5.1	5.4	3	6	−0.08	−0.02	100	5	1
C5V6	5.2	5.6	6	2	4	−0.04	0.04	100	10	2
C6V2	5.8	6.2	6.6	2	3	−0.01	0.06	100	5	2
C6V8	6.4	6.8	7.2	1	3	0	0.07	100	10	3
C7V5	7	7.5	7.9	1	2	0	0.07	100	50	3
C8V2	7.7	8.2	8.7	1	2	0.03	0.08	100	10	3
C9V1	8.5	9.1	9.6	2	4	0.03	0.08	50	10	5
C10	9.4	10	10.6	2	4	0.05	0.09	50	7	7.5
C11	10.4	11	11.6	4	7	0.05	0.10	50	3	8.2
C12	11.4	12	12.7	4	7	0.05	0.10	50	2	9.1
C13	12.4	13	14.1	5	10	0.05	0.10	50	1	10
C15	13.8	15	15.6	5	10	0.05	0.10	50	1	11
C16	15.3	16	17.1	6	15	0.06	0.11	25	1	12
C18	16.8	18	19.1	6	15	0.06	0.11	25	1	13
C20	18.8	20	21.2	6	15	0.06	0.11	25	1	15
C22	20.8	22	23.3	6	15	0.06	0.11	25	1	16
C24	22.8	24	25.6	7	15	0.06	0.11	25	1	18
C27	25.1	27	28.9	7	15	0.06	0.11	25	1	20
C30	28	30	32	8	15	0.06	0.11	25	1	22
C33	31	33	35	8	15	0.06	0.11	25	1	24
C36	34	36	38	21	40	0.06	0.11	10	1	27
C39	37	39	41	21	40	0.06	0.11	10	1	30
C43	40	43	46	24	45	0.07	0.12	10	1	33
C47	44	47	50	24	45	0.07	0.12	10	1	36
C51	48	51	54	25	60	0.07	0.12	10	1	39
C56	52	56	60	25	60	0.07	0.12	10	1	43
C62	58	62	66	25	80	0.08	0.13	10	1	47
C68	64	68	72	25	80	0.08	0.13	10	1	51
C75	70	75	79	30	100	0.08	0.13	10	1	56
C82	77	82	87	30	100	0.08	0.13	10	1	62

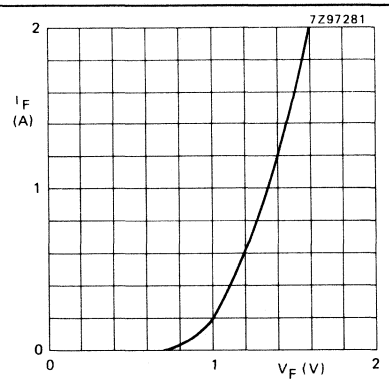
BZD23 XXXXX	WORKING VOLTAGE			DIFFERENTIAL RESISTANCE		TEMPERATURE COEFFICIENT		TEST CURRENT	REVERSE CURRENT at REVERSE VOLTAGE	
	V_Z (V)			r_{diff} (Ω)		S_Z (%/K)		I_Z (mA)	I_R (μA)	V_R (V)
	MIN.	NOM.	MAX.	TYP.	MAX.	MIN.	MAX.		MAX.	
C91	85	91	96	60	200	0.09	0.13	5	1	68
C100	94	100	106	60	200	0.09	0.13	5	1	75
C110	104	110	116	80	250	0.09	0.13	5	1	82
C120	114	120	127	80	250	0.09	0.13	5	1	91
C130	124	130	141	110	300	0.09	0.13	5	1	100
C150	138	150	156	130	300	0.09	0.13	5	1	110
C160	153	160	171	150	350	0.09	0.13	5	1	120
C180	168	180	191	180	400	0.09	0.13	5	1	130
C200	188	200	212	200	500	0.09	0.13	5	1	150
C220	208	220	233	350	750	0.09	0.13	2	1	160
C240	228	240	256	400	850	0.09	0.13	2	1	180
C270	251	270	289	450	1000	0.09	0.13	2	1	200

CHARACTERISTICS

When used as transient suppressor diodes; T_j = 25 °C.

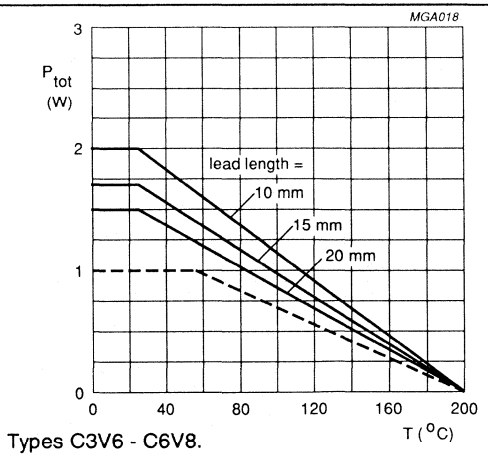
BZD23 XXXXX	CLAMPING VOLTAGE at NON-REPETITIVE PEAK (10/1000 PULSE) REVERSE CURRENT		REVERSE CURRENT AT RECOMMENDED STAND-OFF VOLTAGE	
	$V_{(CL)R}$ (V)	I_{RSM} (A)	I_R (μA)	V_R (V)
	MAX.		MAX.	
C7V5	11.3	13.3	1500	6.2
C8V2	12.3	12.2	1200	6.8
C9V1	13.3	11.3	100	7.5
C10	14.8	10.1	20	8.2
C11	15.7	9.6	5	9.1
C12	17	8.8	5	10
C13	18.9	7.9	5	11
C15	20.9	7.2	5	12
C16	22.9	6.6	5	13
C18	25.6	5.9	5	15
C20	28.4	5.3	5	16
C22	31	4.8	5	18
C24	33.8	4.4	5	20
C27	38.1	3.9	5	22
C30	42.2	3.6	5	24

BZD23 XXXXX	CLAMPING VOLTAGE at NON-REPETITIVE PEAK (10/1000 PULSE) REVERSE CURRENT		REVERSE CURRENT AT RECOMMENDED STAND-OFF VOLTAGE	
	$V_{(CL)R}$ (V)	I_{RSM} (A)	I_R (μA)	V_R (V)
	MAX.		MAX.	
C33	46.2	3.2	5	27
C36	50.1	3	5	30
C39	54.1	2.8	5	33
C43	60.7	2.5	5	36
C47	65.5	2.3	5	39
C51	70.8	2.1	5	43
C56	78.6	1.9	5	47
C62	86.5	1.7	5	51
C68	94.4	1.6	5	56
C75	103.5	1.5	5	62
C82	114	1.3	5	68
C91	126	1.2	5	75
C100	139	1.1	5	82
C110	152	1	5	91
C120	167	0.90	5	100
C130	185	0.81	5	110
C150	204	0.73	5	120
C160	224	0.67	5	130
C180	249	0.60	5	150
C200	276	0.54	5	160
C220	305	0.50	5	180
C240	336	0.45	5	200
C270	380	0.40	5	220
C300	419	0.36	5	240
C330	459	0.33	5	270
C360	498	0.30	5	300
C390	537	0.28	5	330
C430	603	0.25	5	360
C470	655	0.23	5	390
C510	707	0.21	5	430



T_j = 25 °C.

Fig.4 Forward current as a function of forward voltage, typical values.

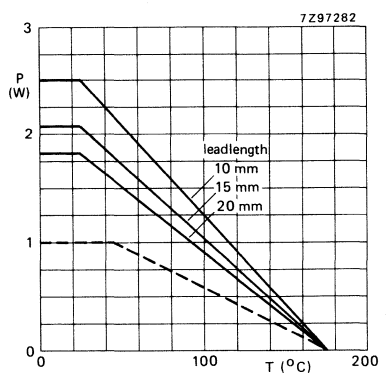


Types C3V6 - C6V8.

Solid line = tie-point temperature.

Dotted line = ambient temperature with device mounted as shown in Fig.2.

Fig.5 Maximum total power dissipation as a function of temperature.

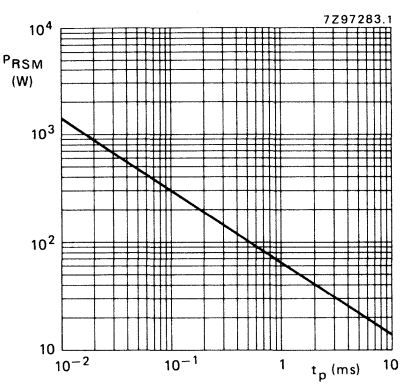


Types C7V5 - C270.

Solid line = tie-point temperature.

Dotted line = ambient temperature with device mounted as shown in Fig.2.

Fig.6 Maximum total power dissipation as a function of temperature.



T_j = 25 °C.

Fig.7 Maximum non-repetitive peak reverse power dissipation (square pulse), prior to surge.

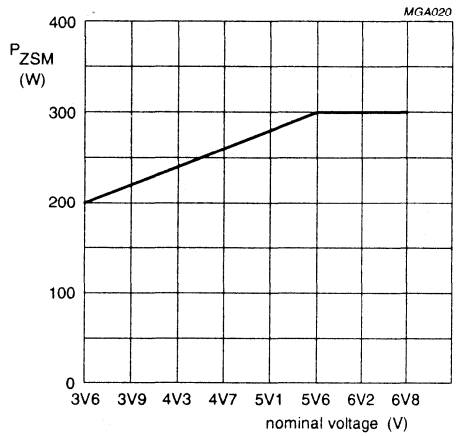
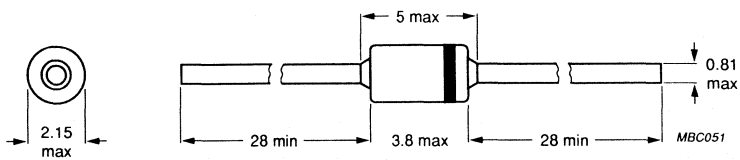


Fig.8 Non-repetitive peak reverse power dissipation as a function of nominal voltage.

PACKAGE OUTLINE



Dimensions in mm.

Marking band indicates the cathode.

Fig.9 SOD81.

Voltage regulator diodes BZD27 series

DESCRIPTION

Glass-passivated diodes in hermetically sealed leadless surface mounted implosion diode (SMID) glass envelopes. They are intended for use as voltage regulator and transient suppressor diodes in medium power regulation and transient suppression circuits.

The series consists of BZD27-C3V6 to C6V8 and BZD27-C7V5 to C510, in the normalized E24 range.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	NOM.	MAX.	UNIT
V_Z	voltage regulator working voltage range			
	C3V6 - C6V8	3.6 to 6.8	–	V
	C7V5 - C270	7.5 to 270	–	V
P_{tot}	total power dissipation			
	C3V6 - C6V8	–	1.7	W
	C7V5 - C510	–	2.3	W
V_R	transient suppressor stand-off voltage			
	C7V5 - C510	6.2 to 430	–	V
P_{RSM}	non-repetitive peak reverse power dissipation	–	300	W

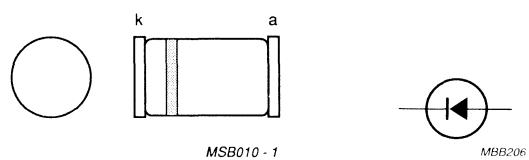


Fig.1 Simplified outline (SOD87) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

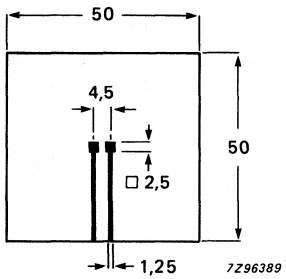
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
P_{tot}	total power dissipation	T_{tp} = 105 °C			
	C3V6 - C6V8		–	1.7	W
	C7V5 - C510		–	2.3	W
		PCB mounting; see Fig.2			
	C3V6 - C6V8	T_{amb} = 60 °C	–	0.8	W
	C7V5 - C510	T_{amb} = 55 °C	–	0.8	W
P_{RSM}	non-repetitive peak reverse power dissipation	t_p = 100 µs, square pulse; T_j = 25 °C (prior to surge); see also Fig.7			
	C3V6 - C6V8	see also Fig.8	–	300	W
	C7V5 - C510		–	300	W
		T_j = 25 °C (prior to surge); waveform 10/1000 exponential pulse; see Fig.3			
	C7V5 - C510		–	150	W
T_{stg}	storage temperature range				
	C3V6 - C6V8		–65	200	°C
	C7V5 - C510		–65	175	°C
T_j	junction temperature				
	C3V6 - C6V8		–	200	°C
	C7V5 - C510		–	175	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}tp}$	from junction to tie-point		
	C3V6 - C6V8		55 K/W
	C7V5 - C510		30 K/W
$R_{th\ j\text{-}a}$	from junction to ambient		
	C3V6 - C6V8	note 1	175 K/W
	C7V5 - C510		150 K/W

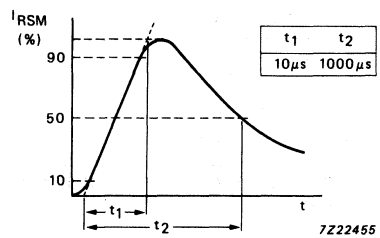
Note

1. Mounted on a 1.5 mm thick epoxy-glass printed circuit board; thickness of copper ≥ 40 µm; see Fig.2.



Dimensions in mm.

Fig.2 Printed circuit board mounting.



t_1 = 10 μs.

t_2 = 1000 μs.

Fig.3 Current pulse (in accordance with IEC 60-2, section 6).

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_F	forward voltage	I_F = 0.2 A; note 1		
	C3V6 - C6V8		1.2	V
	C7V5 - C510		1.2	V

Note

1. Measured under pulse conditions to avoid excessive dissipation.

CHARACTERISTICS

When used as voltage regulator diodes.

BZD27 XXXXX	WORKING VOLTAGE			DIFFERENTIAL RESISTANCE		TEMPERATURE COEFFICIENT		TEST CURRENT	REVERSE CURRENT at REVERSE VOLTAGE	
	V_Z (V)			r_{diff} (Ω)		S_Z (%/K)		I_Z (mA)	I_R (μA)	V_R (V)
	MIN.	NOM.	MAX.	TYP.	MAX.	MIN.	MAX.		MAX.	
C3V6	3.4	3.6	3.8	4	8	−0.14	−0.04	100	100	1
C3V9	3.7	3.9	4.1	4	8	−0.14	−0.04	100	50	1
C4V3	4.0	4.3	4.6	4	7	−0.12	−0.02	100	25	1
C4V7	4.4	4.7	5	3	7	−0.10	0	100	10	–
C5V1	4.8	5.1	5.4	3	6	−0.08	−0.02	100	5	1
C5V6	5.2	5.6	6	2	4	−0.04	0.04	100	10	2
C6V2	5.8	6.2	6.6	2	3	−0.01	0.06	100	5	2
C6V8	6.4	6.8	7.2	1	3	0	0.07	100	10	3
C7V5	7	7.5	7.9	1	2	0	0.07	100	50	3
C8V2	7.7	8.2	8.7	1	2	0.03	0.08	100	10	3
C9V1	8.5	9.1	9.6	2	4	0.03	0.08	50	10	5
C10	9.4	10	10.6	2	4	0.05	0.09	50	7	7.5
C11	10.4	11	11.6	4	7	0.05	0.10	50	3	8.2
C12	11.4	12	12.7	4	7	0.05	0.10	50	2	9.1
C13	12.4	13	14.1	5	10	0.05	0.10	50	1	10
C15	13.8	15	15.6	5	10	0.05	0.10	50	1	11
C16	15.3	16	17.1	6	15	0.06	0.11	25	1	12
C18	16.8	18	19.1	6	15	0.06	0.11	25	1	13
C20	18.8	20	21.2	6	15	0.06	0.11	25	1	15
C22	20.8	22	23.3	6	15	0.06	0.11	25	1	16
C24	22.8	24	25.6	7	15	0.06	0.11	25	1	18
C27	25.1	27	28.9	7	15	0.06	0.11	25	1	20
C30	28	30	32	8	15	0.06	0.11	25	1	22
C33	31	33	35	8	15	0.06	0.11	25	1	24
C36	34	36	38	21	40	0.06	0.11	10	1	27
C39	37	39	41	21	40	0.06	0.11	10	1	30
C43	40	43	46	24	45	0.07	0.12	10	1	33
C47	44	47	50	24	45	0.07	0.12	10	1	36
C51	48	51	54	25	60	0.07	0.12	10	1	39
C56	52	56	60	25	60	0.07	0.12	10	1	43
C62	58	62	66	25	80	0.08	0.13	10	1	47
C68	64	68	72	25	80	0.08	0.13	10	1	51
C75	70	75	79	30	100	0.08	0.13	10	1	56

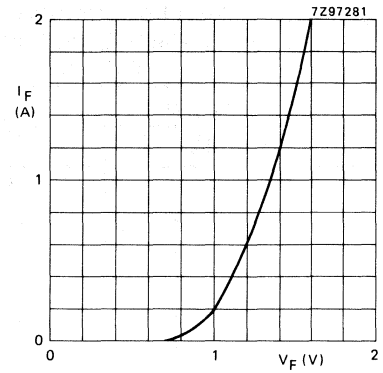
BZD27 XXXXX	WORKING VOLTAGE			DIFFERENTIAL RESISTANCE		TEMPERATURE COEFFICIENT		TEST CURRENT	REVERSE CURRENT at REVERSE VOLTAGE	
	V_Z (V)			r_{diff} (Ω)		S_Z (%/K)		I_Z (mA)	I_R (μA)	V_R (V)
	MIN.	NOM.	MAX.	TYP.	MAX.	MIN.	MAX.		MAX.	
C82	77	82	87	30	100	0.08	0.13	10	1	62
C91	85	91	96	60	200	0.09	0.13	5	1	68
C100	94	100	106	60	200	0.09	0.13	5	1	75
C110	104	110	116	80	250	0.09	0.13	5	1	82
C120	114	120	127	80	250	0.09	0.13	5	1	91
C130	124	130	141	110	300	0.09	0.13	5	1	100
C150	138	150	156	130	300	0.09	0.13	5	1	110
C160	153	160	171	150	350	0.09	0.13	5	1	120
C180	168	180	191	180	400	0.09	0.13	5	1	130
C200	188	200	212	200	500	0.09	0.13	5	1	150
C220	208	220	233	350	750	0.09	0.13	2	1	160
C240	228	240	256	400	850	0.09	0.13	2	1	180
C270	251	270	289	450	1000	0.09	0.13	2	1	200

CHARACTERISTICS

When used as transient suppressor diodes; T_j = 25 °C.

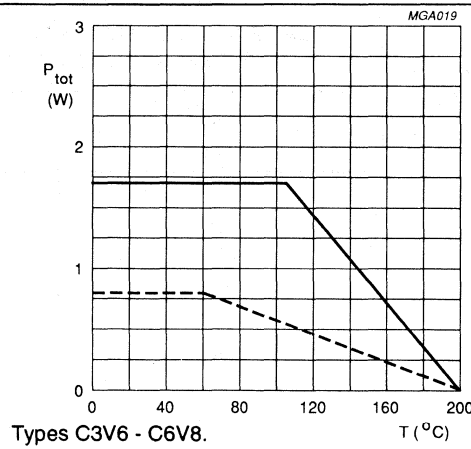
BZD27 XXXXX	CLAMPING VOLTAGE at NON-REPETITIVE PEAK REVERSE CURRENT (10/1000 PULSE)		REVERSE CURRENT AT RECOMMENDED STAND-OFF VOLTAGE	
	$V_{(CL)R}$ (V)	I_{RSM} (A)	I_R (μA)	V_R (V)
	MAX.		MAX.	
C7V5	11.3	13.3	1500	6.2
C8V2	12.3	12.2	1200	6.8
C9V1	13.3	11.3	100	7.5
C10	14.8	10.1	20	8.2
C11	15.7	9.6	5	9.1
C12	17	8.8	5	10
C13	18.9	7.9	5	11
C15	20.9	7.2	5	12
C16	22.9	6.6	5	13
C18	25.6	5.9	5	15
C20	28.4	5.3	5	16
C22	31	4.8	5	18
C24	33.8	4.4	5	20
C27	38.1	3.9	5	22

BZD27 XXXXX	CLAMPING VOLTAGE at NON-REPETITIVE PEAK REVERSE CURRENT (10/1000 PULSE)		REVERSE CURRENT AT RECOMMENDED STAND-OFF VOLTAGE	
	$V_{(CL)R}$ (V) MAX.	I_{RSM} (A)	I_R (μA) MAX.	V_R (V)
C30	42.2	3.6	5	24
C33	46.2	3.2	5	27
C36	50.1	3	5	30
C39	54.1	2.8	5	33
C43	60.7	2.5	5	36
C47	65.5	2.3	5	39
C51	70.8	2.1	5	43
C56	78.6	1.9	5	47
C62	86.5	1.7	5	51
C68	94.4	1.6	5	56
C75	103.5	1.5	5	62
C82	114	1.3	5	68
C91	126	1.2	5	75
C100	139	1.1	5	82
C110	152	1	5	91
C120	167	0.90	5	100
C130	185	0.81	5	110
C150	204	0.73	5	120
C160	224	0.67	5	130
C180	249	0.60	5	150
C200	276	0.54	5	160
C220	305	0.50	5	180
C240	336	0.45	5	200
C270	380	0.40	5	220
C300	419	0.36	5	240
C330	459	0.33	5	270
C360	498	0.30	5	300
C390	537	0.28	5	330
C430	603	0.25	5	360
C470	655	0.23	5	390
C510	707	0.21	5	430



T_j = 25 °C.

Fig.4 Forward current as a function of forward voltage, typical values.

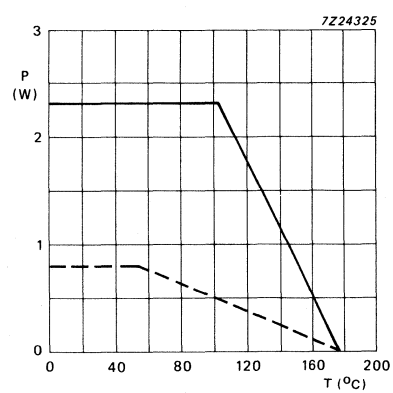


Types C3V6 - C6V8.

Solid line = tie-point temperature.

Dotted line = ambient temperature with device mounted as shown in Fig.2.

Fig.5 Maximum total power dissipation as a function of temperature.

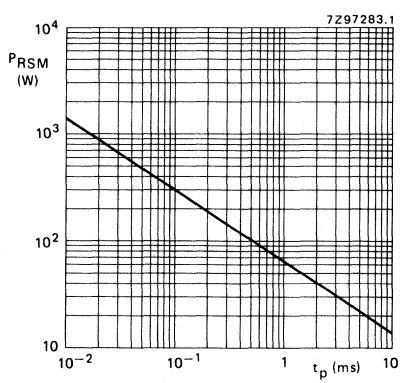


Types C7V5 - C270.

Solid line = tie-point temperature.

Dotted line = ambient temperature with device mounted as shown in Fig.2.

Fig.6 Maximum total power dissipation as a function of temperature.



T_j = 25 °C.

Fig.7 Maximum non-repetitive peak reverse power dissipation (square pulse), prior to surge.

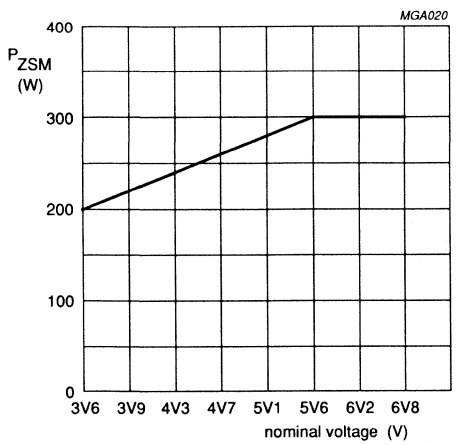
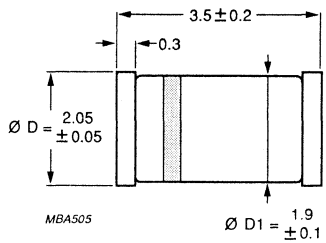


Fig.8 Non-repetitive peak reverse power dissipation as a function of nominal voltage.

PACKAGE OUTLINE



Dimensions in mm.

Marking band indicates the cathode.

Fig.9 SOD87.

REGULATOR DIODES

Glass passivated diodes in hermetically sealed axial-leaded glass envelopes. They are intended for use as voltage regulator and transient suppressor diode in medium power regulation and transient suppression circuits.

The series consists of BZT03-C7V5 to BZT03-C510 in the normalized E24 range.

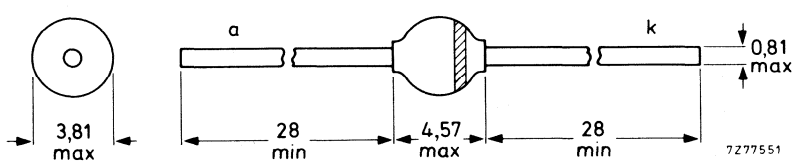
QUICK REFERENCE DATA

			voltage regulator	transient suppressor	
Working voltage range	V_Z	nom.	7.5 to 270		V
Stand-off voltage	V_R			6.2 to 430	V
Total power dissipation	P_{tot}	max.	3.25		W
Non-repetitive peak reverse power dissipation T_j = 25 °C; t_p = 100 μs	P_{RSM}	max.		600	W

MECHANICAL DATA

Dimensions in mm

Fig.1 SOD-57.



The marking band indicates the cathode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Total power dissipation			
T_{tp} = 25 °C; lead length 10 mm	P_{tot}	max.	3,25 W
T_{amb} = 45 °C; p.c.b. mounting (Fig. 2)	P_{tot}	max.	1,3 W
Repetitive peak reverse power dissipation	P_{ZRM}	max.	10 W
Non-repetitive peak reverse power dissipation;			
t_p = 100 μs, square pulse; T_j = 25 °C (prior to surge)	P_{RSM}	max.	600 W
waveform 10/1000 exponential pulse (Fig. 3);			
T_j = 25 °C (prior to surge)	P_{RSM}	max.	300 W
Storage temperature	T_{stg}		−65 to + 175 °C
Junction temperature	T_j	max.	175 °C

THERMAL RESISTANCE

Influence of mounting method

1. Thermal resistance from junction to tie-point at a lead length of 10 mm	$R_{th\ j\text{-}tp}$	=	46 K/W
2. Thermal resistance from junction to ambient when mounted on a 1,5 mm thick epoxy-glass printed-circuit board; Cu-thickness ⩾ 40 μm; Fig. 2 (see "Thermal model")	$R_{th\ j\text{-}a}$	=	100 K/W

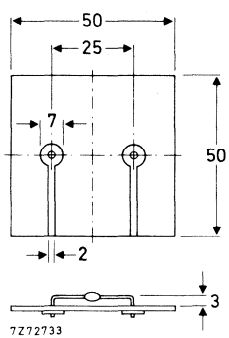


Fig. 2 Mounted on a printed-circuit board.

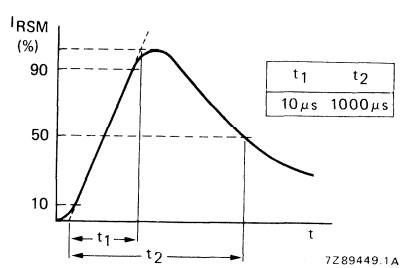


Fig. 3 Current pulse according to IEC 60-2, Section 6.

CHARACTERISTICS

Forward voltage			
I_F = 0,5 A; T_j = 25 °C	V_F	<	1,2 V

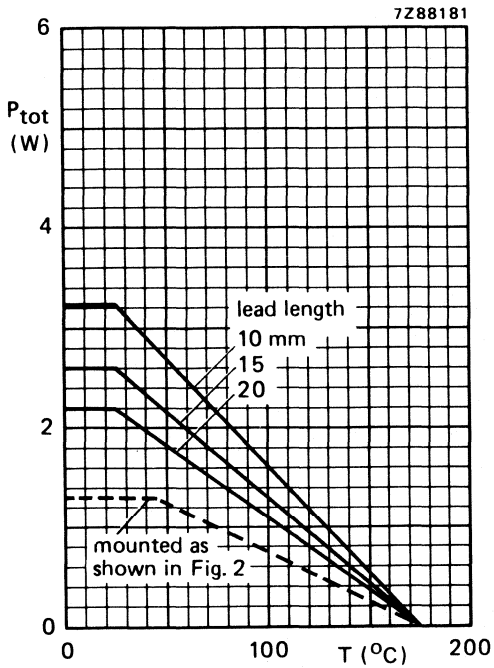


Fig. 4 Maximum total power dissipation as a function of temperature.
——— = T_{tp}; – – – – = T_{amb}; Fig. 2.

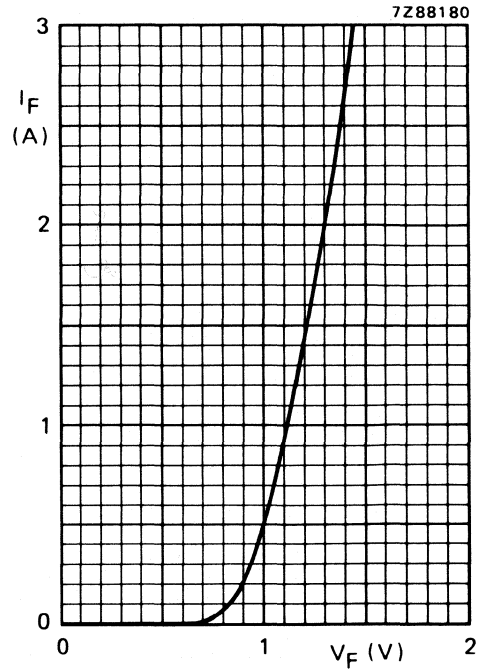


Fig. 5 Typical forward voltage drop T_j = 25 °C.

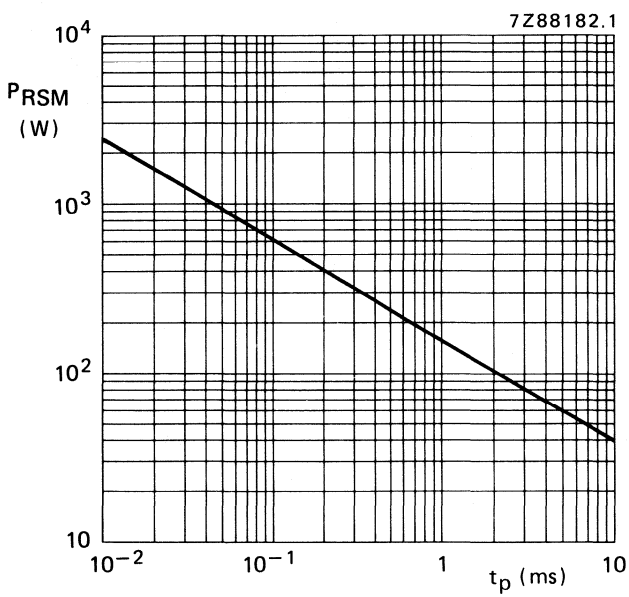


Fig. 6 Maximum non-repetitive peak reverse power dissipation; square current pulse; T_j = 25 °C prior to surge.

CHARACTERISTICS when used as voltage regulator diodes; T_j = 25 °C

BZT03-XXXX	working voltage V_Z V			differential resistance r_{diff} Ω		temperature coefficient S_Z %/K		test current I_Z mA	reverse current at I_R μA	reverse voltage V_R V
	min.	typ.	max.	typ.	max.	min.	max.		max.	
C7V5	7,0	7,5	7,9	1	2	0	0,07	100	750	5,6
C8V2	7,7	8,2	8,7	1	2	0,03	0,08	100	600	6,2
C9V1	8,5	9,1	9,6	2	4	0,03	0,08	50	20	6,8
C10	9,4	10,0	10,6	2	4	0,05	0,09	50	10	7,5
C11	10,4	11,0	11,6	4	7	0,05	0,10	50	4	8,2
C12	11,4	12,0	12,7	4	7	0,05	0,10	50	3	9,1
C13	12,4	13,0	14,1	5	10	0,05	0,10	50	2	10
C15	13,8	15,0	15,6	5	10	0,05	0,10	50	1	11
C16	15,3	16,0	17,1	6	15	0,06	0,11	25	1	12
C18	16,8	18,0	19,1	6	15	0,06	0,11	25	1	13
C20	18,8	20,0	21,2	6	15	0,06	0,11	25	1	15
C22	20,8	22,0	23,3	6	15	0,06	0,11	25	1	16
C24	22,8	24,0	25,6	7	15	0,06	0,11	25	1	18
C27	25,1	27,0	28,9	7	15	0,06	0,11	25	1	20
C30	28	30	32	8	15	0,06	0,11	25	1	22
C33	31	33	35	8	15	0,06	0,11	25	1	24
C36	34	36	38	21	40	0,06	0,11	10	1	27
C39	37	39	41	21	40	0,06	0,11	10	1	30
C43	40	43	46	24	45	0,07	0,12	10	1	33
C47	44	47	50	24	45	0,07	0,12	10	1	36
C51	48	51	54	25	60	0,07	0,12	10	1	39
C56	52	56	60	25	60	0,07	0,12	10	1	43
C62	58	62	66	25	80	0,08	0,13	10	1	47
C68	64	68	72	25	80	0,08	0,13	10	1	51
C75	70	75	79	30	100	0,08	0,13	10	1	56
C82	77	82	87	30	100	0,08	0,13	10	1	62
C91	85	91	96	60	200	0,09	0,13	5	1	68
C100	94	100	106	60	200	0,09	0,13	5	1	75
C110	104	110	116	80	250	0,09	0,13	5	1	82
C120	114	120	127	80	250	0,09	0,13	5	1	91
C130	124	130	141	110	300	0,09	0,13	5	1	100
C150	138	150	156	130	300	0,09	0,13	5	1	110
C160	153	160	171	150	350	0,09	0,13	5	1	120
C180	168	180	191	180	400	0,09	0,13	5	1	130
C200	188	200	212	200	500	0,09	0,13	5	1	150
C220	208	220	233	350	750	0,09	0,13	2	1	160
C240	228	240	256	400	850	0,09	0,13	2	1	180
C270	251	270	289	450	1000	0,09	0,13	2	1	200

CHARACTERISTICS when used as transient suppressor diodes; T_j = 25 °C

	breakdown voltage at test current		clamping voltage at non-repetitive peak reverse current (10/1000 pulse)		reverse current at recommended stand-off voltage	
	$V_{(BR)R}$	I_R	$V_{(CL)R}$	I_{RSM}	I_R	V_R
	V	mA	V	A	μA	V
BZT03-	min.		max.		max.	
C7V5	7.0	100	11.3	26.5	1500	6.2
C8V2	7.7	100	12.3	24.4	1200	6.8
C9V1	8.5	50	13.3	22.7	50	7.5
C10	9.4	50	14.8	20.3	20	8.2
C11	10.4	50	15.7	19.1	5	9.1
C12	11.4	50	17.0	17.7	5	10
C13	12.4	50	18.9	15.9	5	11
C15	13.8	50	20.9	14.4	5	12
C16	15.3	25	22.9	13.1	5	13
C18	16.8	25	25.6	11.7	5	15
C20	18.8	25	28.4	10.6	5	16
C22	20.8	25	31.0	9.7	5	18
C24	22.8	25	33.8	8.9	5	20
C27	25.1	25	38.1	7.9	5	22
C30	28	25	42.2	7.1	5	24
C33	31	25	46.2	6.5	5	27
C36	34	10	50.1	6.0	5	30
C39	37	10	54.1	5.5	5	33
C43	40	10	60.7	4.9	5	36
C47	44	10	65.5	4.6	5	39
C51	48	10	70.8	4.2	5	43
C56	52	10	78.6	3.8	5	47
C62	58	10	86.5	3.5	5	51
C68	64	10	94.4	3.2	5	56
C75	70	10	103.5	2.9	5	62
C82	77	10	114.0	2.6	5	68
C91	85	5	126	2.4	5	75
C100	94	5	139	2.2	5	82
C110	104	5	152	2.0	5	91
C120	114	5	167	1.8	5	100
C130	124	5	185	1.6	5	110
C150	138	5	204	1.5	5	120
C160	153	5	224	1.3	5	130
C180	168	5	249	1.2	5	150
C200	188	5	276	1.1	5	160
C220	208	2	305	1.0	5	180
C240	228	2	336	0.9	5	200
C270	251	2	380	0.8	5	220
C300	280	2	419	0.72	5	240
C330	310	2	459	0.65	5	270
C360	340	1	498	0.60	5	300
C390	370	1	537	0.56	5	330
C430	400	1	603	0.50	5	360
C470	440	1	655	0.45	5	390
C510	480	1	707	0.42	5	430

REGULATOR DIODES

Glass passivated diodes in hermetically sealed axial-leaded glass envelopes. They are intended for use as voltage regulator and transient suppressor diode in medium power regulation and transient suppression circuits.

The series consists of BZW03-C7V5 to BZW03-C510 in the normalized E24 range.

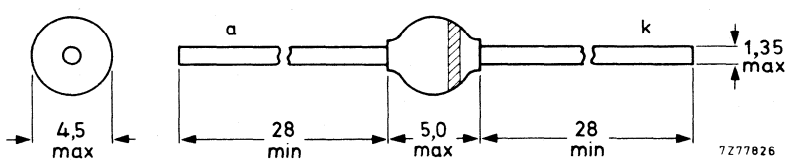
QUICK REFERENCE DATA

			voltage regulator	transient suppressor	
Working voltage range	V_Z	nom.	7,5 to 270		V
Stand-off voltage	V_R			6,2 to 430	V
Total power dissipation	P_{tot}	max.	6		W
Non-repetitive peak reverse power dissipation T_j = 25 °C; t_p = 100 μs	P_{RSM}			1000	W

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-64.



The marking band indicates the cathode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Total power dissipation			
T_{tp} = 25 °C; lead length 10 mm	P_{tot}	max.	6 W
T_{amb} = 45 °C; p.c.b. mounting (Fig. 2)	P_{tot}	max.	1,75 W
Repetitive peak reverse power dissipation	P_{ZRM}	max.	20 W
Non-repetitive peak reverse power dissipation			
t_p = 100 μs square pulse; T_j = 25 °C (prior to surge)	P_{RSM}	max.	1000 W
waveform 10/1000 exponential pulse (see Fig. 3), T_j = 25 °C (prior to surge)	P_{RSM}	max.	500 W
Storage temperature	T_{stg}		−65 to +175 °C
Junction temperature	T_j	max.	175 °C

THERMAL RESISTANCE

Influence of mounting method

1. Thermal resistance from junction to tie-point at a lead length of 10 mm	$R_{th\ j\text{-}tp}$	=	25 K/W
2. Thermal resistance from junction to ambient when mounted on a 1,5 mm thick epoxy-glass printed-circuit board; Cu-thickness ⩾ 40 μm; Fig. 2 (see "Thermal model")	$R_{th\ j\text{-}a}$	=	75 K/W

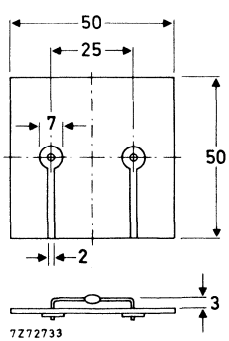


Fig. 2 Mounted on a printed-circuit board.

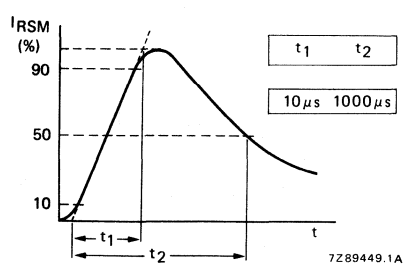


Fig. 3 Current pulse according to IEC 60-2, Section 6.

CHARACTERISTICS

Forward voltage			
I_F = 1 A; T_j = 25 °C	V_F	<	1,2 V

CHARACTERISTICS when used as voltage regulator diodes; T_j = 25 °C

	working voltage V_Z			differential resistance r_{diff}		temperature coefficient S_Z		test current	reverse current at reverse voltage	
	V			Ω		%/K		I_Z mA	I_R μA	V_R V
BZW03-	min.	nom.	max.	typ.	max.	min.	max.		max.	
C7V5	7,0	7,5	7,9	0,7	1,5	0	0,07	175	1500	5,6
C8V2	7,7	8,2	8,7	0,8	1,5	0,03	0,08	150	1200	6,2
C9V1	8,5	9,1	9,6	0,9	2,0	0,03	0,08	150	40	6,8
C10	9,4	10,0	10,6	1,0	2,0	0,05	0,09	125	20	7,5
C11	10,4	11,0	11,6	1,1	2,5	0,05	0,10	125	15	8,2
C12	11,4	12,0	12,7	1,1	2,5	0,05	0,10	100	10	9,1
C13	12,4	13,0	14,1	1,2	2,5	0,05	0,10	100	4	10
C15	13,8	15,0	15,6	1,2	2,5	0,05	0,10	75	2	11
C16	15,3	16,0	17,1	1,3	2,5	0,06	0,11	75	2	12
C18	16,8	18,0	19,1	1,3	2,5	0,06	0,11	65	2	13
C20	18,8	20,0	21,2	1,5	3	0,06	0,11	65	2	15
C22	20,8	22,0	23,3	1,6	3,5	0,06	0,11	50	2	16
C24	22,8	24,0	25,6	1,8	3,5	0,06	0,11	50	2	18
C27	25,1	27,0	28,9	2,5	5	0,06	0,11	50	2	20
C30	28	30	32	4	8	0,06	0,11	40	2	22
C33	31	33	35	5	10	0,06	0,11	40	2	24
C36	34	36	38	6	11	0,06	0,11	30	2	27
C39	37	39	41	7	14	0,06	0,11	30	2	30
C43	40	43	46	10	20	0,07	0,12	30	2	33
C47	44	47	50	12	25	0,07	0,12	25	2	36
C51	48	51	54	14	27	0,07	0,12	25	2	39
C56	52	56	60	18	35	0,07	0,12	20	2	43
C62	58	62	66	20	42	0,08	0,13	20	2	47
C68	64	68	72	22	44	0,08	0,13	20	2	51
C75	70	75	79	25	45	0,08	0,13	20	2	56
C82	77	82	87	30	65	0,08	0,13	15	2	62
C91	85	91	96	40	75	0,09	0,13	15	2	68
C100	94	100	106	45	90	0,09	0,13	12	2	75
C110	104	110	116	65	125	0,09	0,13	12	2	82
C120	114	120	127	90	170	0,09	0,13	10	2	91
C130	124	130	141	100	190	0,09	0,13	10	2	100
C150	138	150	156	150	330	0,09	0,13	8	2	110
C160	153	160	171	180	350	0,09	0,13	8	2	120
C180	168	180	191	210	430	0,09	0,13	5	2	130
C200	188	200	212	250	500	0,09	0,13	5	2	150
C220	208	220	233	350	700	0,09	0,13	5	2	160
C240	228	240	256	450	900	0,09	0,13	5	2	180
C270	251	270	289	600	1200	0,09	0,13	5	2	200

CHARACTERISTICS when used as transient suppressor diodes; T_j = 25 °C

clamping voltage at non-repetitive peak reverse current 10/1000 pulse		reverse current at recommended stand-off voltage		
$V_{(CL)R}$ V	I_{RSM} A	I_R μA	V_R V	
max.	max.	max.		BZW03-
11,3	44,2	3000	6,2	C7V5
12,3	40,6	2400	6,8	C8V2
13,3	37,6	100	7,5	C9V1
14,8	34,0	40	8,2	C10
15,7	31,8	30	9,1	C11
17,0	29,4	20	10	C12
18,9	26,4	10	11	C13
20,9	23,9	10	12	C15
22,9	21,8	10	13	C16
25,6	19,5	10	15	C18
28,4	17,6	10	16	C20
31	16,1	10	18	C22
33,8	14,8	10	20	C24
38,1	13,1	10	22	C27
42,2	11,8	10	24	C30
46,2	10,8	10	27	C33
50,1	10,0	10	30	C36
54,1	9,2	10	33	C39
60,7	8,2	10	36	C43
65,5	7,6	10	39	C47
70,8	7,0	10	43	C51
78,6	6,3	10	47	C56
86,5	5,8	10	51	C62
94,4	5,3	10	56	C68
103,5	4,8	10	62	C75
114,0	4,3	10	68	C82
126	3,9	10	75	C91
139	3,6	10	82	C100
152	3,3	10	91	C110
167	3,0	10	100	C120
185	2,7	10	110	C130
204	2,4	10	120	C150
224	2,2	10	130	C160
249	2,0	10	150	C180
276	1,8	10	160	C200
305	1,6	10	180	C220
336	1,5	10	200	C240
380	1,3	10	220	C270
419	1,2	10	240	C300
459	1,1	10	270	C330
498	1,0	10	300	C360
537	0,93	10	330	C390
603	0,83	10	360	C430
655	0,76	10	390	C470
707	0,71	10	430	C510

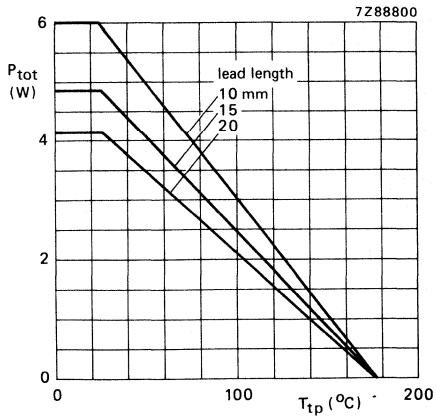


Fig. 4 Maximum total power dissipation as a function of tie-point temperature.

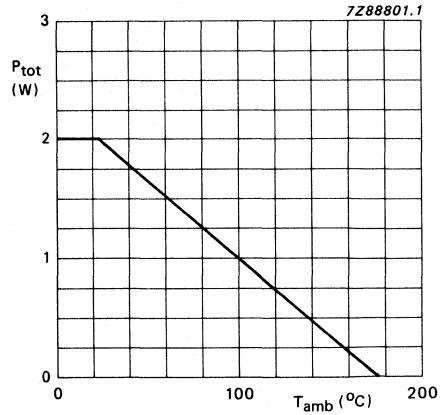


Fig. 5 Maximum total power dissipation as a function of ambient temperature, mounted as shown in Fig. 2.

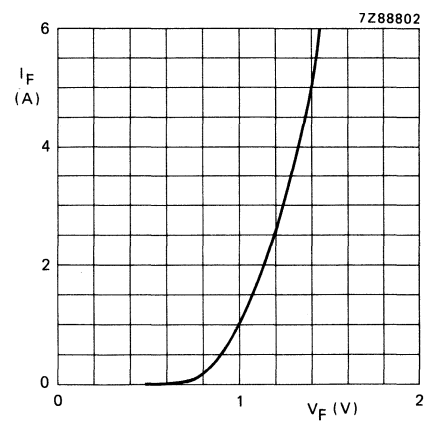


Fig. 6 Typical forward voltage drop at T_j = 25 °C.

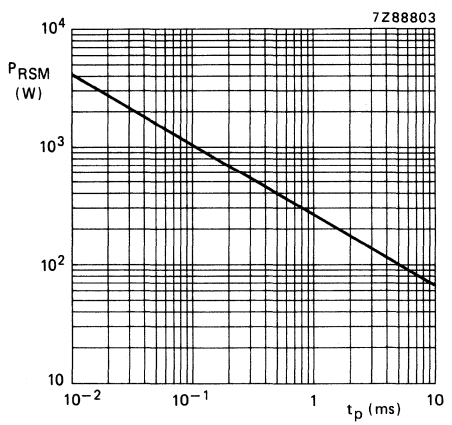


Fig. 7 Maximum non-repetitive peak reverse power dissipation; square current pulse; T_j = 25 °C prior to surge.

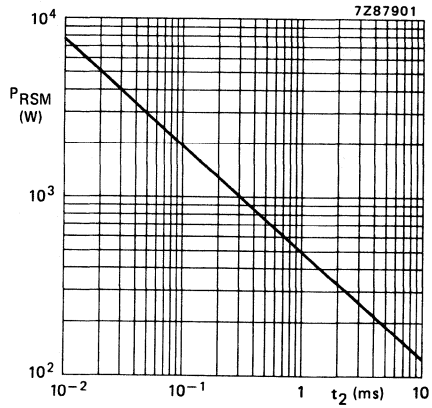


Fig. 8 Maximum non-repetitive peak reverse power dissipation; exponential pulse; T_j = 25 °C prior to surge.

EHT car ignition diode BYX120G

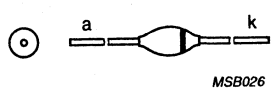
DESCRIPTION

EHT rectifier diodes in glass envelopes intended for use in high-voltage car ignition systems. The devices are designed to cope with the extreme temperature requirements in automotive applications and are capable of absorbing avalanche energy.

Because of the small envelope, the diode should be used in a suitable insulating medium.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage	–	3	kV
$V_{(BR)R}$	reverse avalanche breakdown voltage	3.5	–	kV
$I_{F(AV)}$	average forward current	–	100	mA
P_{RSM}	non-repetitive peak reverse power dissipation	–	3	kW
T_{amb}	ambient operating temperature	–	150	°C
		–	180	°C
t_{rr}	reverse recovery time	–	5	µs



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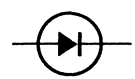

MBB168

Fig.1 Simplified outline (SOD88A) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage		–	3	kV
V_{RWM}	crest working reverse voltage		–	3	kV
$I_{F(AV)}$	average forward current		–	100	mA
I_{FRM}	repetitive peak forward current		–	5	A
I_{FSM}	non-repetitive peak forward current	t = 10 ms; half sinewave; $T_j = T_{j\ max}$ prior to surge	–	15	A
P_{RSM}	non-repetitive peak reverse power dissipation	t = 10 µs; triangular pulse; $T_j = T_{j\ max}$ prior to surge	–	3	kW
T_{stg}	storage temperature range		–65	200	°C
T_{amb}	ambient operating temperature	continuous	–	150	°C
		max. 30 mins; note 1	–	180	°C

Note

1. For a maximum operating time of 30 minutes, a junction temperature of max. 200 °C is allowed.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient	$T_{amb} = T_{leads}$	55 K/W

CHARACTERISTICS

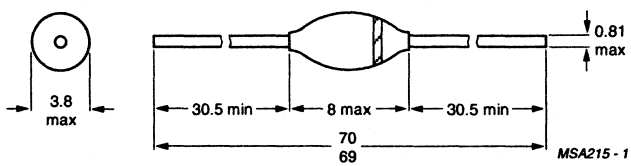
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_F	forward voltage	I_F = 0.1 mA	–	4.4	V
$V_{(BR)R}$	reverse avalanche breakdown voltage	I_R = 100 µA	3.5	–	kV
I_R	reverse current	V_R = 2 kV; T_j = 180 °C	–	75	µA
t_{rr}	reverse recovery time	note 1	–	5	µs

Note

1. When switched from I_F = 0.5 A to I_R = 1 A, measured at I_R = 0.25 A.

PACKAGE OUTLINE



Dimensions in mm.

Fig.2 SOD88A.

REMOTE CONTROL

Low voltage infrared remote control transmitter

PCF1254

FEATURES

- 22 bits of EEPROM code with automatic 2-bit preamble (over 4×10^6 combinations)
- Guaranteed reprogrammable up to 10 times
- Two operating modes: single or continuous transmission
- Supply voltage 2.5 V to 6.5 V
- High output current drive (typ. 50 mA at 5 V)
- Operating ambient temperature –40 to +85 °C
- Designed for minimum 10 years data retention.

GENERAL DESCRIPTION

The PCF1254 is intended for remote control access, security or identification systems. The circuit can be used to transmit a programmable 22-bit code to a receiver by infrared or other transmission means. The code is stored in an EEPROM which is programmed by the equipment manufacturer.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF1254P	8	DIL8	plastic	SOT97–1
PCF1254T	8	SO8	plastic	SOT96–1

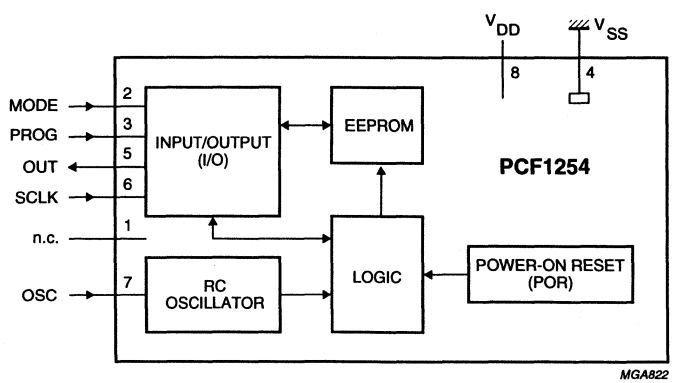


Fig.1 Block diagram.

Low voltage infrared remote control transmitter

PCF1254

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
MODE	2	mode input to select single transmission (LOW), or continuous transmission (HIGH)
PROG	3	programming input for the EEPROM
V_{SS}	4	negative supply
OUT	5	code output
SCLK	6	serial clock input to program the EEPROM
OSC	7	oscillator input and programming input for the EEPROM
V_{DD}	8	positive supply

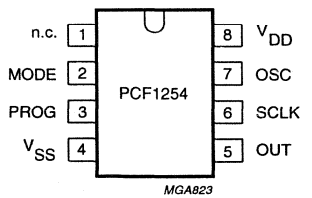
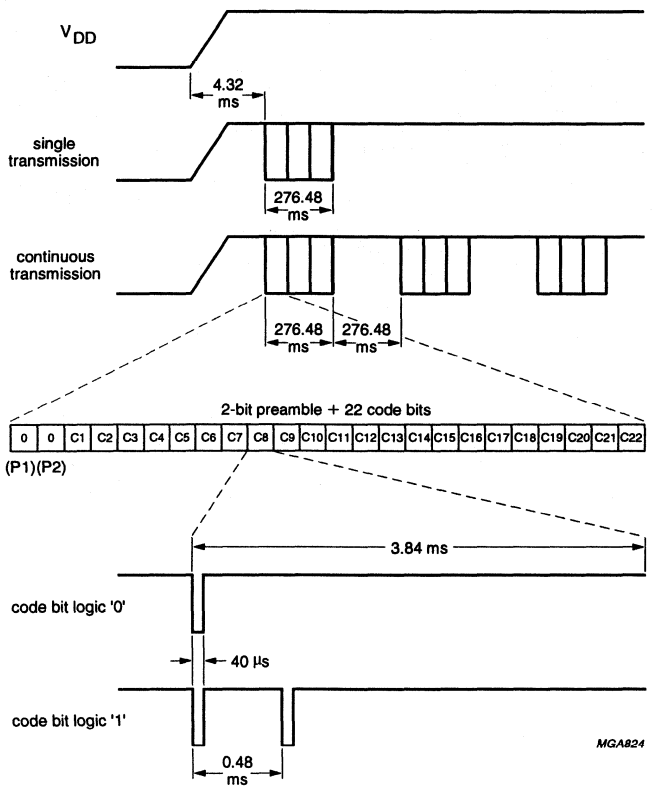


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The PCF1254 uses fixed frequency data coding and a 22-bit EEPROM code. A few milliseconds after application of the power supply, the circuit outputs the 22-bit pre-programmed EEPROM code three times in succession (one burst) at OUT (pin 5) in a pulse-width modulated format (see Fig.3). A sequence of two zeroes is automatically transmitted preceding the 22-bit code (preamble). The MODE input (pin 2) selects either a single burst (MODE = V_{SS}) or continuous transmission of bursts (MODE = V_{DD}).



f_{OSC} = 50 kHz.

Fig.3 Output signal timing for single and continuous transmission.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 8)	−0.3	+7.0	V
V_I	input voltage			
	any input except pin 3	−0.8	V_{DD} + 0.8	V
	pin 3	−0.8	V_{DD} + 3.0	V
T_{amb}	operating ambient temperature	−40	+85	°C
$T_{stg(u)}$	unprogrammed storage temperature	−65	+150	°C
$T_{stg(p)}$	programmed storage temperature	−65	+85	°C

CHARACTERISTICS

V_{DD} = 2.5 to 6.5 V; f_{OSC} = 50 kHz; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	operating supply voltage		2.5	–	6.5	V
I_{DD}	operating supply current	V_{DD} = 5 V; T_{amb} = −25 to +85 °C	–	–	500	µA
Inputs (pins 2 and 6)						
V_{IL}	LOW level input voltage		−0.8	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.8	V
I_{IL}	input leakage current	input pin at V_{DD} or V_{SS}	–	–	1	µA
Input (pin 7)						
V_{IL}	LOW level input voltage	programming	−0.8	–	0	V
V_{IH}	HIGH level input voltage	programming	V_{DD}	–	V_{DD} + 0.8	V
I_{IL}	input leakage current	input pin at V_{SS}	−1	–	+1	µA
Input (pin 3)						
I_I	input current	V_{DD} = 5 V; V_{PROG} = 7.5 V	–	–	3	mA
Output (pin 5)						
I_{OL}	output sink current	V_{DD} = 5 V; V_{OL} = 4 V	25	50	–	mA
I_{OH}	output source current	V_{DD} = 5 V; V_{OH} = 0 V	−400	–	–	µA
Oscillator (pin 7)						
f_{OSC}	frequency range	V_{DD} = 3.5 V; R_{OSC} = 51 kΩ; C_{OSC} = 560 pF	40	–	60	kHz
f_{OSC}	maximum frequency		–	–	500	kHz
Input (pin 6)						
R_{SCLK}	SCLK resistor to V_{SS}		10	–	150	kΩ
EEPROM						
t_{RET}	data retention time		10	–	–	years
t_{CY}	endurance		10	–	–	cycles

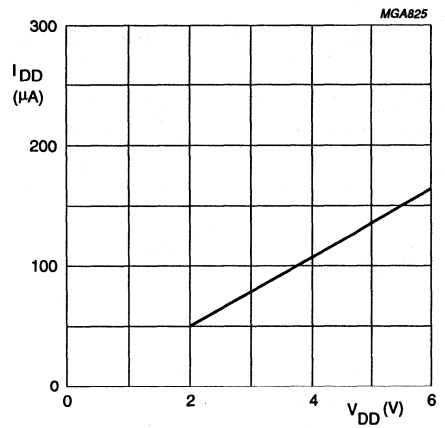
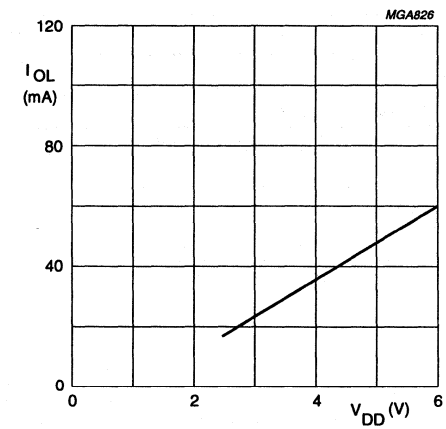


Fig.4 Typical supply current (I_{DD}) as a function of supply voltage (V_{DD}) with 50 kHz oscillator.



$V_{OL} = V_{DD} - 1$ V.

Fig.5 Typical output sink current (I_{OL}) as a function of supply voltage.

APPLICATION INFORMATION

A typical application for an oscillator frequency of 50 kHz is shown in Fig.6. Other frequencies may be obtained using the equation $f \approx 1 / (0.7 \times RC)$. For correct operation the following limits apply:

- Minimum resistance = 10 kΩ
- Maximum capacitance = 560 pF
- Maximum frequency = 500 kHz.

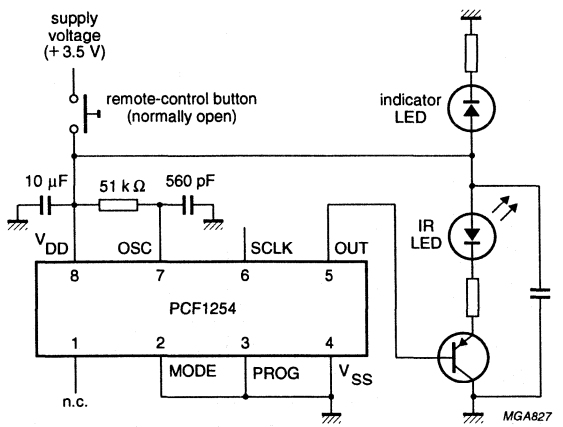


Fig.6 Typical application diagram for single-burst IR code transmission.

EEPROM PROGRAMMING (see Fig.7 and Table 1)

The code is programmed in the EEPROM by the manufacturer. The circuit may be reprogrammed up to a maximum of 10 times. The circuit is delivered with the code all zeroes.

To program the EEPROM the following procedure must be carried out:

- Connect V_{DD} to 5 V; connect pin 3 (PROG) to V_{DD}.

The circuit is now in programming mode. Pin 5 (OUT) is disabled and the oscillator is disabled.

- Apply a 5 V, 2 MHz signal to pin 7 (OSC) and input signals to pin 3 (PROG) and pin 6 (SCLK) as shown in Fig.7.
- Disconnect PROG from V_{DD}.

Erase

PROG is taken to 7.5 V for a time t_P.

Data input

With PROG at 7.5 V, a 5 V pulse on SCLK inputs a logic 1, and with PROG at 5 V, a 5 V pulse on SCLK inputs a logic 0. The data must be valid for a time t_S before and after the negative edge of SCLK. PROG must not be at 7.5 V for longer than time t_H but can remain at 5 V indefinitely. PROG must return to 5 V for a time t_L. 24 SCLK pulses must be given, the code is input on pulses 3 to 24. PROG must be 5 V during the other SCLK pulse(s). The data bits are input in the same order as they are transmitted.

Write

PROG is taken to 7.5 v for a time t_P.

In normal operation PROG must be connected to V_{SS}. The SCLK input has a 50 kΩ pull-down resistor and can be left open-circuit. Programming can be checked by taking V_{DD} to 0 V and back to 5 V and monitoring OUT. For fast checking a 5 V, 500 kHz signal (0.5 µs HIGH; 1.5 µs LOW) can be input at pin 7 (OSC), speeding up the output signal by a factor of 10.

Table 1 Timing values.

PARAMETER	MIN.	TYP.	MAX.	UNIT
t_P	4	5	10	ms
t_S	0.5	1.0	–	µs
t_H	–	2	4	µs
t_L	10	–	–	µs

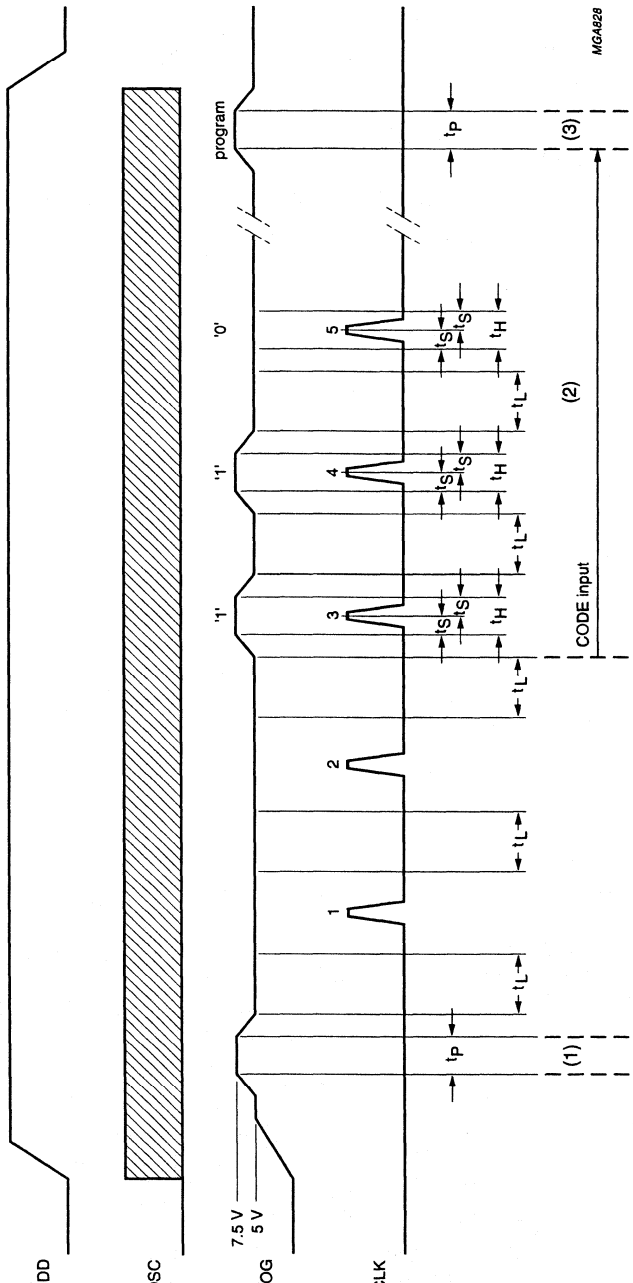


Fig.7 Timing diagram.

(1) Step 1 erase.
(2) Step 2 data input.
(3) Step 3 write.

UHF/VHF remote control receiver UAA3201T

FEATURES

- Oscillator with external SAW resonator
- Wide frequency range: 150 to 450 MHz
- High sensitivity
- Low power consumption
- Automotive temperature range
- Superheterodyne architecture
- Applicable to fulfil FTZ17TR2100
- High integration level, few external components
- Inexpensive external components
- IF-filter bandwidth determined by application.

APPLICATIONS

- Car alarm systems
- Remote control systems
- Security systems
- Gadgets, toys
- Telemetry.

GENERAL DESCRIPTION

The UAA3201T is a fully integrated single chip receiver, primarily intended for use in VHF and UHF systems employing direct AM Return-to-Zero (RZ) Amplitude Shift Keying (ASK) modulation.

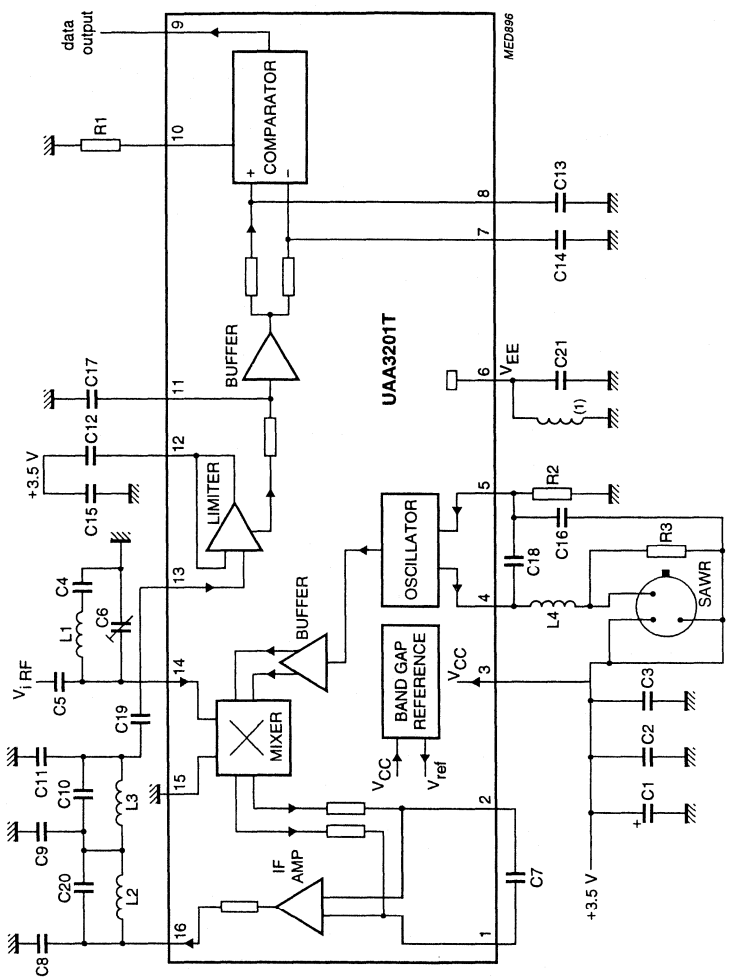
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		3.5	–	6.0	V
I_{CC}	supply current		–	3.4	4.8	mA
P_{ref}	sensitivity	f_i = 433.92 MHz; data rate 250 bits/s; BER $\leq 3 \times 10^{-2}$	–	–	–105	dBm
T_{amb}	operating ambient temperature		–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA3201T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM



(1) Stray inductance; see Chapter "Layout of printed circuit board for test circuit (f_i = 433.92 MHz)".

Fig.1 Block diagram, test and application circuit (f_i = 433.92 MHz); see Table 1.

Table 1 Application component list for Fig.1

COMPONENT	VALUE	TOLERANCE	DESCRIPTION
R1	27 kΩ	±2%	TC = +50 ppm/K
R2	680 Ω	±2%	TC = +50 ppm/K
R3	220 Ω	±2%	TC = +50 ppm/K
C1	4.7 µF	±20%	–
C2	150 pF	±10%	TC = 0 ±30 ppm/K; $\tan\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C3	1 nF	±10%	TC = 0 ±30 ppm/K; $\tan\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C4	820 pF	±10%	TC = 0 ±30 ppm/K; $\tan\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C5	3.3 pF	±10%	TC = 0 ±150 ppm/K; $\tan\delta \leq 30 \times 10^{-4}$; f = 1 MHz
C6	2.5 to 6 pF	–	TC = 0 ±300 ppm/K; $\tan\delta \leq 20 \times 10^{-4}$; f = 1 MHz
C7	56 pF	±10%	TC = 0 ±30 ppm/K; $\tan\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C8	150 pF	±10%	TC = 0 ±30 ppm/K; $\tan\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C9	220 pF	±10%	TC = 0 ±30 ppm/K; $\tan\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C10	27 pF	±10%	TC = 0 ±30 ppm/K; $\tan\delta \leq 20 \times 10^{-4}$; f = 1 MHz
C11	150 pF	±10%	TC = 0 ±30 ppm/K; $\tan\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C12	100 nF	±10%	$\tan\delta \leq 25 \times 10^{-3}$; f = 1 kHz
C13	2.2 nF	±10%	$\tan\delta \leq 25 \times 10^{-3}$; f = 1 kHz
C14	33 nF	±10%	$\tan\delta \leq 25 \times 10^{-3}$; f = 1 kHz
C15	150 pF	±10%	TC = 0 ±30 ppm/K; $\tan\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C16	3.9 pF	±10%	TC = 0 ±150 ppm/K; $\tan\delta \leq 30 \times 10^{-4}$; f = 1 MHz
C17	10 nF	±10%	$\tan\delta \leq 25 \times 10^{-3}$; f = 1 kHz
C18	3.3 pF	±10%	TC = 0 ±150 ppm/K; $\tan\delta \leq 30 \times 10^{-4}$; f = 1 MHz
C19	68 pF	±10%	TC = 0 ±30 ppm/K; $\tan\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C20	6.8 pF	±10%	TC = 0 ±150 ppm/K; $\tan\delta \leq 30 \times 10^{-4}$; f = 1 MHz
C21	47 pF	±5%	TC = 0 ±30 ppm/K; $\tan\delta \leq 10 \times 10^{-4}$; f = 1 MHz
L1	10 nH	±10%	Q_{min} = 50/450 MHz; TC = +25 to +125 ppm/K
L2	330 µH	±10%	Q_{min} = 45/800 kHz; $C_{stray} \leq 1$ pF
L3	330 µH	±10%	Q_{min} = 45/800 kHz; $C_{stray} \leq 1$ pF
L4	33 nH	±10%	Q_{min} = 45/450 MHz; TC = +25 to +125 ppm/K

Table 2 SAWR (Surface Acoustic Wave Resonator) data

DESCRIPTION	SPECIFICATION
Type	one-port (e.g. RFM R02112)
Centre frequency	433.42 MHz ±75 kHz
Maximum insertion loss	1.5 dB
Typical loaded Q	1600 (50 Ω load)
Temperature drift	0.032 ppm/K^2
Turnover temperature	43 °C

PINNING

SYMBOL	PIN	DESCRIPTION
MON	1	negative mixer output
MOP	2	positive mixer output
V_{CC}	3	positive supply voltage
OSC	4	oscillator collector
OSE	5	oscillator emitter
V_{EE}	6	negative supply voltage
CPB	7	comparator input B
CPA	8	comparator input A
DATA	9	data output
CPO	10	comparator offset adjustment
CPC	11	comparator input C
LFB	12	limiter feedback
LIN	13	limiter input
MIXIN	14	mixer input
V_{EM}	15	negative supply voltage for mixer
FA	16	output to elliptic filter

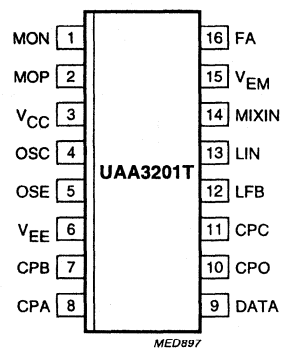


Fig.2 Pin configuration.

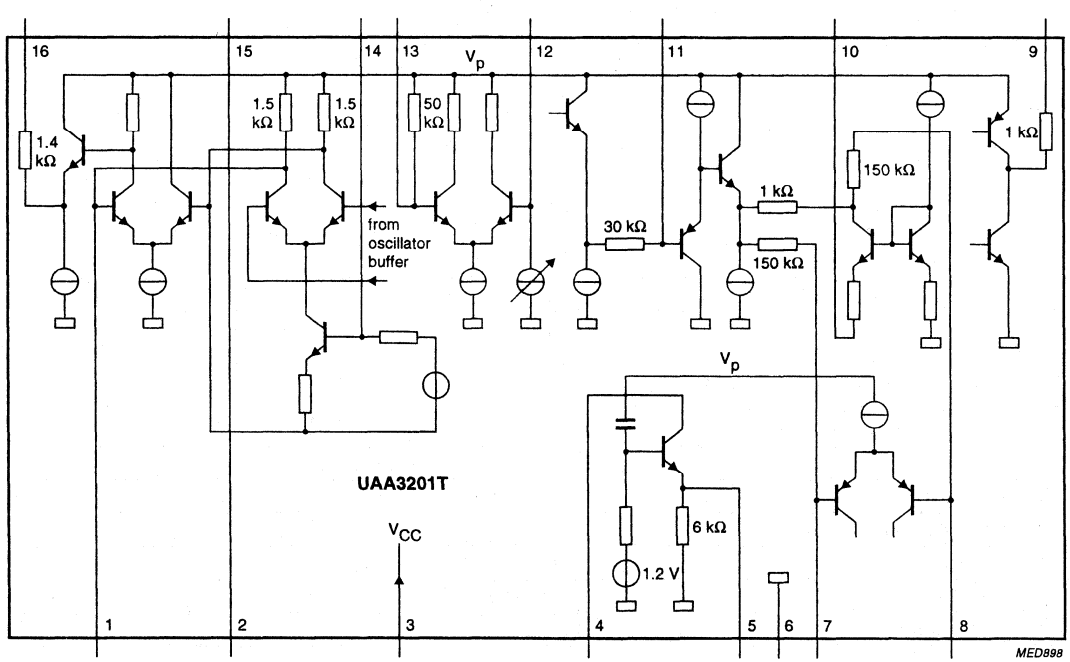


Fig.3 Internal circuits.

FUNCTIONAL DESCRIPTION

The RF signal is fed directly into the mixer stage where it is mixed down to nominal 500 kHz IF by the integrated SAWR controlled oscillator. The IF signal is then passed to the IF amplifier which increases the level. A 5th order elliptic low-pass filter acts as the main IF filtering. The output voltage of that filter is demodulated by a limiting amplifier that rectifies the incoming IF. The demodulated signal passes two RC filter stages and is then limited by a data comparator which makes it available at the data output pin.

Mixer

The mixer is a single balanced emitter coupled pair with internally set bias current. The optimum impedance is 320 Ω at 430 MHz. Capacitor C5 is used to transform a 50 Ω generator impedance to the optimum value.

Oscillator

The oscillator consists of a transistor in common base configuration and a tank circuit including the SAWR. R2 is used to control the bias current through the transistor. R3 is required to reduce unwanted responses of the tank circuit.

IF amplifier

The IF amplifier is a differential input, single ended output emitter coupled pair. It is used to decouple the first and the second IF filter and to provide some additional gain in order to reduce the influence of the noise of the limiter on the total noise figure.

IF filters

The first IF filter is an RC filter formed by internal resistors and an external capacitor. The second IF filter is an external elliptic filter. The source impedance is 1.4 kΩ, the load is high impedance. The bandwidth of the IF filter in the given application is 800 kHz due to the centre frequency spread of the SAWR. It may be reduced when SAWRs with less tolerances are used or temperature range requirements are lower. A smaller bandwidth of the filter will yield a higher sensitivity of the receiver. As the RF is mixed down to a low IF there is no image rejection possible.

Limiter

The limiting amplifier consists of three DC-coupled amplifier stages, with a total gain of 60 dB. An RSSI signal is generated by rectifying the IF signal. The limiter has a lower frequency limit of 100 kHz, which can be controlled by C12 and C19, and an upper frequency limit of 3 MHz.

Comparator

The 2 × IF component in the RSSI signal is removed by the first order low-pass capacitor C17. After passing a buffer stage the signal is split into two paths, leading via RC filters to the inputs of a voltage comparator. The time constant of one path (C14) is compared to the bit duration. Consequently the potential at the negative comparator input represents the average magnitude of the RSSI signal, the second path with a short time constant (C13) allows the signal at the positive comparator input to follow the RSSI signal instantaneously. This results in a variable comparator threshold, depending on the field strength of the incoming signal.

Hence the comparator output is switched on, when the RSSI signal exceeds its average value, i.e. when an ASK ON signal is received.

The low-pass filter capacitor C13 rejects the unwanted 2 × IF and reduces the noise bandwidth of the data filter. The resistor R1 is used to set the current of an internal source. This current is drawn from the positive comparator input thereby applying an offset and driving the output into the OFF state during the absence of an input signal. This offset can be increased by lowering the value of R1 yielding a higher noise immunity at the expense of reduced sensitivity.

Band gap reference

The band gap reference controls the biasing of the whole circuit. In this block currents are generated that are constant over temperature and currents that are proportional to absolute temperature.

The current consumption of the receiver rises with increasing temperature, because the blocks with the highest current consumption are biased by currents that are proportional to absolute temperature.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS.	MIN.	MAX.	UNIT
V_{CC}	supply voltage		−0.3	+8.0	V
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−55	+125	°C
V_{es}	electrostatic handling	note 1			
	pins 4 and 5		−2000	+1500	V
	pins 12 and 14		−1500	+2000	V
	all other pins		−	±2000	V

Note

1. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

DC CHARACTERISTICS

All voltages referenced to V_{EE}; V_{CC} = 3.5 V; T_{amb} = −40 to +85 °C; typical values for T_{amb} = +25 °C; for test circuit see Fig.1; SAWR disconnected; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		3.5	−	6.0	V
V_{DATA}	data output voltage	I_{DATA} = −10 μA (HIGH); note 1	V_{CC} − 0.5	−	−	V
		I_{DATA} = +200 μA (LOW); note 1	−	−	0.6	V
I_{CC}	supply current	R_2 = 680 Ω	−	3.4	4.8	mA

Note

1. I_{DATA} is defined to be positive when current flows into the DATA pin.

AC CHARACTERISTICS

V_{CC} = 3.5 V; T_{amb} = +25 °C; test circuit (see Fig.1); R1 disconnected; for test board see Figs 10 and 11; for AC test conditions see Section "AC test conditions"; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_{ref}	input sensitivity	BER $\leq 3 \times 10^{-2}$; note 1	–	–	–105	dBm
$P_{i(max)}$	maximum input power	BER $\leq 3 \times 10^{-2}$	–	–	–30	dBm
P_{spur}	spurious radiation	note 2	–	–	–60	dBm
$IP3_{mix}$	intercept point (mixer)		–20	–17	–	dBm
$IP3_{IF}$	intercept point (mixer + IF amplifier)		–38	–35	–	dBm
$P_{1\ dB}$	1 dB compression point (mixer)		–38	–35	–	dBm
t_{on}	receiver turn-on time	note 3	–	–	10	ms

Notes

1. P_{ref} is the maximum available power at the input of the test board. The Bit Error Rate (BER) is measured using the test facility shown in Fig.9.
2. Valid only for the reference PCB (see Figs 10 and 11). Spurious radiation is strongly dependent on the PCB layout.
3. C1 disconnected. The supply voltage V_{CC} is pulsed as explained in the Section "AC test conditions".

TEST INFORMATION

Tuning procedure for AC tests

1. Turn on the signal generator (f_i = 433.92 MHz; no modulation; RF input level = 1 mV).
2. Tune C6, RF stage input, to obtain a peak audio voltage on pin LIN.
3. Check that data is appearing on the data output pin, DATA, and proceed with the AC tests.

AC test conditions

Table 3 Test signals

The reference signal level P_{ref} for the following tests is defined as the minimum input level in dBm to give a BER $\leq 3 \times 10^{-2}$ (e.g. 7.5 bit errors per second for 250 bits/s).

TEST SIGNAL	FREQUENCY (MHz)	DATA SIGNAL	MODULATION	MODULATION INDEX
1	433.92	250 bits/s square wave	RZ signal with duty cycle = 66% for logic 1; RZ signal with duty cycle = 33% for logic 0	100%
2	434.02	–	no modulation	–
3	433.92	–	no modulation	–

Table 4 Test results

P_1 is the maximum available power from signal generator 1 at the input of the test board; P_2 is the maximum available power from signal generator 2 at the input of the test board.

TEST	GENERATOR		RESULT
	1	2	
Maximum input power (see Fig.5)	modulated test signal 1; $P_1 = -30$ dBm (minimum P_{max})	–	BER $\leq 3 \times 10^{-2}$ (e.g. 7.5 bit errors per second for 250 bits/s)
Receiver turn-on time; see note 1 and Fig.5	test signal 1; $P_1 = P_{ref} + 10$ dB; error counting is started 10 ms after V_{CC} is switched on	–	check that the first 10 bits are correct
Intercept point (mixer) see note 2 and Fig.6	test signal 3; $P_1 = -50$ dBm	test signal 2; $P_2 = P_1$	IP3 = $P_1 + \frac{1}{2} \times$ IM3 (dB); IP3 ≥ -20 dBm (minimum $IP3_{mix}$)
Intercept point (mixer + IF amplifier) see note 3 and Fig.6	test signal 3; $P_1 = -50$ dBm	test signal 2; $P_2 = P_1$	IP3 = $P_1 + \frac{1}{2} \times$ IM3 (dB); IP3 ≥ -38 dBm (minimum $IP3_{IFa}$)
Spurious radiation see note 4 and Fig.7	–	–	no spuriouses (25 MHz – 1 GHz) with level higher than –60 dBm (maximum P_{spur})
1 dB compression point (mixer) see note 5 and Fig.8	test signal 3; $P_{11} = -70$ dBm; $P_{12} = -38$ dBm (minimum $P_{1\,dB}$)	–	$(P_{o1} + 70\ dB) - [P_{o2} + 38\ dB$ (minimum $P_{1\,dB})] \leq 1$ dB, where P_{o1}, P_{o2} is the output power for test signals with P_{11} or P_{12}, respectively

Notes

1. The supply voltage V_{CC} of the test circuit alternates between 'on' (100 ms) and 'off' (100 ms); see Fig.4.
2. Differential probe of spectrum analyser connected to MOP and MON.
3. Probe of spectrum analyser connected to LIN.
4. Spectrum analyser connected to the input of the test board.
5. Probe of spectrum analyser connected to either MOP or MON.

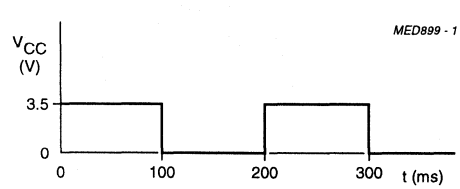
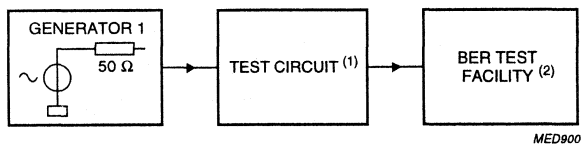
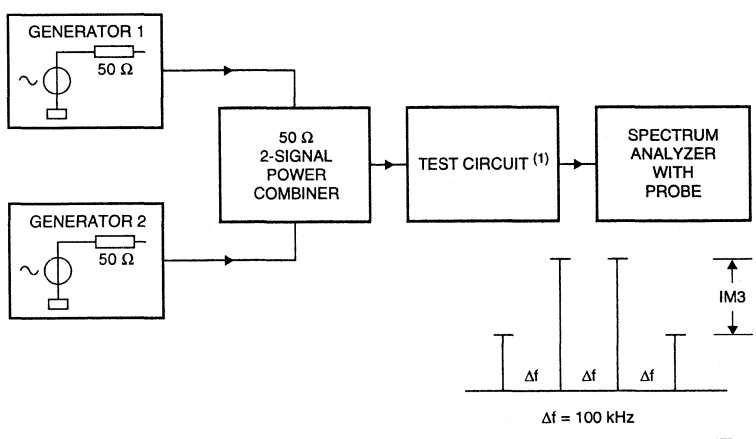


Fig.4 Timing diagram for pulsed supply voltage.



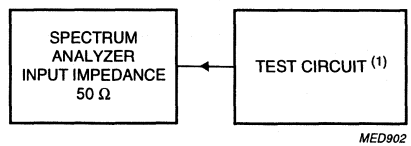
(1) For test circuit see Fig.1.
(2) For BER test facility see Fig.9.

Fig.5 Test configuration A (single generator).



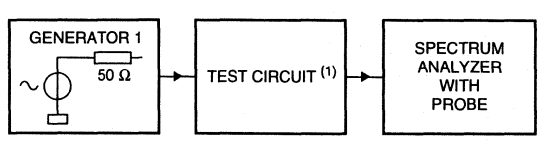
(1) For test circuit see Fig.1.

Fig.6 Test configuration B (IP3).



(1) For test circuit see Fig.1.

Fig.7 Test configuration C (spurious radiation).



(1) For test circuit see Fig.1.

Fig.8 Test configuration D (1 dB compression point).

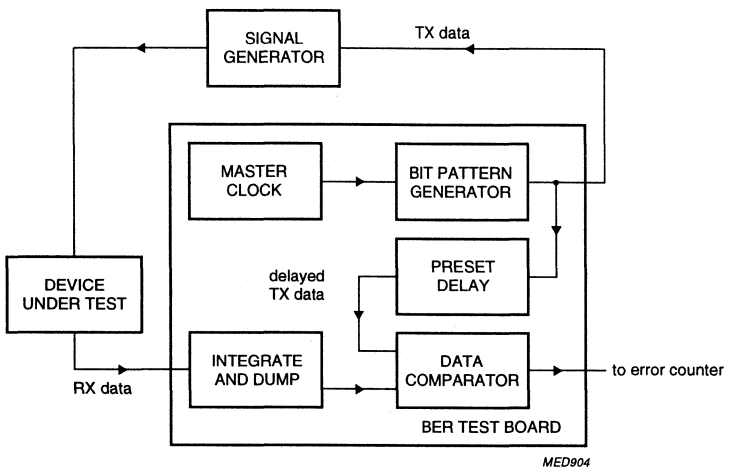
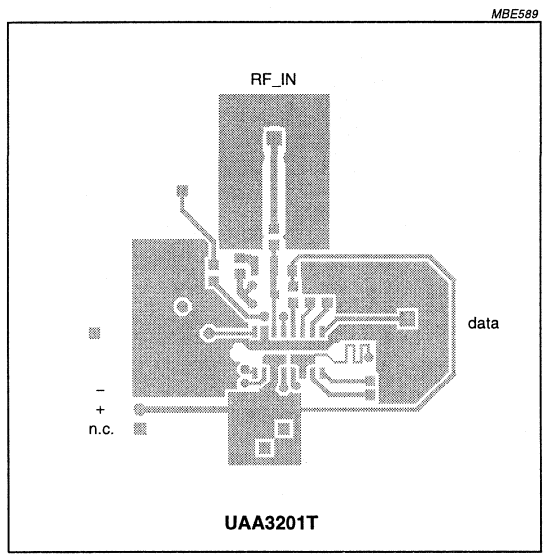


Fig.9 BER test facility.

LAYOUT OF PRINTED CIRCUIT BOARD FOR TEST CIRCUIT (f_i = 433.92 MHz)



H4ACS15

Fig.10 Layout (top side).

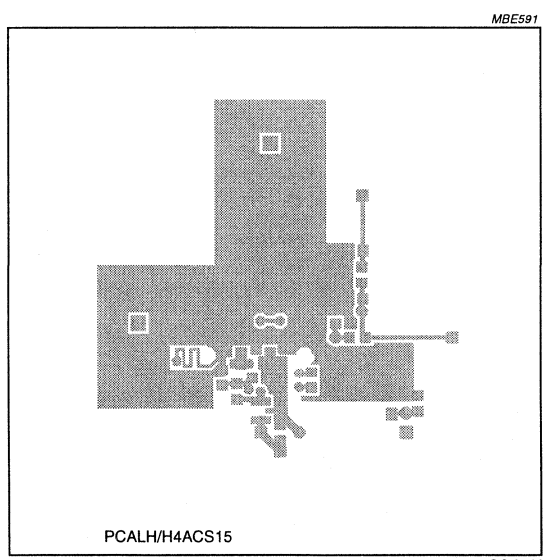


Fig.11 Layout (bottom side).

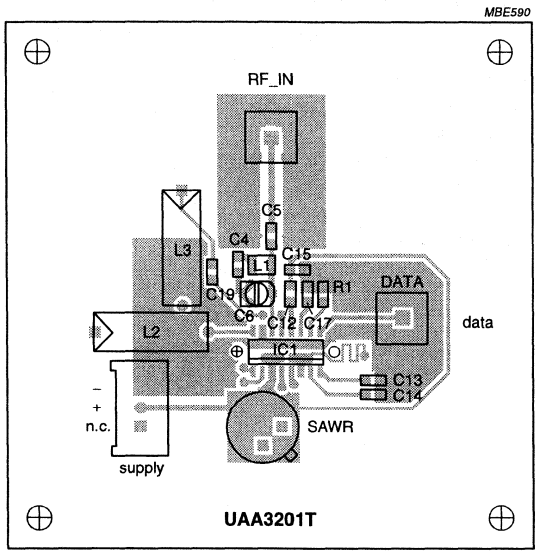


Fig.12 Top side with components.

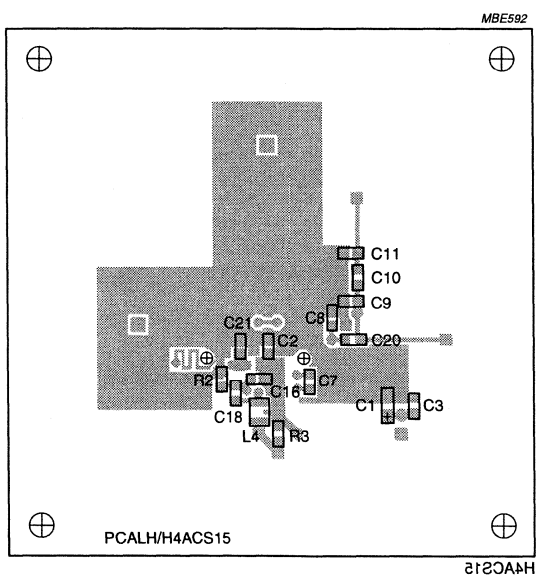


Fig.13 Bottom side with components.

UAA3201T Application report AN95036

Summary

This Application Note introduces the reader to the fully integrated single-chip receiver UAA 3201T, primarily intended for use in VHF and UHF systems employing direct return-to-zero (RZ) Amplitude Shift Keying (ASK) modulation. The UAA 3201T features a low power and low cost solution for keyless entry, car alarm, remote control, security, home appliance or other telemetry systems. Data rates up to 10 kbps and more are feasible without a significant reduction in sensitivity. The UAA 3201T provides a very low radiation and is applicable to fulfil FTZ 17 TR 2100. Compared with a superregenerative receiver, the UAA 3201T is the superior solution. The receiver block diagram is discussed and design formulas presented. A set of application schematics for typical receive frequencies complete the note.

Please note that all figures and measurement results presented indicate typical values only and may vary as a result of device spreads, component tolerances or temperature changes.

CONTENTS

1. Introduction

Infrared based remote control systems for keyless entry, e.g. automotive, garage door, etc. are more and more replaced by RF based systems, because RF offers a number of advantages compared to infrared:

- No optical link is required
- Almost independent of direction and weather conditions
- Larger access range

Today's receiver solutions are mostly based on a so called "superregenerative" architecture. This kind of receiver basically consists of an oscillator running at or close to the desired receive frequency, which is alternated between oscillation and non-oscillation condition by means of a control signal at a low rate know as the quench frequency. The quench frequency is typically below 50 kHz. The antenna signal is feed to the oscillator, so that the oscillator rise time varies as a function of the applied signal strength. The demodulated signal is obtained by simply low pass filtering the oscillator output. Obviously, this receiver is able to detect amplitude modulated carries only.

Depending on the receive frequency and the spurious radiation limits set by the authorities, a regenerative receiver design may consist of 30 discrete and inexpensive components with L/C stabilized oscillator or requires twice the amount of components and a SAW stabilized oscillator. The latter case holds for the UHF range and the stringent spurious radiation limits in Europe.

A receiver design that offers lower component count, better sensitivity and very low radiation is the UAA 3201 T, manufactured by Philips Semiconductors. The UAA 3201T is a fully integrated single-chip receiver, primarily intended for use in VHF and UHF systems employing direct return-to-zero (RZ) Amplitude Shift Keying (ASK) modulation. The UAA 3201 T is based on a superhet architecture and requires 25 external low cost components only. Using the same PCB board layout, the receiver may easily be adapted to other receive frequencies by changing the values of 7 components. Due to the use of a SAW stabilized local oscillator, which requires no adjustment, excellent long term and temperature stability is achieved. The UAA 3201 T may operate with data rates up to some 10 kbit/sec without a significant reduction in sensitivity. As a result of the high integration level the whole receiver may be designed to occupy 5 cm^2 (0,8 square inch) of PCB with single side component placement only. The UAA 3201T features a low power and low cost solution for keyless entry, car alarm, remote control, home appliance, security or other telemetry systems.

1.1 Typical system architecture

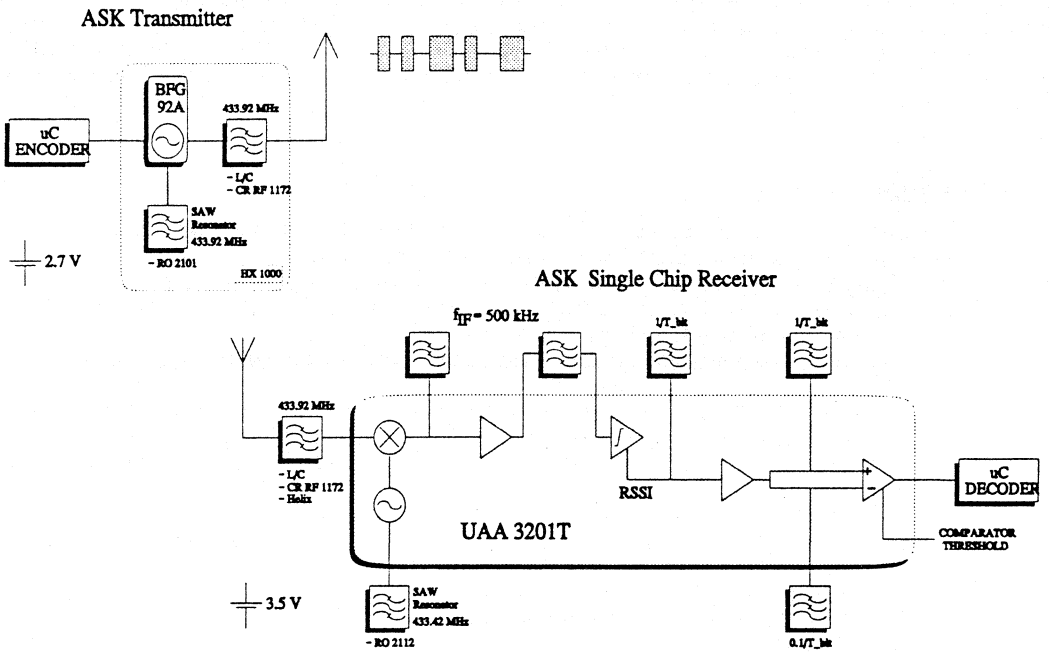


Fig.1 Typical system architecture

Like in figure 1, a typical system architecture emploies a ASK modulated transmitter, with the data to be send generated by a microcontroller or an encoder ASIC. ASK modulation is preferred compared to FSK due to power consumption reasons, since the transmitter is usually battery powered. Furthermore, ASK is easier to design, providing lower transmitter costs. The carrier is generated by means of an oscillator build around a single transistor. L/C stabilized oscillators are used for VHF and low end applications. SAW stabilized oscillators are used at UHF frequencies or when frequency stability is required and oscillator alignment has to be avoided. Usually the antenna is part of the oscillator coil, in order to minimize component count. Depending on the design some filtering has to be provided, in order to suppress harmonics of the carrier frequency. Instead of a discrete solution a complete ASK transmitter module may be used.

It is suggested to use a SAW stabilized transmitter, in order to make use of the relative small system bandwidth of 800 kHz provided by the UAA 3201T on the receive side. Wider or narrower receive bandwidth are applicable when the IF filter design is modified accordingly.

On the receive side all necessary functions are realized by means of the UAA 3201T. The UAA 3201 T is based on a superhet architecture and incorporates a local oscillator stabilized by an external SAW resonator (e.g. RFM RO 2112). Thus no alignment is necessary. After filtering the received signal is feed to the mixer and down converted to the IF band. The UAA 3201T uses an IF frequency of 500 kHz, which allows to use low cost L and C components for IF filtering. After amplification and filtering the signal is demodulated by a limiter amplifier that rectifies the IF signal. The RSSI (receive signal strength indicator) signal derived contains the demodulated data and unwanted frequencies which are removed by low pass filtering. This signal is feed to the positive input of a data slicer (level comparator). The slice reference is derived from the same signal by means of a separate low

pass filter. This low pass filter is designed for a long time constant, so that the average RSSI value is obtained as an adaptive reference for the data slicer. The adaptive reference enables the receiver to detect a modulated carrier over an input signal range of more than 75 dB. By means of an external resistor a data slicer threshold may be applied which inhibits noise to be present at the data output when no RF carrier is present.
Due to the relative low IF frequency of typically 500 kHz and the high receive frequency of up to 450 MHz, the receiver image rejection is limited. With a SAW filter in front of the mixer input (e.g RFM RF 1172), about 20 dB of image rejection could be obtained. With a simple L/C circuit or a helical filter (e.g. double tuned) almost no image rejection is achieved.

1.2 UAA 3201T Features

- The UAA 3201T incorporates the local oscillator, mixer, IF amplifier, demodulator and data slicer.
- No alignment is necessary due to the use of a SAW stabilized local oscillator.
- Data rates up to 10 kbps and more are feasible with a moderate reduction in sensitivity.
- The sensitivity typically achieved is about -108 dBm for a bit error rate (BER) of 1 % and 512 bps and about -106 dBm for a BER of 1% and 10 kbps (NRZ coding).
- The spurious radiation measured at the RF input port is better than -60 dBm in order to fulfil FTZ 17 TR 2100.
- The on-chip local oscillator allows a receive frequency range from 150 MHz to 450 MHz. When used with an external local oscillator the receive frequency may be as low as 27 MHz.
- The IF filter bandwidth is typically 800 kHz, but may be modified since it is determined by the application.
- Operates from 3,5 V to 6,0 V.
- The device supply current is 3,7 mA, which may be reduced to an average of e.g. 1 mA with a proper pulsed receiver operation.
- Meets the automotive temperature range from -40 to +85 °C.
- Requires about 25 external low cost components only.
- SO 16 plastic package

Figure 2 shows the block diagram of the UAA 3201T.

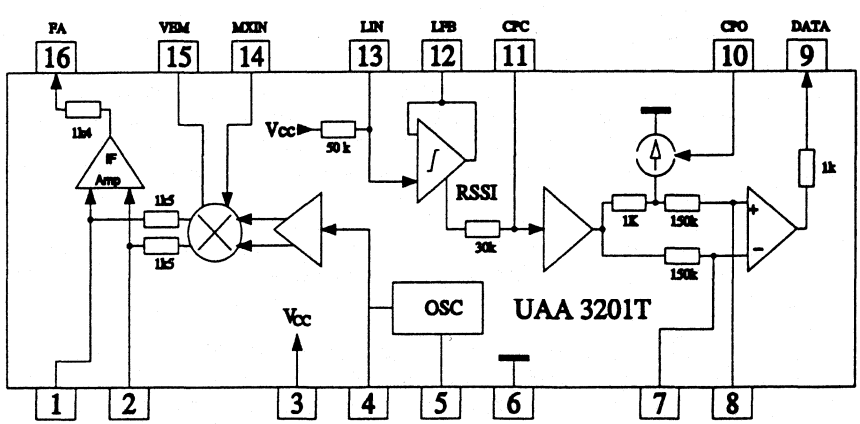


Fig.2 UAA 3201T Block diagram

2. UAA 3201T Application details

Beside the UAA 3201T about 25 external low cost components are required to build a low cost ASK receiver. The components determine the receive frequency, the IF bandwidth, the data rate and the data slicer threshold. Thus, the designer has full control over the application, enabling him to adapt the UAA 3201T to almost any system specification. Figure 3 shows a typical schematic for a receive frequency of 433.92 MHz and a data rate of 512 bps.

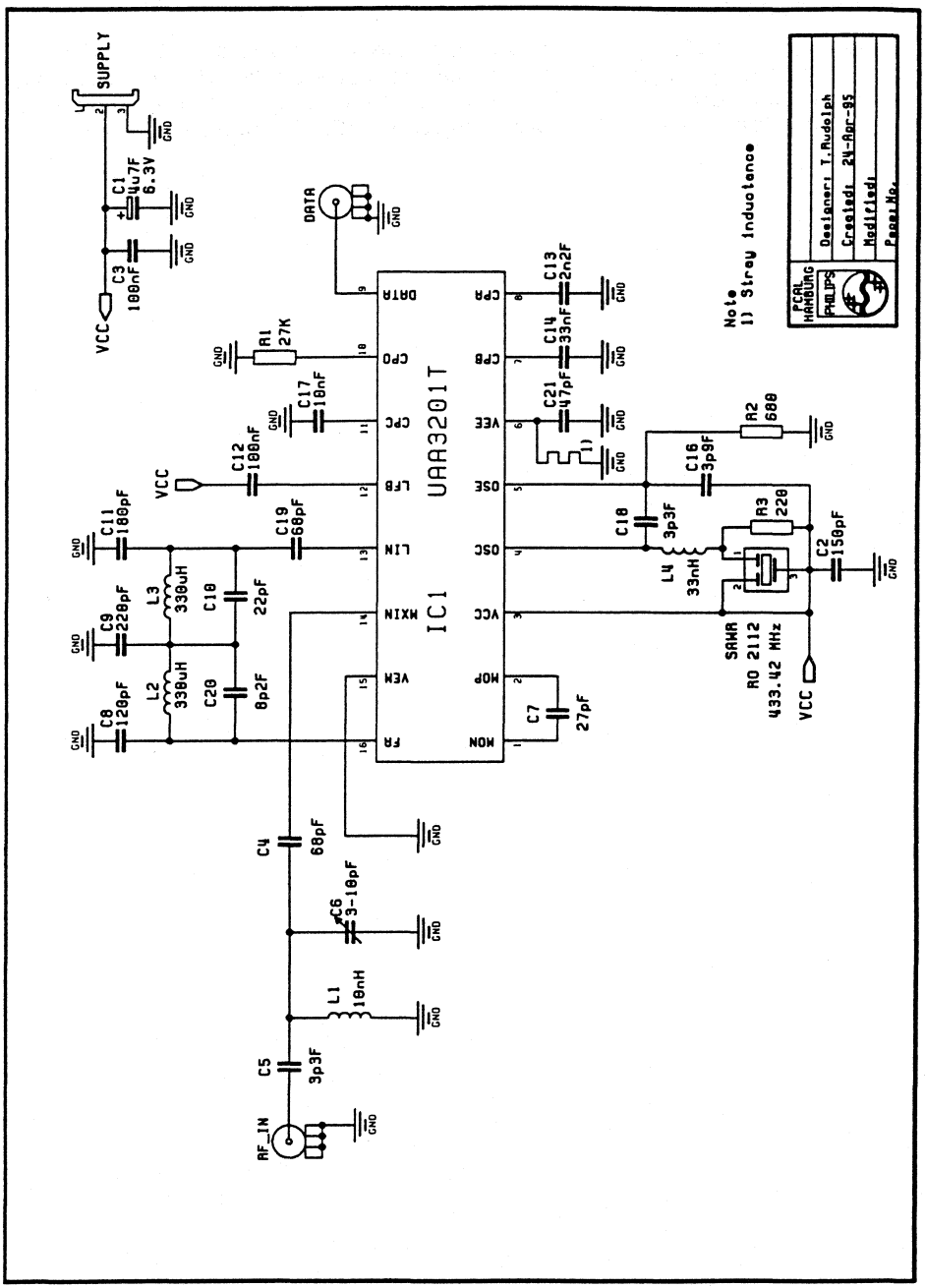


Fig.3 Typical UAA 3201T application for 433,92 MHz and 512 bps

In some environments it is desirable to improve the receiver performance by means of a SAW based front-end filter, which gives a better immunity to interfering signals. Figure 4 shows a typical schematic SAW front end filter for a receive frequency of 433,92 MHz and 512 bps.

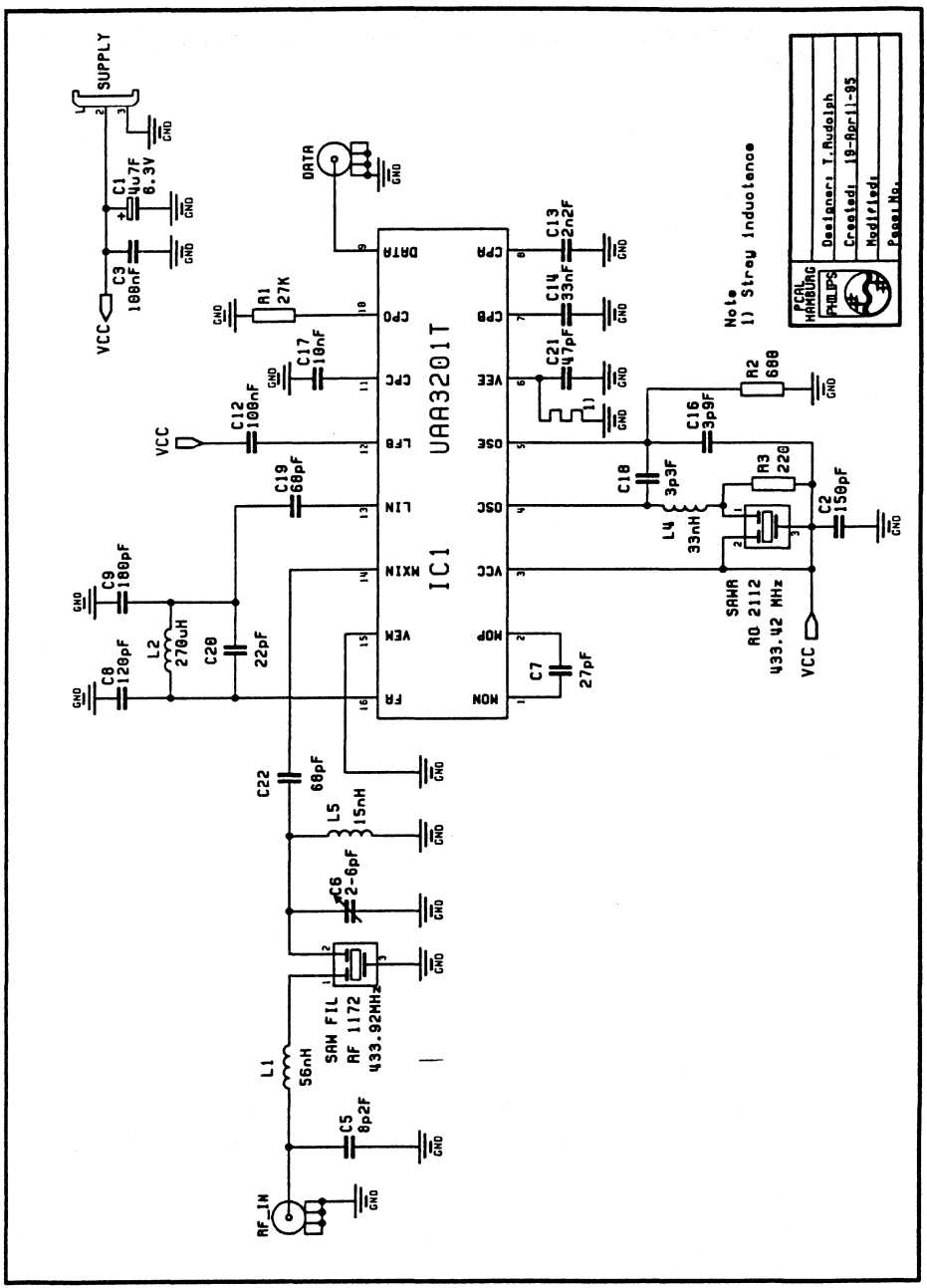


Fig.4 Typical UAA 3201T application with SAW front end filter for 433,92 MHz and 512 bps

The following sections discuss the receiver blocks in more detail and do provide a number of formulas for the designer.

2.1 Mixer

The UAA 3201T incorporates a single balanced emitter coupled mixer with internal biasing, see figure 5

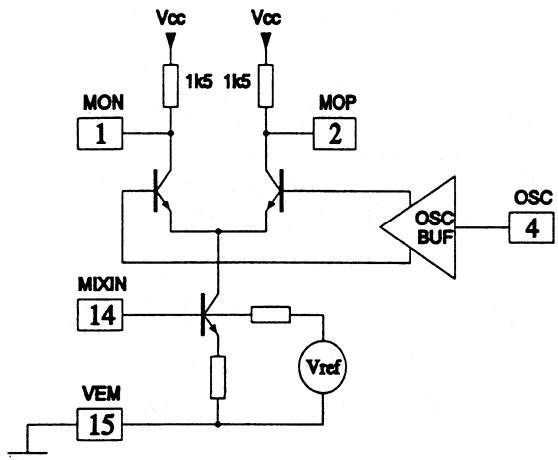


Fig.5 UAA 3201T Mixer

The RF input signal is supplied to the base of the lower stage (pin 14). The mixer input will be matched by means of an external matching network to the desired source impedance. An external DC block has to be provided since the base is biased internally. The separate ground connection (pin 15) provided for the mixer has to be connected externally with the circuit ground.

The mixer load is formed by two resistors and a high input impedance IF amplifier. For filtering purposes a capacitor will be connected externally between the mixer outputs (pin 1 and pin 2).

The local oscillator signal is buffered in order to provide a symmetric drive of the upper mixer stage. The UAA 3201T may be used with an external oscillator source although a typical application would make use of the SAW based on-chip oscillator. In any case the oscillator signal is applied to the input of the buffer (pin 4).

2.1.1 Mixer characteristics

The mixer efficiency is a function of the oscillator drive level. Figure 6 shows the mixer conversion efficiency versus the oscillator drive level applied at the oscillator buffer input (pin 4).

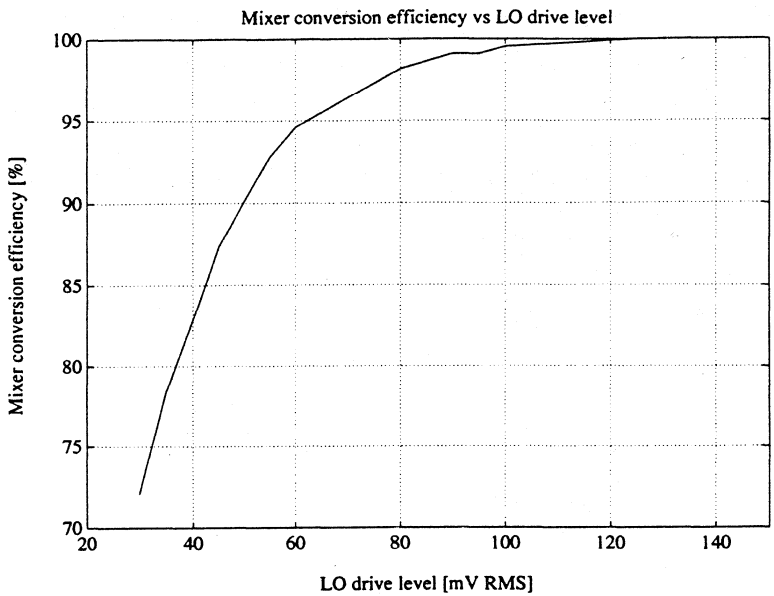


Fig.6 UAA 3201T Mixer efficiency

As can be seen, for sufficient mixer performance it is mandatory to provide at least 70 mV RMS (100 mV peak) of oscillator signal. However, it is recommended to keep the drive level below 140 mV RMS (200 mV peak).

The mixer provides a conversion gain (power gain) of about 15 dB, see figure 7.

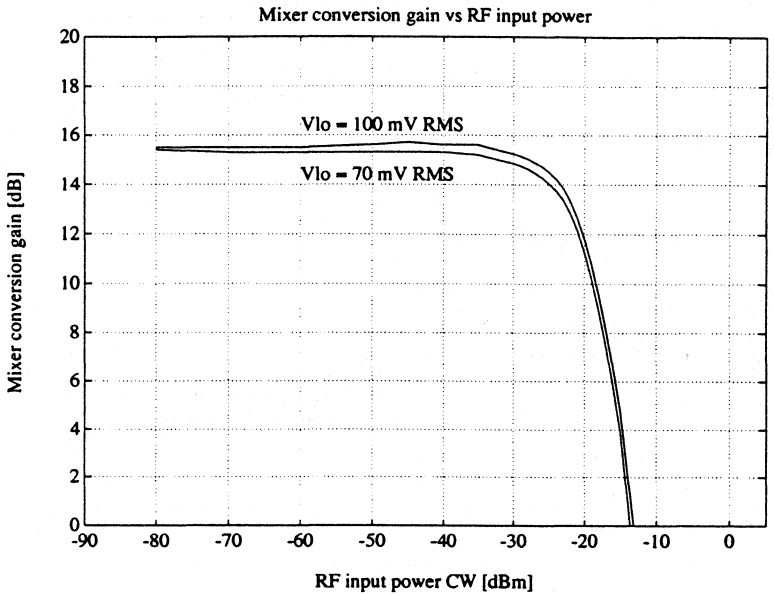


Fig.7 UAA 3201T Mixer conversion gain

As demonstrated in figure 6 the mixer efficiency is a function of the oscillator drive level. However, the mixer provides sufficient conversion gain when the oscillator drive level is at least 70 mV RMS (100 mV peak). A 1 dB conversion compression takes place when the RF input power reaches about -30 dBm. If the RF input power is increased further the mixer saturates and the mixer output power reaches an upper limit of about -9 dBm, see figure 8.

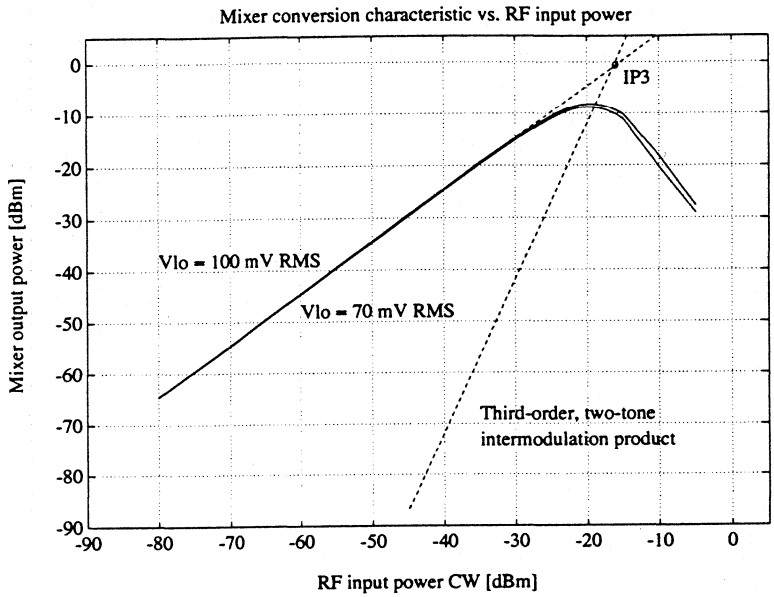


Fig.8 UAA 3201T Mixer conversion characteristic

If the input power is increased further a bias clamping circuit internal to the UAA 3201T will become operational. As a result the mixer output power decreases, starting at about -20 dBm input power.

The mixer provides a third-order intercept point of about -17 dBm, with respect to the input.

Please note that due to the limited amount of filtering after the mixer stage, the following IF amplifier has to be taken into account for a intermodulation analysis. For this purpose figure 9 shows the UAA 3201T Mixer/IF-Amplifier conversion characteristic.

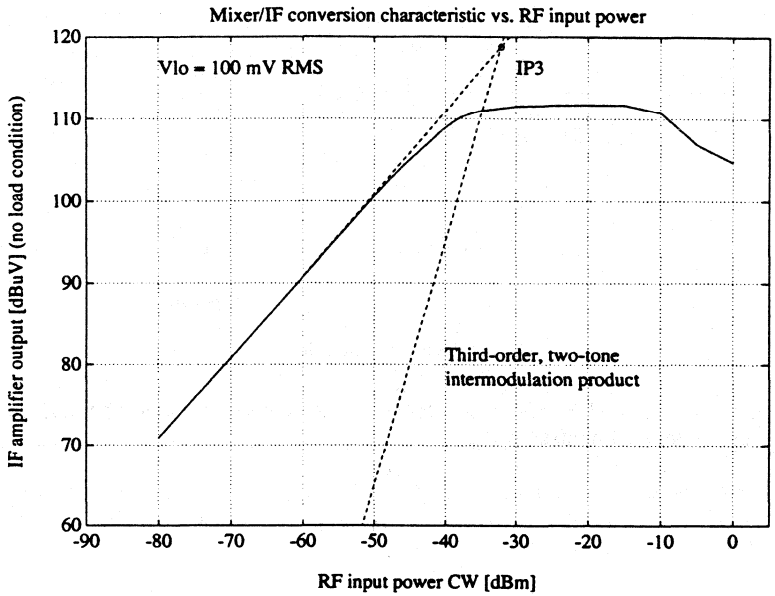


Fig.9 UAA 3201T Mixer/IF amplifier conversion characteristic

For RF input signals stronger than -35 dBm the IF-Amplifier starts to saturate, providing an output level of about 111 dBuV at the IF amplifier output (pin 16, no load condition). The Mixer/IF-Amplifier chain comes up to a third-order intercept point of about -32 dBm.

Due to the mixer bias clamping circuit the IF-Amplifier output level decrease when the RF input power exceeds -15 dBm.

The Mixer/IF intermodulation characteristic presented is valid for interfering signals that fall inside the pass band of the low pass filter that is connected at the mixer output (C7 between pin 1 and pin 2). The Mixer/IF-Amplifier conversion characteristic would improves for interfering signals that are attenuated by means of the low pass filter. The low pass is designed for a 3 dB cut frequency of typically 2 MHz, but may be changed if desired, see section IF filtering.

2.1.2 Mixer input matching

The mixer input is a single ended input which requires some impedance match, in order to obtain the best sensitivity, see figure 10.

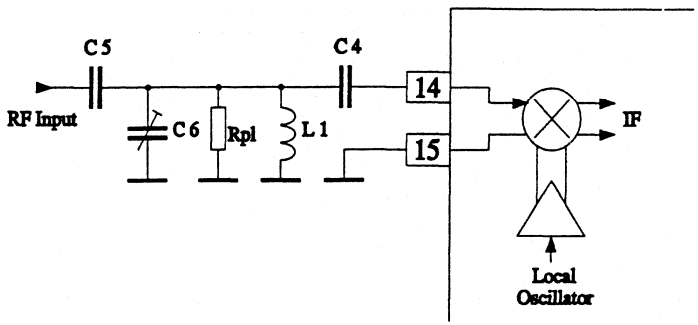


Fig.10 Mixer input matching

When noise matching is desired, the RF source impedance should be transformed to about 320 Ω (f_{RX} = 430 MHz) and presented to the mixer input.

However, evaluation of the device revealed that for best sensitivity a power match should be provided, since a typical UAA 3201T application is gain limited rather than noise limited. The mixer parallel input resistance (Rp) and capacitance (Cp) are given in figure 11 and 12.

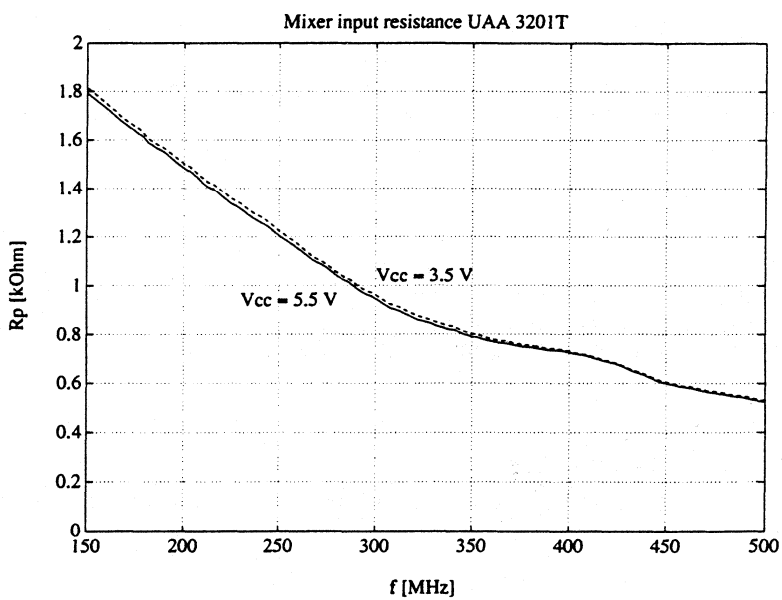


Fig.11 Typical mixer input resistance

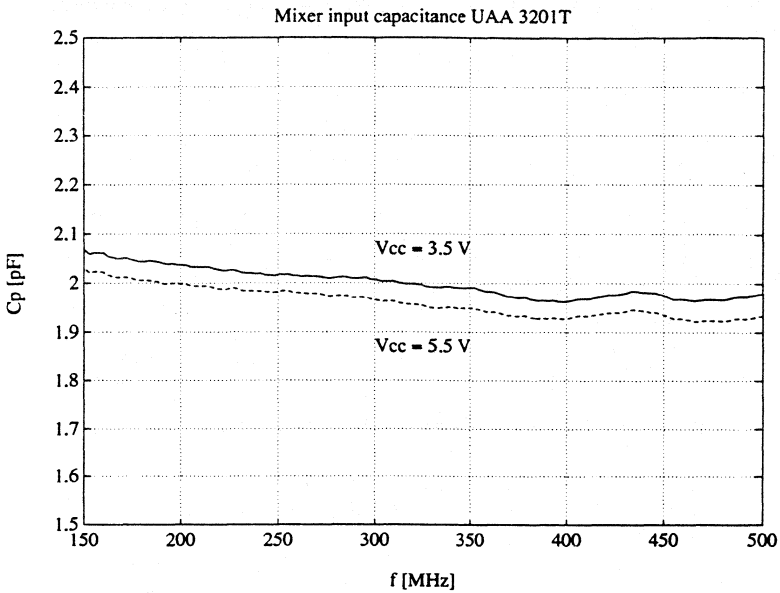


Fig.12 Typical mixer input capacitance

The matching may be performed by a simple L-network with series capacitor (L 1 and C 5). Due to the high receive frequency possible, the network inductance might become relatively small. Please be aware of the limited quality factor for the inductance used and take the additional loss, expressed by Rpl, into account. C 6 might be introduced for tuning purposes, in order to achieve best sensitivity. If a loss of sensitivity over component and device spreads are tolerated, C 6 may be replaced by a fixed capacitor.

Since the mixer input is DC coupled internally, it is mandatory to provide a DC blocking capacitor externally. For easy PCB layout it is practical to use a capacitor in series with the mixer input (C 4).

2.2 Image rejection and front-end filtering

Typically the receivers image response falls into the operating frequency band as a result of the relative small IF (typically 500 kHz). Since the receive frequency may be as high as 450 MHz, image rejection is difficult to provide with a simple L/C input filter resp. matching network as provided by the standard application. However, the standard application has been accepted to lack image rejection in order to keep the receiver system cost at a minimum. The limited filtering capabilities of the L/C matching network is caused by the low loaded Q (typically 15) and limited roll off characteristics (single tuned). Customers who wish to improve this performance are suggested to place in front of the mixer a bandpass filter by means of a Helical (double or triple tuned) or a SAW Filter

A double tuned Helical filter (e.g. TOKO 492S-1053A) would yield a 10 MHz bandwidth while a SAW filter does reduce the bandwidth the to about 800 kHz. Suitable SAW Filters are available from RFM (e.g. RF 1172 433,92 MHz, RF 1211 315 MHz) or Siemens (e.g. B 3530 433,92 MHz, B 3531 315 MHz). Due to the low insertion loss, narrow bandwidth, small size and no need for tuning SAW filters provide an effective and economic

means of front end filtering. An example of a front end SAW filter application at a receive frequency of 433,92 MHz is presented in figure 13.

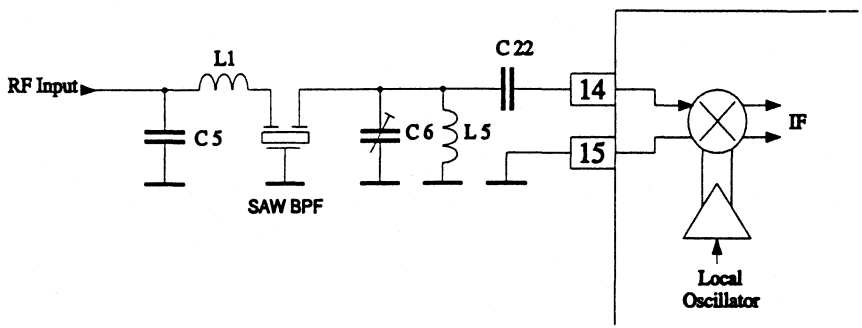


Fig.13 Typical application of a SAW front end filter

Input and output impedance matching of the filter will be necessary to achieve the specified filtering characteristics. For details regarding the terminating impedances consult the filter specifications.

For a receiver operating in Europe at a receive frequency of 433,92 MHz, it is suggested to provide some input filtering by means of a Helical or SAW filter. Please note that due to the analog cellular phone system (C-Netz 450 MHz), the pager system (Cityruf 469 MHz) or broadcast transmitters a number of potential interfering carriers with strong transmit powers are present. Of course this holds in a similar sense for other areas.

In the case a SAW filter is used some simplification for the IF filtering is possible. Due to the narrow SAW filter bandwidth the UAA 3201T IF filter order may be reduced, which saves one chip inductor and two capacitors. For details please refer to the section IF filtering.

A comparison of the receiver response versus frequency with and without SAW front end filter is given in figure 14. The receiver center receive frequency is 433,92 MHz. For a complete schematic of the receiver application used please refer to figure 3 and figure 4.

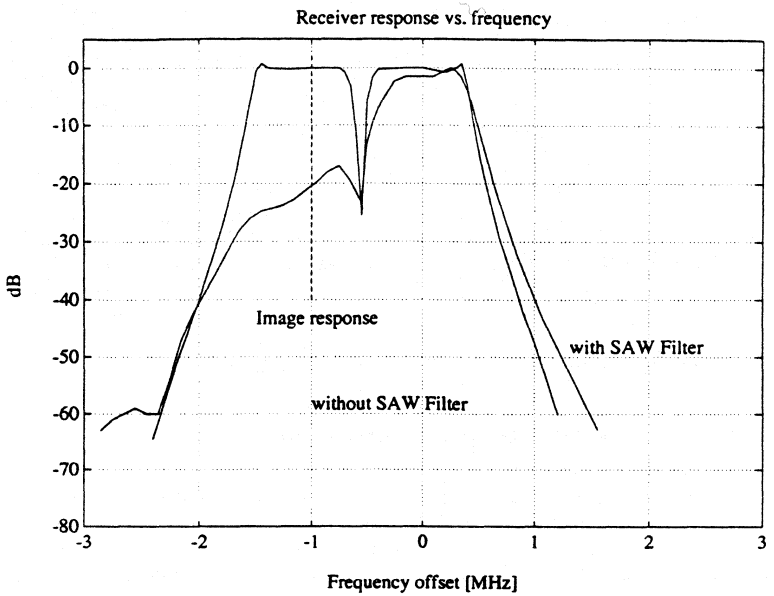


Fig.14 Receiver frequency response

With SAW front end filter (e.g. RFM RF 1172) the image response is attenuated by about 20 dB.

The notch at a frequency offset of about -500 kHz is caused by the fact that the local oscillator is placed about 500 kHz below the desired receive frequency which causes the IF to cross DC.

The receiver response with SAW front end filter shows a less steep stopp band roll-off. At a frequency offset of 1 MHz the difference is about 7 dB. Please note that this is not necessarily the case and caused by the fact that the receiver application with SAW front end filter has been designed for a low order IF filter. This has been done in order to compensate some of the additional cost caused by the SAW filter employed. Of course the designer is free to choose the same IF filter for both applications. In the latter case the application with SAW front end filter does show a better stopp band roll-off characteristic than the application without SAW front end filter.
Obviously the receiver sensitivity reduces slightly due to the SAW-filter insertion loss. In our example the reduction is about 3 dB, as a result the typical receiver sensitivity with SAW front end filter is -105 dBm instead of -108 dBm without filter.

2.3 Local oscillator

The UAA 3201T has been designed to employ a SAW stabilized local oscillator without the need for any frequency multiplication. The SAW device is embedded in a Colpits oscillator with the transistor on-chip, refer to figure 15. Receive frequency and oscillator biasing are controlled by means of the external components.

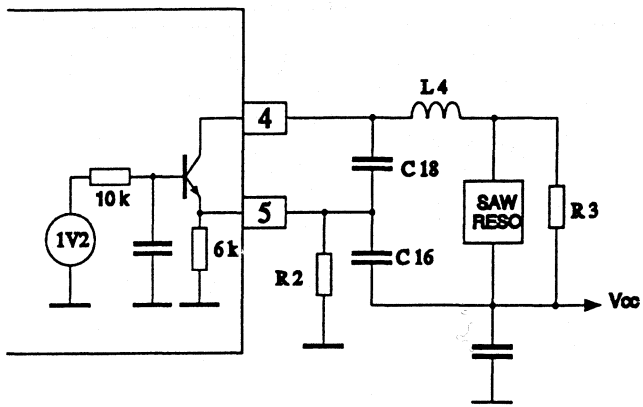


Fig.15 Local oscillator configuration

The on-chip transistor operates in common base configuration by means of the internal capacitor to ground. The transistor operates with the resonant load connected to the collector. The resonant load consists of the SAW and its matching inductance L 4 in parallel with the capacitive divider C 18 and C 16 which provide the oscillator feedback also. The SAW is configured for 1-part operation. Since the SAW operates in series resonant mode its low series resonant resistance of typically some 10 Ω is being transformed to some 100 Ω and presented to the collector. Despite the oscillation condition the design goal is to provide a signal level of at least 100 mVpeak (70 mV RMS) at the collector (pin 4) in order to provide sufficient drive level for the mixer section.

Resistor R 3 serves two functions, first of all it provides the necessary DC path for the transistor biasing. Secondly, it avoids parasitic oscillation of the oscillator due to the SAW's static shunt capacitance.

In order to keep the DC voltage between the SAW terminals small the SAW is connected to VCC instead of to ground. In the latter case an additional DC blocking capacitor should be added.

Resistor R 2 sets the transistor bias current by overriding the internal 6 kΩ resistor. Practical bias current values range between 500 uA and 1 mA.

2.3.1 Local oscillator design examples

Due to the limited number of receive frequencies used so far, ready calculated component values are given rather than an extensive design discussion. As a reference the corresponding part No. from RFM is included. SAW resonators with a similar specification are available from Siemens also.

TABLE 1

f_{RX}	SAW f_{CENTER}	RFM part No.	SAW Rs	L4	C16	C18	R2	R3
433,92 MHz	433,42 MHz	RO 2112	15 Ω	33 nH	3p9 F	3p3 F	680 Ω	220 Ω
433,92 MHz	433,42 MHz	RO 2112A	12 Ω	33 nH	3p9 F	3p3 F	680 Ω	220 Ω
315 MHz	314,5 MHz	RO 2113	12 Ω	39 nH	10p F	6p8 F	680 Ω	220 Ω
315 MHz	314,5 MHz	RO 2113A	12 Ω	39 nH	10p F	6p8 F	680 Ω	220 Ω
315 MHz	314,55 MHz	RO 2076	19 Ω	56 nH	5p6 F	3p9 F	680 Ω	220 Ω
418 MHz	417,5 MHz	RO 2115	19 Ω	39 nH	4p7 F	3p3 F	680 Ω	220 Ω
418 MHz	417,5 MHz	RO 2115A	12 Ω	39 nH	4p7 F	3p3 F	680 Ω	220 Ω
318 MHz	317,5 MHz	RO 2119	12 Ω	39 nH	10p F	6p8 F	680 Ω	220 Ω
318 MHz	317,5 MHz	RO 2119A	12 Ω	39 nH	10p F	6p8 F	680 Ω	220 Ω

Please note that due to the IF frequency of 500 kHz, the SAW center frequency has to be set 500 kHz below (or above) the desired receive frequency. Please note further that due to SAW loading effects, the board oscillation frequency will occur typically about 50 kHz below the specified SAW center frequency. The latter condition holds for the transmit side in a similar sense and as a result will be compensated more or less.

2.4 IF section

2.4.1 IF gain

The total IF gain of over 70 dB is provided by means of two amplifier stages which are connected via low and high pass filters. The first IF amplifier gives about 11 dB of gain and the second amplifier, referred to as the limiter, gives about 63 dB of gain. Hence the overall IF gain is about 70 dB including filter insertion losses, see figure 16.

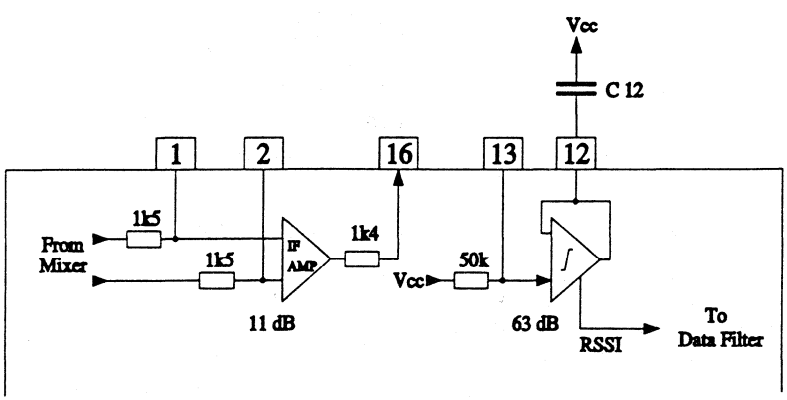


Fig.16 IF gain distribution

The IF amplifier chain itself has an upper frequency limit of about 3 MHz. The lower frequency limit is determined by the limiter feedback capacitor (C 12) and is typically 100 kHz (C 12 = 100 nF).

2.4.2 IF bandwidth

The IF bandwidth has to be chosen according to the frequency error occurring on the receive and transmit side. Due to the SAW cutting tolerance, temperature drift and SAW loading the frequency error may become up to +/- 150 kHz on the receive and on the transmit side. This yields a minimum IF bandwidth of 600 kHz. In order to provide some safety margin, the IF bandwidth has been selected to be 800 kHz, giving additional room for ageing and component tolerances in the oscillator section as well as in IF filter. Assuming an IF center frequency of about 500 kHz, this yields an upper IF cut frequency of about 900 kHz and a lower IF cut frequency of about 100 kHz.
Narrowing the IF bandwidth is troublesome with the SAW resonators available when alignment and components with small manufacturing tolerances have to be avoided. If one even desires to reduce the IF bandwidth down to some 10 kHz he has to accept to replace the SAW by XTAL based oscillators. Due to the upper frequency limit of reasonable XTAL oscillators of about 100 MHz and the limited upper IF frequency possible (about 3 MHz), frequency multiplication has to be employed. On the other hand, narrowing the IF bandwidth would require to use ceramic filters instead of inexpensive L, C and R components.
However, a ceramic filter may be applied to the UAA 3201T. The ceramic filter would be placed in-front of the limiter, thus replacing the Cauer filter. The IF amplifier source impedance (1,4 kΩ) fits to the impedance requirements of standard filter elements. Unfortunately the ceramic filter would require an output impedance match due to the high limiter input impedance (50 kΩ).

2.4.3 IF filtering

Due to the low IF frequency of typically 500 kHz, it is possible to make use of low cost L and C components for IF filtering. The IF filter consists of a simple low pass (C 7) followed by a 5th order Cauer (Elliptic) low pass, see figure 17.

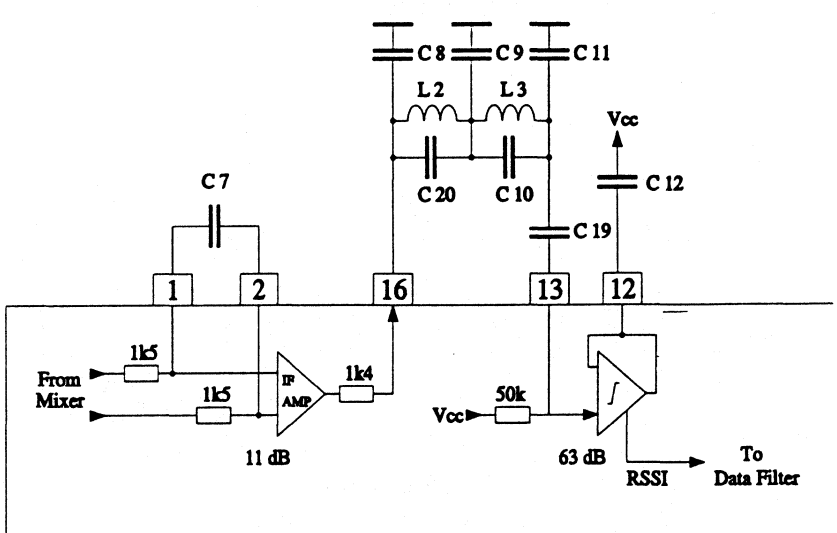


Fig.17 IF filter configuration

In the case of an application with SAW based front end filter, the Cauer filter order may be reduced to a 3rd order type, which saves one inductor and two capacitors. For details refer to the section reduced IF filtering

In any case high pass characteristics is added by means of the limiter feedback capacitor (C 12) and a capacitor in series with the limiter input (C 19). This IF filtering approach is sufficient for a low cost systems which are targeted by the UAA 3201T.

The simple low pass following directly the mixer consists of a capacitor between pin 1 and pin 2 (C 7) with on-chip resistors of 1,5 kΩ for each branch. C7 should be chosen to provide about 1 dB attenuation at the desired upper IF cut frequency:

$$C_7 = \frac{0,51 \times (53,2E-6)}{f_{LP1dB}}$$

The major portion of the IF selectivity is provided by means of a 5th order Cauer (Elliptic) low pass filter in-front of the limiter, connected between pin 16 and 13. The Cauer component values are calculated from normalized values given in a filter catalogue with the desired cut frequency as a parameter. Assuming a cut frequency of 900 kHz, a stopp band start at 1,8 MHz, a pass band ripple of 1,25 dB and a source impedance of 1,4 kΩ the normalized values are as follows:

c_{N11} = 1,580
c_{N9} = 1,883
c_{N8} = 1,097
c_{N10} = 0,171
c_{N20} = 0,070
l_{N3} = 1,340
l_{N2} = 1,346

With

$$L_{CX} = l_{NX} \times \frac{222,8}{f_{CUT}} \text{ and } C_{CX} = c_{NX} \times \frac{113,7E-6}{f_{CUT}}$$

the calculated component values yield:

C_{C11} = 200pF
C_{C9} = 238pF
C_{C8} = 139pF
C_{C10} = 22pF
C_{C20} = 9pF
L_{C3} = 331uH
L_{C2} = 333uH

The real board values differ from the calculated values in order to meet a standard value and in order to take the parasitic capacitance of the coils L 2 and L 3 into account. L 2 and L 3 should provide a high self resonance frequency (SRF), in order to keep the parasitic capacitance at a minimum. We recommend to use coils with a minimum SRF of 4 MHz and a tolerance of 5 % (e.g. TOKO 43FS 300HS-331J, TDK NL453232T-331J-3). Coils having a tolerance of 10 % may be used, when a reduced filter performance as a result of component variations is accepted.

The limiter high-pass characteristic is determined by the value of C 12 at pin 12. C 12 is the limiter feedback

capacitor, which provides a DC feedback, in order to set the appropriate bias conditions. AC wise C 12 short circuits the negative limiter input to ground, enabling the limiter gain to become 63 dB. Designing the capacitor for the 3 dB cut off point yields:

$$C_{12} = \frac{10,7E-3}{f_{HP3dB}}$$

For a cut frequency of about 100 kHz C 12 becomes a 100 nF capacitor. C 12 is connected to Vcc in order to minimize the receiver settling time after power-up. When receiver settling is not an issue, C 12 may be connected to ground in order to ease board layout.

The second high-pass is formed by means of C19. C19 provides the necessary DC block to the limiter input and forms a high pass filter taking advantage from the limiter input resistance of about 50 kΩ. C19 should be chosen to provide about 1 dB attenuation at the desired cut frequency:

$$C_{19} = \frac{2 \times (3,2E-6)}{f_{HP1dB}}$$

Figure 18 shows the IF frequency response with standard component values according to the application diagram given in figure 3.

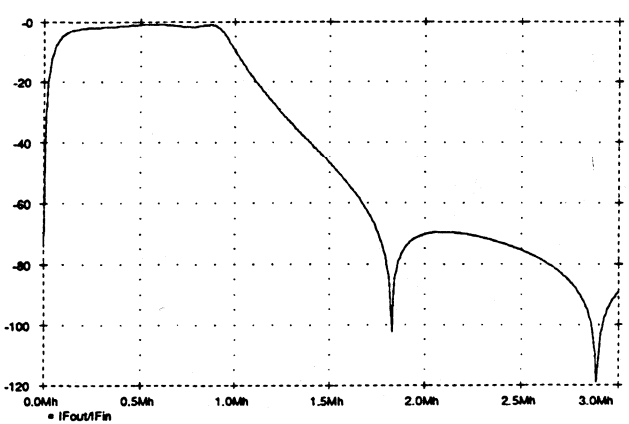


Fig.18 IF frequency response

2.4.4 Reduced IF filtering

As mentioned already the Cauer filter order may be reduced to a 3rd order type in the case of an application with SAW based front end filter. On the one hand, this saves one inductor and two capacitors in order to compensate for some of the additional SAW filter costs. On the other hand, this reduces the IF filter stopp band roll-off characteristic and ultimate stopp band attenuation. However, due to the action of the SAW front end filter the ultimate stopp band attenuation reduction is fully compensated by the SAW filter. The difference in the stopp band roll-off remains, but usually does not cause any major problems.

Figure 19 gives the modified schematic for the 3rd order Cauer filter.

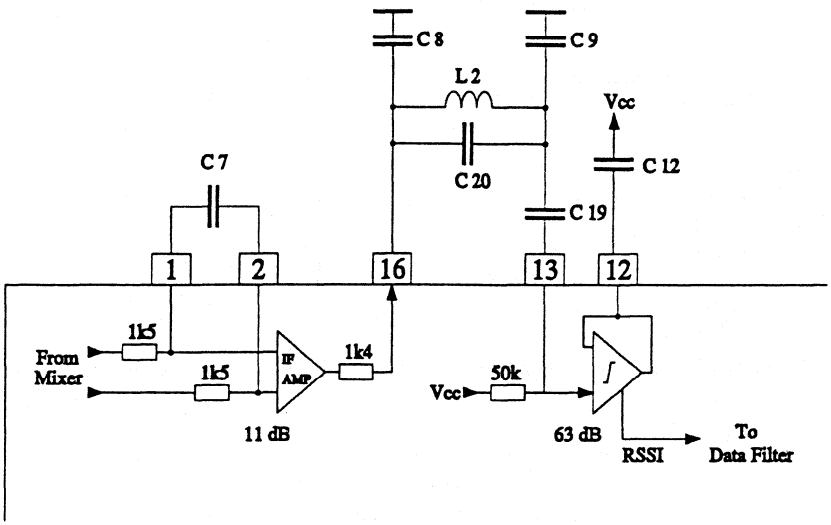


Fig.19 IF filter configuration with 3rd order Cauer filter

The design of a 3rd order Cauer filter is similar to the design of a 5th order Cauer filter. Apart from the configuration only the normalized values are different. Assuming a cut frequency of 900 kHz, a stopp band start at 1,8 MHz, a pass band ripple of 1,25 dB and a source impedance of 1,4 kΩ the normalized values from the filter catalogue are as follows:

c_{N9} = 1,472
c_{N8} = 0,965
c_{N20} = 0,171
l_{N2} = 1,132

With

$$L_{CX} = l_{NX} \times \frac{222,8}{f_{CUT}} \quad \text{and} \quad C_{CX} = c_{NX} \times \frac{113,7E-6}{f_{CUT}}$$

the calculated component values yield:

C_{C9} = 186pF
C_{C8} = 122pF
C_{C20} = 22pF
L_{C2} = 280uH

The real board values differ from the calculated values in order to meet a standard value and in order to take the parasitic capacitance of the coils L 2 into account. L 2 should provide a high self resonance frequency (SRF), in order to keep the parasitic capacitance at a minimum. We recommend to use coils with a minimum SRF of 4 MHz and a tolerance of 5 % (e.g. TOKO 43FS 300HS-271J, TDK NL453232T-271J-3). Coils having a tolerance of 10 % may be used, when a reduced filter performance as a result of component variations is accepted.

Figure 20 shows the IF frequency response with standard component values according to the application diagram given in figure 4.

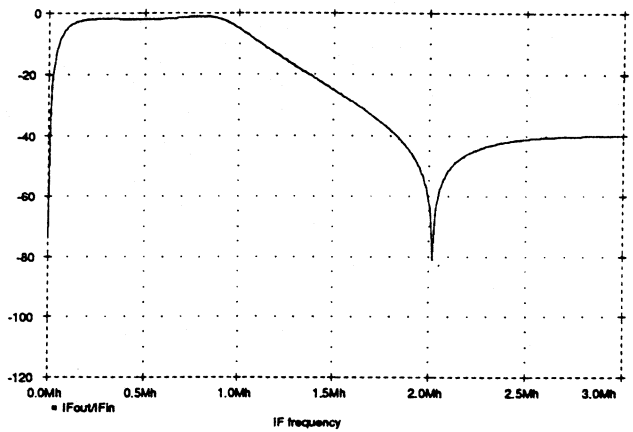


Fig.20 IF frequency response with 3rd order Cauer filter

Compared with the IF response employing a 5th order Cauer filter (figure 18) it becomes evident that the 3rd order Cauer application has a less steep stopp band roll-off and a weaker ultimate stopp band attenuation. However, the lack of ultimate stopp band attenuation is compensated by the action of the SAW front end filter and thus not critical.
In the case one doesn't accept the reduced stopp band roll-off characteristic the 5th order Cauer application should be used.

2.4.5 Demodulation

After passing the Cauer filter the IF signal is feed to the limiter, according to figure 17 resp 19. The limiter serves two functions, amplification and demodulation of the filtered IF signal.

The limiter amplifier rectifies the IF in order to demodulate the received signal. The demodulated signal is refered to as the RSSI (receive signal strength indicator) signal. Figure 21 shows the relation between RSSI level and limiter input level.

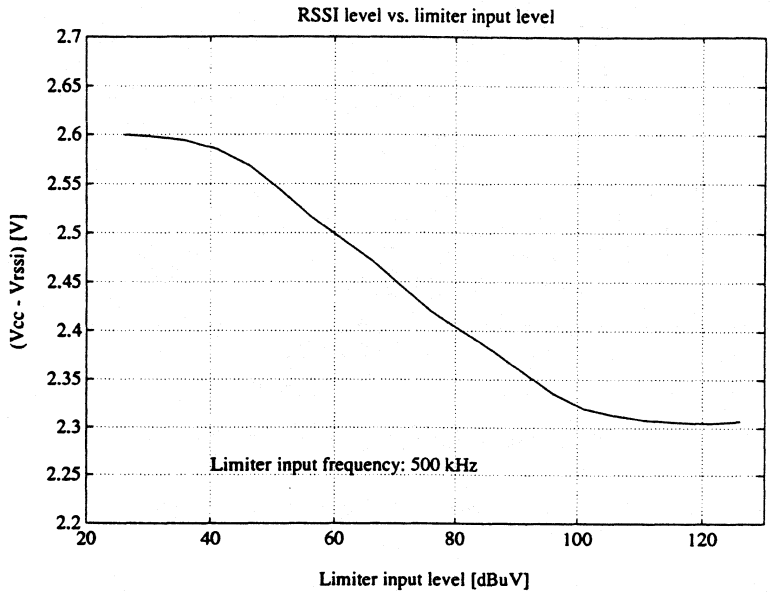


Fig.21 Limiter demodulator characteristics

Please note that figure 21 gives the voltage difference between V_{CC} and the RSSI node, in order to provide an RSSI reading which is independent from the actual supply voltage (V_{CC}). In any case the RSSI signal is a measure of the transmitted data due to the use of ASK modulation .

2.5 Data filtering

Apart from the demodulated data, the RSSI signal contains unwanted frequencies which are removed by low pass filtering before data slicing takes place, see figure 22.

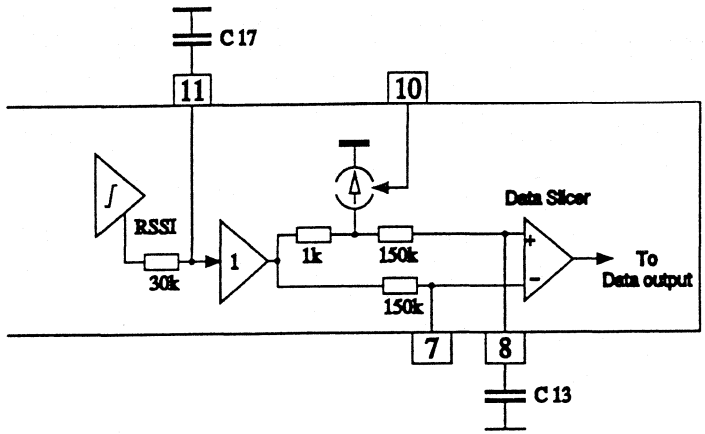


Fig.22 Data filtering

Data filtering is provided by means of two R/C low pass filters. The low pass cut frequencies are determined by the external capacitors C 17 and C 13.

The data filter bandwidth has to be selected wide enough in order to allow the data to pass and on the other hand, should be as narrow as possible to keep the noise bandwidth small. Thus a trade off has to be made. The standard filter design would target a 1,5 dB attenuation of the data at each filter stage, thus the capacitors would yield:

$$C17 = \frac{2,66E-6}{f_{DAT}}$$

and

$$C13 = \frac{0,53E-6}{f_{DAT}}$$

Where f_{DAT} is the highest frequency component of the data signal received. For example, a 1 kbit/sec Bi-Phase modulated signal corresponds basically to a 1 kHz tone, the same holds for a RZ (return to zero) resp. PWM (pulse width modulated) code.

Although the data sheet gives a typical data rate of 250 bps (RZ), the UAA 3201T can handle higher data rates when the application is modified accordingly. Up to 20 kbit/sec have been achieved with a couple of dB reduction in sensitivity only. Due to the relative high IF bandwidth of typically 800 kHz the data rate limits are set by data slicer and its pre-filtering rather than by the IF filter. A typical figure for the sensitivity reduction is about 2 dB when the data rate is increased from 512 bits/sec to 10 kbit/sec while the data filter capacitors (C 17 and C 13) are reduced accordingly.

Please note that some data coding schemes require a relatively large data filter bandwidth although the effective data rate is relatively low. This holds for Pulse Width Modulation (PWM) when the duty cycle is extremely low, e.g. 10 %. In this case small data pulses need to pass the data filter although the bit period is 10 times the pulse

period (10 % duty cycle assumed). The data filter bandwidth required may be estimated from:

$$BW_{FIL} = \frac{1}{3,14 \times t_{PulseWidth}}$$

In some cases the data filter bandwidth need even be selected wider, in order to recover the transmitted pulse shape as far as possible. As mentioned above, a wider data filter bandwidth does reduce the sensitivity and should be avoided. Thus, an appropriate data coding scheme should be selected. We suggest to use Bi Phase (Manchester) coding or Pulse Width Modulation (PWM) with a duty cycle close to 50 % (e.g. zero equals 40 % and one equals 60 %) or similar methods.

Please note further that the coding scheme should employ a DC average value which is independent of the data content. This is important for a proper operation of the data slicer discussed next.

2.6 Data slicer and slicer threshold

2.6.1 Data slicer

The filtered data signal (RSSI) is feed to the positive input of a data slicer (level comparator) with adaptive slice reference. The slice reference is derived from the data signal by means of a separate low pass filter (C 14), see figure 23.

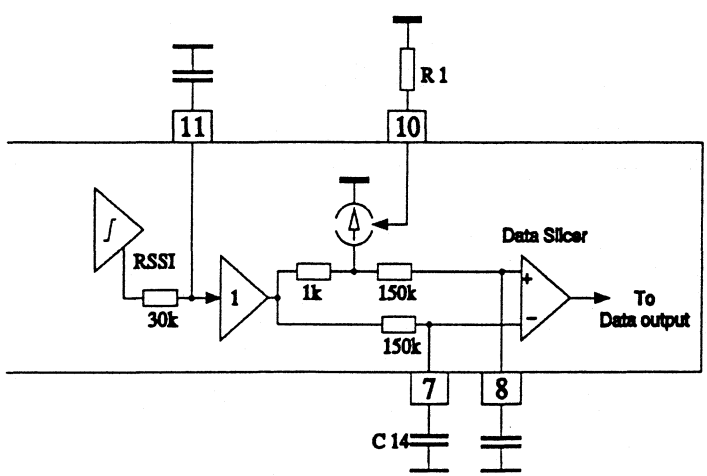


Fig.23 Data slicer with adaptive slice reference

The low pass filter is designed for a long time constant, in order to derive the average RSSI value (DC component of data) as an adaptive reference for the data slicer. The adaptive reference enables the receiver to detect a modulated carrier over a input signal range of more than 75 dB.

Typically the low pass time constant is chosen to be 10 times larger than the data filter time constant:

C14 = 10 x C13

In the case of a modulation signals with a low duty cycle, it might be necessary to increase this time constant. Obviously, it is mandatory that the data coding scheme employs an average DC value that is independent of the data content. Otherwise the data slicer reference would shift according to the data transmitted which has to be avoided for proper receiver operation.

Please note that the time constant selected directly affects the data slicer run-in time and as a result the receiver settling time.

Both input terminals of the data comparator are extremely sensitive to external leakage currents. Especially the slice reference capacitor (C 14) has to be selected very carefully with respect to its leakage current, since this capacitor is typically relative large in terms of its value. Excellent results have been obtained with X7R material which provides low leakage and relatively high capacitance values at small SMD outlines.

2.6.2 Data slicer threshold

By means of an external resistor, a data slicer threshold may be applied which inhibits noise to be present at the data output when no RF carrier is present. This function is similar to a squelsh function. The data output will remain low until sufficient RF power is applied to the RF input. The threshold is basically a voltage drop across the on-chip 1 kΩ resistor in series with the positive comparator input, which acts like an additional offset voltage across the comparator inputs, see figure 23.

An external resistor (R 1) controls the current source that determines the voltage drop across the on-chip 1 kΩ resistor. Figure 24 gives a plot of the additional offset voltage as a function of R 1.

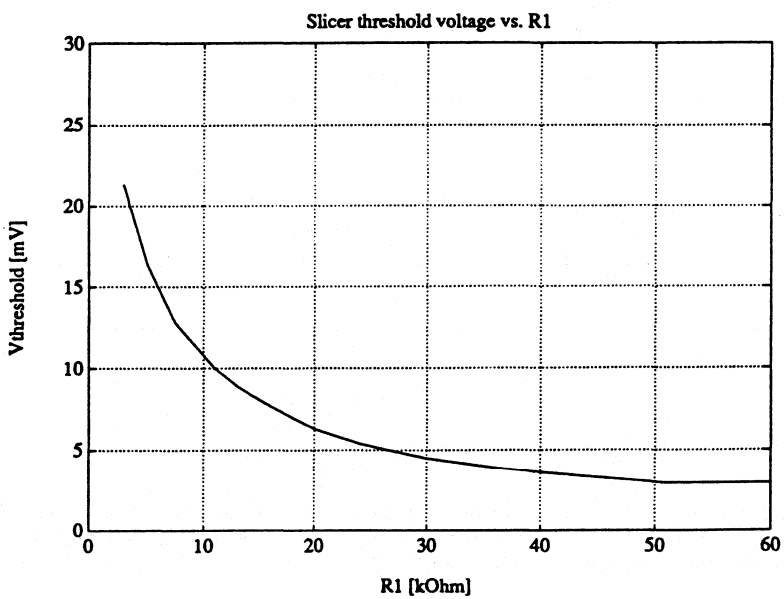


Fig.24 Data slicer threshold voltage.

As a result, the receiver sensitivity drops since the mixer input power has to exceed a certain level before data

slicing takes place. Figure 25 gives a typical plot for the receiver sensitivity measured with a demonstration board H5ACS01 as a function of R1 (receive frequency 433,92 MHz, modulation 250 Hz ASK).

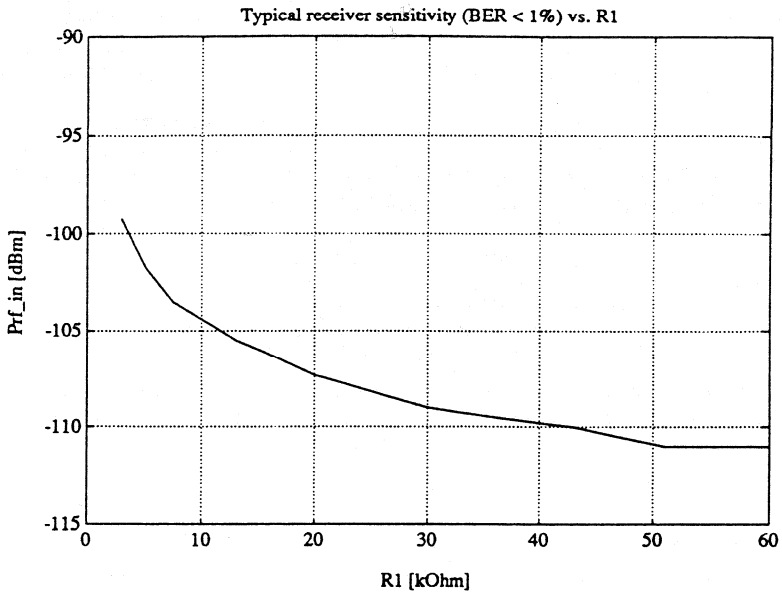


Fig.25 Typical receiver sensitivity

The data slicer threshold is useful for systems where the digital part, responsible for data decoding, shall consume minimum power by means of a power down mode. For such a system the digital part will be powered-up only, when a RF carrier is detected. Connecting the data slicer output to some kind of wake-up control input for the digital part, would not power-up the digital part before a RF carrier with sufficient power is detected.

When R 1 is not applied, thus no threshold is present, the receiver sensitivity will be best. According to figure 24 the receiver sensitivity improves to about -113 dBm when R1 is not applied, while it is -109 dBm when a 27 kΩ is selected for R1.

Again, please note that with no RF input present and R 1 not applied some sort of digital noise will be present at the data output during the absense of a RF carrier.

2.7 Data output configuration

The UAA 3201T data output is basically a open collector architecture with internal pull-up by means of a current source, see figure 26.

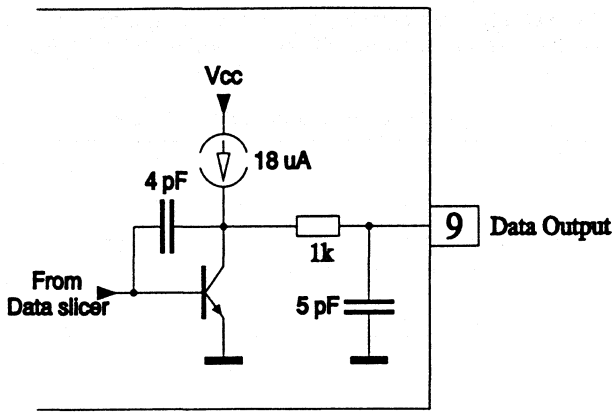


Fig.26 Data output configuration

The source capabilities are limited due to the internal current source of 18 uA. The data output is typically able to sink about 200 uA. An on-chip protection resistor of 1 kW and a dump capacitor of 5 pF are placed between the transistor and the data output port.

3. Supply current reduction by intermittend receiver operation

The typical operating supply current for the UAA 3201T is about 3,7 mA. However, various receiver applications target an average receiver supply current of 2 mA and less. If an intermittent receiver operation is allowed the average supply current may easily be reduced to less than 2 mA. For an intermittent receiver operation a number of parameter need to be considered, like receiver settling time, receiver On/Off duration and system response time.

Although the data sheet UAA 3201T specifies a receiver settling time of 10 ms, one can reduce the receiver settling time to 5 ms and less by proper application. As a result, the designer is almost free to choose the system response time and receiver On/Off duration according to his needs, so that the average supply current requirements are met.

The receiver settling time depends on a number of application parameter:

- The power supply slew rate
- The receiver On/Off duration
- The data filter design
- RF input power applied to the mixer

From the above the most important one is the power supply slew rate. It is important to note that the power On as well as the power Off slew rate need to be considered. In order to minimize the receiver settling time, the receiver power supply should be switched Off and On very fast providing a very steep voltage step at the UAA 3201T V_{CC} terminals. This avoids a complete discharge of the capacitor external to the UAA 3201T and as a result a fast recovery from receiver Off is achieved.

In order to provide a steep change at the V_{CC} terminals, it is mandatory to place the large electrolyte by-pass

capacitor right before the supply switch, see figure 27.

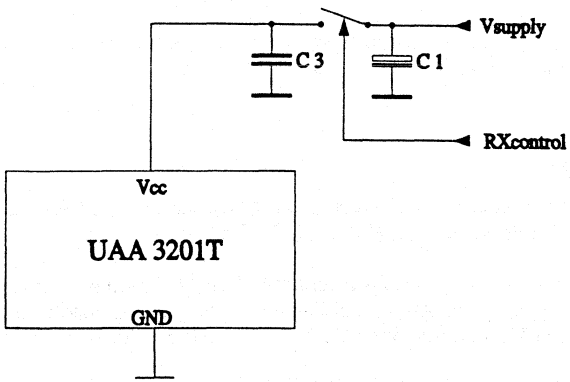


Fig.27 Power supply concept for intermittent receiver operation

The IC supply now drops more or less instantly when the switch is opened avoiding discharge of the external capacitors as much as possible. As a result, the settling time achieved is about 10 ms when the receiver is switched On and Off periodically. Please note that the initial settling time, when the receiver is Off for a very long time, will increase to a couple of 10 ms depending on the capacitor values external to the UAA 3201. However, the initial settling time is of minor interest usually.

The receiver settling time may be reduced to about 5 ms and less when an additional discharge resistor is incorporated. The resistor shall accelerates the discharge of the V_{CC} by-pass capacitor (C3), see Figure 28.

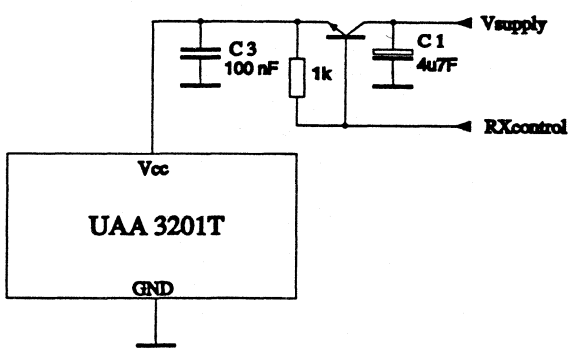


Fig.28 Power supply concept for intermittent receiver operation with fast recovery

Care has to be taken during selection of the receiver On time. For a proper intermittent receiver operation it is recommended to select a receiver On time of at least 20 ms for the application given above. Shorter receiver On times may be obtained when the value of capacitor C 14 (data slicer reference) is reduced.

Since the value of C14 is fixed during the design of the data filter it is recommended to make use of a data coding scheme that allows C14 to become relatively small. More exactly speaking, it is suggested to use Bi-Phase coding rather than Pulse-Width coding when a fast receiver settling is desired.

Please note that the receiver settling time values mentioned so far have been measured at the threshold of sensitivity. When the receiver RF input power is increased the settling time reduces at the same time. The lowest settling time that could be expected is about 1 ms with a RF input power of approx. 10 dB above the threshold of sensitivity or higher.
Almost any average supply current could be achieved by proper selection of the duty cycle, while having control over the system response time by means of the repetition rate used.

4. Spurious radiation

Like any other communication equipment a receiver application based on the UAA 3201T has to meet the requirements of the local PTT authorities (e.g. FCC, CEPT, FTZ, etc).

Of special interest are the spurious radiation characteristics of the whole receiver and special care has to be taken during PCB layout and component placement. The most stringent regulations in terms of spurious radiation have been set by the German FTZ. According to FTZ 17 TR 2100 the limits for spurious radiation on the receive side are:

- 60 dBm in the range 25 MHz to 1 GHz respectively
- 45 dBm in the range 1 GHz to 40 GHz

The UAA 3201T is applicable to meet these requirements.

Two different radiation sources have to be considered, antenna radiation and board radiation.

Obviously, antenna radiation can not be controlled by means of shielding, it need to be controlled by proper application. Detailed evaluation of the UAA 3201T revealed that in order to meet the radiation limit of -60 dBm at the antenna input (mixer input), a special device ground configuration need to be employed, figure 29.

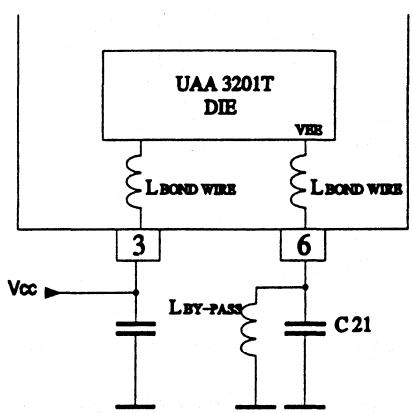


Fig.29 Recommended UAA 3201T ground configuration

Due to the internal bond wire and package inductance between the die and the solder pad, the die ground connection presents a relative high series impedance at radio frequencies (e.g. 10 Ω at 450 MHz). Because of the local oscillator AC current a small RF voltage drop develops which will be present at the mixer input also due to parasitic effects.

In order to meet the spurious radiation limit of -60 dBm at the mixer input, the unwanted ground impedance has to be cancelled by means of a series capacitance (C 21) in resonance with the parasitic inductance. Assuming a parasitic inductance of 3 to 4 nH the capacitor yields:

$$C21 = \frac{1}{(2 \times 3,14 \times f_{SAW})^2 \times 3nH}$$

Please note that for effectiveness of this circuit it is important to keep any additional board stray inductance at a minimum. It is therefore mandatory to place the capacitor C 21 as close as possible to the solder pad for pin 6. Any millimetre of stray length would add about 0,8 nH of additional inductance. With the result that the capacitor value would have to be reduced and the effectiveness is decreased. Obviously, it is mandatory to provide a very short connection form the capacitor to the board ground plane also. A number of hints regarding the board layout are going to be presented in the chapter layout considerations.

By proper circuit application the spurious radiation decreases by about 16 dB to approximately -70 dBm, as demonstrated by the reference board given in the data sheet or by the demonstration boards H4ACS21. For details regarding the demonstration boards please refer to the corresponding laboratory notes published. In the case less attention is paid to this part of the board layout 6 dB may easily be lost, resulting in a spurious radiation of -64 dBm only. Nevertheless, this is still sufficient for meeting the regulations of FTZ 17 TR 2100, providing sufficient safety margin for component tolerances.

Since the DC biasing for the UAA 3201T has to be maintained, the compensation capacitor has to be by-passed with a sufficient large inductance (e.g. 10 times 3 nH). The by-pass inductance may be a chip inductance type or an almost free of charge stray inductance, if free board space is available. The later one has been proved to be very effective.

In the case the local authorities set less stringent limits for the spurious radiation (e.g. US, FCC Part 15) one could even try to omit the components and connect the device ground directly to the board ground reference. In this case the spurious radiation does not exceed -52 dBm.

Apart from antenna radiation board radiation is also present. Unlike antenna radiation, board radiation can be controlled by means of board shielding. Since shielding is expensive, one is keen to solve the board radiation by proper application. According to our experience shielding can be avoided when special care is taken during PCB layout, component selection and component placement.

The source of unwanted radiation is the local oscillator. In order to minimize the board radiation the board layout for the oscillator section should be as compact as possible.

Please note that long interconnecting traces act as an antenna and are likely to emit spurious signals. Due to the availability of small SMD components this task may easily be performed.

For the oscillator section it is therefore recommended to use SMD components of style 0805 or even 0603. Although SAW resonators are available in SMD package (e.g. from RFM or Siemens) one might prefer to use a pin through type. In this case it is recommended to place the SAW resonator on the opposite side of the board, right below the IC in order to keep the interconnecting traces short. The oscillator layout of the UAA 3201T demonstration board H5ACS01 with single sided component placement may be used as a reference, please refer to the corresponding laboratory note and to the chapter layout considerations.

Apart from the layout, a major portion of board radiation is caused by L 4 in the local oscillator section, please refer to figure 15. For minimum board radiation it is recommended to use a shielded inductance. Suitable shielded inductance are available from Coilcraft (e.g. 164-02A06S resp. -03A06S). Unfortunately this inductance are not available in SMD style today.

Finally it should be noted that an application like this, running at a high frequency, requires a proper by-passing resp. blocking of the supply rails. With respect to spurious radiation the value and placement of the oscillator supply by-pass capacitor is important.

5. Supply by-pass considerations

Proper by-passing respectively blocking of the supply rails is mandatory for a good receiver performance. Three areas should be paid special attention. The oscillator section, the limiter section and the supply feed point, please refer to figure 3 resp. 4.

For a safe oscillator operation it is mandatory to place the supply by-pass capacitor (C 2) as close as possible to the oscillator section, providing a well by-pass for the V_{CC} and SAW feed point to the ground plane. For receive frequencies in the 400 MHz region a capacitor value of about 150 pF should be preferred, while in the 300 MHz region a value of about 220 pF should be selected. The capacitor must not become to large, otherwise its inherent series inductance would dominate and cause the by-pass to become inductive instead of capacitive. The required by-pass capacitor may be estimated from a calculation of the series resonant frequency (SRF) assuming an inherent self-inductance of approximately 1 nH for capacitors style 0805 NPO.

$$C = \frac{1}{(2 \times 3,14 \times f_{RX})^2 \times 1nH}$$

Improper by-passing may result in a unstable oscillator operation and an increased spurious radiation.

For reasons of a minimum receiver settling time, the limiter feedback capacitor (C 12) is connected to the supply rail instead of to the ground plane. Since the limiter provide more than 60 dB of gain, any noise or ripple at this supply feed point degrades the receiver sensitivity. It is therefore recommended to employ short connections for the capacitor to the IC solder pad (pin 12) as well as to the supply rail. A sufficient large by-pass capacitor for the supply rail (C 3) should be placed at the point where the limiter feedback capacitor connects to the supply rail. Improper by-passing or extreme long traces may results in a decreased sensitivity or an susceptibility to interfering signals by capacitive or inductive coupling .

The supply feed point should employ an medium value by-pass capacitor (e.g. 100 nF) as well as a relatively large electrolytic or tantal capacitor (e.g. 4u7 F). In the case the receiver shall operate in an intermittent way, the supply control switch should be placed between these two by-passing capacitors in order to achieve fast receiver settling. Please consult the chapter supply current reduction by intermittent receiver operation also.

6. Layout considerations

For optimum receiver performance in terms of sensitivity, spurious radiation and susceptibility to interfering signals the following layout hints should be considered. Many of the hints presented in this chapter have been discussed in earlier chapters already and are presented here again in a more dense context. For details please consult the previous sections.

It is recommended to use a double sided PCB which provides an almost solid ground plane for connection of the device ground by-pass capacitor, oscillator by-pass capacitor and the mixer ground. As demonstrated by the demonstration board H5ACS01 single sided component placement is feasible which occupies about 5 cm^2 (0,8 square inch) of PCB area only, please refer to the corresponding laboratory report for PCB drawing details. A single sided PCB may be used, however, it is expected that the receiver performance in terms of spurious radiation and sensitivity will be reduced significantly.

Layout and component placement should start with the device ground by-pass capacitor and the oscillator section, since these areas are the most important ones with respect to spurious radiation and oscillator stability resp. receiver sensitivity. The ground by-pass capacitor (C 21) should be as close as possible to the device solder pad (pin 6), any millimetre of wire length counts (less than 2 millimetre wire length is recommended). At the same time the opposite side of the capacitor should be routed directly to the ground plane. A well design would use two vias for the connection to the ground plane on the opposite PCB side. Figure 30 and 31 show the H5ACS01 PCB layout as a reference. For your reference the H5ACS01 schematic is given in figure 32 at the end of this chapter, however, it is mostly identical with the typical application given in chapter 2. It differs from it in two respects, first it allows different SAW resonators packages to be assembled (pin through and SMD style) and secondly it provides a measure for an intermittent receiver operation by means of a power supply switch (T 1).

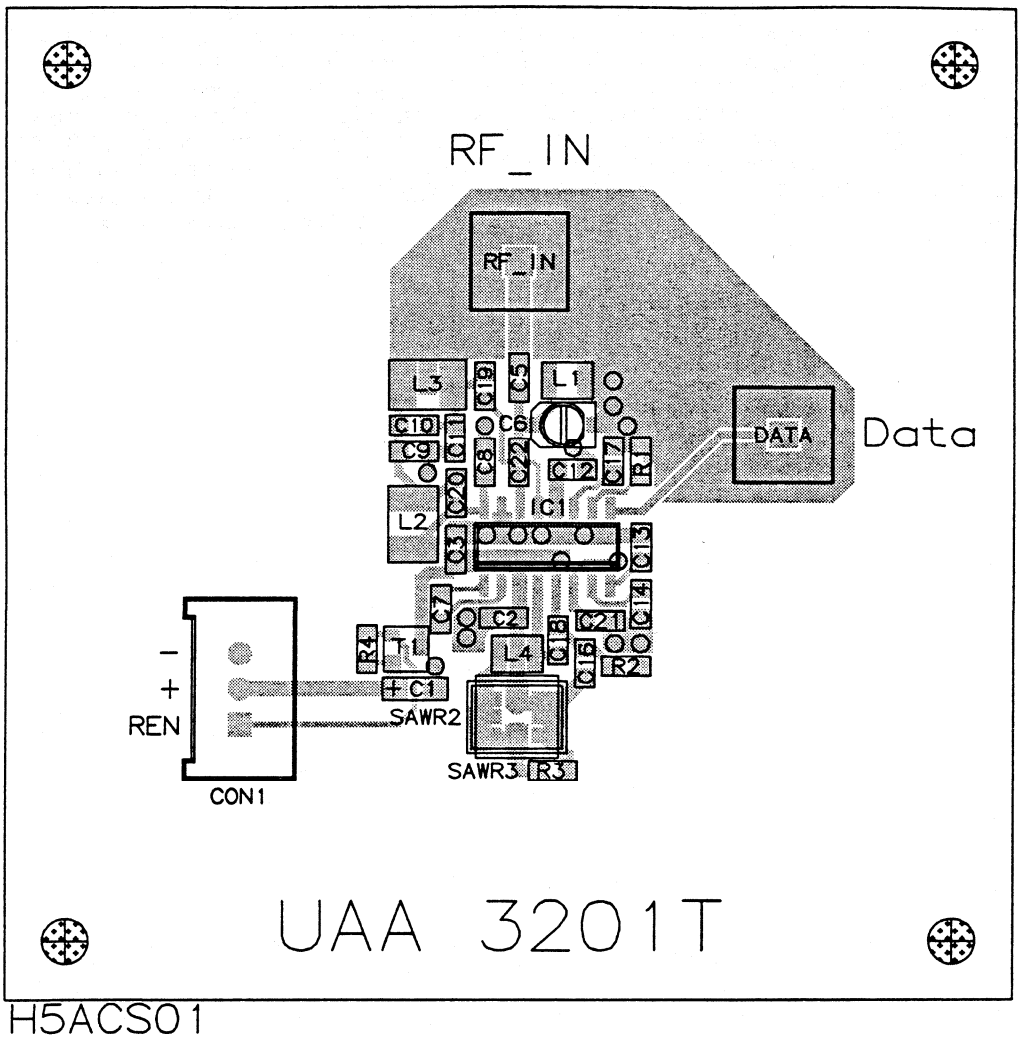


Fig.30 PCB layout example, topside

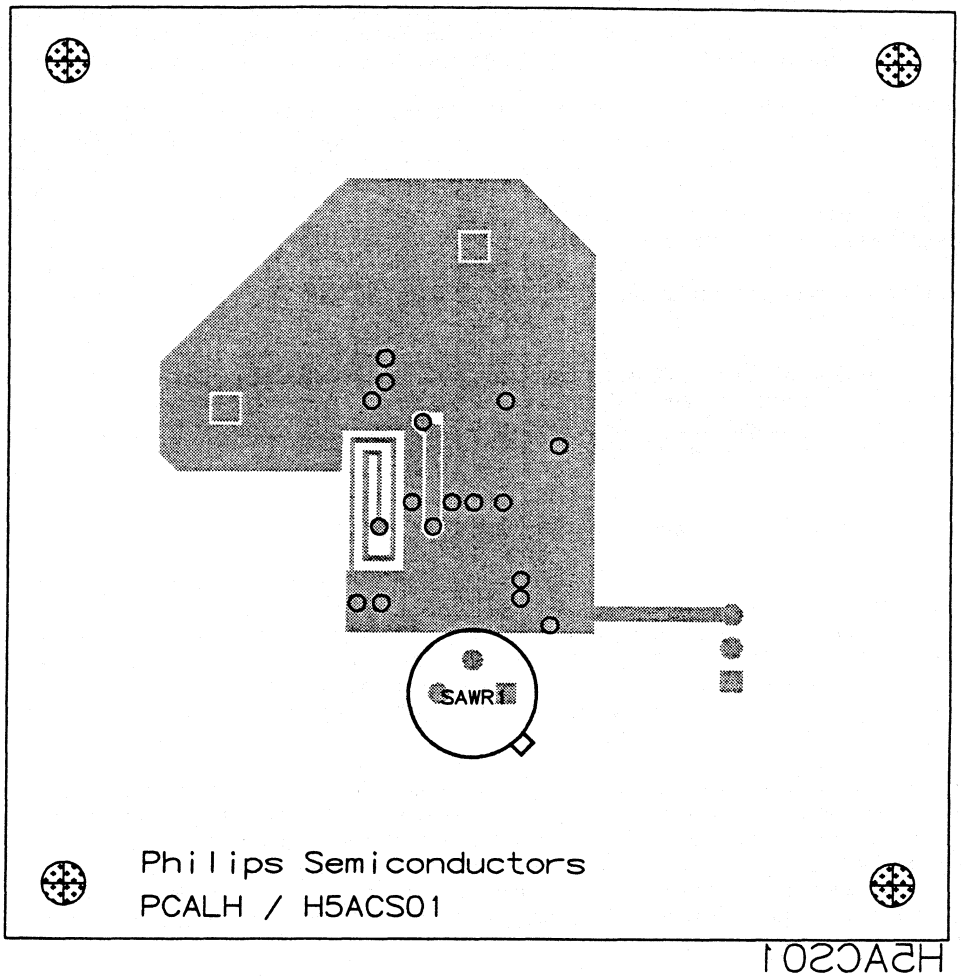


Fig.31 PCB layout example, bottomside

'lease note that the H5ACS01 layout may beoptimized with respect to the LO radiation measured at the mixer ıput by means of a reduced wire length between pin 6 and C 21. The LO radiation at the mixer input can be nproved by 3 to 6 dB, when C 21 is placed closer to the UAA 3201T pin 6. The value of the by-pass capacitor ; 21 may likely be modified slightly in order to account for the actual PCB layout.

:xcellent results are obtained with a PCB using double sided component placement, since the by-pass capacitor ıay be placed on the back side directly under the IC within the ground plane. This allows to run an extreme short ire to the solder pad, again two vias are recommended.

The DC by-pass inductance may be placed according to the options the designer has, either as SMD chip inductance or as a wire stray inductance if sufficient space is available. Specific rules do not exists, with the exception that the inductance value should exceed 20 nH (a value of 30 nH is sufficient).

After having placed the ground by-pass capacitor the oscillator components should be placed. As a general guide-line it is suggested to keep the capacitors (C 18 and C 16) as close as possible to the SAW resonator and oscillator inductance (L 4). Please note that the SAW resonator, the inductance and the two capacitors form a resonant loop with the loop AC current being approximately Q times higher than the AC feed current. Any superfluous length of wire may be the source of undesired emission. This includes that the oscillator component should be as close as possible to the corresponding device solder pads (pin 4 and pin 5).

At the same time the oscillator by-pass capacitor (C 2) should be placed close to the SAW resonator and close to the device V_{CC} solder pad (pin 3).

A good compromise has been found for the demonstration board H5ACS01, figure 30. Please note that the layout allows to place SAW resonators with either SMD package (RFM style or Siemens style) or a standard pin through package (1-Port configuration). In the latter case the SAW is placed on the bottom side. The drill holes for the SAW resonator pins should be of an unplated type, in order to avoid a short to the SAW case during the soldering process.

Having routed the most critical areas the board layout should precede with the limiter feedback capacitor (C12) IF section and mixer input.

For reasons of a minimum receiver settling time, the limiter feedback capacitor (C 12) is connected to the supply rail instead of to the ground plane. It is recommended to employ short connections for the capacitor to IC solder pad (pin 12) as well as to the supply rail. A sufficient large by-pass capacitor for the supply rail (C 3) should be placed at the point where the limiter feedback capacitor connects to the supply rail. Improper by-passing or extreme long traces may results in a decreased sensitivity or an susceptibility to interfering signals by capacitive or inductive coupling.

A similar problem might be encountered for the IF filter, especially the Cauer filter. Since relatively large inductors are required (typically 330 uH) it is recommended to use magnetic shielded inductors. Please use inductors with a self resonant frequency (SRF) that exceeds 4 MHz. It is worth to note that the inductors should be placed rectangular to each other when the inductor core direction is not rectangular to the PCB surface, this minimizes cross coupling between the inductors itself. Furthermore the inductors should not be placed too close to each other, again in order to avoid cross coupling between the inductors itself. Otherwise the receiver IF response lacks stopp band attenuation.

The layout for the mixer input should employ a short wire from the mixer ground connection (pin 15) to the ground plane. The final mixer input routing depends on the antenna system to be used, either external or on board. It is worth to note that in any case the resonant loop formed by the matching components and the antenna should be as compact as possible since the loop AC current being approximately Q times higher than the AC feed current.

Finally we like to note that PCB layout at radio frequencies is always a difficult task and that we suggest to adopt as much as possible from the demonstration board layouts.

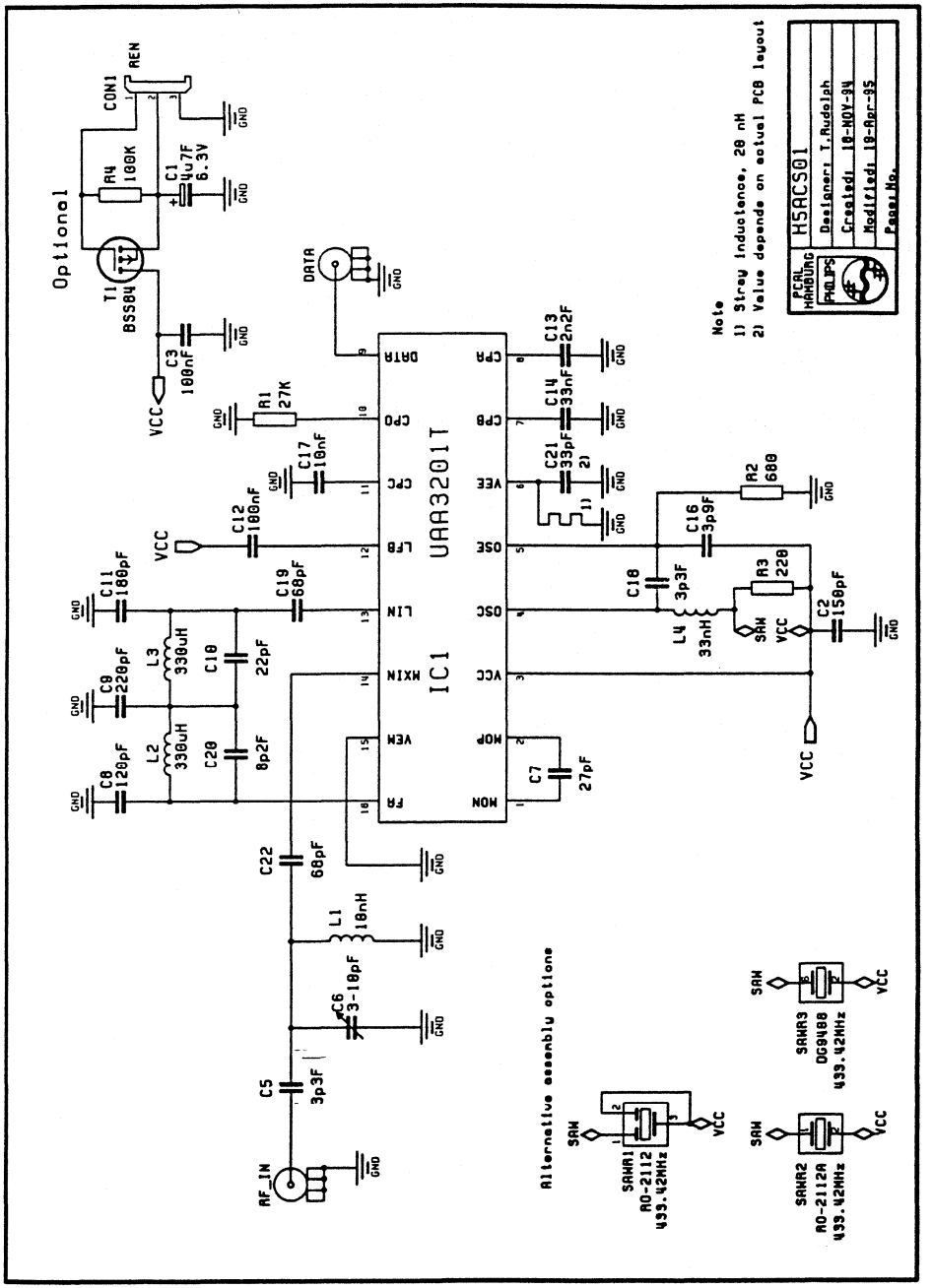


Fig.32 UAA 3201T application for 433,92 MHz and intermittent receiver operation

IDENTIFICATION PRODUCTS

Measurement and dimensioning of coils for an inductive coupled data carrier

Application report HACS/LR93 010

Contents

1 Model of datacarrier

1.1 Equivalent circuit diagram and external wiring of PIT

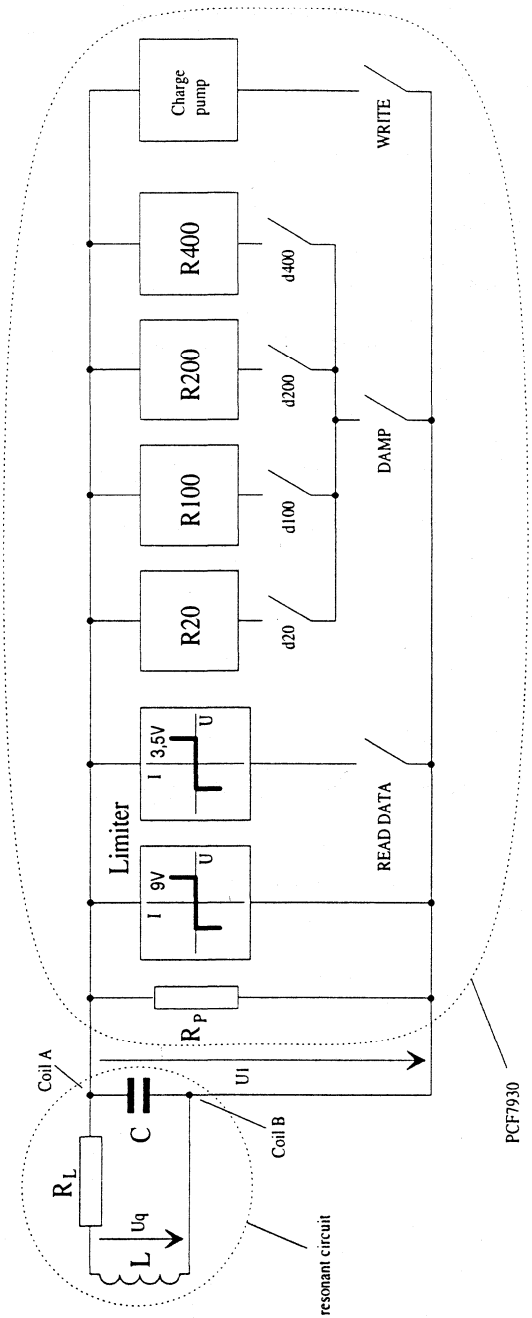


Fig. 1 Equivalent circuit diagram

Definitions concerning the equivalent circuit diagram and the external wiring of PIT

The following labelling is introduced for the components shown in Fig. 1 .

External parts:

L	inductance of coil
C	capacitance at resonance
R_L	resistance of the coil

Components of the TAG:

R_P	base-load resistance (active resistance), present also in READ_MODE
R20..R400	additional non-linear impedance during data transfer in PROGRAM_MODE
U_q	source voltage, induced by coil of basestation
U_I	input voltage of TAG
Limiter	voltage level limiter
READ DATA	data switch for load modulation in READ_MODE, switched by CDP-Signal
DAMP	damping switch, switched on during data transfer in PROGRAM_MODE
d20..d400	damping adjustment for PROGRAM_MODE, controlled by internal status register. Damping values are preset
WRITE	switch of the charge pump to generate the voltage for programming

1.2 Measurement of the components

The prototype IC was designed with testlogic and testpins, to allow the IC parameters to be measured. Hence it could be addressed with a special software. This is necessary to measure the characteristics of limiters and dampings. The different testmodes are transmitted in a defined transmission protocol. The connections to be measured are set high impedance by the testing schedule, that the voltage could fed into the corresponding input terminals externally. It seemed appropriate in this case to take a variable d.c. voltage. The testlogic will be removed from the IC before production. Two connections for the resonant circuit will remain at the PIT. Before this the status register is set with the desired damping value.
The measurement of the base-load is realized in a different way, see Chapter 1.2.3 .
The charge pump which is to produce the voltage for programming will be ignored in the following because it operates only when no data transmission.

For clarity the test set-up for plotting the limiter and damping characteristics shall be shown first:

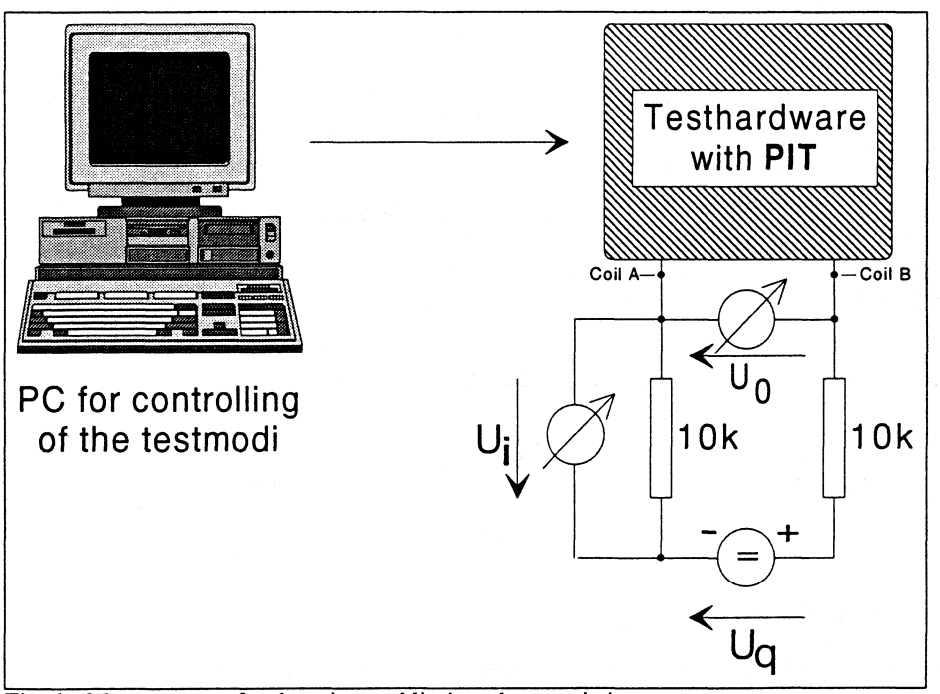


Fig. 2 Measurement for damping and limiter characteristics

1.2.1 Plot of the limiter characteristics

The limiters are responsible for current modulation. They limit the voltage on a low level and on a high level, so that in case of more power only the current increases. To get a clear modulation it is necessary that the current-voltage characteristic shape runs steep. If the data carrier dips into the field which is built up by the basestation the modulation begins, if sufficient energy is transmitted. The limiters are nearly frequency independent below 300 kHz so they were measured with d.c. voltage.
The following figure shows the shape of the limiter characteristics. The lower characteristic is not as steep as the upper one. That is a result of the circuit design.

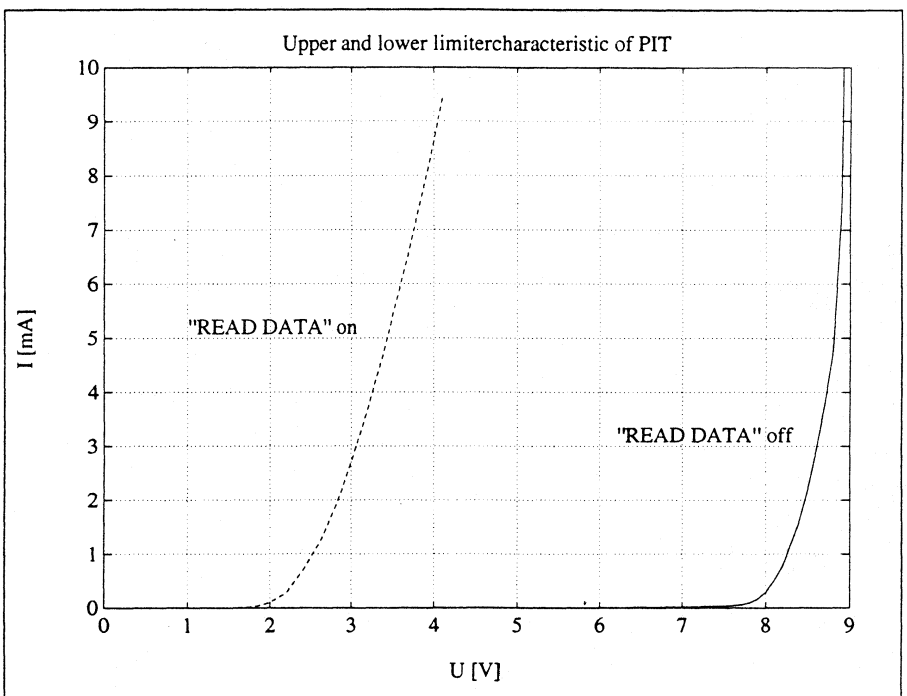


Fig. 3 Limiter characteristics

1.2.2 Plot of the damping characteristics

The damping characteristics determine the programming distances for the different tasks. These settings have no influence while reading the tag. Later on these non linear characteristics are used for optimizing the external circuit, because the non linear impedance of the PIT can be defined with these characteristics.
During the operation the dampings are determined by the internal status register.
With the testmode it is possible to set four different damping values. The characteristics of the damping values R20, R100, R200 and R400 were plotted. When the tag is programmed by the status register these values can be set independently. Only the positive

parts of the characteristics are displayed because the curves shapes are symmetrical about the origin. The dampings are nearly frequency independent up to 300 kHz, hence it is used a d.c. source for measurement here too.

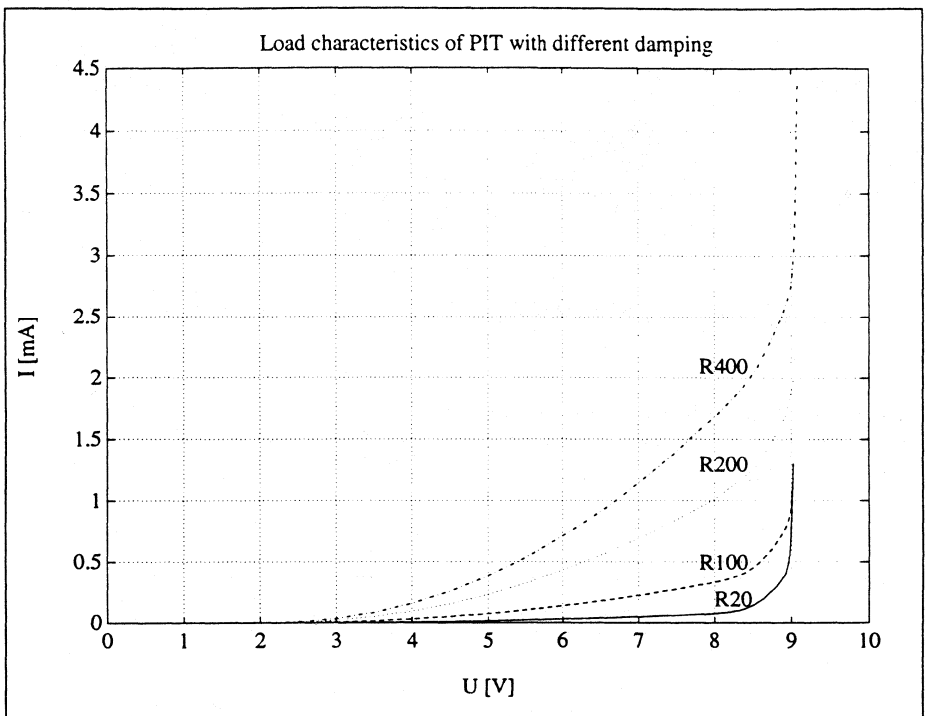


Fig. 4 Characteristics of the programmable damping values

1.2.3 Measurement without modulation

The base-load impedance appears before the modulation of the data carrier begins. For this measurement the test set-up isn't applied because the voltage level at the receiver coil is measured before modulation starts. It is important to use the transmission frequency for this measurement since this non linear base-load is dependent on frequency. To plot the characteristic the rms value of current and voltage is measured. With an oscilloscope it is checked that modulation has not started.

The test set-up to measure the base-load is realized in Fig. 5 :

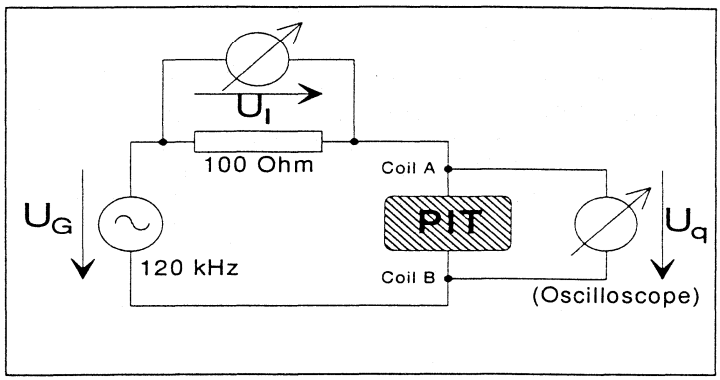


Fig. 5 Measurement of the base-load

The voltage-to-current characteristic of the base-load can be approximated with a quadratic function, shown in the next figure. This is due to the CMOS-technology applied in the IC. In Fig. 6 the measured values are smoothed using a 2nd order curve approximation.

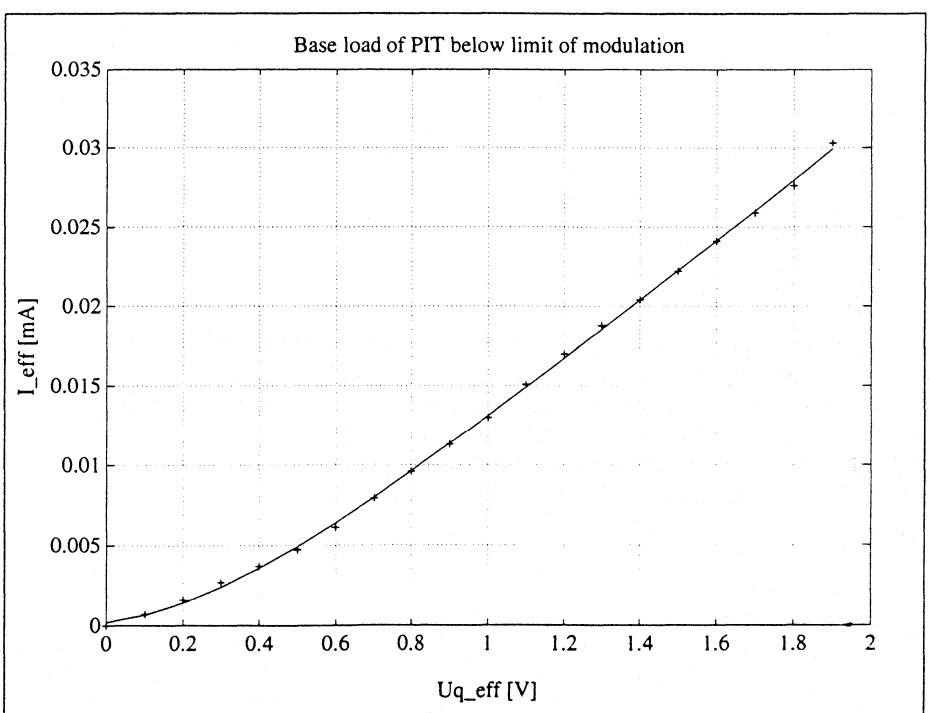


Fig. 6 Current characteristic without modulation

The dynamic impedance is calculated as a function of the voltage. The plot of non linear resistance R_P is generated by dividing voltage by current of the quadratic curve. The values are valid up to a voltage of ~ 1.9V since then the characteristics of the limiters dominate above this voltage. Fig. 7 shows the shape of the base-load characteristic.

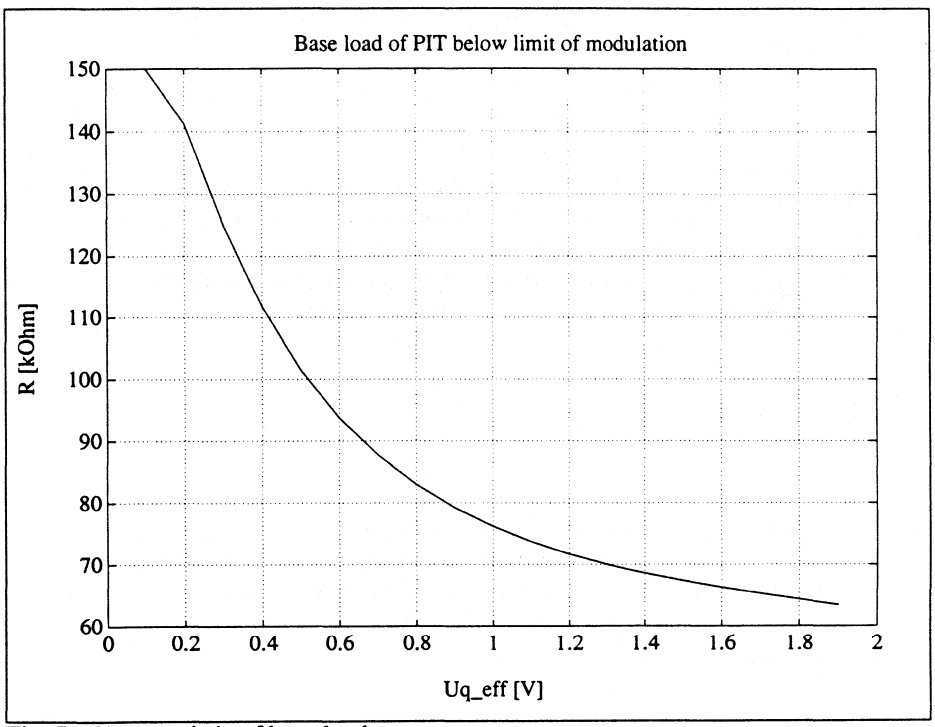


Fig. 7 Characteristic of base-load

2 Transient response

2.1 Equivalent voltage source as a model of the secondary circuit

The reactive effect of the tag on the base-station is neglected when they are isolated. Thus we get the model of the secondary circuit, with an equivalent voltage source set to the induced voltage, at the resonant circuit of the data carrier.
First of all the circuit is shown unloaded:

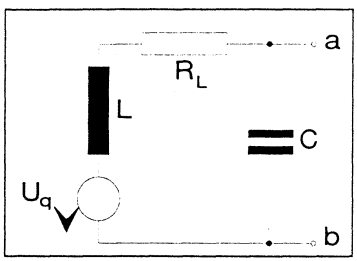


Fig. 8 Model of the secondary circuit

The connections a and b are the same as the connections COIL A and COIL B of the PIT which are the only external connections. U_q is the induced voltage. The resistor R represents the active resistance of the coil.

The model simplifies further if the resonant circuit is defined as internal resistance (here: Z_i). First a equivalent circuit diagram with a current source is built. This is used to create the equivalent circuit diagram with the voltage source and an internal resistance.

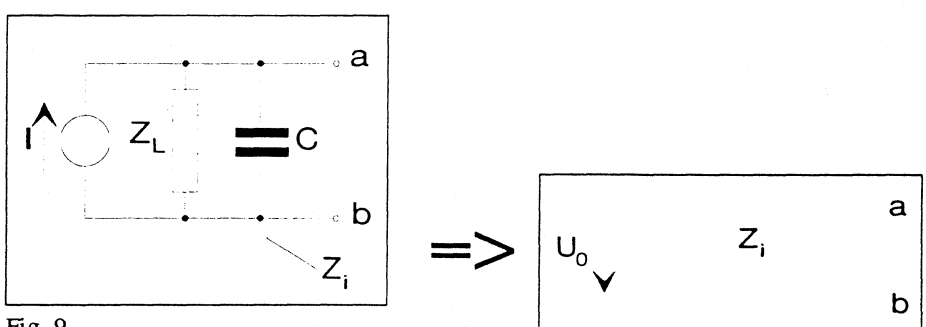


Fig. 9

In fig. 9 holds $Z_L = R_L + j\omega L$ and $I = U_q \cdot \frac{1}{R_L + j\omega L}$.

Hence it follows

$$Z_i = \frac{(R_L + j\omega L)\frac{1}{j\omega C}}{R_L + j\omega L + \frac{1}{j\omega C}} = \frac{R_L + j\omega L}{1 - \omega^2 LC + j\omega C R_L} \quad (1)$$

U_0 in fig. 10 :

$$U_0 = I \cdot Z_i = U_q \cdot \frac{1}{R_L + j\omega L} \cdot \frac{R_L + j\omega L}{1 - \omega^2 LC + j\omega C R_L}$$

=>

$$U_0 = U_q \cdot \frac{1}{R_L + j\omega L} \cdot Z_i \qquad (2)$$

From transformation of a series connection to a parallel connection and

$$Q = \frac{\omega_r L}{R} \qquad (3)$$

we get the

resonant impedance

$$R_r = \frac{R_L^2 + (\omega_r L)^2}{R_L} = R_L (1 + Q^2) \qquad (4)$$

in case of high Q factor (Q > 10):

$$\boxed{Z \approx R_L Q^2} \quad \text{or:} \quad \boxed{Z \approx \omega_r L \cdot Q} \qquad (5)$$

This must be the same value as Z_i in the equivalent circuit.

To get the resonant frequency, equation (1) must be taken and converted to ω_r, because $\omega_r = \omega$ when the argument of Z_i is zero.

Hence it follows the relation

$$\frac{R_L}{j\omega L} = \frac{1 - \omega^2 LC}{j\omega R_L C} \Rightarrow \omega^2 = \frac{1}{LC} - \frac{R_L^2}{L^2}$$

and with

$$\omega_0 = \sqrt{\frac{1}{LC}}, \qquad Z_0 = \sqrt{\frac{L}{C}}$$

=>

$$\boxed{\omega_r = \omega_0 \sqrt{1 - \frac{R_L^2}{Z_0^2}}}$$

with (2) , (4) there is a new relation for U_0:

$$U_0 = U_q \cdot \frac{1}{R_L + jR_L Q} \cdot R_L (1 + Q^2)$$

$$U_0 = U_q \cdot \frac{R_L (1 + jQ)(1 - jQ)}{R_L (1 + jQ)} = U_q \cdot (1 - jQ)$$

=>

$$\boxed{|U_0| \approx |U_q| \cdot Q} \qquad (6)$$

2.1.1 Comparison of calculation and measurement of an example

Now the calculation of Z_i shall be checked with an analogue measurement. The measurement is used for verifying the order of value of the internal resistance since

- the equivalent circuit represents only a model and
- in the following example the non linear resistance of the PIT is substituted by a fixed resistor

At an existing resonant circuit which is adequate for the application the following values are measured:

$$\omega_r L = 2262\ \Omega \qquad Q = 27.6$$

Thus a calculated value of $Z_i \approx 62.4\ k\Omega$ is generated.

According to (2) there is a voltage induced in this circuit that represents equivalent voltage $U_0 = 24.2\ V_{rms}$

Now the circuit is loaded with several fixed resistors which are at the order of value of the non linear PIT resistance. In Fig. 11 the "resistor" Z_i symbolizes the resonant circuit and the "voltage source" U_0 represents the by the circuit amplified induced voltage.

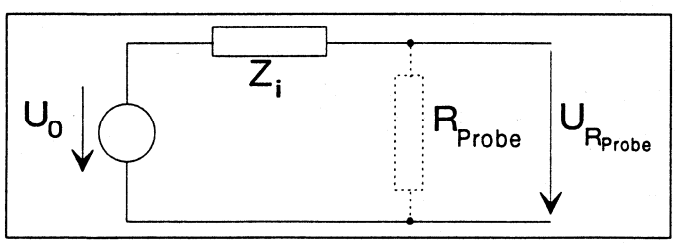


Fig. 11 Measurement of Z_i

The measurements of three fixed loads result the values in

R_{Probe}	U_{RProbe}	Z_i
10 kΩ	3.5 V	59.14 kΩ
20 kΩ	6.1 V	59.34 kΩ
100 kΩ	14.8 V	62.51 kΩ

Table 1 Measured values of Z_i

The values of Z_i are calculated with the formula $Z_i = R_{Probe}\left(\frac{U_0}{U_{R_{Probe}}} - 1\right)$.

The measured values are very close to the calculated value (62.4 kW) thus the chosen model is valid.

2.2 Parameters of transmission

2.2.1 Power transmission (dimensioning of the secondary coil)

To find out the maximum power transfer the voltage ratios are important. This is based on the calculations made in chapter 2.1 . The values of U_q and U_0 were introduced there. In this chapter the voltage value U_{q0} as a reference voltage shall be introduced, which is due to the induced source voltage U_q based on one turn. Now we get a function of the turns N. The relation of formula (6) is to be extended with:

$$U_q = N \cdot U_{q0}$$

$$\Rightarrow \quad \boxed{U_0 = U_{q0} \cdot N \cdot Q} \qquad (7)$$

The voltage at the PIT is defined as U_p. This voltage is now set in ratio to U_{q0}. It results the equation

$$\frac{U_p}{U_{q0}} = \frac{R_{PIT}}{R_{PIT} + Z_i} \cdot N \cdot Q \; . \qquad (8)$$

With (3) and (5) the following equation results:

$$\frac{U_p}{U_{q0}} = \frac{R_{PIT} \cdot N \cdot \dfrac{\omega_r L}{R_L}}{R_{PIT} + \dfrac{\omega_r^2 L^2}{R_L}} \qquad (9)$$

Maximum power transfer is achieved by maximizing the voltage ratio U_p/U_{q0}. The equation (9) shows a function of the three coil parameters R, L and N. These three parameters are functions of each other thus there must be further conditions made.
Now there shall be shown a practicable calculation based on optimizing the number of turns N. The basis is a flat coil with a given diameter. To calculate the values of R(N) and L(N) the geometry of bobbin was preset.

The calculation for a **constant bobbin** shall be illustrated.

Here are the geometrical dimensions of the bobbin given. This is often the done thing in practice. Because of the constant external dimensions it's important to notice that the diameter of wire varies. Thus the number of turns N doesn't vary linearly but quadratically with the resistance of the coil.

First of all some new variables are introduced:

d_m	average diameter of the coil
d_0	diameter of the wire
h	height of the coil
x	length of filling area
A	filling area
k	space factor
k	specific conductance of the wire

Fig. 12 helps to clarify the calculation.

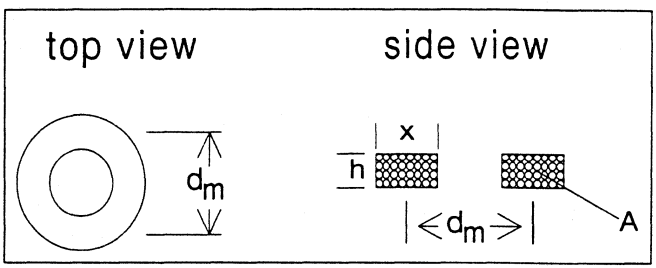


Fig. 12 Dimensions of a flat coil

This data is used to find formulas for L and R_L.
Taking the geometrical dimensions:

$$R_L = \frac{4 \cdot l}{\pi \kappa d_0^2}$$

With $l = N \cdot d_m \cdot \pi$ and $N = \frac{4Ak}{\pi d_0}$

results $$R_L = \frac{N^2 \pi d_m}{\kappa k A}$$

Here the quadratic function $R = f(N^2)$

With $R_L = R_{L0} N^2$ follows $$\boxed{R_{L0} = \frac{\pi d_m}{\kappa k x h}}$$

To calculate the inductance there is the following relation: With flat coils ($h > d_m$) the equation

$$\frac{L}{nH} = \frac{78N^2 \cdot (d_m/cm)^2}{3d_m/cm + 9h/cm + 10x/cm}$$

After conversion to SI units follows:

$$L = \frac{78N^2 \cdot d_m^2}{3d_m + 9h + 10x} \cdot 10^{-7} \cdot \frac{H}{m}.$$

With $L = L_0 N^2$ follows

$$\boxed{L_0 = \frac{78 \cdot d_m^2}{3d_m + 9h + 10x} \cdot 10^{-7} \cdot \frac{H}{m}}$$

Like with the first method equation (8) is basis for the following calculation.

With $L = N^2 L_0$ and $R_L = N^2 R_{L0}$ arises from formula (9):

$$\frac{U_p}{U_{q0}}(N) = \frac{R_{PIT} \cdot N \cdot \dfrac{N^2 \omega_r L_0}{N^2 R_{L0}}}{R_{PIT} + \dfrac{N^4 \omega_r^2 L_0^2}{N^2 R_{L0}}} \qquad (10)$$

and thus

$$\frac{U_p}{U_{q0}}(N) = \frac{N \cdot \dfrac{\omega_r L_0}{R_{L0}}}{1 + N^2 \dfrac{\omega_r^2 L_0^2}{R_{PIT} R_{L0}}} \qquad (11)$$

To get the optimum number of turns of the coil, the peak of this function has to be determined. This is realized again by setting the first derivative of the voltage ratio with respect to turns to zero.

$$\frac{\partial \dfrac{U_p}{U_{q0}}}{\partial N} = 0$$

With

$$\alpha = \frac{\omega_r^2 L_0^2}{R_{L0} R_{PIT}} \quad \text{and} \quad \beta = \frac{\omega_r L_0}{R_{L0}}$$

results

$$\frac{U_p}{U_{q0}} = \frac{\beta N}{1 + \alpha N^2}.$$

Hence it follows

$$\frac{\partial \dfrac{U_p}{U_{q0}}}{\partial N} = \frac{\beta(1 + \alpha N^2) - 2\alpha\beta N^2}{(1 + \alpha N^2)^2} = 0$$

This gives the following relation to get the optimum turns N_{opt} :

$$N_{opt} = \sqrt{\frac{1}{\alpha}} \qquad \boxed{N_{opt} = \sqrt{\frac{R_{L0}R_{PIT}}{\omega_r^2 L_0^2}}} \qquad (12)$$

With the parameter of a sample coil

d_m = 26 mm **x = 2 mm** **h = 1.5 mm** **k = 0.5** **k = 56 m/Wmm^2**

it results **L_0 = 47.3 nH** and **R_{L0} = 972.4 mW.**

According to Fig. 7 the value of R_{PIT} was assumed to 60 kW. The transmission frequency is 125 kHz.

Thus the optimum number of turns must be with this coil dimensions **N_{opt} = 205 turns**

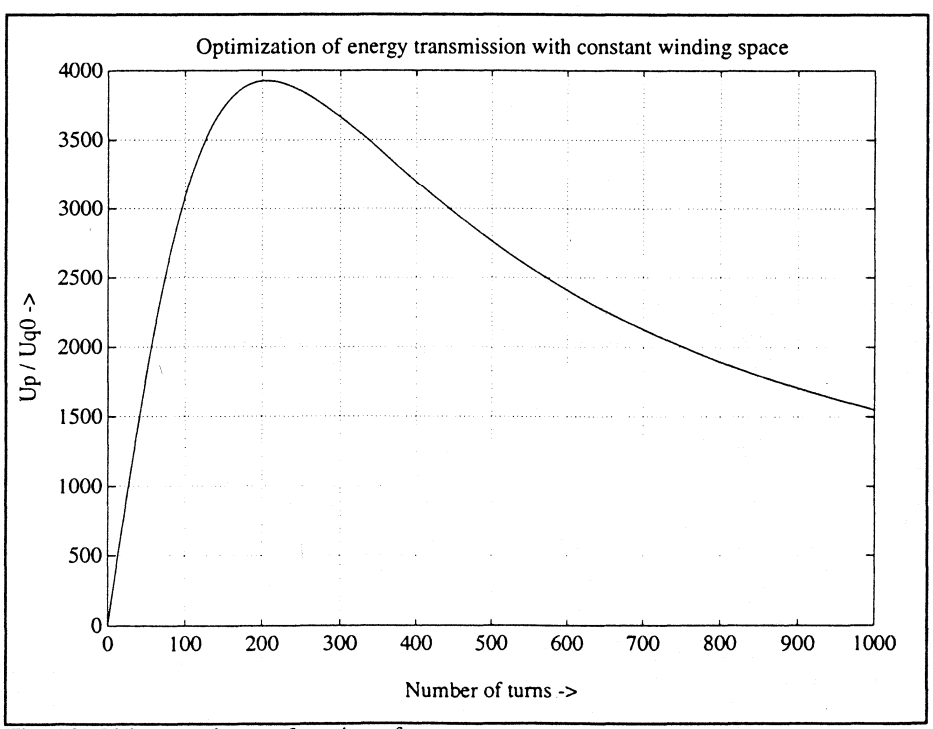


Fig. 13 Voltage ratio as a function of turns

The figure shows a very distinctive range to find the optimum number of turns. This effects only on the secondary coil.

2.2.2 Dimensioning of the primary coil

In this chapter shall be shown different resonant circuits as the base station antenna in reference to the ampere turns.

It shall be compared a series resonant circuit, a series-parallel resonant circuit and a series-parallel resonant circuit with a tap.
The aim is to reach the maximum ampere turns Q with maximum available voltage U_0 and current I_0 delivered by the base station amplifier.

a) Series resonance

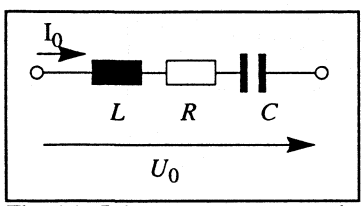


Fig. 14 Primary antenna as series circuit

$$\Theta = N \cdot I_L = N \cdot I_0$$

at resonance there is $$I_0 = \frac{U_0}{R}$$

with $$R = \frac{\omega_r L}{Q}$$

because Q can be determined since the bandwidth $$b_\omega = \frac{\omega_0}{Q}$$ is given.

Hence it follows $$I_0 = \frac{U_0 Q}{\omega_r L}$$

and thus $$L = \frac{U_0}{I_0} \cdot \frac{Q}{\omega_r}$$

Assuming again $L = N^2 L_0$, after a short conversion follows

$$N^2 = \frac{U_0}{I_0} \cdot \frac{Q}{\omega_r L_0}$$

This leads to $$\boxed{N = \sqrt{\frac{U_0}{I_0} \cdot \frac{Q}{\omega_r L_0}}}$$ and $$\Theta = \sqrt{U_0 \cdot I_0 \cdot \frac{Q}{\omega_r L_0}}\,.$$

Example:
with the given or generated values
L_0 = 0.1 mH, Q = 30, w = 2p125 kHz, U_0 = 2.5 V, I_0 = 100 mA

the results are N = 98 turns and Q = 9.77 ampere turns.

With the values from the example the number of turns for different output voltage current ratios can be found out:

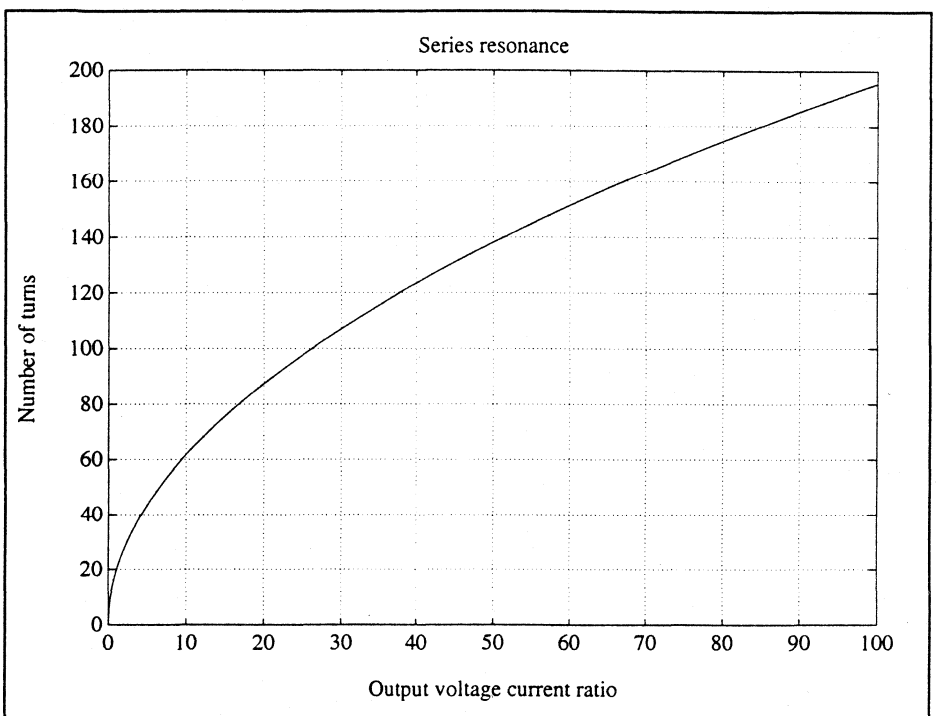


Fig. 15 Number of turns as a function of the output voltage to current ratio [U_0 / I_0]

b) Series-parallel resonance

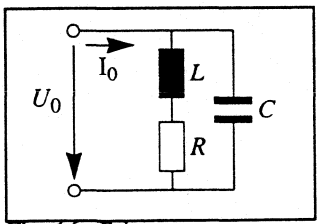


Fig. 16 Primary antenna as a series-parallel circuit

The following approximations are to be assumed during this calculation:

For high Q factor, $\omega_r \approx \omega_0$ and the resonant impedance $Z_r \approx Q\omega_r L$

$$\Theta = N \cdot I_L$$

With $I_L = Q \cdot I_0$ and $Q = \dfrac{\omega_r L}{R}$

$$\Theta = I_0 \cdot Q \cdot N.$$

$$I_0 = \frac{U_0}{Q\omega_r L}$$

and thus $$L = \frac{U_0}{I_0} \cdot \frac{1}{Q\omega_r}$$

Assuming again $L = N^2 L_0$, after a short conversion

$$N^2 = \frac{U_0}{I_0} \cdot \frac{1}{Q\omega_r L_0}$$

This leads to $$\boxed{N = \sqrt{\frac{U_0}{I_0} \cdot \frac{1}{Q\omega_r L_0}}}$$ and $$\Theta = \sqrt{U_0 \cdot I_0 \cdot \frac{Q}{\omega_r L_0}}.$$

Example:
with the given or generated values
L_0 = 0.1 mH, Q = 30, w = 2p125 kHz, U_0 = 2.5 V, I_0 = 100 mA

the results are N = 3 turns and Q = 9.77 ampere turns.

With the values from the example the number of turns for different maximum output voltage current ratios can be found out:

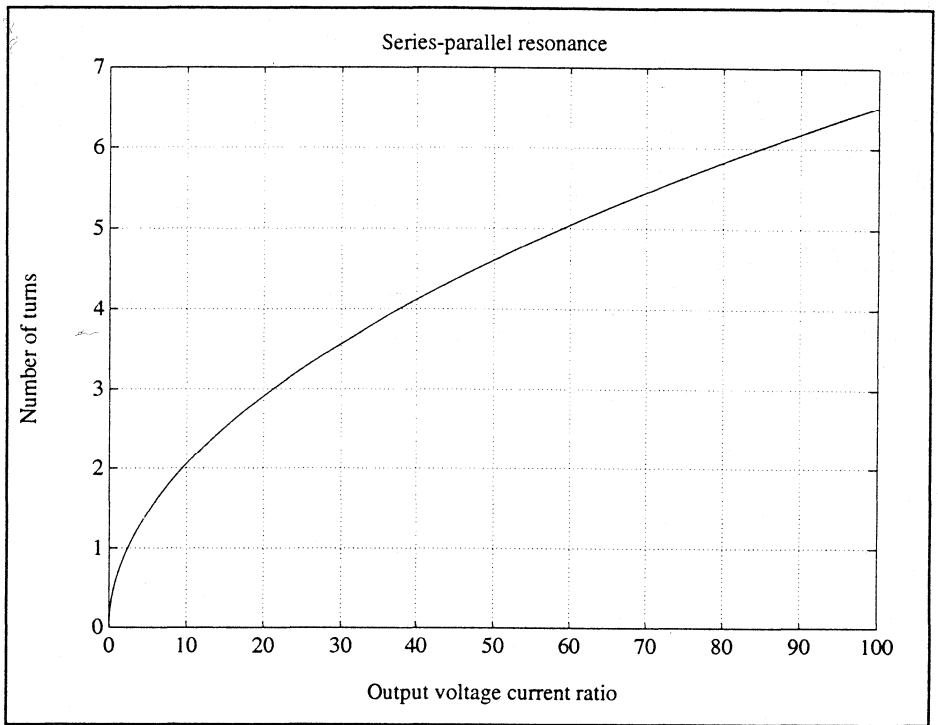


Fig. 17 Number of turns as a function of the output voltage to current ratio [U_0 / I_0]

c) Series-parallel resonant circuit with a tap.

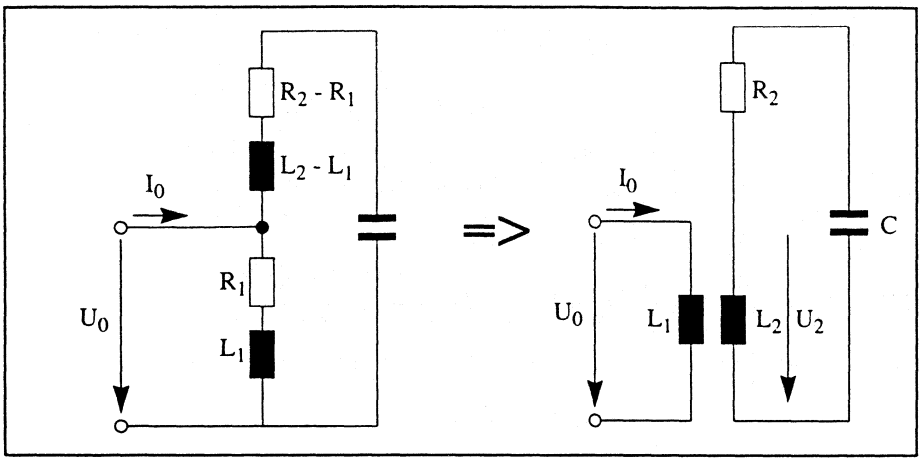


Fig. 18 Conversion of the circuit for calculating with the tap

Also in this chapter the approximations $\omega_r \approx \omega_0$ and $Z_r \approx Q\omega_r L$ are made for high Q.

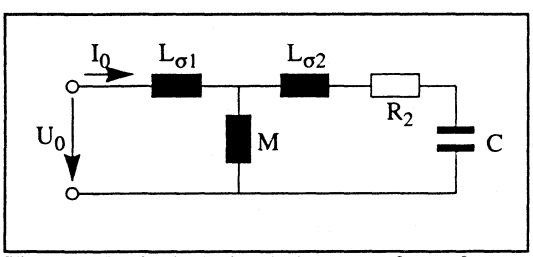


Fig. 19 Equivalent circuit diagram of transformer

There is

L_2 = Inductance of all windings
L_1 = Inductance of the tap winding
R_2 = Resistance of all windings
N_2 = Turns of all windings
N_1 = Turns of the tap winding

$$C = \frac{1}{\omega_r^2 L} \quad \text{(tuned to resonance)} \qquad (13)$$

(14)

leakage inductance 1 $$L_{\sigma 1} = L_1 - M \qquad (15)$$

leakage inductance 2 $$L_{\sigma 2} = L_2 - M \qquad (16)$$

mutual inductance $$M = k\sqrt{L_1 L_2}$$

with k = 1 (unity coupling)

response ratio $$a = \frac{N_1}{N_2} = \sqrt{\frac{L_1}{L_2}}$$

Thus $$\frac{U_0}{I_0} = j\omega_r L_{\sigma 1} + \frac{j\omega_r M\left(j\omega_r L_{\sigma 2} + R_2 + \frac{1}{j\omega_r C}\right)}{j\omega_r M + j\omega_r L_{\sigma 2} + R_2 + \frac{1}{j\omega_r C}}$$

with (13) , (15) , (16) $$\frac{U_0}{I_0} = j\omega_r L_1 - j\omega_r M + \frac{j\omega_r M\,(R_2 - j\omega_r M)}{R_2}$$

=> $$\frac{U_0}{I_0} = j\omega_r L_1 + \frac{\omega_r^2 L_1 L_2}{R_2}$$

with $$Q_2 = \frac{\omega_r L_2}{R_2}$$

follows $$\frac{U_0}{I_0} = \omega_r L_1\,(j - Q_2)$$

With the approximation $|Q_2| \gg |j|$ for high Q there is

$$L_1 = \left|\frac{U_0}{I_0} \cdot \frac{1}{\omega_r Q_2}\right|$$

Assuming $L_1 = N_1^2 L_0$ the correlation between N_1 and U_0/I_0 is now:

$$\boxed{|N_1| = \sqrt{\left|\frac{U_0}{I_0} \cdot \frac{1}{Q\omega_r L_0}\right|}}$$

Compared to the result from the parallel circuit the number of turns after that the tap must be the same number of turns in the parallel circuit.

In this case the ampere turns are defined by $\Theta = N_2 I_2 - N_1 I_0$ (17)

To get I_2 :

$$\frac{I_2}{I_0} = \frac{\frac{1}{R_2 - j\omega_r M}}{\frac{1}{R_2 - j\omega_r M} + \frac{1}{j\omega_r M}} = \frac{j\omega_r M}{R_2}$$

Hence it follows $$I_2 = I_0 \cdot \frac{j\omega_r L_2}{R_2} \sqrt{\frac{L_1}{L_2}} = I_0 \cdot jQ_2 a$$

with $$N_2 = \frac{N_1}{a}$$

equation (17) delivers $$\Theta = I_0 N_1 (jQ_2 - 1)$$

Approximating a high Q factor the ampere turns can be expressed by

$$|\Theta| = |I_0 N_1 Q_2| = \sqrt{\left| U_0 I_0 \frac{Q_2}{\omega_r L_0} \right|}$$

Again there is the same result with the ampere turns.This means that the three shown circuits have the same ampere turns and they can be compared.

Example:
with the given or generated values
L_0 = 0.1 mH, Q = 30, w = 2p125 kHz, U_0 = 2.5 V, I_0 = 100 mA

the results are N_1 = 3 turns and Q = 9.77 ampere turns.

The number of turns of the whole coil depends on the given Q factor and the parameters of the chosen wire. First the inductance L_2 must be calculated, then the number of turns can be found out with the empirical value L_0.

To set the three methods in comparison there are:

	series resonance	**series-parallel resonance**	**series-parallel resonance with a tap**
L	955 µH	1.06 µH	*
C	1.7 nF	1.53 µF	depends on L
N	98 turns	3 turns	N_1 = 3 turns
Θ	97.7 A turns	97.7 A turns	97.7 A turns

Table 2 Comparison of the three methods

* To get the same voltage characteristic as the series resonance circuit, L has to be set to 955 mH. According to L, N has to be set to 98 turns. This results in a turns ratio of $a = N_1 / N_2 = 0.03$.

Thus it is possible to adapt the antenna to the basestation with the desired response characteristics.

The right inductance can be found out because there can be build a standardized inductance. This is defined by

$$L_{Norm} = \frac{L}{Q} \qquad \text{for series circuits}$$

$$L_{Norm} = L \cdot Q \qquad \text{for series-parallel circuits (= } L_1 \text{ with tap)}$$

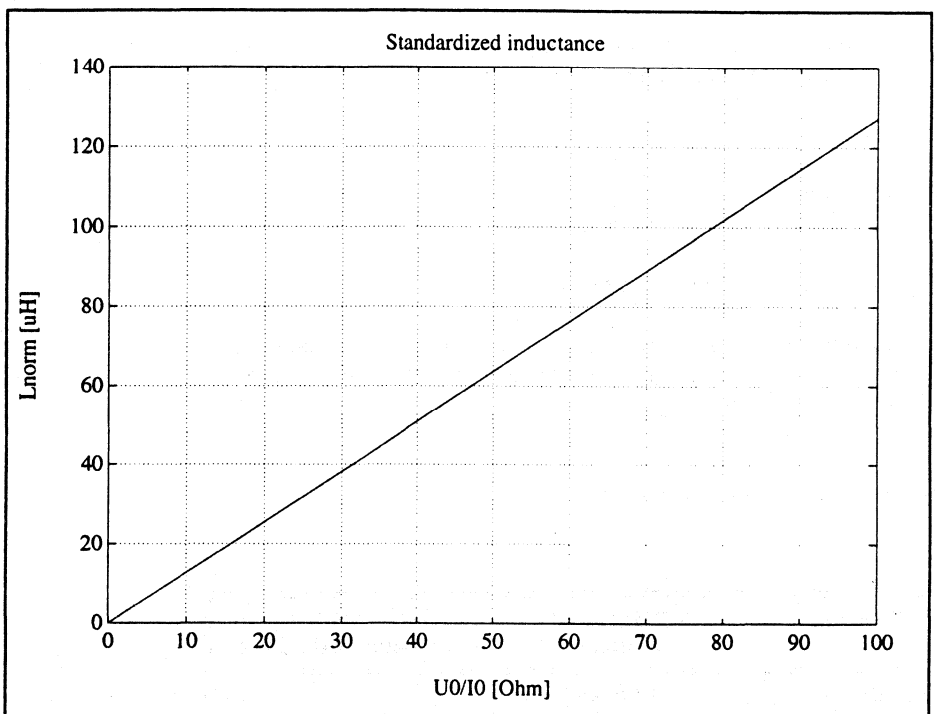


Fig. 20 Standardised inductance for all circuits

2.2.3 Programming data

For data programming the transient time is crucial. To get a clear signal with a greater distance, the transmitted data must be recognized in a short time.
First shall be shown a part of a voltage characteristic to see the problem(Fig. 21). The voltage shape was simulated with values from Chapter 2.1.1 and with the values from PIT for damping = 100, taken from Fig. 4 .
After each 50 ms the voltage is switched over. The voltage cut-off at 9 V is due to the upper limiter.
The appertaining circuit is shown in Fig. 22 .

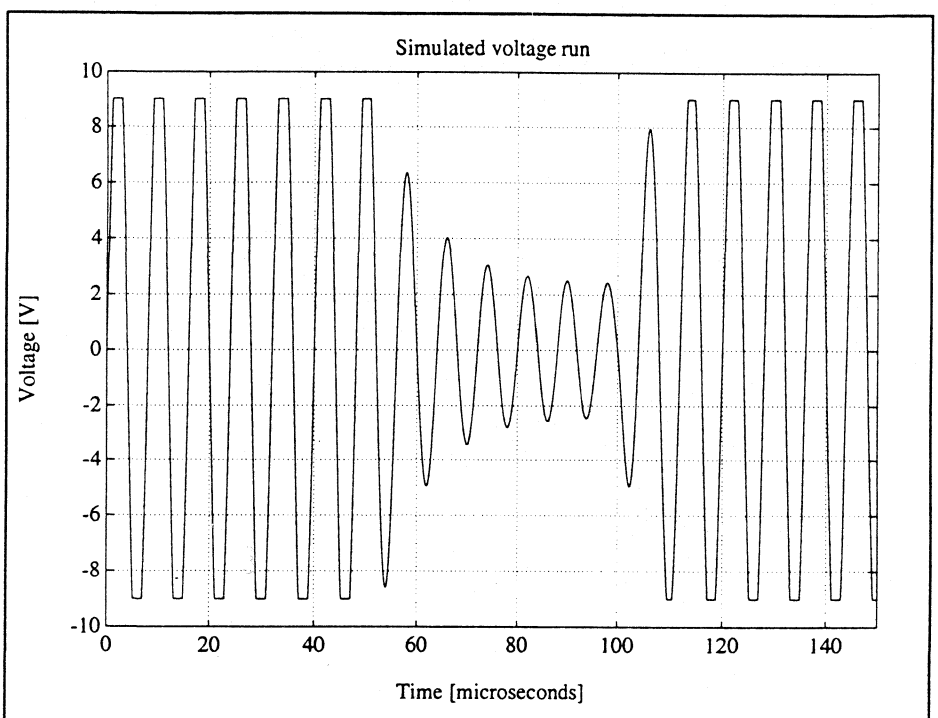


Fig. 21 Simulated transient voltage characteristic

Now it is to be referred again to the equivalent circuit in Fig. 8 . It is extended with the load that symbolizes the PIT. That load is determined with the non linear characteristic shown in Fig. 4. In the following figure the load is denoted with R_{PIT}.

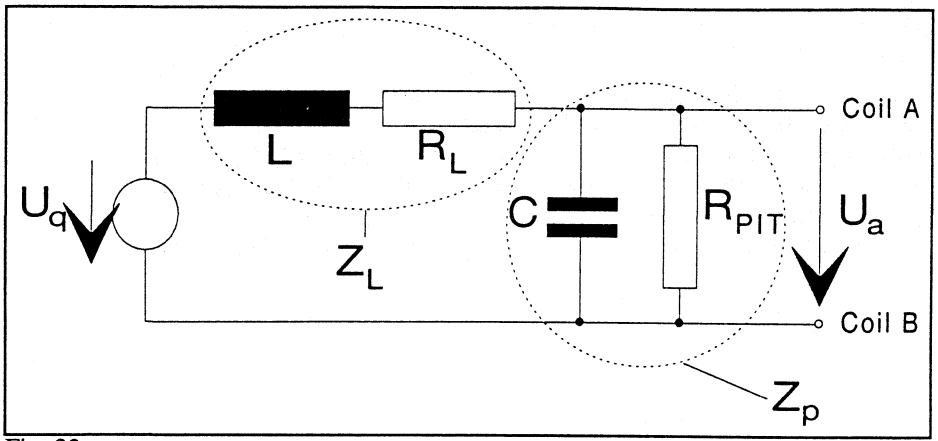


Fig. 22

To determine the transient time:

$$G(s) = \frac{U_a(s)}{U_q(s)} = \frac{Z_L}{Z_L + Z_p} = \frac{1}{R_L Cs + \frac{R_L}{R_{PIT}} + LCs^2 + \frac{Ls}{R_{PIT}} + 1}$$

$$= \frac{1}{1 + \frac{R_L}{R_{PIT}}} \cdot \frac{1}{1 + \frac{R_{PIT}R_L C + L}{R_{PIT} + R_L}s + \frac{R_{PIT}LC}{R_{PIT} + R_L}s^2}$$

The standard transfer function is defined by

$$G(s) = k \cdot \frac{1}{1 + 2\frac{\delta}{\omega_0^2}s + \frac{1}{\omega_0^2}s^2}$$

The comparison of the coefficients delivers

$$\frac{1}{\omega_0^2} = \frac{R_{PIT}LC}{R_{PIT} + R_L} \Rightarrow \omega_0^2 = \frac{R_{PIT} + R_L}{R_{PIT}LC}$$

$$\frac{2\delta}{\omega_0^2} = \frac{R_{PIT}R_L C + L}{R_{PIT} + R_L} \Rightarrow 2\delta = \frac{R_{PIT}R_L C + L}{R_{PIT}LC}$$

with $\tau = \frac{1}{\delta}$ and $T_0 = \frac{1}{\omega}$

follows the Transient period

$$\tau = T_0 \cdot \frac{1}{\pi\left(\frac{1}{Q} + \frac{\omega_r L}{R_{PIT}}\right)} \qquad (18)$$

To have a short transient period t should be very small. It is useful to set up the ratio t/T_0. Assuming a constant winding space Q remains constant. Q should be set to a quite high value, e.g. 30. The difficulty with the function is the non linearity of R_{PIT}. For calculating the function, constant voltage is taken (operating point). The value of this voltage is set to the average level of the "recognized" voltage in this case 7 to 9 V, see Fig. 4 .This is considered in the following figure.
Now it's possible to build a function $t/T_0 = f(L)$.

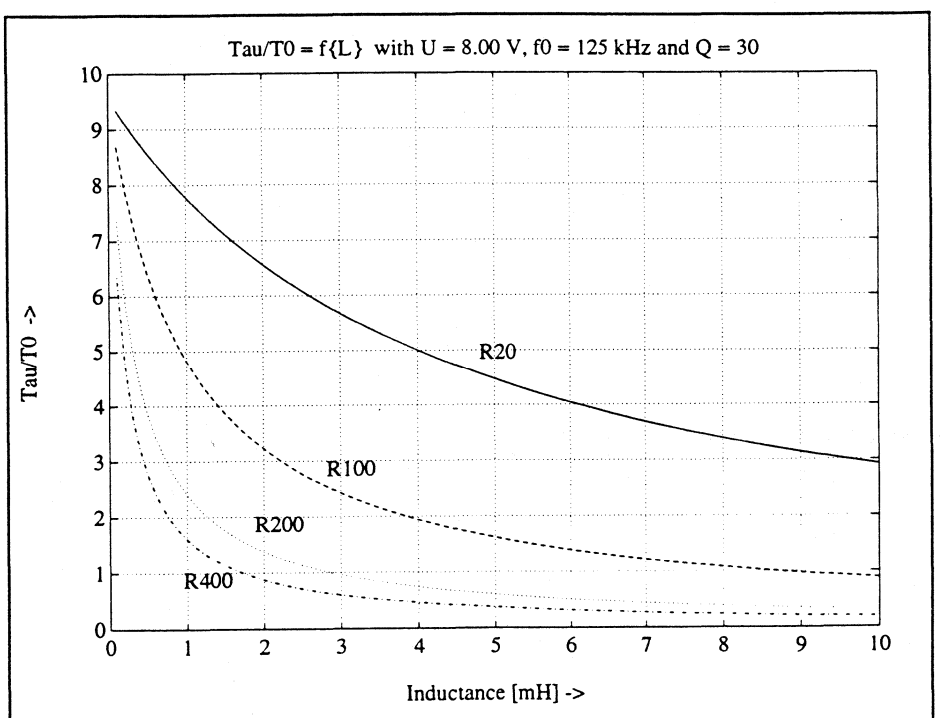


Fig. 23 Oscillation time ratio as a function of the inductance

With this method it is possible to check the data programming possibilities.This calculations should be used just for verification, because the power transmission is much more important.

Assuming $L \sim N^2$ with an empirical proportional control factor the oscillation time ratio as a function of N can be found out.

Basic Equations for oscillator circuits

1.) Non-dissipative oscillator circuits

Radian frequency $\omega_0 = \frac{1}{\sqrt{LC}}$

Impedance $Z_0 = \sqrt{\frac{L}{C}}$

Admittance $Y_0 = \sqrt{\frac{C}{L}}$

Relative frequency $\Omega = \frac{\omega}{\omega_0}$

Frequency increment $v = \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} = \Omega - \frac{1}{\Omega}$

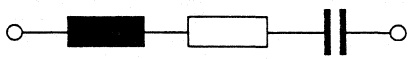
Approximation for small frequency increments: $v_n = 2\left(\frac{\omega}{\omega_0} - 1\right)$

Parallel-resonant circuit: Susceptance $B = Y_0 v$

Series-resonant circuit: Reactance $X = Z_0 v$

2.) Dissipative oscillator circuits

a) **Series-resonant circuit**



Impedance $$Z = R + j\left(\omega L - \frac{1}{\omega C}\right)$$

in case of resonance: $$Z = R$$

Q factor $$Q = \frac{\omega_r L}{R} = \frac{1}{\omega_r C R} = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{Z_0}{R}$$

Damping $$d = \frac{1}{Q}$$

Voltage resonance step-up at capacitor $$\omega_{s1} = \omega_0\sqrt{1 - \frac{1}{2Q^2}}$$

in case of high Q factor (Q > 10): $$\omega_{s1} \approx \omega_0\left(1 - \frac{1}{4Q^2}\right)$$

Voltage resonance step-up at coil $$\omega_{s2} = \omega_0\frac{1}{\sqrt{1 - 1/(2Q^2)}}$$

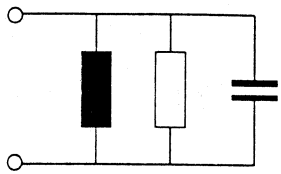
in case of high Q factor (Q > 10): $$\omega_{s2} \approx \omega_0\left(1 + \frac{1}{4Q^2}\right)$$

Value of resonance step-up $$\left(\frac{U_C}{U}\right)_{\omega_{s1}} = \left(\frac{U_L}{U}\right)_{\omega_{s2}} = \frac{Q}{\sqrt{1 - 1/(4Q^2)}}$$

Voltage ratio at resonance $$\left(\frac{U_C}{U}\right)_{\omega_0} = \left(\frac{U_L}{U}\right)_{\omega_0} = Q$$

Frequency rise $$q = \frac{U_R}{U} = \frac{d\Omega}{\sqrt{(1 - \Omega^2)^2 + (d\Omega)^2}}$$

b) **Parallel-resonant circuit**



Admittance $$Y = G + j\left(\omega L - \frac{1}{\omega L}\right)$$

in case of resonance: $Z = R$

Q factor $$Q = \frac{\omega_r C}{G} = \frac{1}{\omega_r L G} = \frac{1}{G}\sqrt{\frac{C}{L}} = \frac{Y_0}{G}$$

Damping $$d = \frac{1}{Q}$$

Current resonance step-up through coil $$\omega_{s1} = \omega_0\sqrt{1 - \frac{1}{2Q^2}}$$

in case of high Q factor (Q > 10): $$\omega_{s1} \approx \omega_0\left(1 - \frac{1}{4Q^2}\right)$$

Current resonance step-up through capacitor $$\omega_{s2} = \omega_0\frac{1}{\sqrt{1 - 1/(2Q^2)}}$$

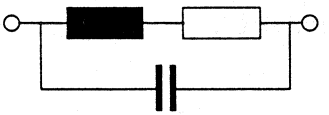
in case of high Q factor (Q > 10): $$\omega_{s2} \approx \omega_0\left(1 + \frac{1}{4Q^2}\right)$$

Value of resonance step-up $$\left(\frac{I_L}{I}\right)_{\omega_{s1}} = \left(\frac{I_C}{I}\right)_{\omega_{s2}} = \frac{Q}{\sqrt{1 - 1/(4Q^2)}}$$

Voltage ratio at resonance $$\left(\frac{I_L}{I}\right)_{\omega_0} = \left(\frac{I_C}{I}\right)_{\omega_0} = Q$$

Frequency rise $$q = \frac{I_G}{I} = \frac{d\Omega}{\sqrt{(1 - \Omega^2)^2 + (d\Omega)^2}}$$

c) **Parallel-series resonant circuit**



Resonant radian frequency $\omega_r = \omega_0 \sqrt{1 - \left(\frac{R}{Z_0}\right)^2}$

Impedance $Z = \frac{R + j\omega L}{1 + j\omega RC - \omega^2 LC}$

Resonant admittance $G_r = \frac{R}{R^2 + (\omega_r L)^2}$

Resonant impedance $R_r = \frac{R^2 + (\omega_r L)^2}{R} = R(1 + Q^2)$

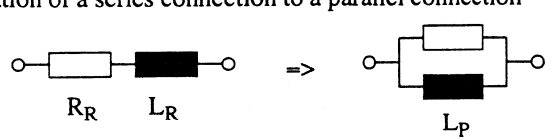
in case of high Q factor (Q > 10): $Z \approx RQ^2$

Q factor $Q = \frac{\omega_r L}{R} = \frac{\omega_r C (R^2 + (\omega_r L)^2)}{R}$

(with $\omega_r C = \frac{\omega_r L}{R^2 + (\omega_r L)^2}$)

$$\Rightarrow Z = \omega_r L \cdot Q$$

Transformation of a series connection to a parallel connection



$$R_P = \frac{R_R^2 + (\omega L_R)^2}{R_R} \qquad \omega L_P = \frac{R_R^2 + (\omega L_R)^2}{\omega L_R}$$

3.) Further Parameters of resonant circuits

Damping $$d = \frac{1}{Q}$$

Damping ratio $$\vartheta = \frac{d}{2} = \frac{1}{2Q}$$

High and low frequency cutoff ω_1 and ω_2 at phase angle of ±45°

$$\left(\frac{U}{U_{max}}\right)_{\omega_{1,2}} = \left(\frac{I}{I_{max}}\right)_{\omega_{1,2}} = \frac{1}{\sqrt{2}} \approx -3dB$$

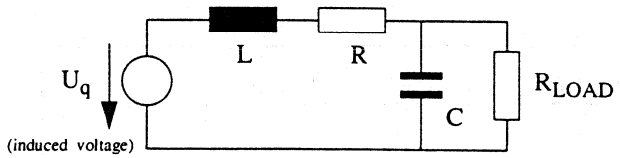
Frequency increment at these frequencies: $$v_{1,2} = \left(\frac{\omega_{1,2}}{\omega_0}\right) - \left(\frac{\omega_0}{\omega_{1,2}}\right) = \pm\frac{1}{Q}$$

$$\omega_{1,2} = \pm\vartheta + \sqrt{1+\vartheta^2}$$

Bandwidth $$b_\omega = |\omega_2 - \omega_1| = \frac{\omega_0}{Q} = d\omega_0 = 2\vartheta\omega_0$$

$$\omega_1 \cdot \omega_2 = \omega_0^2$$

4.) Systemconstants at loaded resonant circuit



Transfer Function $$G(s) = \frac{1}{1+\frac{R}{R_{LOAD}}} \cdot \frac{1}{1+\frac{R_{LOAD}RC+L}{R_{LOAD}+R}s+\frac{R_{LOAD}LC}{R_{LOAD}+R}s^2}$$

with $$G(s) = \frac{K_P}{1+\frac{2\vartheta}{\omega_0}s+\frac{1}{\omega_0^2}s^2} = \frac{K_P}{1+\frac{2\delta}{\omega_0^2}s+\frac{1}{\omega_0^2}s^2}$$

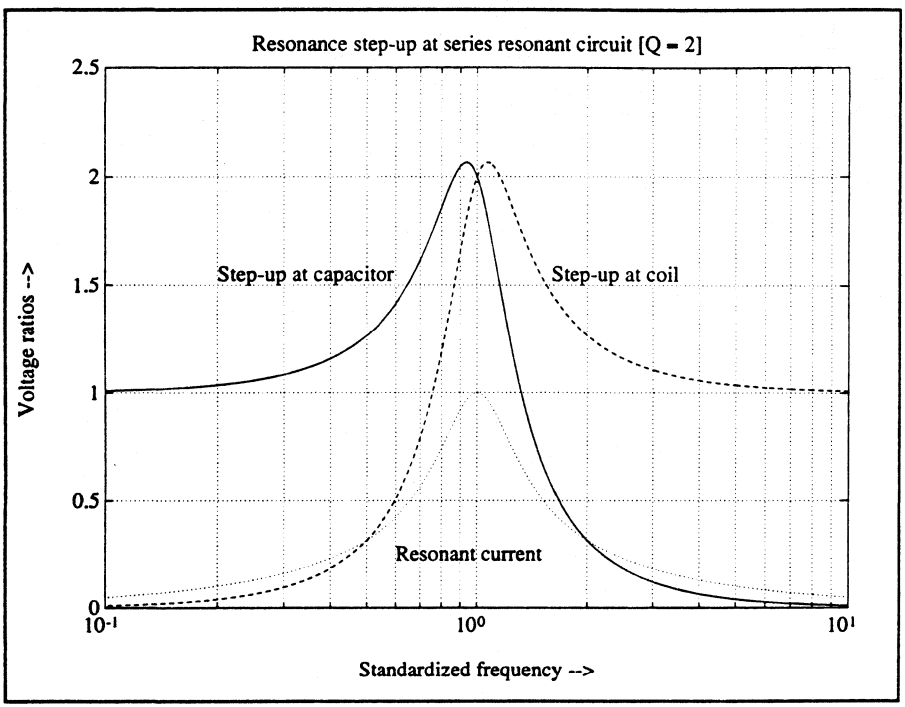
$$\Rightarrow \delta = \frac{R_{LOAD}RC+L}{2R_{LOAD}LC}$$

$$\Rightarrow \vartheta = \frac{\delta}{\omega_0} = \frac{R_{LOAD}RC+L}{2\sqrt{R_{LOAD}LC \cdot (R_{LOAD}+R)}}$$

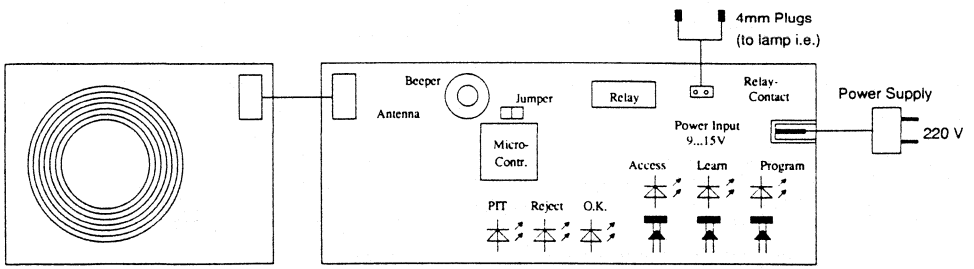
with $\tau = \frac{1}{\delta}$ and $T_0 = \frac{1}{f_0}$

Transient period $$\tau = T_0 \cdot \frac{1}{\pi\left(\frac{1}{Q}+\frac{\omega_r L}{R_{LOAD}}\right)}$$

Example for resonant step-up voltage ratio runs:



Exhibition Model PIT ACCESS SYSTEM



Antenna-Board PIT Access-Board

The Exhibition Model consists of the following parts:

1. PIT Access Board
2. Antenna-Board inclusive cable to connect with the PIT Access Board
3. Cable for the relay contact
4. 7 Access-PIT (PCF7930) with Pseodo Random Numbers
5. 3 Master-Key PIT (Access-, Learn- and Program Mode)
6. Power Supply (220V Main Voltage)
7. Description of the PIT ACCESS SYSTEM
8. Hardware operation sheet to place under the PIT Access-Board

Usage:

An Access System with up to 7 different Access Numbers (16 byte Pseudo Random Number PRN) can be demonstrated. The Access Numbers are stored in Access-PITs. The sytem can be set into the Access-, Learn- or Program Mode via push-buttons or Master-Key PITs. If a valid Access-PIT is recognized, a relay is activated until the PIT is in the rf-field. The relay can control i.e. a lamp.

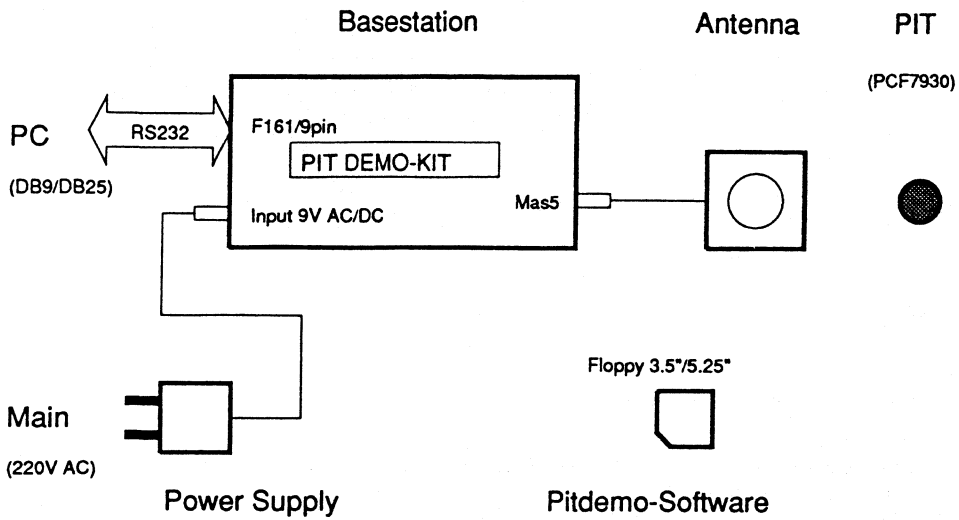
Recommended table size:

80cm x 60cm

Handling cost fee:

1000 DM

Exhibition Model RF-Identification



The Exhibition Model consists of the following parts:

1. Basestation
2. Antenna
3. PIT (4 PCF7930)
4. Power Supply (220V Main Voltage)
5. Data Cable RS232/DB9
6. Adapter RS232/DB9(plug) - RS232/DB25(socket)
7. Demonstration Software on 3.5"/5.25" Floppy
8. Manual Hardware Description & Tutorial
9. Manual Software Command Reference & RS232 Transmission Protocol
10. Several distance holders

Usage:

Reading and writing of a Transponder can be demonstrated. The user interface further allows to show the password feature. A detailed "walk through" the software is standing in the manual "Hardware Description & Tutorial".

Recommended table size:

80cm x 60cm

Handling cost fee:

2000 DM

PRODUCT PROFILE '7930XP/030612

- Stick–shaped Identification Transponder for use in contactless car immobilizer applications
- Read and write operation over full temperature range
- Non volatile memory of 1024 bits (768 bits user data, 256 bits control data)
- Periodically automatic data read out
- Data transmission and supply energy via RF link
- Write protection
- 7 byte password
- Resonance/operating frequency 125 kHz nominal
- 20 years non–volatile data retention
- At least 250000 erase/write cycles per byte for blocks 1 and 2, 50000 for following blocks
- Extended temperature range: –40°C to +85°C
- Contactless plastic stick SOT385

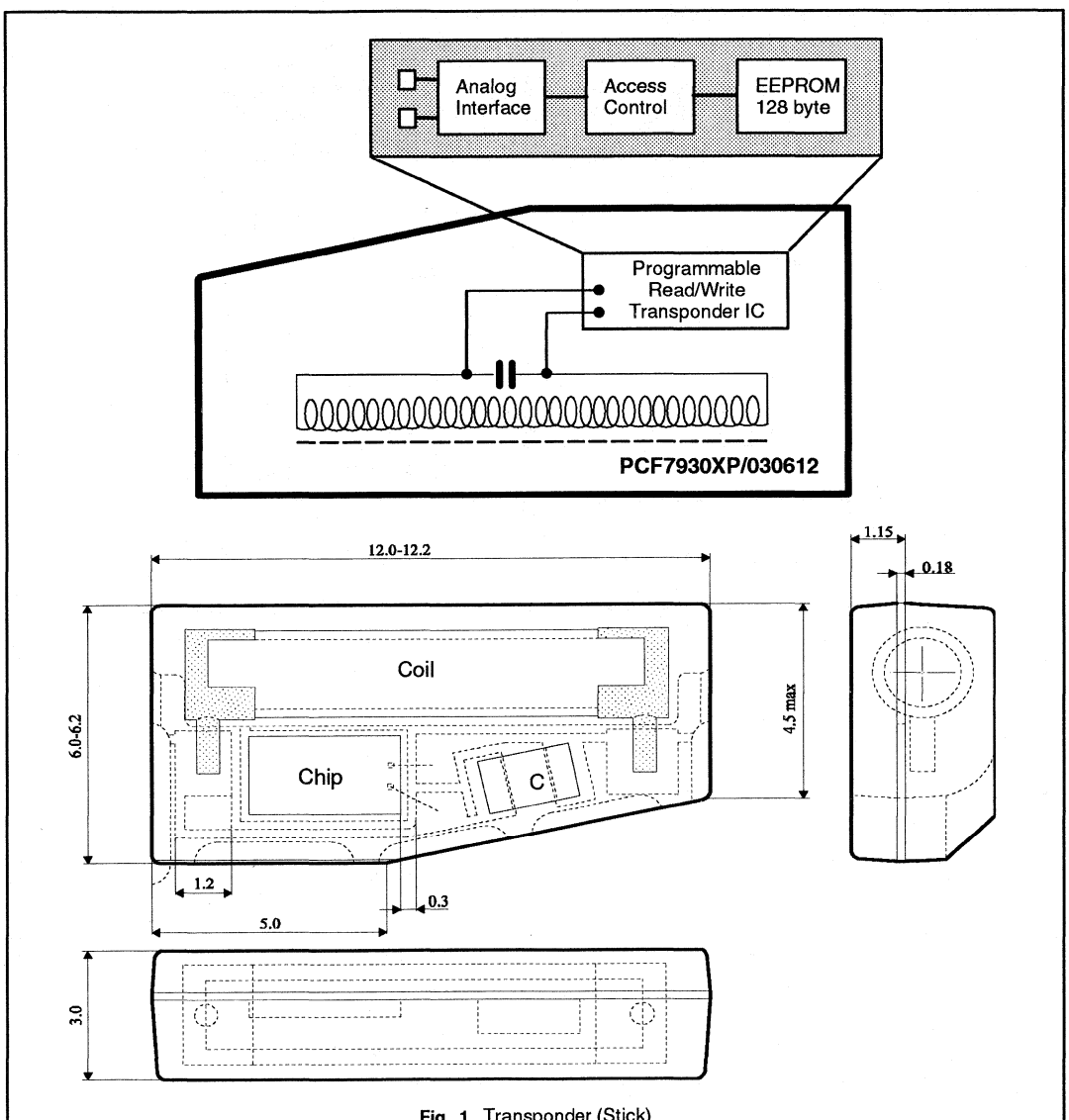


Fig. 1 Transponder (Stick)

PRODUCT PROFILE '7930XP/030612

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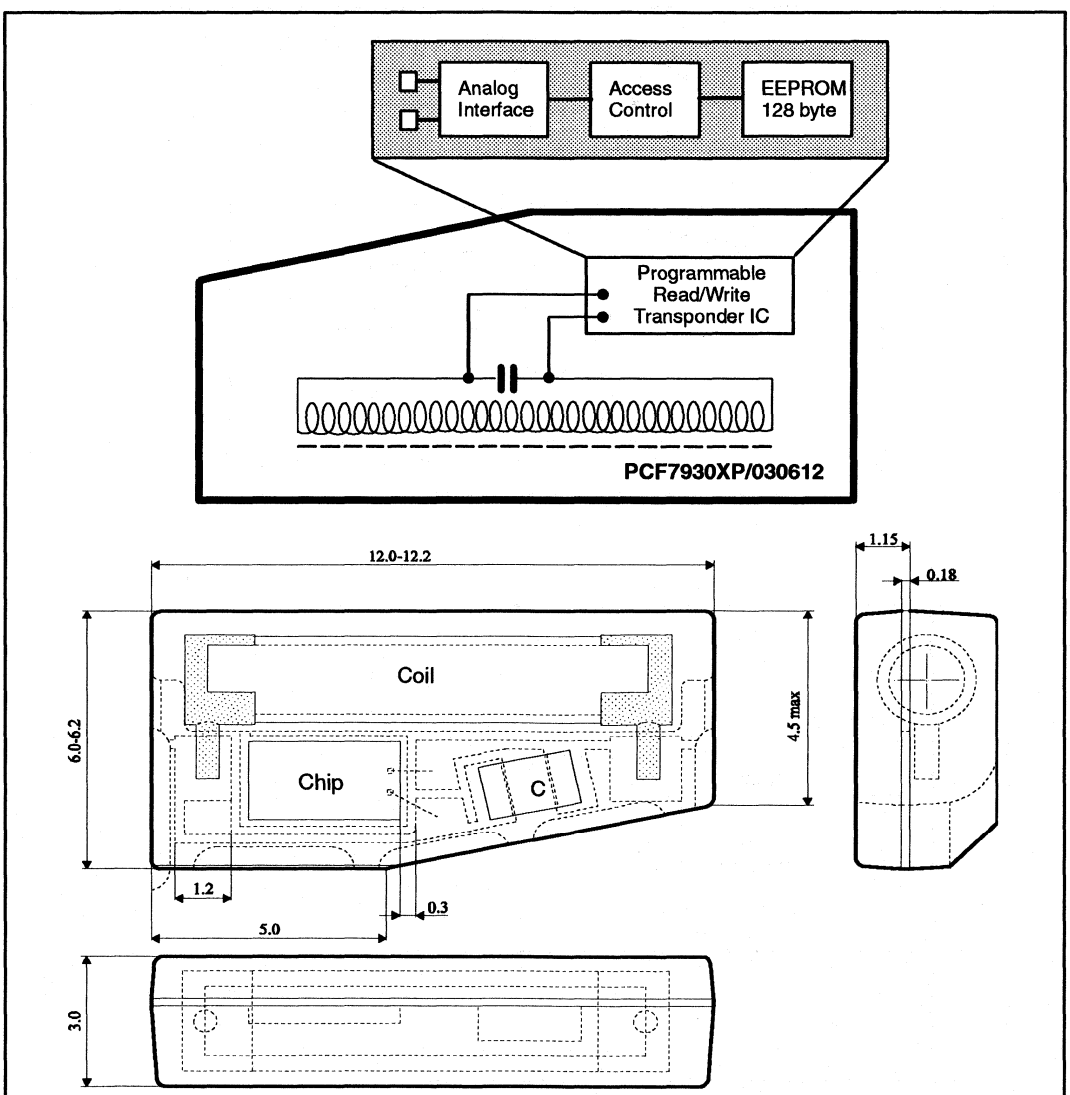

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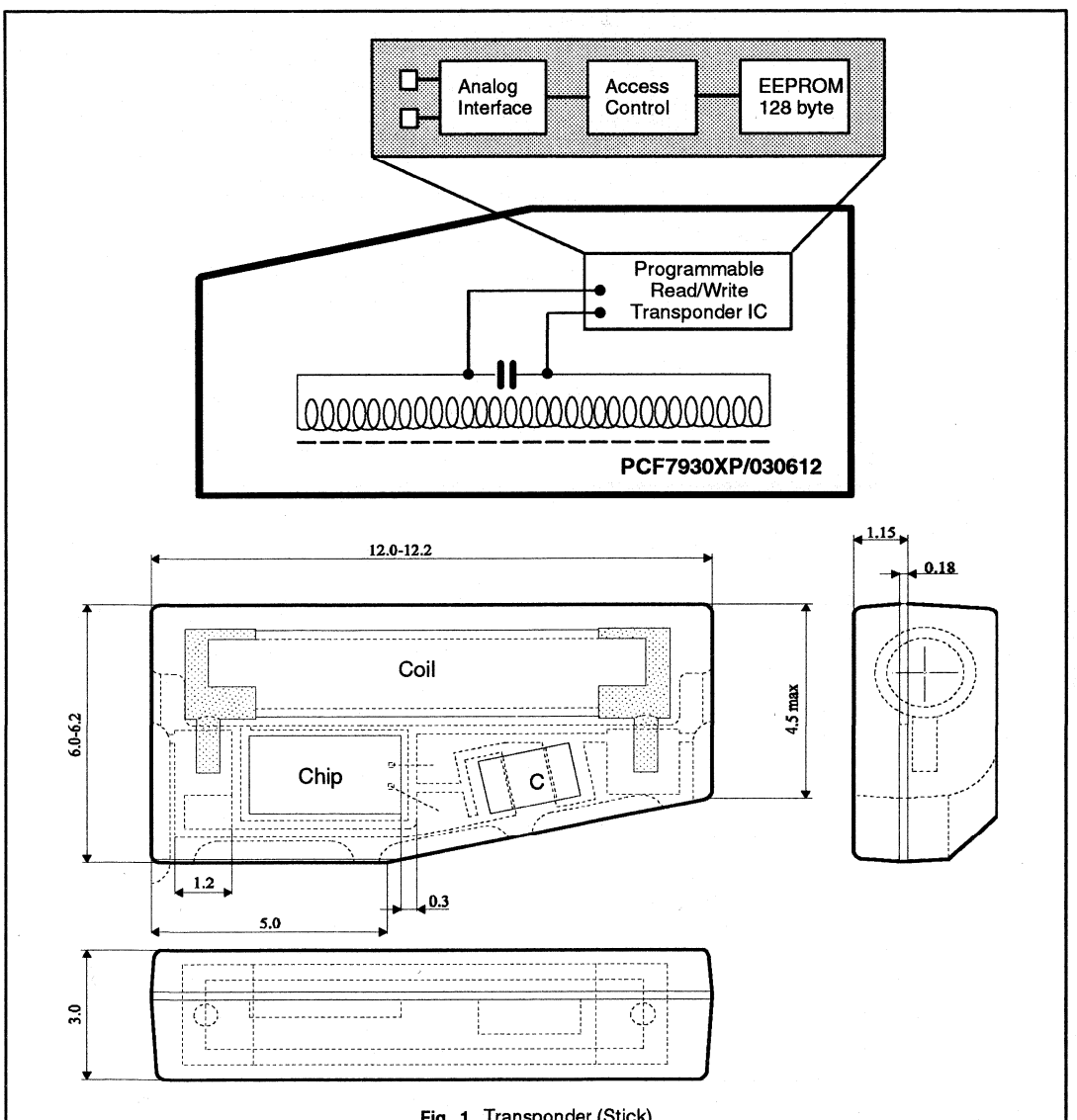

Fig. 1 Transponder (Stick)

PRODUCT PROFILE '7931XP/C

- Stick–shaped Identification Transponder for use in contactless car immobilizer applications
- Non volatile memory of 1024 bits (768 bits user data, 256 bits control data)
- Periodically automatic data read out
- Data transmission and supply energy via RF link
- Programmable Read–only operation
- 7 byte password
- Operating/resonance frequency 125 kHz nominal
- 20 years non–volatile data retention
- 100 erase/write cycles per byte with write protection
- Extended temperature range: –40°C to +85°C
- Contactless plastic stick SOT385

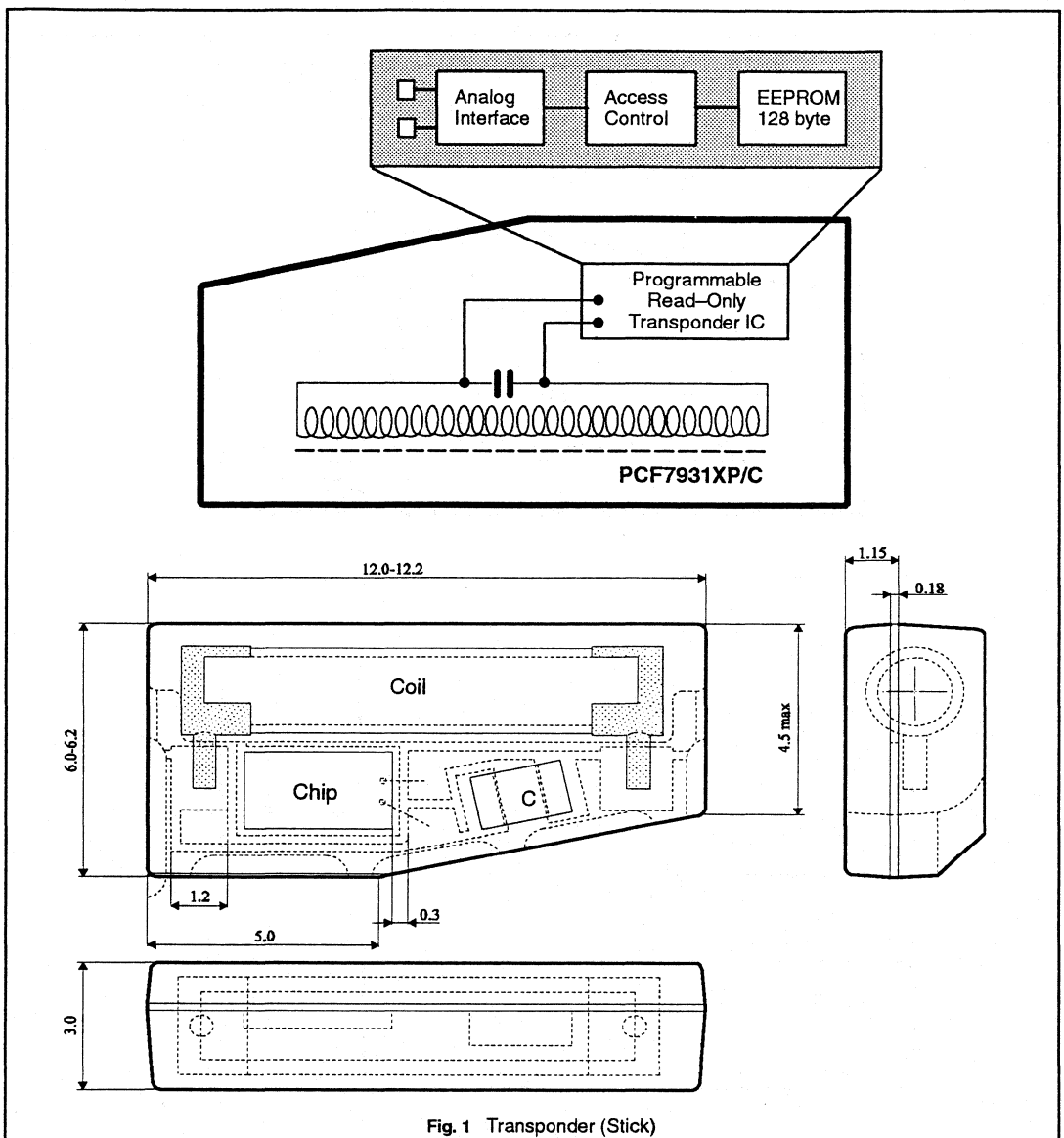

Fig. 1 Transponder (Stick)

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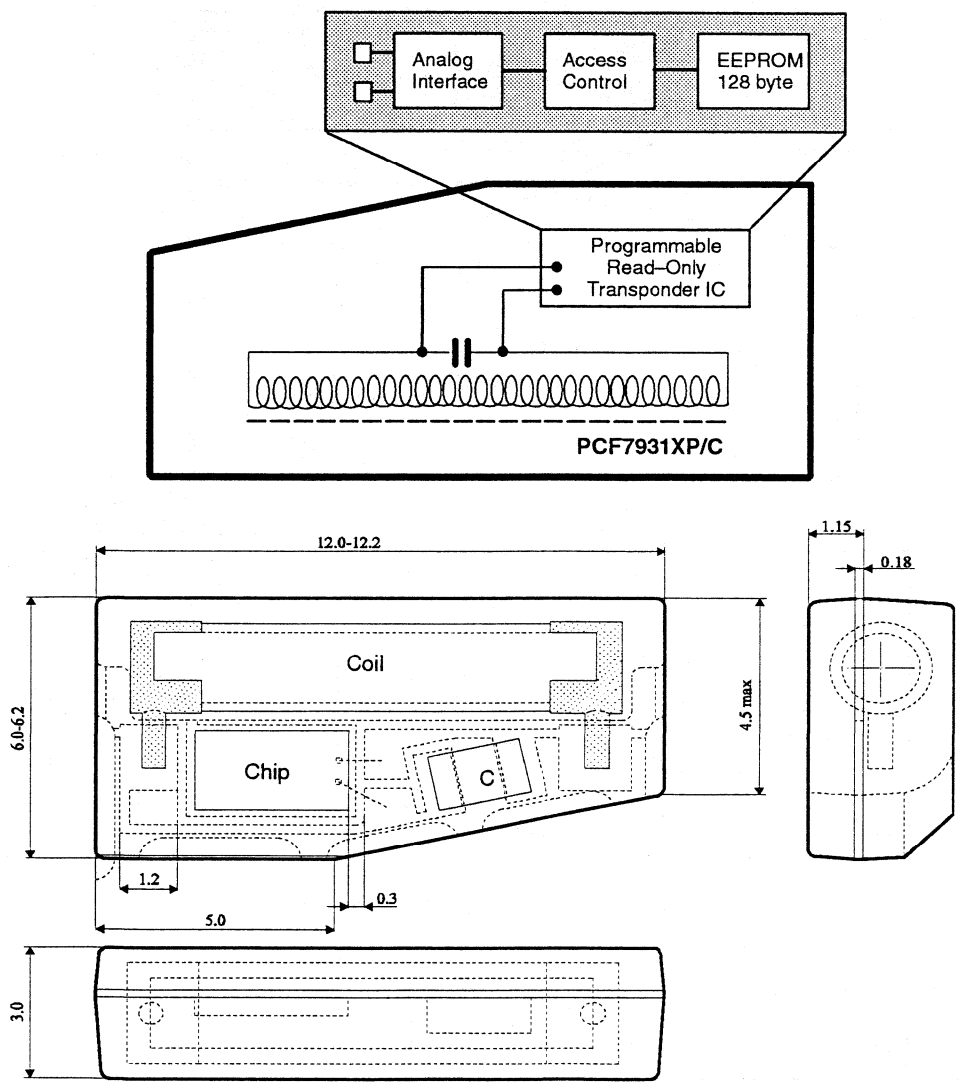

Fig. 1 Transponder (Stick)

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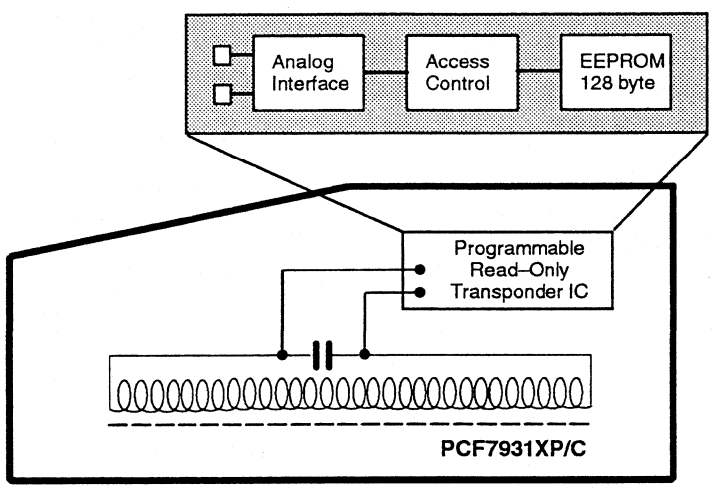

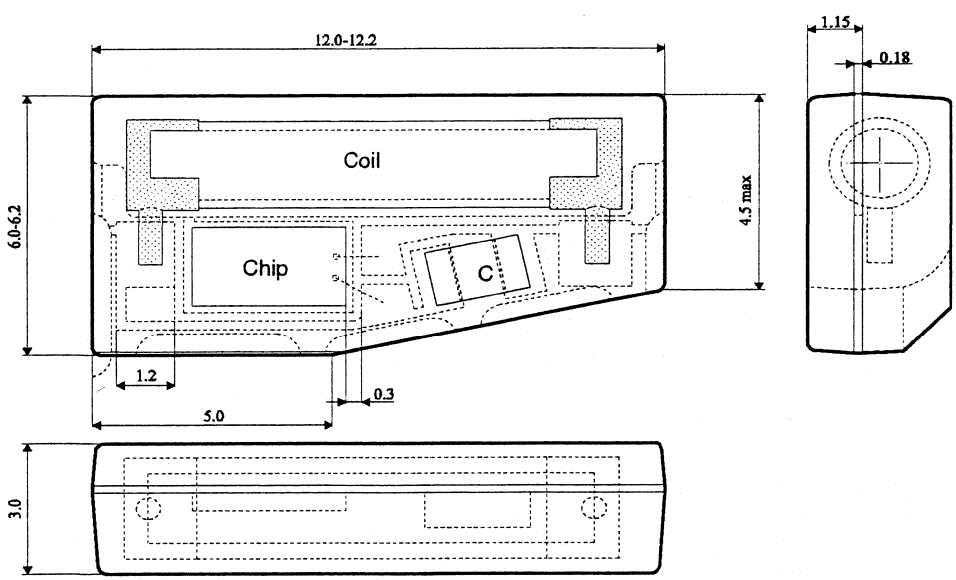

Fig. 1 Transponder (Stick)

PRODUCT PROFILE '79735S

- Stick-shaped Identification Transponder for use in contactless car immobilizer applications
- Non volatile memory of 1152 bits (768 bits user data, 256 bits control data, 128 bits secret memory) organized in 9 blocks, 16 bytes each
- Challenge/response authentication function
- Periodically automatic data read out
- Data transmission and supply energy via RF link
- Write protection
- 7 byte password
- Operating frequency 125 kHz (nominal)
- 20 years non-volatile data retention
- At least 250000 erase/write cycles per byte for blocks 0, 1 and shadow memory block 2, 50000 for the other blocks
- Extended operating temperature range -40°C to +85°C
- Contactless plastic stick SOT385

BLOCK DIAGRAM

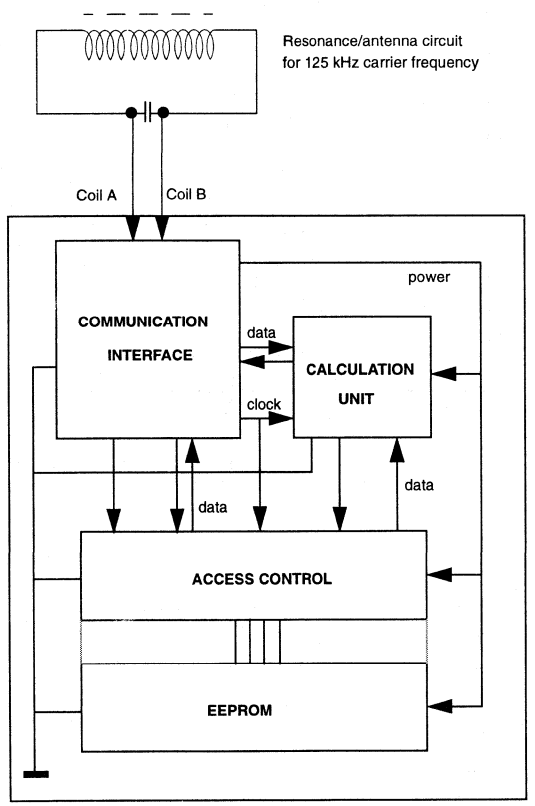

Fig. 1 Block diagram PCF79735S (SECT).

PRODUCT PROFILE '79735S

STICK PACKAGE SOT-385-1

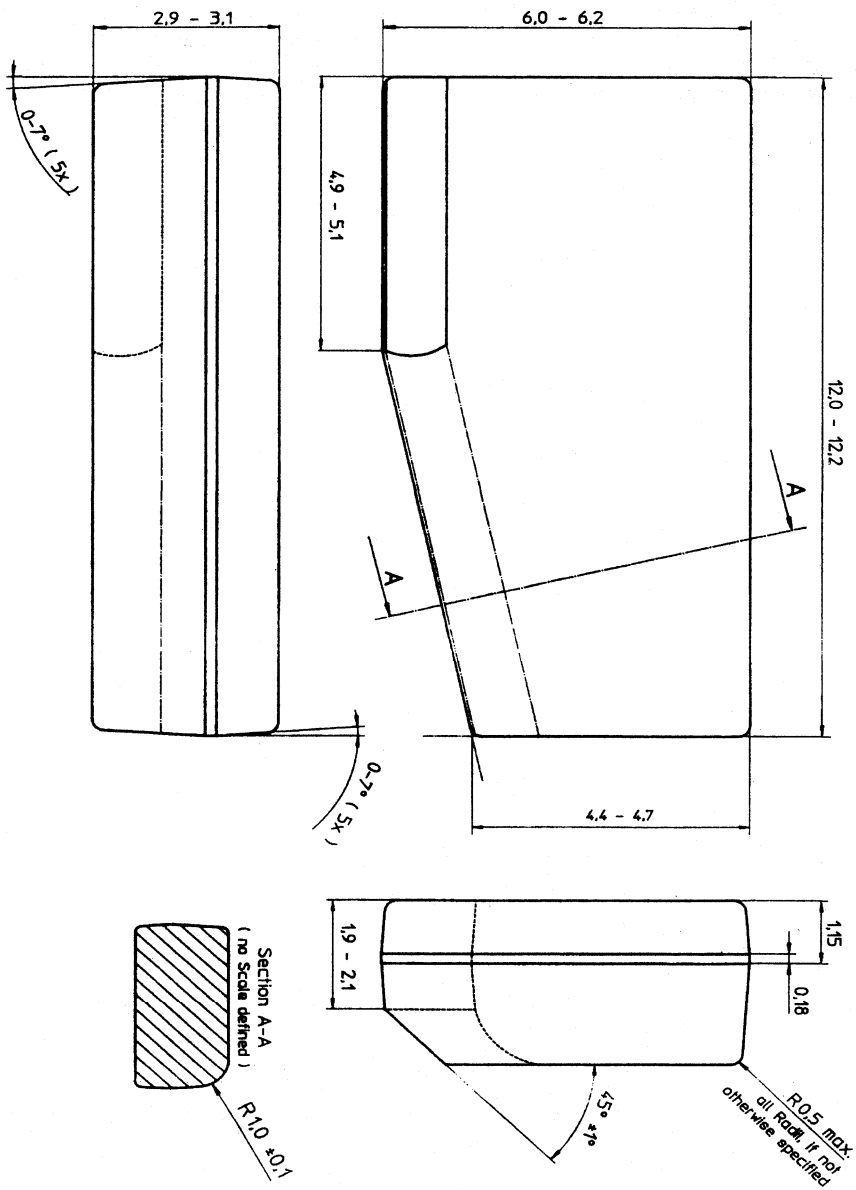

Fig. 2 Stick package SOT385-1.

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BLOCK DIAGRAM

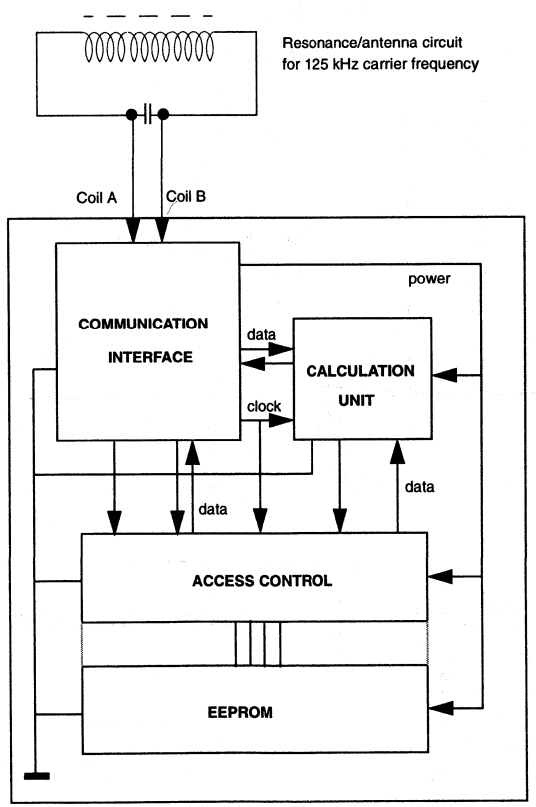

Fig. 1 Block diagram PCF79735S (SECT).

PRODUCT PROFILE '79735S

STICK PACKAGE SOT-385-1

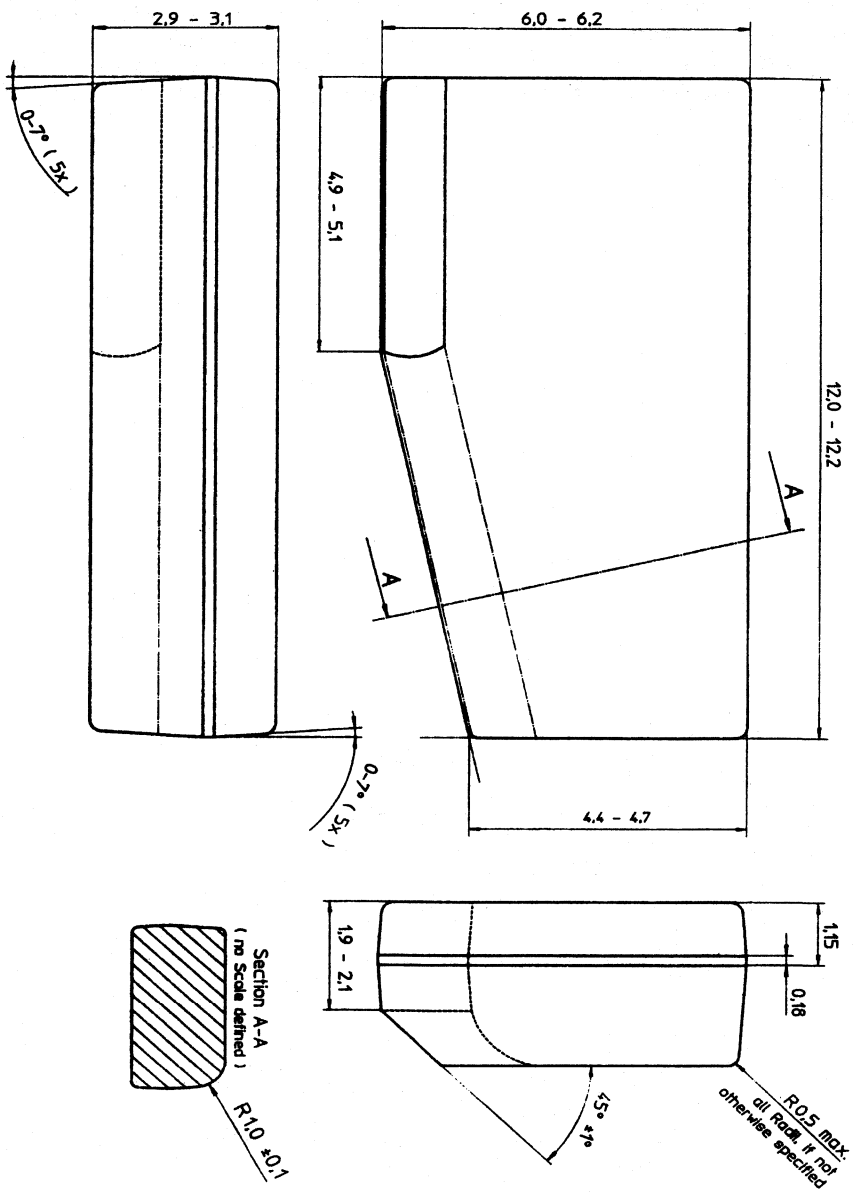

Fig. 2 Stick package SOT385-1.

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BLOCK DIAGRAM

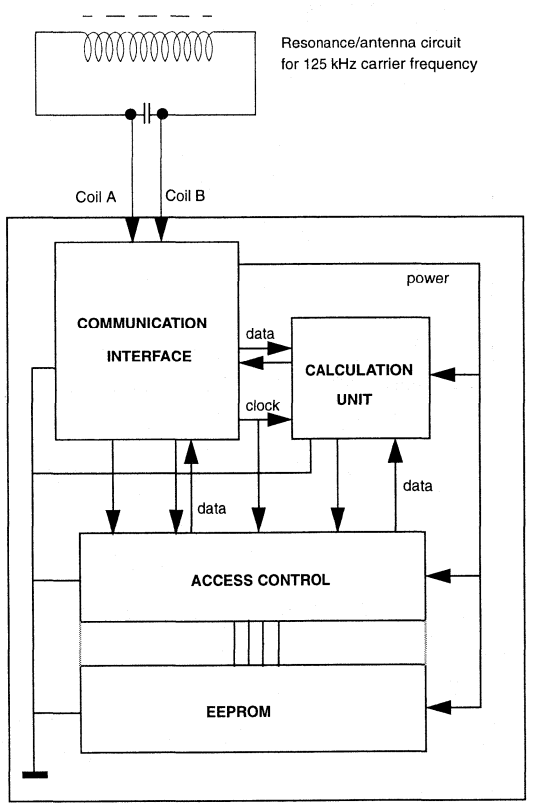


Fig. 1 Block diagram PCF79735S (SECT).

PRODUCT PROFILE '79735S

STICK PACKAGE SOT-385-1

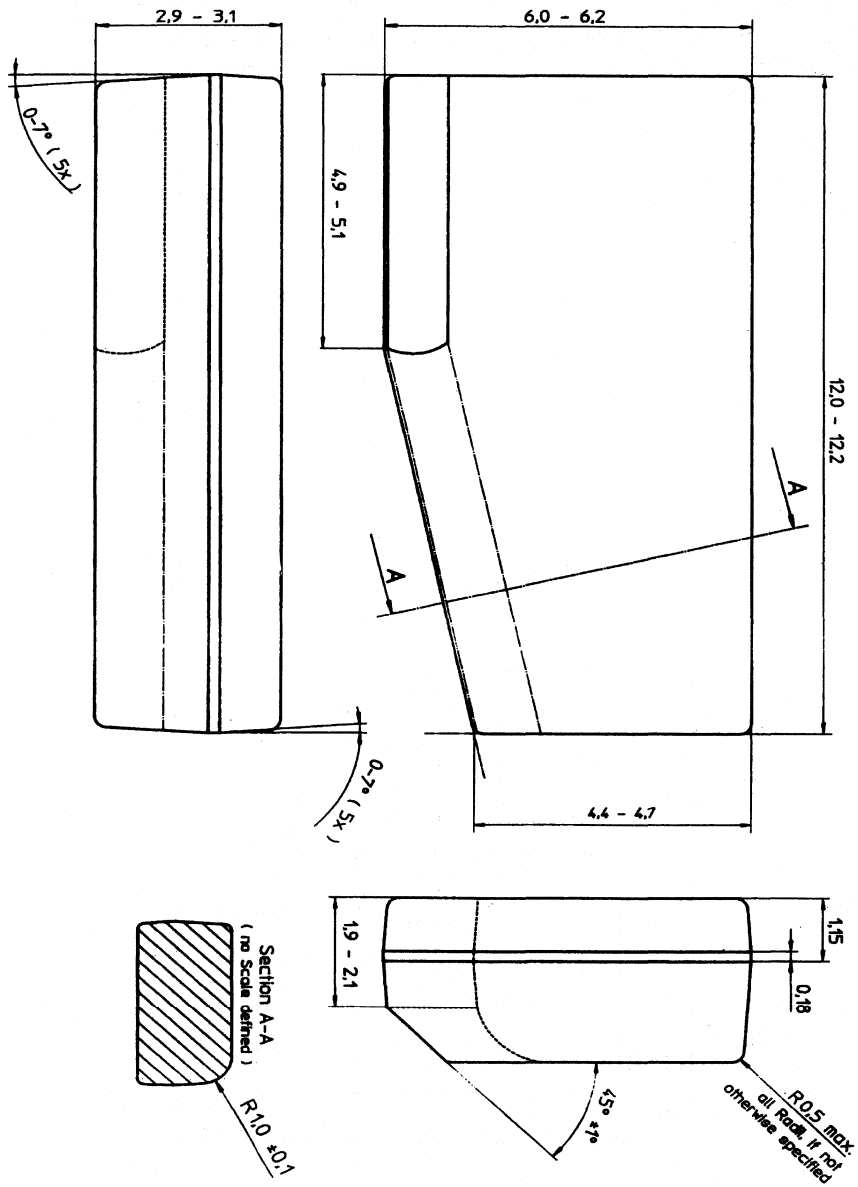


Fig. 2 Stick package SOT385-1.

PRODUCT PROFILE '7990

- Fully transparent operation
- Data transmission and supply energy via RF field
- Modulation of the field (write transponder)
- Demodulation of the field modulation applied by the transponder (read transponder)
- Supply Voltage: 5V
- Typ. Clock/Osc. frequency: 4MHz
- Antenna carrier frequency 125kHz
- Receiver sensitivity: 54 dB (signal to carrier)
- Typ. antenna driver current: 100mA (rms)
- Max. power dissipation: 300 mW (IC without antenna)
- Data In/Out: CMOS compatible
- EMC: according to DIN 40 839, Part 4, class A
- Plastic small outline package: SO20
- Operation Temp. Range: -40°C to +85°C

BLOCK DIAGRAM

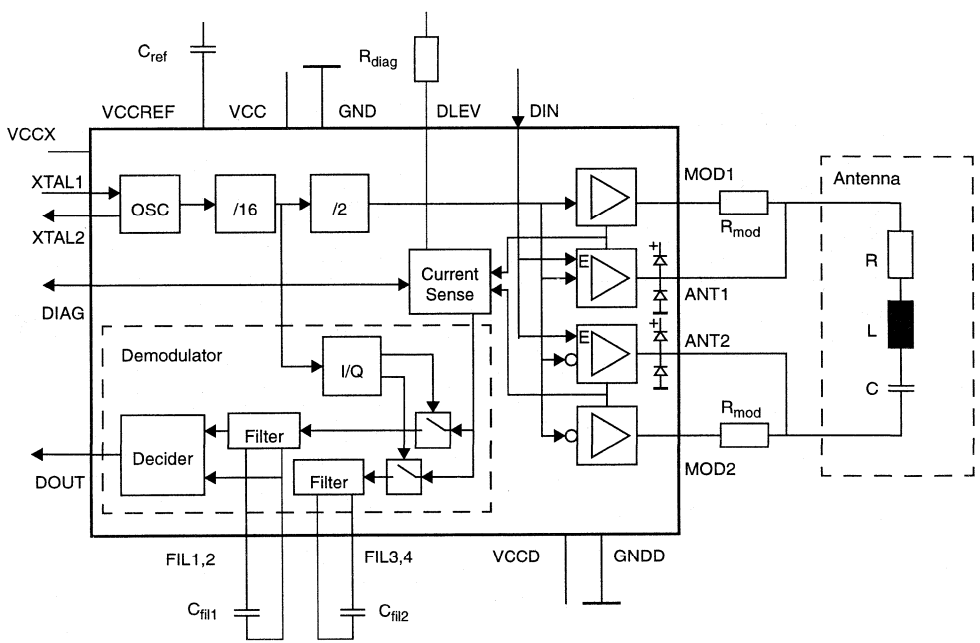
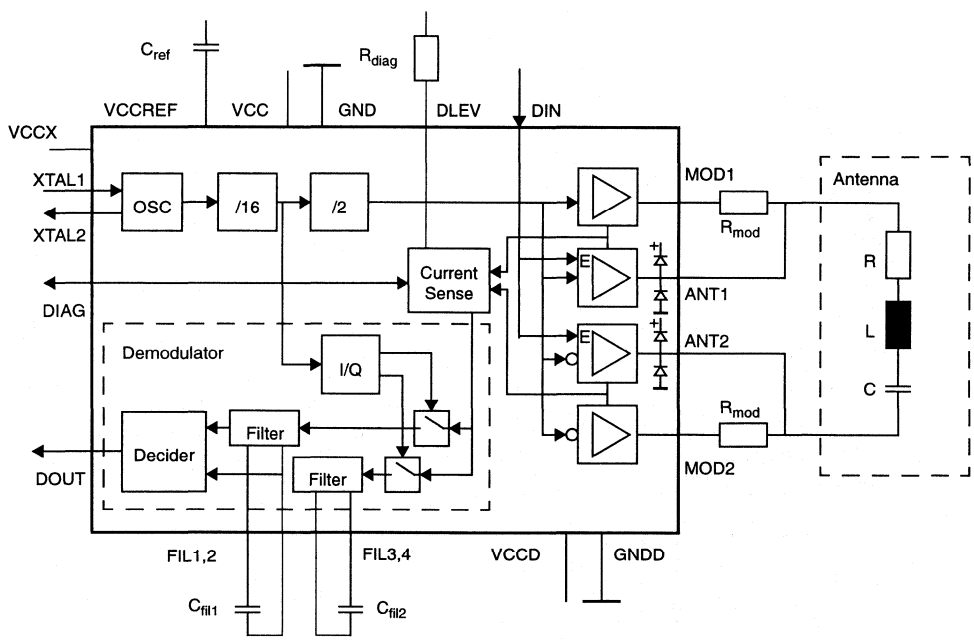


Fig. 1 Block diagram Basestation IC PCF7990.

PRODUCT PROFILE '7990

- Fully transparent operation
- Data transmission and supply energy via RF field
- Modulation of the field (write transponder)
- Demodulation of the field modulation applied by the transponder (read transponder)
- Supply Voltage: 5V
- Typ. Clock/Osc. frequency: 4MHz
- Antenna carrier frequency 125kHz
- Receiver sensitivity: 54 dB (signal to carrier)
- Typ. antenna driver current: 100mA (rms)
- Max. power dissipation: 300 mW (IC without antenna)
- Data In/Out: CMOS compatible
- EMC: according to DIN 40 839, Part 4, class A
- Plastic small outline package: SO20
- Operation Temp. Range: -40°C to +85°C

BLOCK DIAGRAM



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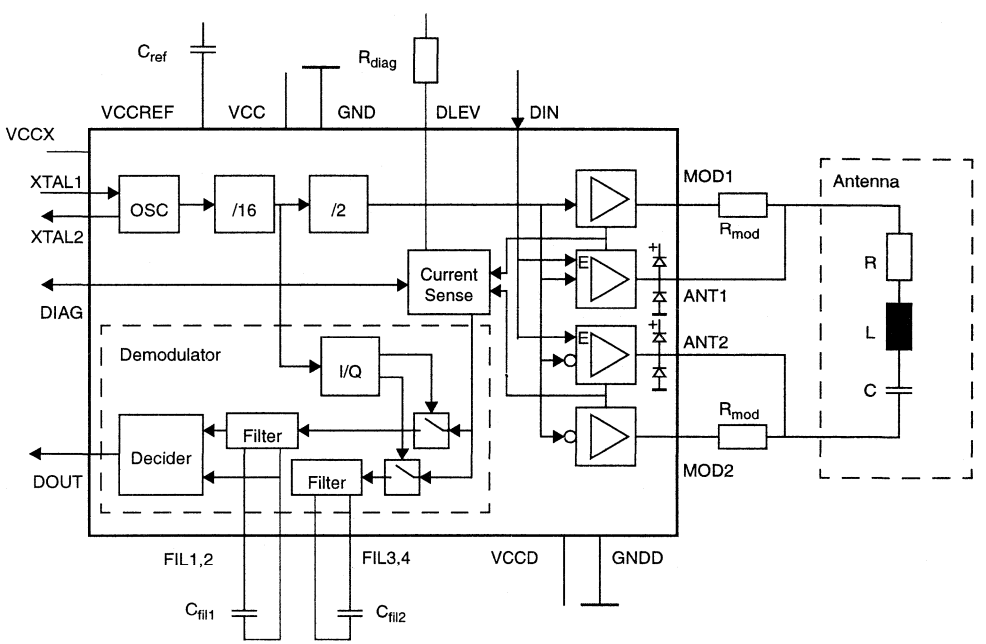


Fig. 1 Block diagram Basestation IC PCF7990.

VOLTAGE STABILIZERS

Multiple output voltage regulators

TDA3601Q
TDA3601AQ

FEATURES

- Six fixed voltage regulators
- Three microprocessor-controlled regulators
- Two V_P-state controlled regulators
- One fixed voltage regulator (can operate during load dump or thermal shutdown)
- V_{P1} supply pin (low current pin)
- V_{P2} supply pin (high current pin)
- RESET output (TDA3601Q) or $\overline{\text{RESET}}$ output (TDA3601AQ)
- Internally fixed timer of 100 µs
- Externally fixed delay timer
- High ripple rejection
- Flexible leads.

PROTECTION

- Current limit protection for regulator 1
- Foldback current limit protection (regulators 2 to 6)
- Load dump protection
- Thermal protection
- Regulator outputs DC short-circuit-safe to ground, V_P and other regulator outputs
- Capable of handling high energy on any of the output pins
- Reverse polarity safe.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Entire device						
V_{P1}	supply voltage range	operating	11	13.2	18	V
		load dump; notes 1 and 2	–	–	50	V
V_{P2}	supply voltage range	operating	11	13.2	18	V
		non-operating	–	–	30	V
		load dump; note 1	–	–	50	V
$I1_{tot}$	total quiescent current, V_{P1}	V_{P2} = 0; note 3	–	1	1.4	mA
T_c	crystal temperature		–	–	150	°C
Voltage regulators						
V_{R1}	output voltage regulator 1	0.5 mA ≤ I_{R1} ≤ 20 mA	4.75	5	5.25	V
V_{R2}	output voltage regulator 2	5 mA ≤ I_{R2} ≤ 200 mA	1.9	2.1	2.3	V
V_{R3}	output voltage regulator 3	5 mA ≤ I_{R3} ≤ 150 mA	4.75	5	5.25	V
V_{R4}	output voltage regulator 4	5 mA ≤ I_{R4} ≤ 150 mA	9	9.5	10	V
V_{R5}	output voltage regulator 5	5 mA ≤ I_{R5} ≤ 200 mA	9	9.5	10	V
V_{R6}	output voltage regulator 6	5 mA ≤ I_{R6} ≤ 200 mA	9.3	9.75	10.2	V

Notes

1. Load dump, during 50 ms, t_r > 2.5 ms.
2. Regulator 1 operating, 0.5 mA ≤ I_{R1} ≤ 20 mA.
3. V_{P1} = 13.2 V; V_{P2} = R4-sel = R5-sel = 0; I_{R1} = 0.

BLOCK DIAGRAM

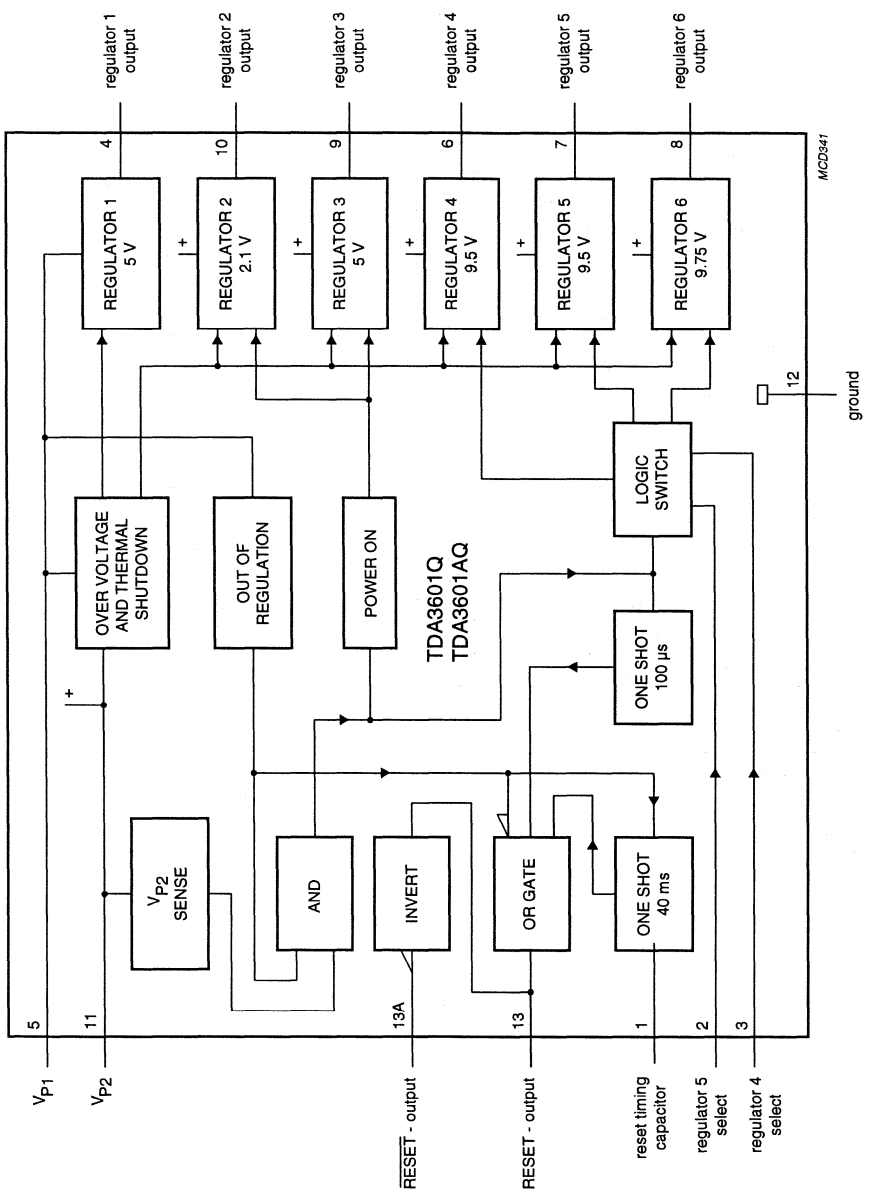


Fig.1 Block diagram.

Multiple output voltage regulators

TDA3601Q
TDA3601AQ

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3601Q/AQ	13	DIL	plastic	SOT141-6

GENERAL DESCRIPTION

The circuit contains five fixed voltage regulators with foldback current protection and one fixed voltage regulator (REGULATOR 1) that also operates during a load dump. In addition, a RESET function (TDA3601Q) or $\overline{\text{RESET}}$ function (TDA3601AQ), timer functions and a logic multiplexer are implemented.

PINNING

SYMBOL	PIN	DESCRIPTION
C_{RESET}	1	reset timing capacitor
R5-sel	2	regulator 5 select
R4-sel	3	regulator 4 select
REG1	4	regulator 1 output (5 V)
V_{P1}	5	supply voltage
REG4	6	regulator 4 output (9.5 V)
REG5	7	regulator 5 output (9.5 V)
REG6	8	regulator 6 output (9.75 V)
REG3	9	regulator 3 output (5 V)
REG2	10	regulator 2 output (2.4 V)
V_{P2}	11	supply voltage
GND	12	ground
RES	13	RESET output (TDA3601Q)
$\overline{\text{RES}}$	13A	$\overline{\text{RESET}}$ output (TDA3601AQ)

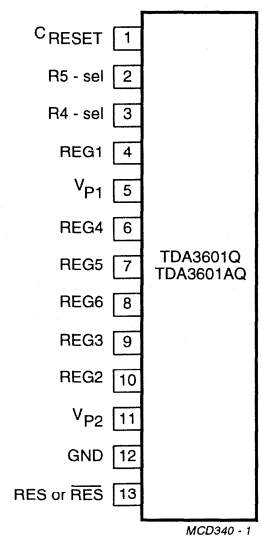


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA3601Q is a multiple output voltage regulator with six fixed voltage regulators. Three, logical switch controlled, voltage regulators (numbers 4 to 6) are available, and one non-switchable voltage regulator (number 1). In addition, there are two further regulators (numbers 2 and 3), which are controlled by supply voltages V_{P1} and V_{P2} (Schmitt trigger).

Regulator 1 is not affected by load dump or thermal shutdown. Regulators 2 to 6 are supplied by V_{P2}; they can therefore be switched of by an ignition switch, for example. An internal bandgap voltage reference, which provides a reference voltage for each independent regulator, is supplied by V_{P1}. This supply voltage V_{P1} also supplies regulator 1.

A V_{P2} sense circuit outputs a logical high when the V_{P2} voltage rises through V_{thr}, which remains high until the V_{P2} voltage falls through V_{thf}.

The supply voltage V_{P1} is sensed by an out-of-regulation Schmitt trigger.

When this voltage drops below 5.95 V typical, the reset output is disabled, to prevent a microprocessor being disturbed by a too-low supply voltage. An out-of-regulation condition is indicated by a logical low and an in-regulation condition indicated by a logical high.

The 'Power On' switch low will disable regulator 2 and 3 outputs. In addition, the logic switch will be disabled, so that regulators 4 to 6 are switched off. When both V_{P2}-sense and out-of-regulation are high, the 'Power On' will be high, so that the logic multiplexer and regulators 2 and 3 are enabled. Regulators 4 to 6 can now be selected by the multiplexer.

Re-triggerable one-shot circuits produce a RESET (open collector output) when V_{P1} is available (40 ms delay signal), or when both V_{P1} and V_{P2} are available (100 µs pulse). RESET will be held in a constant high state when the supply voltage V_{P1} is less than 5.5 V (5.95 V typical).

The TDA3601 has a RESET output, but the TDA3601A has an inverted RESET output ($\overline{\text{RESET}}$).

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{P1}, V_{P2}	supply voltage	operating	–	18	V
		non-operating	–	30	V
		load dump protected; during 50 ms; $t_r > 2.5$ ms; note 1	–	50	V
P_{tot}	total power dissipation	$T_{case} < 30$ °C	–	15	W
T_{stg}	storage temperature range	non-operating	–55	150	°C
T_{vj}	virtual junction temperature	operating	–40	150	°C
V_{pr}	reverse polarity	non-operating	–	6	V

Note

1. Regulator 1 operating, $0.5 \text{ mA} \leq I_{R1} \leq 20 \text{ mA}$.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	8	K/W
$R_{th\ j\text{-}amb}$	thermal resistance from junction to ambient in free air	40	K/W

QUALITY SPECIFICATION

Quality according to UZW-BO/FQ-0601.

CHARACTERISTICS

$V_{P1} = V_{P2} = 13.2$ V, $T_{amb} = 25$ °C, $C_{out} = 10$ µF; unless otherwise specified (see Fig.5).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{P1}	supply voltage range	operating	11	13.2	18	V
V_{P1}	supply voltage range	load dump; notes 1and 2	–	–	50	V
V_{P2}	supply voltage range	operating	11	13.2	18	V
V_{P2}	supply voltage range	load dump; note 1	–	–	50	V
I_{P1}	quiescent current	$V_{P2} = 0$; note 3	–	1.1	1.4	mA
Schmitt triggers						
V_{P2}-SENSE THRESHOLD						
V_{thr}	rising threshold voltage		7.6	8	8.4	V
V_{thf}	falling threshold voltage		6.2	6.5	6.8	V
V_{hy}	hysteresis		1.35	1.5	1.65	V
OUT-OF-REGULATION THRESHOLD						
V_{thr}	rising threshold voltage		6.8	7.35	7.9	V
V_{thf}	falling threshold voltage		5.5	5.95	6.4	V
V_{hy}	hysteresis		1.2	1.4	1.6	V
Reset circuits (for timing, see Fig.3)						
t_{rst1}	reset delay time	$C_{rst} = 100$ nF	20	40	100	ms
t_{rst}	reset hold time		50	100	150	µs
V_{rl}	reset low	$I_{sync} = 1$ mA	–	0.15	0.8	V
I_{cr}	delay current (pin 1 to C_{rst})		–	–5	–	µA
t_r	reset rise time	note 4	–	–	1	µs
t_f	reset fall time	note 4	–	–	1	µs
V_{CAP}	voltage pin 1	$C_{rst} = 0$	5.5	6.0	–	V
R_{sp}	spike-on reset	on-state; note 5	–	0	100	mV
Regulators						
SELECTOR CONTROL INPUTS R4-SEL AND R5-SEL						
V_{sl}	input low voltage		–0.5	–	0.8	V
V_{sh}	input high voltage		2	–	–	V
I_{hs}	input high current	$V_{RXsel} > 2$ V	–	–	1	µA
I_{ls}	input low current	$V_{RXsel} < 0.8$ V	–1	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REGULATOR 1 (I_{R1} = 1 mA UNLESS OTHERWISE SPECIFIED)						
V_{R1}	output voltage	0.5 mA ≤ I_{R1} ≤ 20 mA	4.75	5	5.25	V
		6.25 V ≤ V_{P1} ≤ 18 V	4.75	5	5.25	V
V_{R1L}	output voltage	18 V ≤ V_P ≤ 50 V	4.75	5	5.25	V
ΔV_{R1}	line regulation	6.25 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL1}	load regulation	0.5 mA ≤ I_{R1} ≤ 20 mA	–	–	60	mV
RR1	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
V_{Rd1}	drop-out voltage	I_{R1} = 20 mA	–	–	1	V
I_{Rm1}	current limit		30	–	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C
REGULATOR 2 (I_{R2} = 5 mA UNLESS OTHERWISE SPECIFIED)						
V_{R2}	output voltage	5 mA ≤ I_{R2} ≤ 200 mA	1.9	2.1	2.3	V
		7 V ≤ V_P ≤ 18 V	1.9	2.1	2.3	V
ΔV_{R2}	line regulation	7 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL2}	load regulation	5 mA ≤ I_{R2} ≤ 200 mA	–	–	70	mV
RR2	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
I_{Rm2}	current limit	V_{R2} > 1.75 V; note 7	250	–	–	mA
I_{Rsc2}	short-circuit current	R_L ≤ 0.5 Ω; note 7	–	tbn	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C
REGULATOR 3 (I_{R3} = 5 mA UNLESS OTHERWISE SPECIFIED)						
V_{R3}	output voltage	5 mA ≤ I_{R3} ≤ 150 mA	4.75	5	5.25	V
		7 V ≤ V_P ≤ 18 V	4.75	5	5.25	V
ΔV_{R3}	line regulation	7 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL3}	load regulation	5 mA ≤ I_{R3} ≤ 150 mA	–	–	70	mV
RR3	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
I_{Rm3}	current limit	V_{R3} > 4.5 V; note 7	200	–	–	mA
I_{Rsc3}	short-circuit current	R_L ≤ 0.5 Ω; note 7	–	tbn	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C
REGULATOR 4 (I_{R4} = 5 mA UNLESS OTHERWISE SPECIFIED)						
V_{R4}	output voltage	5 mA ≤ I_{R4} ≤ 150 mA	9	9.5	10	V
		11 V ≤ V_P ≤ 18 V	9	9.5	10	V
ΔV_{R4}	line regulation	11 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL4}	load regulation	5 mA ≤ I_{R4} ≤ 150 mA	–	–	70	mV
RR4	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
V_{Rd4}	drop-out voltage	I_{R4} = 150 mA	–	–	1	V
I_{Rm4}	current limit	V_{R4} > 8.5 V; note 7	200	–	–	mA
I_{Rsc4}	short-circuit current	R_L ≤ 0.5 Ω; note 7	–	tbn	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REGULATOR 5 (I_{R5} = 5 mA UNLESS OTHERWISE SPECIFIED)						
V_{R5}	output voltage	5 mA ≤ I_{R5} ≤ 200 mA	9	9.5	10	V
		11 V ≤ V_P ≤ 18 V	9	9.5	10	V
ΔV_{R5}	line regulation	11 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL5}	load regulation	5 mA ≤ I_{R5} ≤ 200 mA	–	–	70	mV
RR5	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
V_{Rd5}	drop-out voltage	I_{R5} = 200 mA	–	–	1	V
I_{Rm5}	current limit	V_{R5} > 8.5 V; note 7	250	–	–	mA
I_{Rsc5}	short-circuit current	R_L ≤ 0.5 Ω; note 7	–	tbn	–	mA
$\Delta V/\Delta T$	thermal drift	−40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C
REGULATOR 6 (I_{R6} = 5 mA UNLESS OTHERWISE SPECIFIED)						
V_{R6}	output voltage	5 mA ≤ I_{R6} ≤ 200 mA	9.3	9.75	10.25	V
		11 V ≤ V_P ≤ 18 V	9.3	9.75	10.25	V
ΔV_{R6}	line regulation	11 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL6}	load regulation	5 mA ≤ I_{R6} ≤ 200 mA	–	–	70	mV
RR6	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
V_{Rd6}	drop-out voltage	I_{R6} = 200 mA	–	–	0.5	V
I_{Rm6}	current limit	V_{R6} > 8.5 V; note 7	300	–	–	mA
I_{Rsc6}	short-circuit current	R_{bel} ≤ 0.5 Ω; note 7	–	tbn	–	mA
$\Delta V/\Delta T$	thermal drift	−40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C

Notes

1. During 50 ms, t_r > 2.5 ms.
2. Regulator 1 operating, 0.5 mA ≤ I_{R1} ≤ 20 mA.
3. V_{P1} = 13.2 V, V_{P2} = R4-sel = R5-sel = 0, I_{R1} = 0.
4. External pull-up resistor of 10 kΩ to 5 V required, and C_{load} ≤ 10 pF.
5. Spike-on reset measured within a time frame of 75 msec.
6. V_{P1} = V_{P2} = 13.2 V, ripple on V_{P1} = V_{P2} of: 1 $V_{(p-p)}$, f_o = 120 Hz.
7. Foldback current protection behaviour: see Fig.4.

Reset circuits

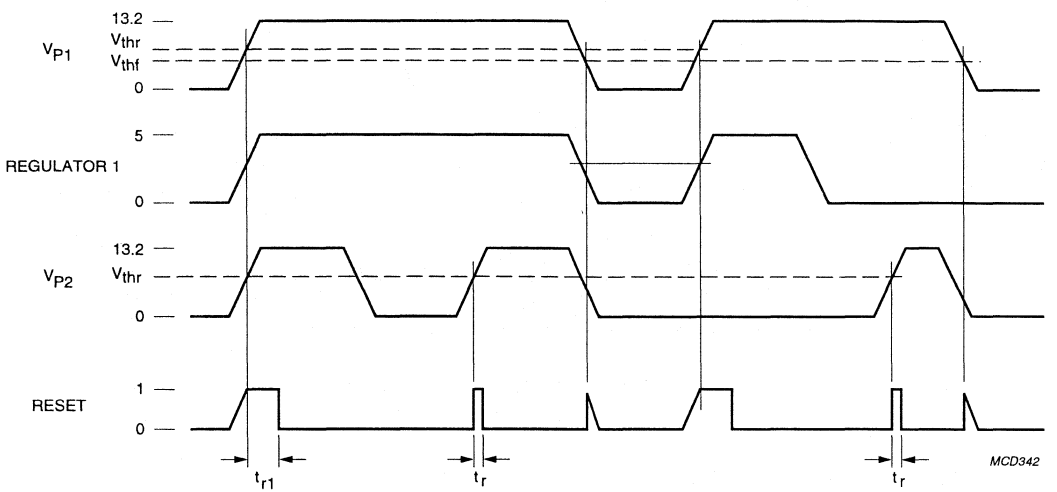


Fig.3 Timing reset.

Regulators truth table (see note 1).

INPUTS				OUTPUTS				
V_{P1}	V_{P2}	R4-SEL	R5-SEL	REG.1	REGS 2 & 3	REG.4	REG.5	REG.6
0	X	X	X	0	0	0	0	0
1	0	X	X	1	0	0	0	0
1	1	0	0	1	1	0	0	0
1	1	1	0	1	1	1	0	1
1	1	0	1	1	1	0	1	1
1	1	1	1	1	1	0	0	1

Note

1. 0 = LOW/OFF;
   1 = HIGH/ON;
   X = don't care.

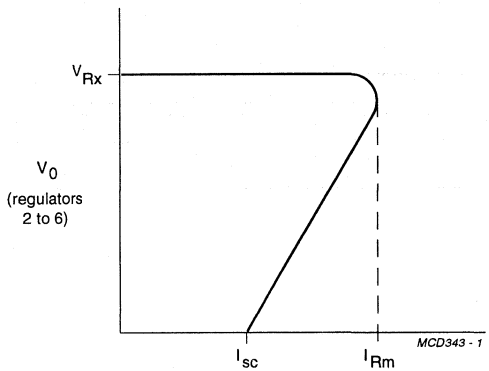
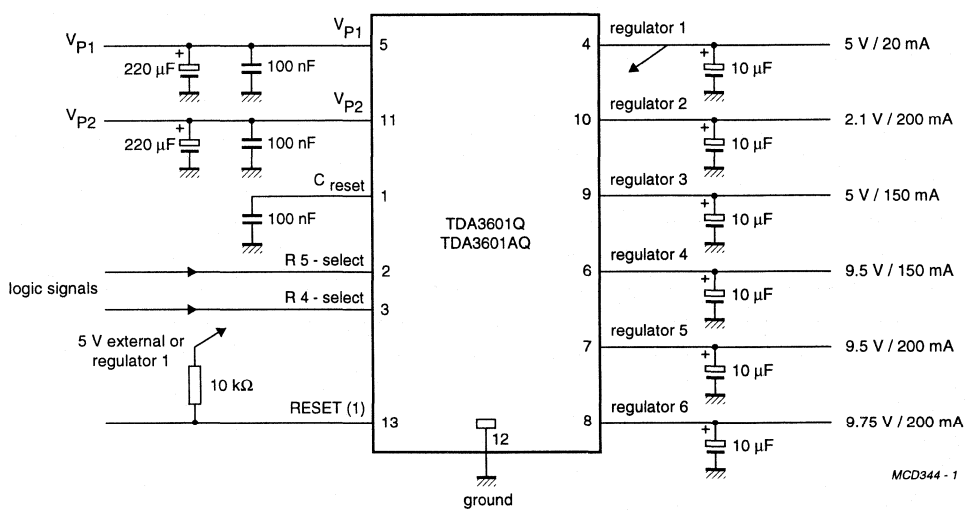


Fig.4 Foldback current protection behaviour.

TEST AND APPLICATION INFORMATION



(1) RESET output for TDA3601Q; $\overline{\text{RESET}}$ output for TDA3601AQ.

Fig.5 Application circuit.

Multiple output voltage regulator TDA3602

FEATURES

- Two V_P state controlled regulators (REG1 and REG2)
- Regulator 3 operates during load dump or thermal shutdown
- Multi-function control pin
- A back-up circuit for Regulator 3 via a single capacitor
- Supply voltage of −6 V to 50 V (a voltage of −3 V on V_P does not discharge capacitor C_{bu})
- Low reverse current Regulator 3
- Low quiescent current in coma mode
- HOLD output
- RESET output (LOW at load dump)
- High ripple rejection.

PROTECTIONS

- Foldback current limit protection (Regulators 1 and 2)
- Load dump protection
- Thermal protection
- DC short-circuit safe to ground and V_P of all regulator outputs
- Reverse polarity safe of pin 1 (V_P). No high currents are flowing which can damage the IC
- Capable of handling high energy on the regulator outputs.

GENERAL DESCRIPTION

The TDA3602 is a multiple output voltage regulator, intended for use in car radios with or without a microprocessor. It contains two fixed voltage regulators with foldback current protection (Regulators 1 and 2), and one fixed voltage regulator that also operates during load dump and thermal shutdown. This regulator can be used to supply a microprocessor.

A back-up circuit supplies Regulator 3 during a short period after the power is cut off (negative field decay or engine start procedure). A state control pin (pin 4) controls the device, which can be switched through four stages using the information at this pin. The switching levels at this pin contain hysteresis.

RESET and HOLD outputs can be used to interface with a microprocessor. The RESET signal can be used to call up or initialize a microprocessor (power-on reset). The HOLD signal can be used to control the power stages (mute signal in a low end application), or to generate a HOLD interrupt (microprocessor application).

An internal Zener diode on the back-up pin allows this pin to withstand a load dump when supplied by the pin using a 100 Ω series resistor.

The supply pin can withstand load dump pulses and negative supply voltages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage					
	operating		9.2	14.4	18	V
	Regulator 3 on		6.0	14.4	18	V
	jump start		–	–	30	V
	load dump; Regulator 3 on		–	–	50	V
	operating	note 1	6.5	–	30	V
	load dump; Regulator 3 on	note 1	–	–	50	V
I_P	total quiescent current	coma mode	–	290	–	µA
T_{vj}	virtual junction temperature		–	–	150	°C
Voltage regulators						
V_{R1}	output voltage Regulator 1	$0.5\ mA \leq I_{R1} \leq 250\ mA$	8.2	8.5	8.8	V
V_{R2}	output voltage Regulator 2	$0.5\ mA \leq I_{R2} \leq 140\ mA$	4.8	5.0	5.2	V
V_{R3}	output voltage Regulator 3	$0.5\ mA \leq I_{R3} \leq 50\ mA$	4.8	5	5.2	V

Note

1. V_{bu} (pin 8) supplied by V_{P2} with a 100 Ω series resistor and $I_{REG3} < 10\ mA$.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3602	9	SIL	plastic	SOT110-1

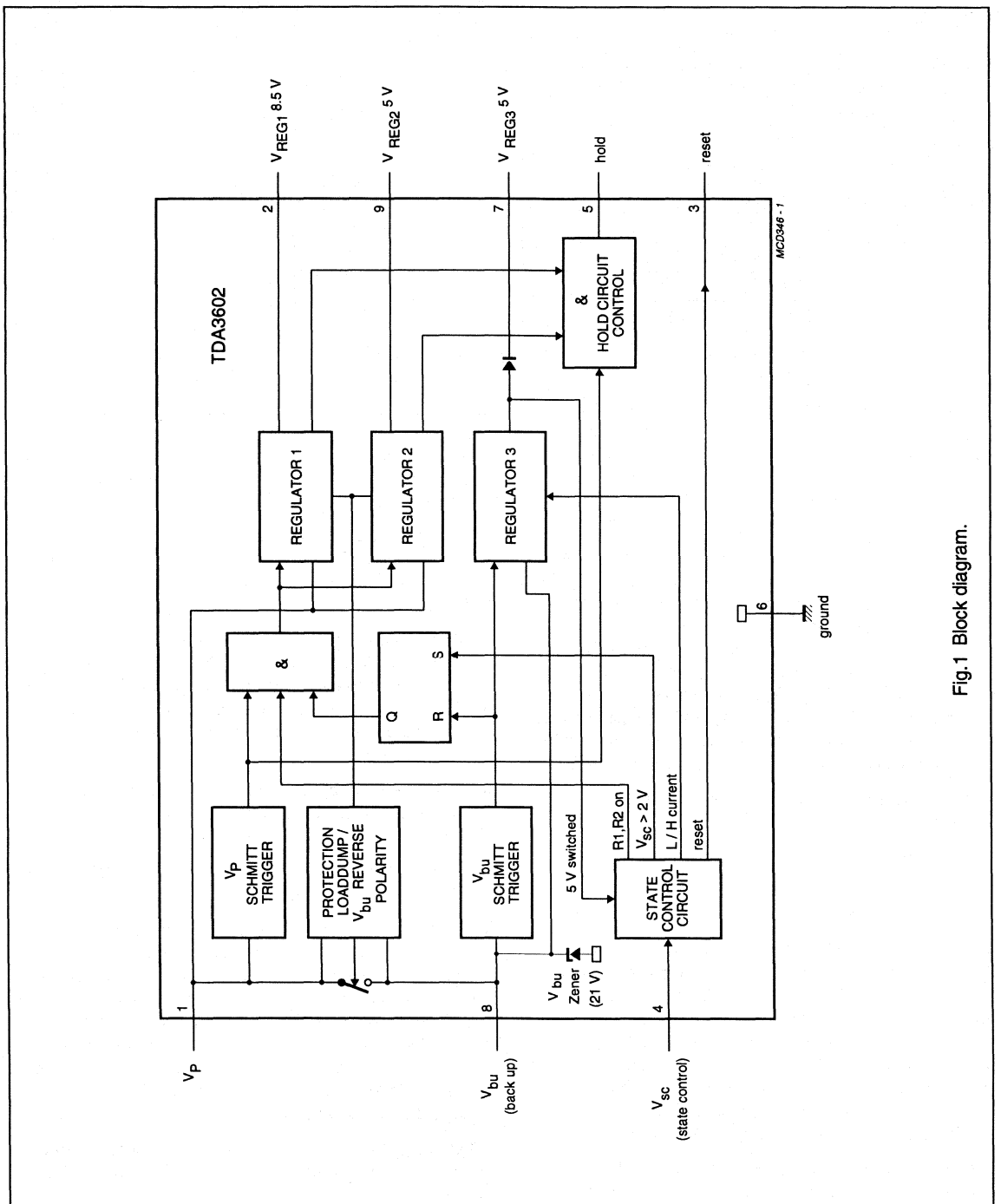


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
REG1	2	Regulator 1 output
RESET	3	reset output
V_{sc}	4	state control input
HOLD	5	hold output
GND	6	ground
REG3	7	Regulator 3 output
V_{bu}	8	back-up
REG2	9	Regulator 2 output

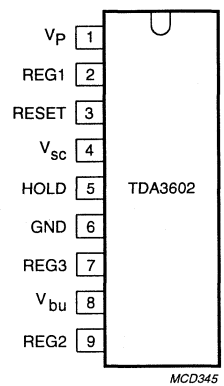


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

This multiple output voltage regulator contains three fixed voltage regulators, numbered 1, 2 and 3. Two of these can be switched between the on and off states using the state control pin (pin 4). The third (Regulator 3), which is continuously in, can be switched by the state control pin between a low and a high current mode.

In addition to Regulators 1 and 2, the device is supplied by an internal switch that is open when the supply voltage falls below the back-up voltage (negative field decay or engine start procedure), or during a load dump. (During this load dump, Regulators 1 and 2 are switched off and RESET is switched LOW). This switched supply voltage (the so-called back-up voltage (V_{bu}), is available at pin 8. An electrolytic capacitor can be connected to this pin, and the charge on this capacitor can be used to supply the device for a short period after the supply voltage is removed.

Three pins are provided for interfacing with a microprocessor:

- state control pin
- hold output pin
- reset output pin.

When the supply voltage (V_P) is connected to the device, V_{bu} will rise. When V_{bu} reaches 7.9 V, the device is in the power-on mode. The RESET output goes HIGH and Regulator 3 is switched on. In a microprocessor application, the RESET output can be used to call up the CPU and to initialize the program. What follows depends on the voltage at the state control pin (V_{sc}). In most applications, when the supply voltage is connected, V_{sc} will rise slowly (e.g. by charging a capacitor).

The device will leave the power-on mode and enter the reset mode when V_{sc} rises above 2.2 V. In both the power-on and reset modes, Regulator 3 will be in the high current mode, Regulators 1 and 2 will be switched off and the RESET output will be HIGH.

The device will enter the wake mode when V_{sc} reaches 2.8 V. The RESET pin will go LOW and the CPU must be switched to the sleep mode. Regulator 3 is still in the high current mode.

As V_{sc} continues rising and the voltage reaches 3.6 V, the stabilizer will be switched into the sleep mode. It will be in a coma mode when V_{sc} is greater than 3.8 V. In this mode, only the relevant circuits remain operating; this is to keep the power consumption as low as possible i.e. typically 290 μA.

If the device is switched on with V_{sc} already higher than 3.8 V, the device will be switched directly from the power-on mode into the coma mode.

When V_{sc} is lowered gradually from 3.6 V (or higher) to 2 V, the device will go from sleep to reset again.

V_{sc} must be lower than 1.1 V to bring the device into the on mode; note that this is not the same as the power-on mode. In this condition, Regulator 3 is in the high current mode, both Regulators 1 and 2 are switched on and the HOLD output will be HIGH (depending on the state of V_P and the in-regulation condition of Regulators 1 and 2). When the device is in the on mode, it will switch back to the reset mode when V_{sc} rises to 2 V, or when the supply voltage drops below 7.3 V.

When V_{REG3} drops below 3 V, the device will return to the power off mode, regardless of the condition the device was in.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage				
	operating		–	18	V
	jump start	$t \leq 10$ min	–	30	V
	load dump	$t \leq 50$ ms; $t_r \geq 2.5$ ms	–	50	V
	Regulator 3 on	$V_P > -3$ V; note 1	–	30	V
	load dump	$t \leq 50$ ms; $t_r \geq 2.5$ ms; note 1	–	50	V
	reverse battery voltage		–6	–	V
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{vj}	virtual junction temperature	operating	–40	+150	°C
V_{pr}	reverse polarity	non-operating	–	6	V
P_{tot}	total power dissipation		–	15	W

Note

1. V_{bu} (pin 8) supplied by V_{P2} with a 100 Ω series resistor and $I_{REG3} < 10$ mA.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	50 K/W
$R_{th\ j\text{-}c}$	from junction to case (see Fig.6)	12 K/W

CHARACTERISTICS

$V_P = 14.4$ V; $T_{amb} = 25$ °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage					
	operating		9.2	14.4	18	V
	Regulator 3 on	note 1	6.0	14.4	18	V
	jump start	$t \leq 10$ min	–	–	30	V
	load dump	$t \leq 50$ ms; $t_r \geq 2.5$ ms	–	–	50	V
I_P	quiescent current	$V_{sc} > 4$ V; note 2				
	$V_P = 12.4$ V		–	280	360	µA
	$V_P = 14.4$ V		–	290	–	µA
Schmitt triggers						
V_{P2} SCHMITT TRIGGER (FOR HOLD AND REGULATORS 1 AND 2)						
V_{thr}	rising voltage threshold		7.3	7.6	8.0	V
V_{thf}	falling voltage threshold		6.8	7.1	7.5	V
V_{hy}	hysteresis		–	0.5	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REGULATOR 1 SCHMITT TRIGGER (FOR HOLD)						
V_{thr}	rising voltage threshold		–	V_{R1} – 0.2	–	V
V_{thf}	falling voltage threshold		–	V_{R1} – 0.3	–	V
V_{hy}	hysteresis		–	0.1	–	V
REGULATOR 2 SCHMITT TRIGGER (FOR HOLD)						
V_{thr}	rising voltage threshold		–	V_{R2} – 0.2	–	V
V_{thf}	falling voltage threshold		–	V_{R2} – 0.3	–	V
V_{hy}	hysteresis		–	0.1	–	V
VBU SCHMITT TRIGGER (REGULATOR 3)						
V_{thr}	rising voltage threshold V_{bu}		7.3	7.9	8.4	V
V_{thf}	falling voltage threshold V_{REG3}		2.5	3	3.5	V
V_{hy}	hysteresis		–	4.9	–	V
State control pin						
V_{th}	voltage threshold between sleep and coma	note 2	–	V_{thr1} + 0.2	–	V
V_{thr1}	voltage threshold wake to sleep		3.35	3.6	3.85	V
V_{thf1}	voltage threshold sleep to wake		2.5	2.7	2.9	V
V_{hy1}	hysteresis wake/sleep		0.85	0.92	1.0	V
V_{thr2}	voltage threshold reset to wake		2.6	2.8	3.0	V
V_{thf2}]	voltage threshold wake to reset		1.75	1.9	2.05	V
V_{hy2}	hysteresis reset/wake		0.85	0.92	1.0	V
V_{thr3}	voltage threshold on to reset		1.85	2.0	2.15	V
V_{thf3}	voltage threshold reset to on		1.0	1.1	1.2	V
V_{hy3}	hysteresis on/reset		0.85	0.92	1.0	V
I_{scl}	input current	$V_{sc} \leq 0.8$ V $V_{sc} \geq 4$ V	– –	– –	–1 1	µA µA
Reset output						
V_{OL}	LOW level output voltage	$I_{OL} = 0$	0	0.2	0.8	V
V_{OH}	HIGH level output voltage		2.0	5.0	5.25	V
I_{OL}	LOW level output current	$V_{OL} \leq 0.8$ V	0.3	0.8	–	mA
I_{OH}	HIGH level output current	$V_{OH} > 3$ V	–0.3	–2.0	–	mA
Hold output						
V_{OL}	LOW level output voltage	$I_{OL} = 0$	0	0.2	0.8	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OH}	HIGH level output voltage		2.0	5.0	5.25	V
I_{OL}	LOW level output current	$V_{OL} \leq 0.8$ V; note 3	0.3	1.0	–	mA
I_{OH}	HIGH level output current	$V_{OH} > 3$ V	−1.5	−9.0	–	mA
Regulator 1 (I_{REG1} = 5 mA unless otherwise specified)						
V_{REG1}	output voltage off	$V_{sc} > 2.1$ V	–	1	400	mV
V_{REG1}	output voltage					
		$0.5\ V \leq I_{REG1} \leq 250$ mA	8.2	8.5	8.8	V
		$10\ V \leq V_P \leq 18$ V	8.2	8.5	8.8	V
ΔV_{REG1}	line regulation	$10\ V \leq V_P \leq 18$ V	–	–	50	mV
ΔV_{REGL1}	load regulation	$0.5\ mA \leq I_{REG1} \leq 250$ mA	–	–	50	mV
SVRR1	supply voltage ripple rejection	f = 200 Hz; 2 V (p-p)	60	–	–	dB
V_{REGd1}	drop-out voltage	I_{REG1} = 250 mA	–	–	0.4	V
I_{REGm1}	current limit	$V_{REG1} > 7$ V; note 4	0.4	–	1.2	A
I_{REGsc1}	short-circuit current	$R_L \leq 0.5\ \Omega$; note 4	–	250	–	mA
Regulator 2 (I_{REG2} = 10 mA unless otherwise specified)						
V_{REG2}	output voltage off	$V_{sc} > 2.1$ V	–	1	400	mV
V_{REG2}	output voltage					
		$0.5\ V \leq I_{REG2} \leq 140$ mA	4.8	5.0	5.2	V
		$8\ V \leq V_P \leq 18$ V	4.8	5.0	5.2	V
ΔV_{REG2}	line regulation	$8\ V \leq V_P \leq 18$ V	–	–	50	mV
ΔV_{REGL2}	load regulation	$0.5\ mA \leq I_{REG2} \leq 140$ mA	–	–	50	mV
SVRR2	supply voltage ripple rejection	f = 200 Hz; 2 V (p-p)	60	–	–	dB
V_{REGd2}	drop-out voltage	I_{REG2} = 140 mA	–	1.2	–	V
I_{REGm2}	current limit	$V_{REG2} > 4.5$ V; note 4	200	–	600	mA
I_{REGsc2}	short-circuit current	$R_L \leq 0.5\ \Omega$; note 4	–	130	–	mA
Regulator 3 (I_{REG3} = 5 mA unless otherwise specified)						
V_{REG3}	output voltage					
		$0.5\ mA \leq I_{REG3} \leq 50$ mA	4.8	5.0	5.2	V
		$7\ V \leq V_P \leq 18$ V	4.8	5.0	5.2	V
		$18 \leq V_P \leq 50$ V	4.8	5.0	5.2	V

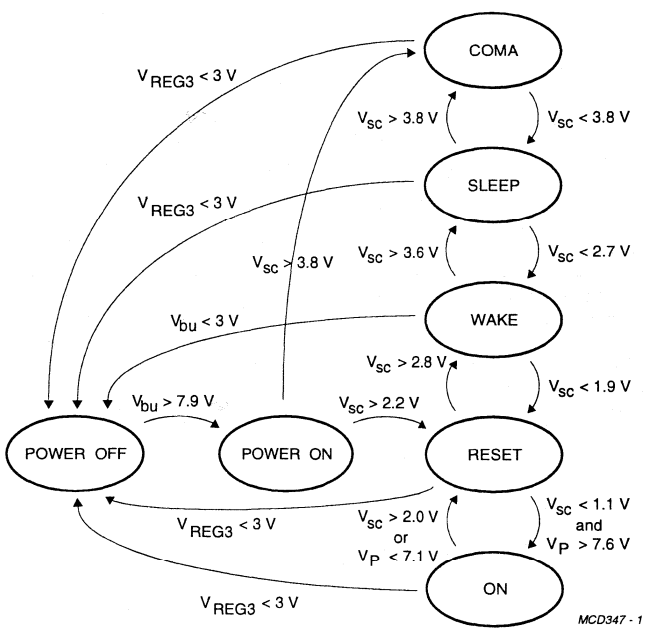
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔV_{REGL3}	output voltage	sleep mode; $I_{REG3} \leq 10$ mA; note 2	4.5	5.0	5.5	V
I_{LO1}	leakage output current	$V_P = 0$; $V_{bu} = 6$ V; $V_{REG3} = 6$ V	–	–	−1	μA
ΔV_{REG3}	line regulation	$7 \text{ V} \leq V_P \leq 18$ V	–	–	50	mV
ΔV_{REGL3}	load regulation	$0.5 \text{ mA} \leq I_{REG3} \leq 50$ mA	–	–	50	mV
SVRR3	supply voltage ripple rejection	f = 200 Hz; 2 V (p-p)	60	–	–	dB
V_{REGd3}	drop-out voltage	$I_{REG3} = 50$ mA; note 5	–	–	0.4	V
I_{REGm3}	current limit	$V_{REG3} > 4.5$ V; note 6	140	–	500	mA
Switch						
V_{swd}	drop-out voltage	$I_{sw} = 50$ mA	–	–	0.45	V
I_{swm}	maximum current		140	–	–	mA

Notes

1. Minimum operating voltage only if V_P has exceeded 8 V.
2. In the sleep mode, Regulators 1 and 2 are off. In the coma mode, the state control circuit is also switched off, to make the quiescent current as low as possible.
3. Hold circuit can sink this current in the RESET state and the ON state.
4. The foldback current protection limits the dissipated power at short-circuit (see Fig.5).
5. The drop-out voltage of Regulator 3 is measured between V_{bu} and V_{REG3} (pins 8 and 7).
6. At current limit, I_{REGm} is held constant (behaviour in accordance with the broken line in Fig.5)

Table 1 State control pin.

V_{P1} SCHMITT TRIGGER IS TRUE				
STATE	**REG3 (5 V)**	**REG1 + REG2**	**RESET**	**REMARKS**
Coma	LOW current	off	0	stabilizer consumes low quiescent current; state control circuit is switched off to lower the quiescent current
Sleep	LOW current	off	0	state control circuit on
Wake	HIGH current	off	0	CPU in sleep mode
Reset	HIGH current	off	1	CPU called up
On	HIGH current	on	1	normal operation
Power on	HIGH current	off	1	V_{P1} rises from 0 to 8.5 V or higher (first start-up)
Power off	off	off	0	V_{P2} falls from V_P to less than 3 V (V_{REG3} = 2.5 V)



V_{bu} = back-up voltage.
V_{sc} = state control voltage.
V_{REG3} = Regulator 3 output voltage.

Fig.3 State diagram.

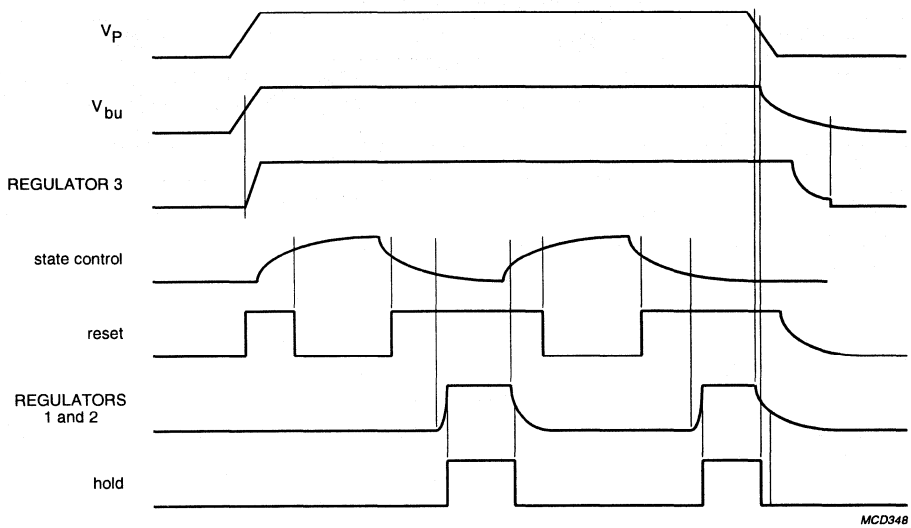


Fig.4 Timing diagram.

Table 2 Logic table HOLD function.

INPUTS FOR HOLD (note 1)					OUTPUT
V_{bu}	V_P SCHMITT TRIGGER	ON STATE	REG1	REG2	HOLD
1	0	X	0	0	0
0	1	X	0	0	0
1	1	0	0	0	0
1	1	1	0	X	0
1	1	1	X	0	0
1	1	1	1	1	1

Note

1. 0 = off; 1 = on; X = don't care.

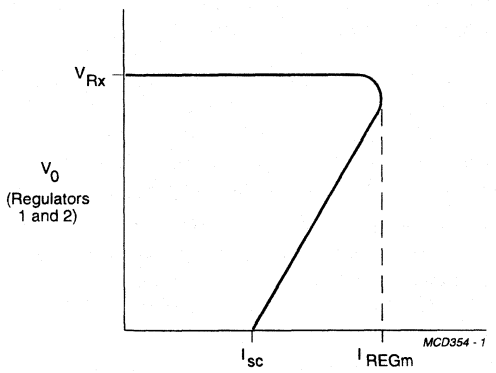


Fig.5 Foldback current protection.

QUALITY SPECIFICATION

Quality in accordance with UZW-BO/FQ-0601.

TEST INFORMATION

The outputs of the regulators are measured by means of a selector switch (one by one). In addition, switch SW2 is only closed when V_{bu} is greater than V_P; then the internal switch of the TDA3602 is opened. V_{bu} (pin 8) can only withstand a 50 V load dump pulse when switch SW2 is kept open or when switch SW2 is replaced by a 100 Ω resistor.

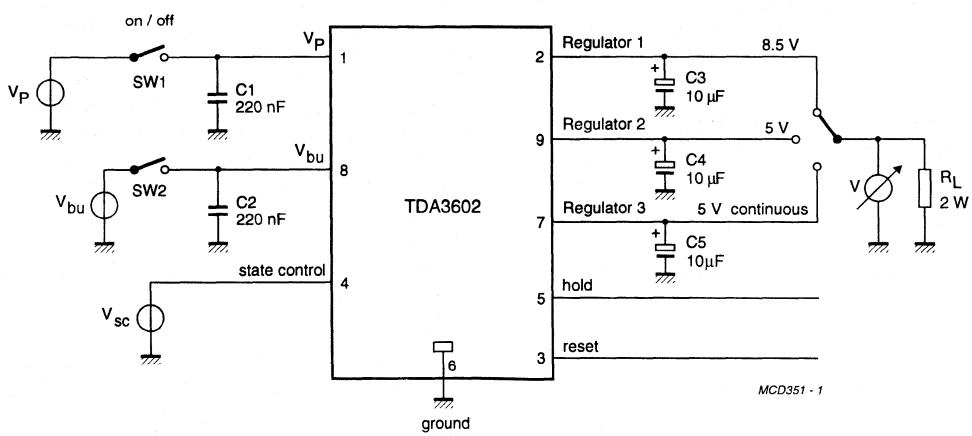


Fig.6 Test circuit.

APPLICATION INFORMATION

Noise

Table 3 Noise at regulator outputs dependent on capacitive load (C_L).

REGULATOR (note 1)		C_L		
REG	I_L	10 µF	47 µF	220 µF
1	150 mA	800 µV	220 µV	160 µV
2	100 mA	500 µV	115 µV	
3	50 mA	350 µV	190 µV	

Note

1. Regulators loaded with 100 mA; noise in µV RMS (B = 10 Hz to 1 MHz).

The available noise at the output of the regulators depends on the bandwidth of the regulators, which can be adjusted by means of the load capacitors. The noise figures are given in Table 3.

Although stability is guarenteed when C_L is higher than 10 µF (over temperature range) with tan (ϕ) = 1 in the frequency range 1 kHz to 20 kHz, it is recommended to use a 47 µF load capacitor for Regulators 1 and 2. When a microprocessor is supplied by Regulator 3 much noise can be produced by this microprocessor. This noise is not influenced by increasing the load capacitor of Regulator 3.

The noise on the supply line depends on the supply capacitor. When a high frequency capacitor of 220 nF with an electrolytic capacitor of 100 µF in parallel is placed directly over pin 1 (V_P) and pin 6 (ground) the noise is minimized.

The stabilizer is in 'power on' after the supply is reconnected ($V_{bu} > 7.9$ V) and $0.1 < V_{sc} < 2.2$ V.

Application circuits

STABILIZER WITHOUT MICROPROCESSOR 1

The low end application is illustrated in Fig.7. When switch SW1 is closed, a pulse is generated at the state control input by C5 and R1, and the regulator is switched from power off to the on mode (all three regulators are on). The HOLD signal can be used to control the mute signal for the power amplifiers. This signal is HIGH when all the regulators are in regulation and V_{P1} Schmitt trigger is true.

STABILIZER WITHOUT MICROPROCESSOR 2

Fig.8 illustrates the application circuit for a low end radio set with push switches when no microprocessor is used. The stabilizer can be switched to the on mode by pressing switch SW1. In this mode, Regulators 1 and 2 are switched on, so transistor T1 takes over from switch SW1. The stabilizer can only be switched off by connecting the base of T1 to ground (SW1 not pressed). This can be achieved by pressing switch SW2.

The hold signal is only HIGH when the device is in the on mode and both V_P and the regulators are available, so that this signal can be used to control the power stages (mute). During a fault condition, this signal turns LOW immediately.

When the stabilizer is connected to the supply for the first time, the initial state will be the power-on stage, so Regulators 1 and 2 are not switched on.

STABILIZER USED WITH MICROPROCESSOR

For a good understanding of the high end application, shown in Fig.10, consult the flow chart of Fig.9.

When the set is off, a reset can be generated by connecting the set to the supply for the first time (stabilizer in power-on), or by pressing any key on the key matrix (stabilizer in reset mode). When the reset is generated, the stabilizer is held in the reset mode for a short period by T1. The microprocessor has to take over control by making reset mode equal to 0. The microprocessor can then proceed with the initializing process. After this action, the microprocessor has to check if the correct key has been pressed. If so, the radio can be switched on by making on equal to 0; if not, the microprocessor must switch the device to the coma mode again, by making reset mode and on both equal to 1; (wake mode is entered after a short time constant, determined by R1 x C7 x constant), and switch itself to sleep mode.

When the reset is generated for the first time (power-on mode), the mode of the device can be detected by the hold signal. If on = 0 and hold remains LOW, then the microprocessor is in the power-on mode. In this event, the microprocessor must go to the switch-off routine (making on and reset mode both equal to 1).

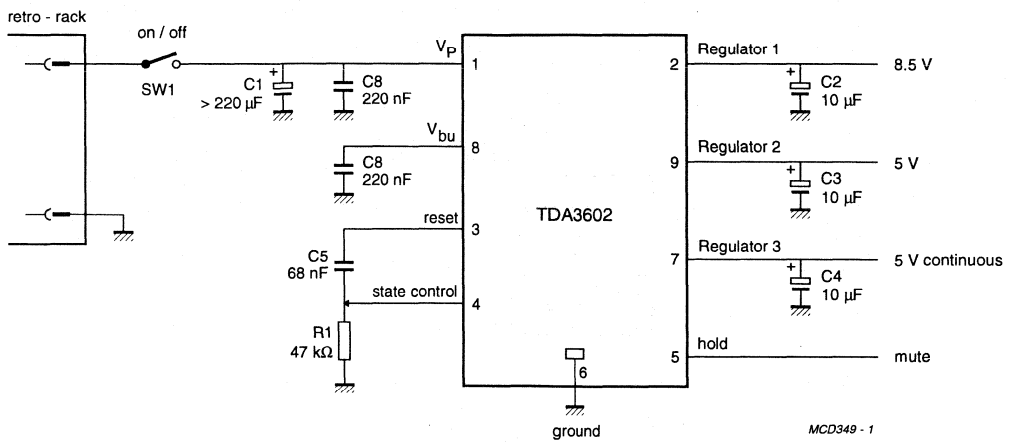


Fig.7 Low end application circuit.

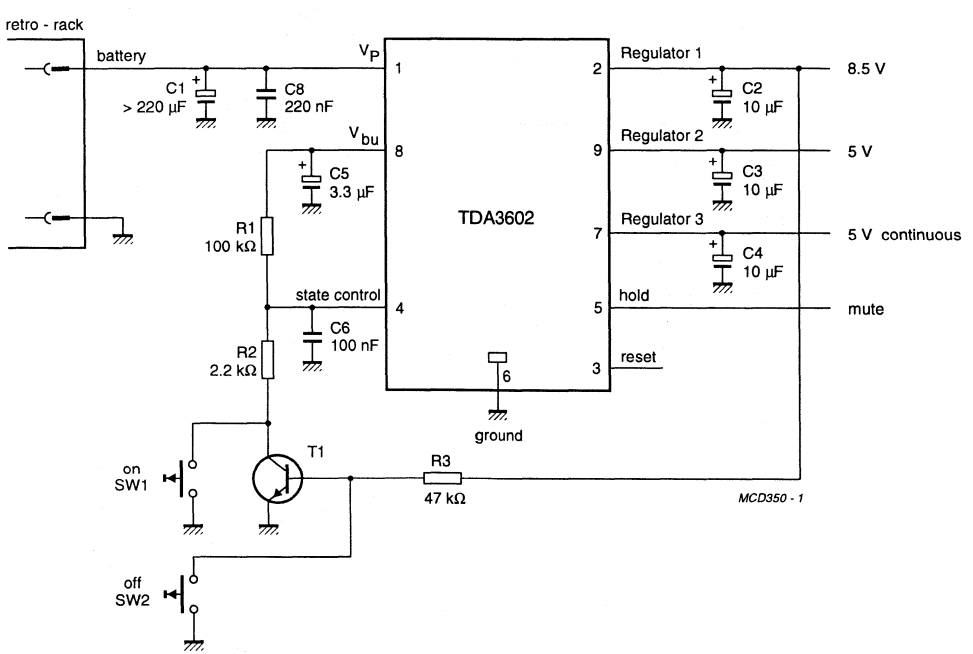


Fig.8 Application circuit 2.

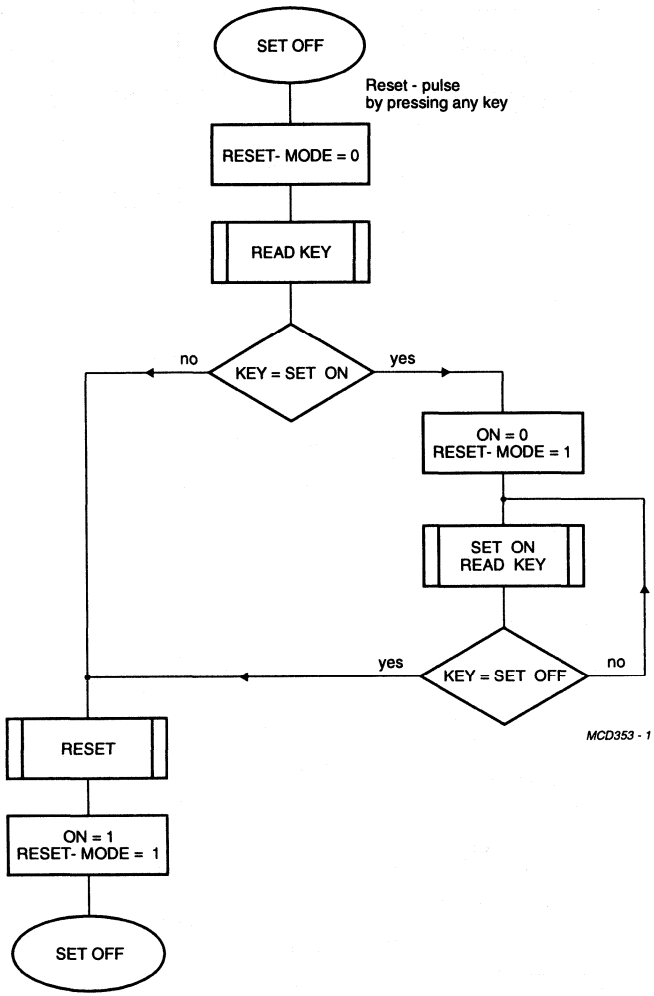


Fig.9 Flow chart for high end application.

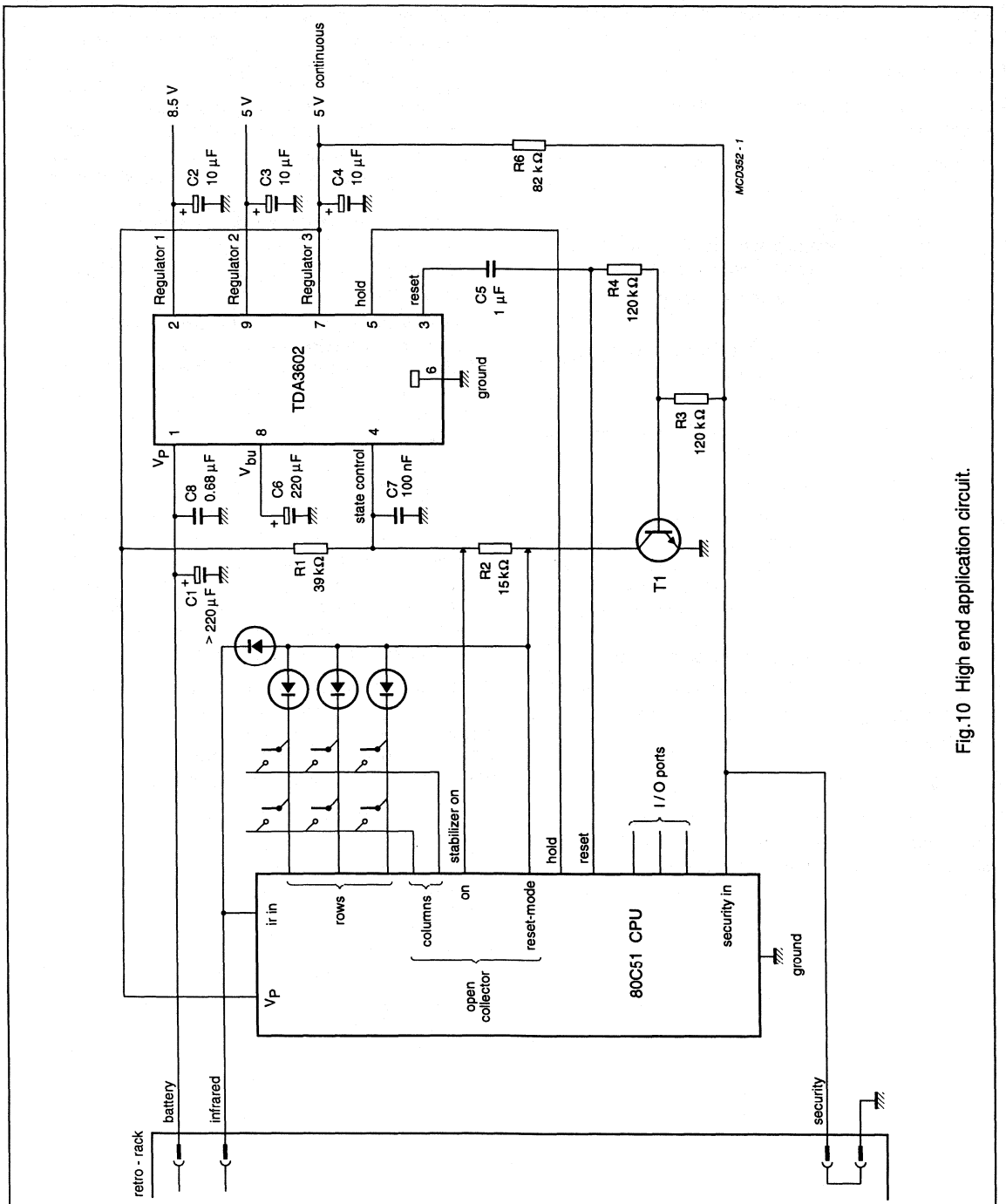


Fig.10 High end application circuit.

Example of a modern car radio design with the TDA3602

DESIGN CONSIDERATIONS

A modern car radio set meets the following design considerations:

1. Semi on/off logic. The radio set has to switch on/off by pressing the on/off key or by switching the ignition
2. Security code check
3. Low quiescent current in standby (this means that the microprocessor is off when the set is off)
4. The set must recover the state it had before an engine start or load dump
5. Apart from HOLD, RESET and V_P only two more I/O lines are used for full on/off logic
6. Supply by 1 or 2 supply lines
7. Radio Data System (RDS) should be implemented in the set, but this is not a regulator problem
8. Lights must switch off during load dump

Although the TDA3602 is designed only to be supplied by a continuous supply (battery), it is also possible to use both a continuous and a switchable supply (ignition). The ignition can be used to supply also the TDA3602, although in this event additional circuitry is needed.

APPLICATION CIRCUIT WITH (SEMI-)FULL ON/OFF LOGIC

The application circuit of Fig.11 will meet all the above mentioned design considerations. Three circuit parts can be distinguished:

Reset circuitry

A reset is required to call-up the microprocessor when it is switched to the sleep mode or the power-on reset (first initialization of the microprocessor). To achieve this, three different types of resets should be generated:

1. When the set has been disconnected from the supply, the microprocessor must be initialized at connection to the supply for the first time. The output ports of the microprocessor are in a random state. To ensure correct initialization, a reset has to be generated. This is accomplished by the power-on state of the TDA3602. In this state the reset output is HIGH and Regulators 1 and 2 are disabled (despite the voltage on the state control pin V_{sc} being below 1.1 V). Only after the voltage on the state control pin has risen above 2.2 V can Regulators 1 and 2 be switched on again by pulling the state control pin below 1.1 V.
2. In the sleep mode the microprocessor should be called up by pressing the on/off key (normal off condition). Now the reset is also generated by the RESET output of the TDA3602. This reset output will go HIGH when V_{sc} decreases from the value V_{REG3} to below 1.9 V.
3. At fault conditions (V_P below 7.1 V, $V_{REG1} < V_{REG1}$ nominal –0.3 V or $V_P > 1$ 8 V), HOLD drops to logic 0 and the microprocessor switches off the set. In accordance with the design considerations is that the mode of operation must switch to the state it was in before an engine start or load dump occurred. To achieve this the HOLD output of the TDA3602 can be used to generate a reset pulse (only when V_{sc} remains below 1.1 V).

The RESET and HOLD outputs of the TDA3602 are combined to generate the reset pulses. The pulses are created by differentiating the outputs, using capacitors C8 and C9. The reset pulses are added by means of the diodes D2 and D3. The time constants are:

- $tres_{res(rise)} = 3 \times R7 \times C8 = 3 \times 10\,k\Omega \times 1uF = 30$ ms

  on/off button S1 should be pressed for at least 30 ms, before the microprocessor will see this
- $tres_{hold(rise)} = 3 \times R7 \times C9 = 5.4$ ms
- $tres_{(die)} = 3 \times R8 \times C8 = 140$ ms
- $tres_{hold(disl)} = 3 \times R9 \times C9 = 25$ ms

  the microprocessor has to wait and check if HOLD remains LOW for at least 25 ms before it switches off; now it is certain that a correct reset will occur to wake up the microprocessor again.

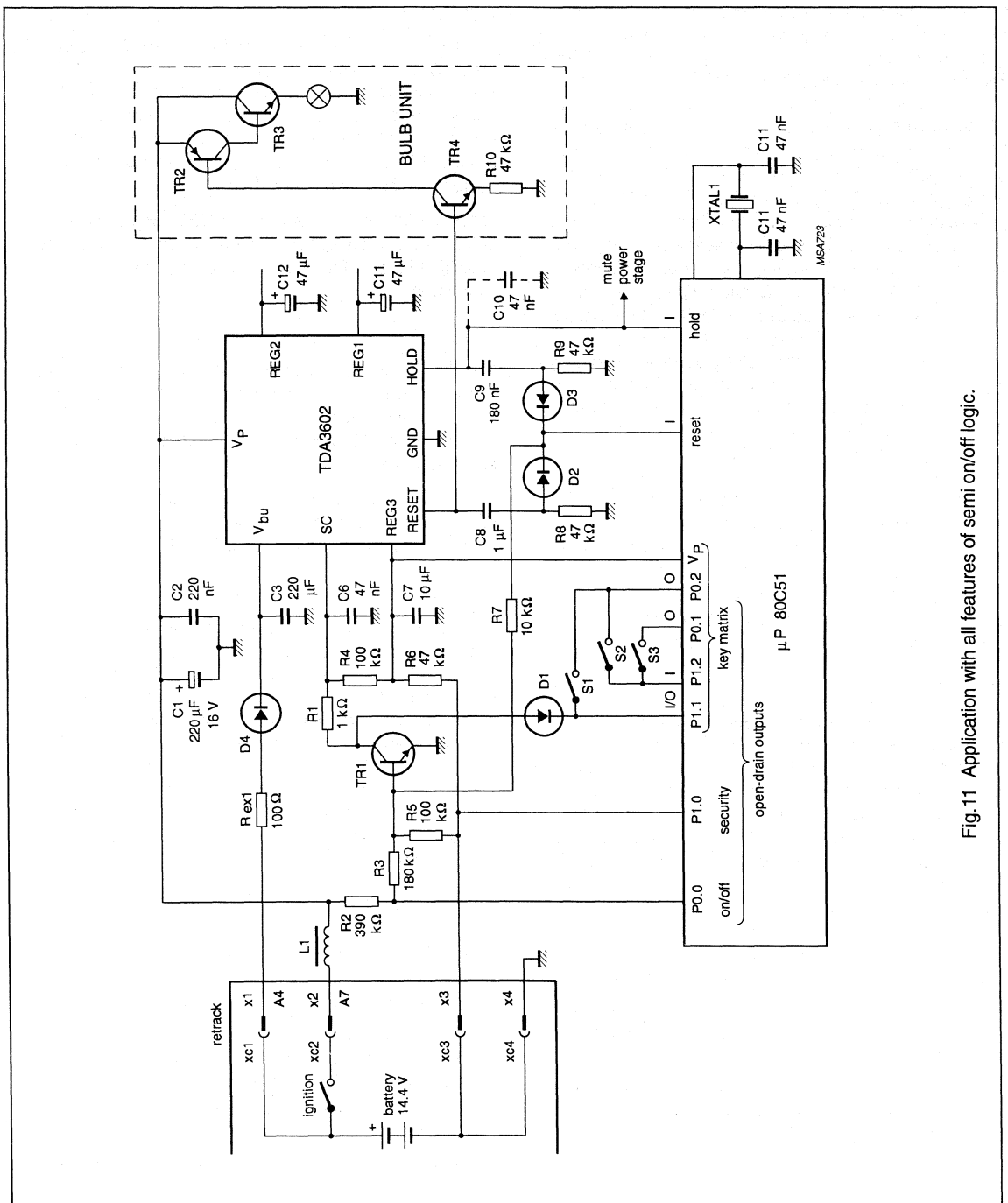


Fig.11 Application with all features of semi on/off logic.

A reset by the hold function can only be created when the state control pin remains LOW. This is accomplished by means of transistor T1 when Port P0,0 is high ohmic. Because of resistors R2, R3 and R5 the transistor will switch off when $V_{ignition}$ falls below a level of 5.0 V. During an engine start, when $V_{ignition}$ reaches voltages as low as 5 V, the transistor will switch off. Regulators 1 and 2 are already switched of by means of the V_P Schmitt-trigger, causing the HOLD output to go LOW. When $V_{ignition}$ again increases the transistor will be switched on again (Port P0,0 has to be open = logic 1), thereby switching the state control pin to 0 V. As $V_{ignition}$ continues to increase above 7.6 V (V_{rise} of the V_{P1} Schmitt-trigger) Regulators 1 and 2 will again switch on causing the HOLD output to go HIGH, creating a new reset pulse.
The set can also be switched off by opening the ignition key, causing transistor T1 to switch off. When the ignition key is closed again, the set will restart to the original situation that existed before the ignition key was opened. The charge time of C6 equals 3 x R4 x C6 = 14 ms. This is less than the reset time $tres_{res(rise)}$. To avoid the TDA3602 switching to coma mode before the microprocessor is awakened, a double function has been given to T1. During a reset pulse T1 is on (because of resistor R7), thus V_{sc} will remain 0 V provided a reset occurs. After the reset pulse has disappeared, the microprocessor is able to fully control V_{sc} by mean of Port P0,0 or Port P1,1.

Security code circuitry

When the set is off and it is pulled out of RETRACK, x3 and x4 are disconnected thereby switching the base of transistor T1 to the output voltage of Regulator 3 (using resistors R5 and R6). Transistor T1 is starting to conduct and a RESET pulse is generated. The microprocessor is activated and checks if Port P1,0 = logic 1. If this is so, the microprocessor knows that the set is pulled out of RETRACK and that time is limited to finish the program correctly (because the microprocessor is operating on the charge of capacitor C3). The security flag has to be set in an EEPROM and the microprocessor can switch to power-down before Regulator 3 switches to power-off.

Another possibility is that the set was running and pulled out of RETRACK. Now a hold is generated, and the hold interrupt routine has to check the security in Port P1,0.

R6 is an internal resistor in the microprocessor. An external resistor limits however the spread.

Bulb circuitry

The lights are switched on provided the RESET output of the TDA3602 is HIGH. This normally occurs when the set is switched on. Only at first connection (power-off) will the RESET output be HIGH when the set is off. In this event the lights are also switched on. This is not a problem because the required time for initializing the microprocessor will be very short.

When a load dump occurs, the RESET output will go LOW, disabling the lights. With the aid of this feature it is possible to prevent the light bulbs being damaged at load dump.

Noise.

Regulators 1 and 2 are loaded with a 47 µF/16 V load capacitor because of output noise. With this value the output noise will be lower than 220 µV for Regulator 1 and lower than 120 µV for Regulator 2 (see Table 3 and associated text).

To minimize the noise on the supply line, capacitors C1 and C2 should be placed as close as possible across the supply and ground pins of the TDA3602.

Timing diagram

In the timing diagram all of the situations which can occur are shown (see Fig.12). A HIGH of switch S1 indicates that S1 is pressed. A HIGH on Port P0,0 indicates that Port P0,0 is high ohmic (Port P0 is an open-collector output). If no open-collector output is available another port can be used, but an extra diode has to be added in series with this port to prevent T1 being switched on by this port. A HIGH for the microprocessor indicates that the microprocessor is operating, a LOW indicates that the microprocessor is in standby mode.

The following situations are covered in the timing diagram:

1. Initialization of the microprocessor (TDA3602 in power-off mode)
2. Switching the ignition with the set off (Port P0,0 = logic 0)
3. Switching the set on/off/on by pressing S1 sequentially (ignition available)
4. Switching behaviour at engine start and load dump (set on)
5. Switching the set off and on again by switching the ignition.

The timing diagram can only be understood after a thorough investigation of the flow charts (see section Flow chart semi on/off logic with security code). Furthermore short and long RESET pulses can be seen (see Fig.12).

Flowchart semi on/off logic with security code

This section describes the software for controlling the TDA3602 (semi on/off logic). A "o" in the flowchart flow diagram Fig.13, indicates that the port mentioned is switched as an output. A "1" indicates that the port mentioned is switched as an input (temporarily).

The flowchart of figure 13 can be used for semi on/off logic.

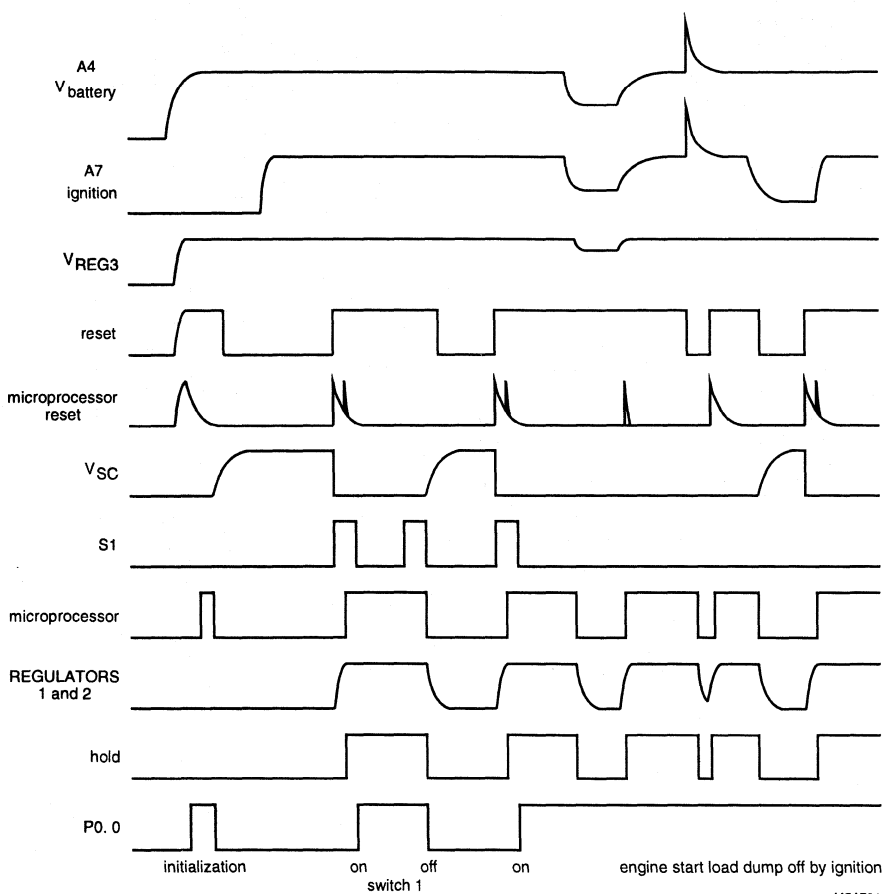


Fig.12 Timing of the applications.

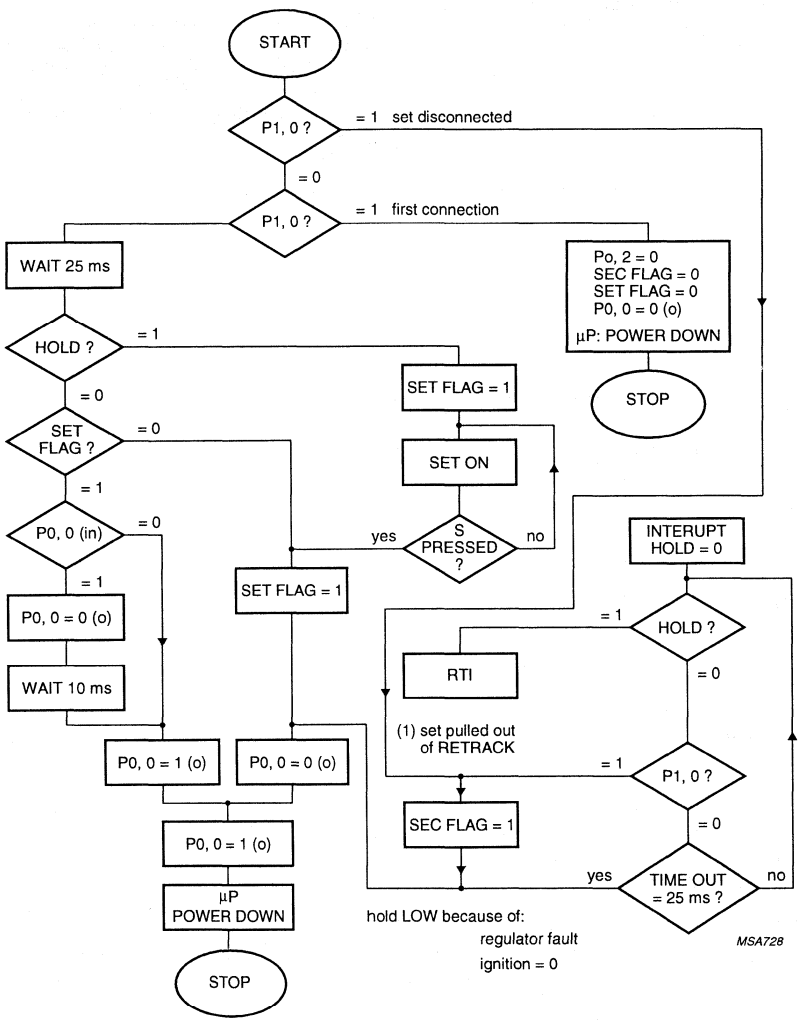


Fig.13 Interfacing flow chart TDA3602.

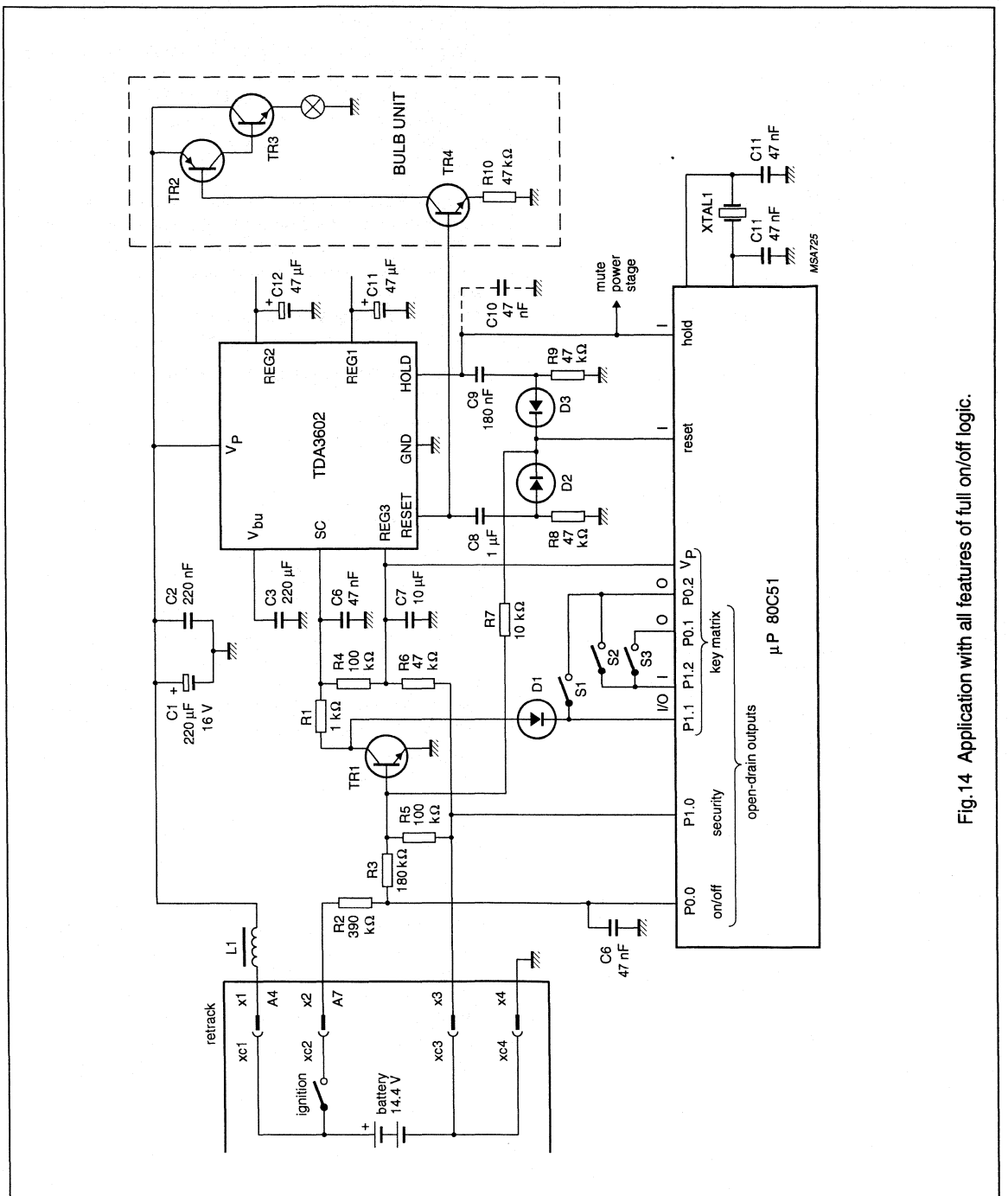


Fig.14 Application with all features of full on/off logic.

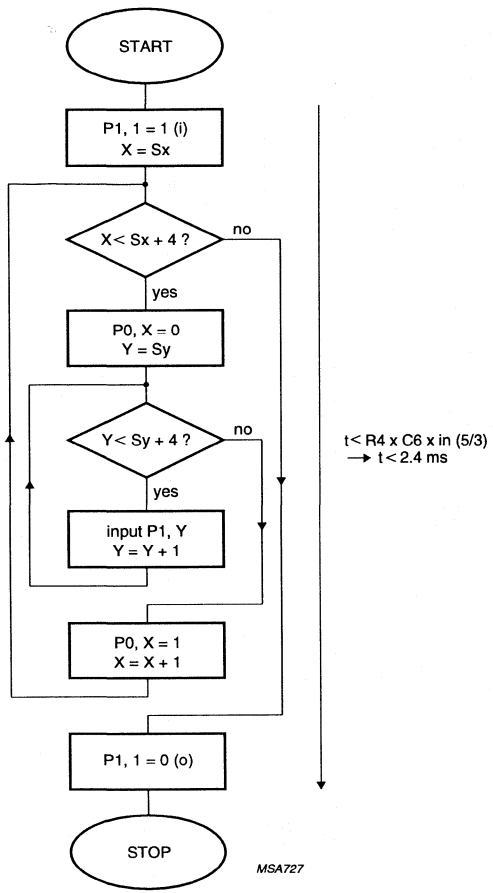


Fig.15 Software key matrix with loops.

FULL ON/OFF LOGIC

Using application circuit Fig.14, full on/off logic can be achieved. Also extra software loops are required to enable the set when ignition is off. The set can be controlled by Port P1,1 if the ignition is off (thus no extra I/O ports of the microprocessor are required for full on/off logic).

Because Port P1,1 is a part of the key matrix the complete key-scan loop must be finished within less than 0.5 x R4 x C6 = 2.4 ms, otherwise the TDA3602 will enter the reset state and Regulators 1 and 2 are switched off during this key-scan loop. When the time of the complete loop is within 2.4 ms the V_{sc} will remain below 2 V (thus Regulators 1 and 2 remain on).

It is also possible to switch Port P1,1 during the key-scan loop sequentially from output (logic 0) to input. If this is achieved within a time period of 1 ms, V_{sc} cannot become HIGH long enough to switch Regulators 1 and 2 off.

When ignition is available, transistor T1 overrules Port P1,1. In this event no variation on V_{sc} is seen during the key-scan loop.
The flow chart presented in Fig.15 is only required for the full on/off logic application of Fig.14.
The complete key-scan routine must be finished within 2.4 ms (when ignition is off) and that the key-scan routine has to end with a statement P1,1 = logic 0. In the flow chart of the key-scan routine, Sx is the start value of the rows and Sy the start value of the columns. With Sx = 1 and Sy = 1, one '0' is shifted on the output ports P0,1 to P0,5 and the input ports P1,1 to P1,5 are being read sequentially per shift action.

Connections between microprocessor and Regulator 2 supplied

When digital ICs, supplied by Regulator 2, are connected to I/O ports (especially Ports 1 and 2), special attention in the software has to be taken to avoid currents flowing from Regulator 3 to Regulator 2. Because of ESD diodes in digital ICs a current can flow from an output port (which is in a high state) through the ESD diode into Regulator 2. This will cause an increase in the quiescent current of the set. The recommended action to avoid this problem is to switch the specific I/O ports to logic 0.

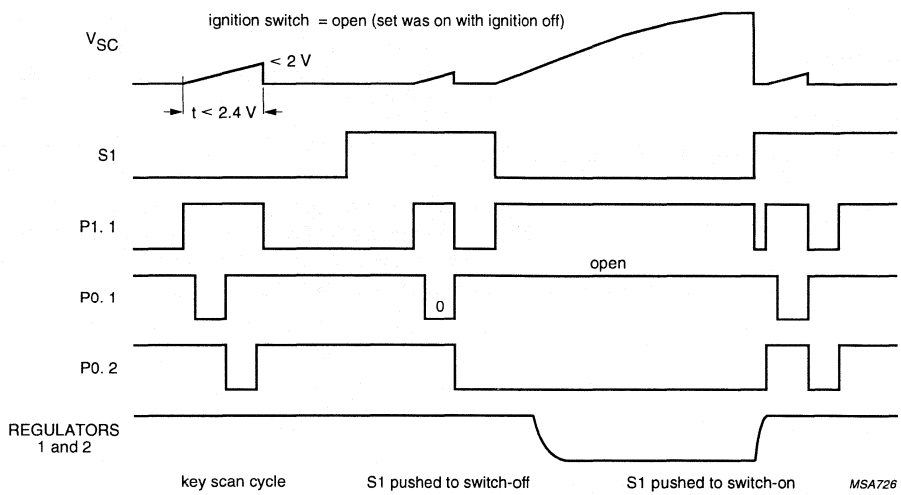


Fig.16 Timing key matrix.

Multiple voltage regulator with switch TDA3603

FEATURES

- One V_P state controlled regulator (regulator 2)
- Regulator 2, reset and ignition buffer operates during load dump and thermal shutdown
- One control pin for switching regulator 1 and the power switch
- Supply voltage range of −18 to +50 V (operating from 9.75 V)
- Low reverse current of regulator 2
- Low quiescent current (when regulator 1 is switched off, standby)
- Ignition input/output
- Reset output
- High ripple rejection
- Power switch.

PROTECTIONS

- Reverse polarity safe (down to −18 V without high reverse current)
- Able to withstand voltages up to 18 V at the outputs (supply line may be shortened)
- ESD protected on all pins
- Thermal protection
- Load dump protection
- Foldback current limit protection for regulators 1 and 2
- Delayed second current limit protection for the power switch
- The regulator outputs and the power switch are DC short-circuited safe to ground and V_P.

GENERAL DESCRIPTION

The TDA3603 is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller.

It contains one fixed voltage regulator with a foldback current protection (regulator 1) and one fixed voltage regulator (regulator 2), intended to supply a microcontroller, that also operates during load dump and thermal shutdown.

There is a power switch with protections, operated by the enable input.

The reset and ignition outputs can be used to interface by the microcontroller. The reset signal can be used to call up the microcontroller and the ignition output indicates ignition voltage available.

The supply pin can withstand load dump pulses and negative supply voltages.

Regulator 2 will be switched on at a supply voltage >6.5 V and off at a voltage of regulator 2 <1.9 V.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3603	SIL9MPF	plastic single in-line medium power package with fin; 9 leads	SOT110-1
TDA3603P	HDIP18	plastic heat-dissipating dual in-line package; 18 leads	SOT398-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage					
	operating		9.75	14.4	25	V
	regulator 2 on	note 1	2.4	14.4	25	V
	jump start	$t \leq 10$ minutes	–	–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	–	50	V
I_q	total quiescent current	standby mode	–	400	500	µA
T_{vj}	operating virtual junction temperature		–	–	150	°C
Voltage regulators						
V_{REG1}	output voltage regulator 1	$0.5\ mA \leq I_{REG1} \leq 300\ mA$	8.65	9.0	9.35	V
V_{REG2}	output voltage regulator 2	$0.5\ mA \leq I_{REG2} \leq 30\ mA$; $V_P = 14.4\ V$	4.8	5.0	5.2	V
$V_{drop(REG1)}$	drop-out voltage	$I_{REG1} = 0.3\ A$; note 2	–	–	0.5	V
Power switch						
$V_{drop(sw)}$	drop-out voltage	$I_{sw} = 0.3\ A$; note 3	–	–	0.9	V
I_M	peak current	$t \leq 10$ ms	1.4	–	–	A

Notes

1. Minimum operating voltage, only if V_P has exceeded 6.5 V.
2. The drop-out voltage of regulator 1 is measured between V_P and V_{REG1}.
3. The drop-out voltage of the power switch is measured between V_P and V_{sw}.

BLOCK DIAGRAM

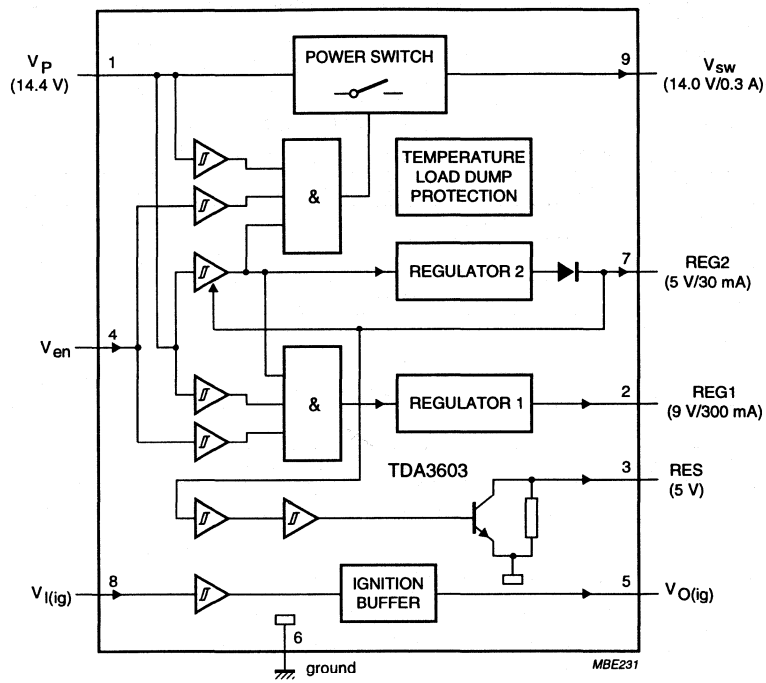


Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT110-1	SOT398-1	
V_P	1	1	supply voltage
REG1	2	2	regulator 1 output
RES	3	3	reset output voltage (+5 V)
V_{en}	4	4	enable input voltage
$V_{O(ig)}$	5	5	ignition output voltage
GND	6	6	ground (0 V)
REG2	7	7	regulator 2 output
$V_{I(ig)}$	8	8	ignition input voltage
V_{sw}	9	9	power switch output voltage
i.c.	–	10 to 18	can be connected to a heat spreader

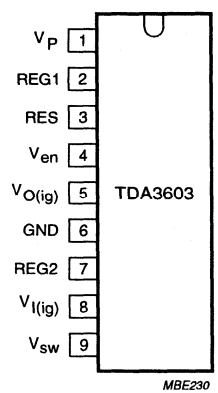
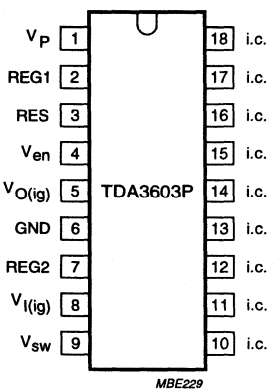


Fig.2 Pin configuration for SOT110-1.



Pins 10 to 18 can be connected to a heat spreader.

Fig.3 Pin configuration for SOT398-1.

FUNCTIONAL DESCRIPTION

The TDA3603 is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller. Because of low-voltage operation of the car radio, low-voltage drop regulators are used.

Regulator 2 will switch on when the supply voltage exceeds 6.5 V for the first time and will switch off again when the output voltage of regulator 2 is below 1.9 V (this is below an engine start). When regulator 2 is switched on and the output voltage of this regulator is within its voltage range, the reset output will be enabled (reset will go HIGH via a pull-up resistor) to generate a reset to the microcontroller. The reset cycles can be extended by an external capacitor at the reset output (pin 3). The start-up feature is built-in to ensure a smooth start-up of the microcontroller at first connection, without uncontrolled switching of regulator 2 during the start-up sequence.

When both regulator 2 and the supply voltage ($V_P > 4.5$ V) are available, regulator 1 and the switch can be operated by an enable input (pin 4).

All output pins are fully protected. The regulators are protected against load dump (regulator 1 will switch off at supply voltages higher than 25 V) and short-circuit (foldback current protection).
The switch contains a current protection which is delayed for ≥10 ms (in short-circuit condition). During this time the current is limited to 1.4 A ($V_P \leq 18$ V).

At supply voltages over 16.9 V the switch is clamped at 15.0 V (to avoid externally connected circuitry being damaged by an overvoltage) and the switch will switch off at load dump.

Interfacing with the microcontroller can be accomplished by an ignition Schmitt-trigger and ignition output buffer, (simple full/semi on/off logic applications).

The total timing of a semi on/off logic set is shown Fig.4.

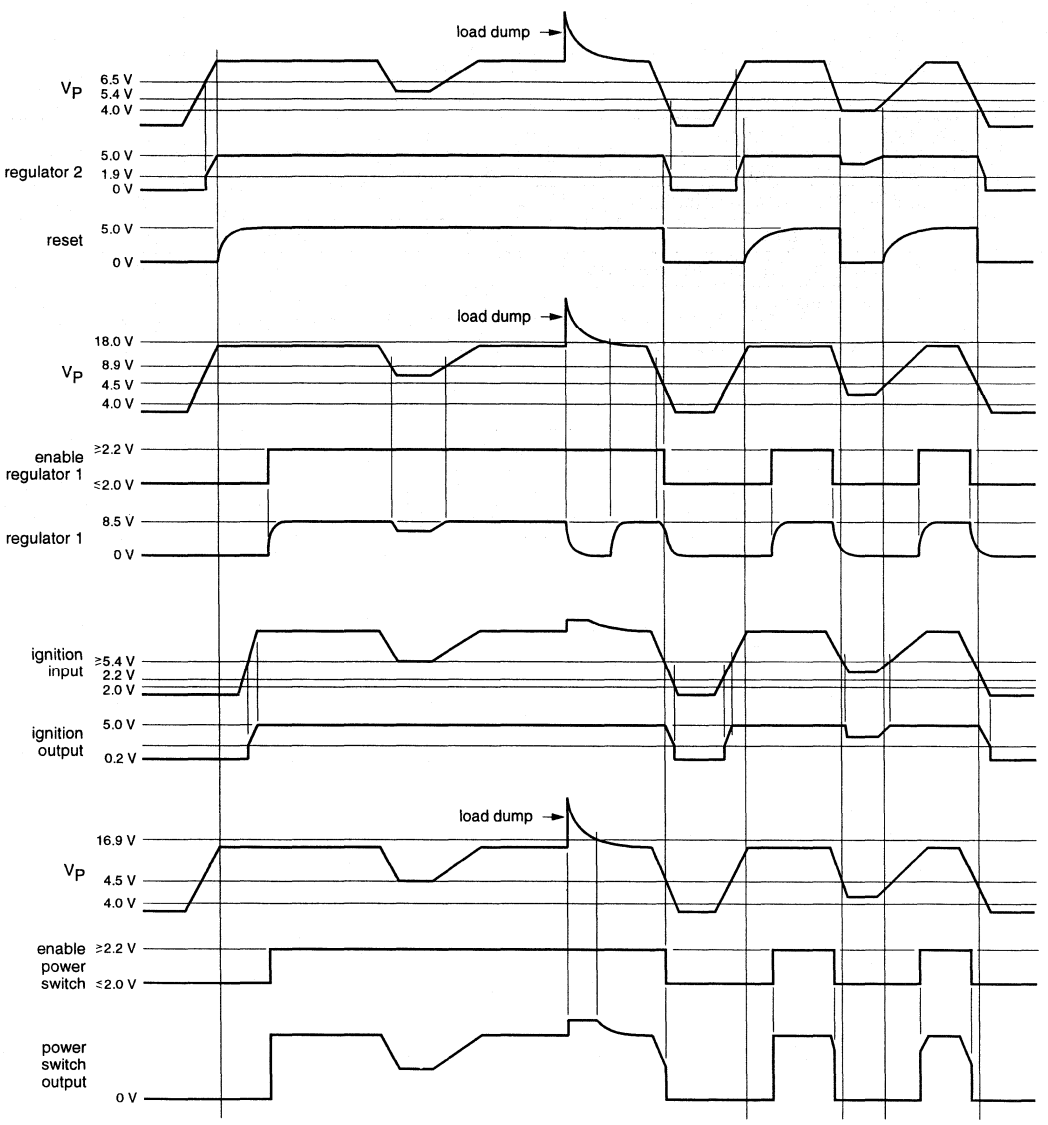


Fig.4 Timing diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage				
	operating		–	25	V
	jump start	$t \leq 10$ minutes	–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	50	V
V_P	reverse battery voltage	non-operating	–	–18	V
V_{ppi}	positive pulse voltage at ignition buffer	$V_P = 14.4$; $R_I = 1$ kΩ	–	50	V
V_{npi}	negative pulse voltage at ignition buffer	$V_P = 14.4$; $R_I = 1$ kΩ	–	–100	V
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{vj}	operating virtual junction temperature		–40	+150	°C
P_{tot}	total power dissipation	SOT110-1	–	10.4	W
		SOT398-1	–	tbf	W

THERMAL CHARACTERISTICS

SYMBOL	TYPE NUMBER	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	TDA3603	thermal resistance from junction to case	12	K/W
$R_{th\ j\text{-}p}$	TDA3603P	thermal resistance from junction to pins	15	K/W

CHARACTERISTICS

V_P = 14.4 V; Tamb = 25 °C; see Figs 5 and 6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage					
	operating		9.75	14.4	25	V
	regulator 2 on	note 1	2.4	14.4	25	V
	jump start	t ≤ 10 minutes	–	–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	–	50	V
I_q	quiescent current	V_P = 12.4 V; note 2	–	400	500	μA
		V_P = 14.4 V; note 2	–	420	–	μA
Schmitt-trigger power supply for the power switch						
V_{thr}	rising voltage threshold		4.0	4.5	5.0	V
V_{thf}	falling voltage threshold		3.5	4.0	4.5	V
V_{hys}	hysteresis		–	0.5	–	V
Schmitt-trigger power supply for regulator 1						
V_{thr}	rising voltage threshold		4.0	4.5	5.0	V
V_{thf}	falling voltage threshold		3.5	4.0	4.5	V
V_{hys}	hysteresis		–	0.5	–	V
Schmitt-trigger power supply for regulator 2						
V_{thr}	rising voltage threshold		6.0	6.5	7.1	V
V_{thf}	falling voltage threshold		1.7	1.9	2.2	V
V_{hys}	hysteresis		–	4.7	–	V
Schmitt-trigger for enable input						
V_{thr}	rising voltage threshold		1.7	2.2	2.7	V
V_{thf}	falling voltage threshold		1.5	2.0	2.5	V
V_{hys}	hysteresis		–	0.2	–	V
Schmitt-trigger for reset buffer						
$V_{r(REG2)}$	rising voltage of regulator 2	note 3	–	V_{REG2} – 0.15	–	V
$V_{f(REG2)}$	falling voltage of regulator 2	note 3	–	V_{REG2} – 0.25	–	V
V_{spread}	voltage spread on tracking	note 4	–	10	–	mV
Schmitt-trigger for ignition buffer						
V_{thr}	rising voltage threshold		1.7	2.2	2.7	V
V_{thf}	falling voltage threshold		1.5	2.0	2.5	V
V_{hys}	hysteresis		–	0.2	–	V
Reset buffer						
I_{sink}	LOW-level sink current	$V_{RES} \leq 0.8$ V	15	20	–	mA
I_{leak}	leakage current	V_P = 14.4 V; V_{RES} = 5 V	25	50	100	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ignition buffer						
V_{OL}	LOW-level output voltage	I_{OL} = 0 mA	0	0.2	0.8	V
V_{OH}	HIGH-level output voltage	note 5	–	5.0	5.2	V
I_{OL}	LOW-level output current	$V_{OL} \leq 0.8$ V	0.3	0.8	–	mA
I_{OH}	HIGH-level output current	$V_{OH} \geq 3$ V	0.3	2.0	–	mA
Regulator 1 (note 6)						
V_{REG1}	output voltage off		–	1	400	mV
V_{REG1}	output voltage	0.5 mA $\leq I_{REG1} \leq$ 300 mA	8.65	9.0	9.35	V
		10 V $\leq V_P \leq$ 18 V	8.65	9.0	9.35	V
ΔV_{REG1}	line regulation	10 V $\leq V_P \leq$ 18 V	–	–	50	mV
ΔV_{REGL1}	load regulation	0.5 mA $\leq I_{REG1} \leq$ 300 mA	–	–	70	mV
SVRR1	supply voltage ripple rejection	f_i = 200 Hz; V_I = 2 V (p-p)	60	–	–	dB
V_{REGd1}	drop-out voltage	I_{REG1} = 300 mA; note 7	–	0.4	0.5	V
I_{REGm1}	current limit	V_{REG1} > 7 V; note 8	0.45	-	1.2	A
I_{REGsc1}	short-circuit current	$R_L \leq 0.5\ \Omega$; note 9	50	300	–	mA
α_{ct}	cross talk	note 10	–	50	–	dB
Regulator 2 (note 11)						
V_{REG2}	output voltage	0.5 mA $\leq I_{REG2} \leq$ 30 mA	4.8	5.0	5.2	V
		7 V $\leq V_P \leq$ 18 V	4.8	5.0	5.2	V
		18 V $\leq V_P \leq$ 50 V	4.75	5.0	5.25	V
ΔV_{REG2}	line regulation	7 V $\leq V_P \leq$ 18 V	–	–	50	mV
ΔV_{REGL2}	load regulation	0.5 mA $\leq I_{REG1} \leq$ 30 mA	–	–	50	mV
SVRR2	supply voltage ripple rejection	f_i = 200 Hz; V_I = 2 V (p-p)	60	–	–	dB
V_{REGd2}	drop-out voltage	I_{REG2} = 30 mA; note 12	–	0.3	0.4	V
I_{REGm2}	current limit	V_{REG2} > 4.5 V; note 8	0.1	-	0.5	A
I_{REGsc2}	short-circuit current	$R_L \leq 0.5\ \Omega$; note 9	–	50	–	mA
α_{ct}	cross talk	note 13	–	50	–	dB
Power switch						
V_{swd}	drop-out voltage	I_{sw} = 0.3 A; note 14	–	0.4	0.9	V
I_{swcc}	continuous current		0.5	–	–	A
V_{swcl}	clamping voltage	$V_P \geq 16.9$ V	–	15.0	16.2	V
I_M	peak current	t ≤ 10 ms	1.4	–	–	A
V_{swfb}	fly back voltage behaviour	I_{sw} = –200 mA	–	–	20	V
$I_{lim(sw)}$	current limit	V_P = 14.4 V; V_{sw} = 10 V; note 8	0.6	–	1.0	A

Notes to the characteristics

1. Minimum operating voltage, only if V_P has exceeded 6.5 V.
2. Enable and ignition inputs are low and regulator 2 is unloaded.
3. Voltage drop due to load condition.
4. The spread on tracking is one sigma value.
5. Ignition output voltage will be less than or equal to the output voltage of regulator 2.
6. I_{REG1} = 5 mA.
7. The drop-out voltage of regulator 1 is measured between V_P and V_{REG1}.
8. At current limit, I_{REGm} is held constant (behaviour in accordance with the broken line in Fig.5).
9. The foldback current protection limits the dissipated power at short-circuit (see Figs 5 and 6).
10. The cross talk of regulator 1 is measured with an I_{REG2} = 0.5 mA up to 30 mA with an input frequency of f_i = 100 kHz.
11. I_{REG2} = 5 mA.
12. The drop-out voltage of regulator 2 is measured between V_P and V_{REG2}.
13. The cross talk of regulator 2 is measured with an I_{REG1} = 0.5 mA up to 100 mA with an input frequency of f_i = 100 kHz.
14. The drop-out voltage of the power switch is measured between V_P and V_{sw}.

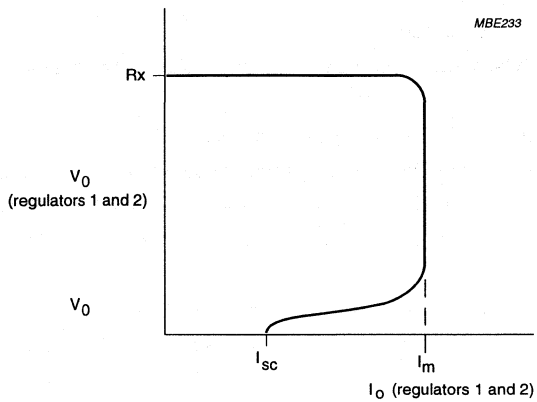


Fig.5 Foldback current protection of the regulators.

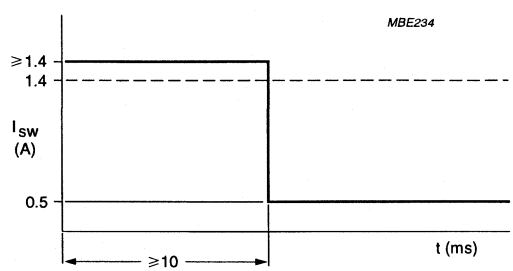
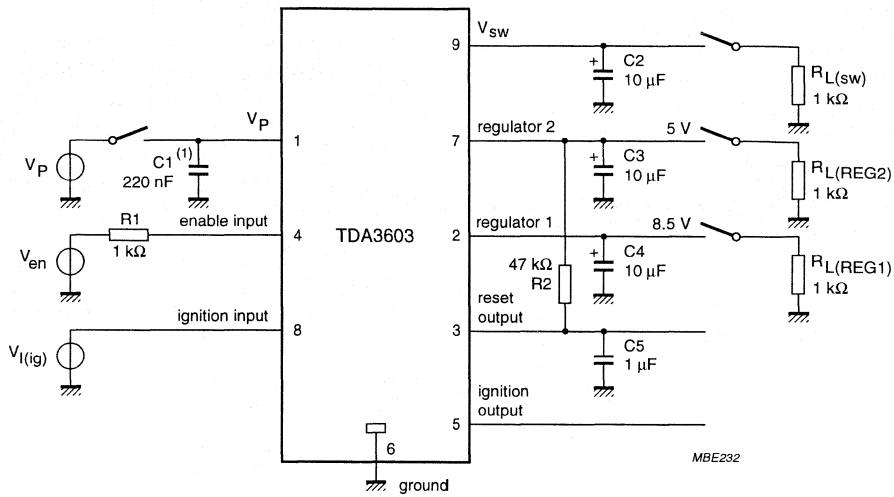


Fig.6 Foldback current protection of the power switch.

TEST AND APPLICATION INFORMATION



(1) Capacitor not required for stability.

Fig.7 Test circuit.

Noise information

The noise at the output of the regulators depends on the bandwidth of the regulators, which can be adjusted by the output capacitors. Table 1 shows the noise figures.

Although stability is guaranteed when C_L is higher than 10 µF (over temperature range) with tan (ϕ) = 1 in the frequency range 1 to 10 kHz, however, for low noise, a 47 µF load capacitor is required.

The noise on the supply line depends on the value of the supply capacitor and is caused by a current noise (output noise of the regulators is translated into a current noise by the output capacitors). When a high frequency capacitor of 220 nF with an electrolytic capacitor of 100 µF in parallel is placed directly over pins 1 and 6 (supply and ground) the noise is minimized.

Table 1 Noise figures

REGULATOR	NOISE (µV)(1)	OUTPUT CAPACITOR (µF)
1	tbf	10
	150	47
	tbf	100
	tbf	220
2	tbf	10
	100	47
	tbf	100
	tbf	220

Note

1. Bandwidth of 100 kHz.

Multiple voltage regulator with external reset delay and switch

TDA3604

FEATURES

- One V_P state controlled regulator (regulator 2)
- Regulator 2, reset and ignition buffer operates during load dump and thermal shutdown
- Separate control pins for switching regulator 1 and the power switch
- Supply voltage range of –18 to 50 V (operating from 9.75 V)
- Low reverse current of regulator 2
- Low quiescent current (when regulator 1 is switched off, standby)
- Ignition input/output
- Reset output
- Reset delay time adjustable
- High ripple rejection
- Power switch
- Separate supply for the power switch.

PROTECTIONS

- Reverse polarity safe (down to –18 V without high reverse current)
- Able to withstand voltages up to 18 V at the outputs (supply line may be shortened)
- ESD protected on all pins
- Thermal protection
- Load dump protection
- Foldback current limit protection for regulators 1 and 2
- Delayed second current limit protection for the power-switch
- The regulator outputs and the power switch are DC short-circuited safe to ground and V_P.

GENERAL DESCRIPTION

The TDA3604 is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller.

It contains one fixed voltage regulator with a foldback current protection (regulator 1) and one fixed voltage regulator (regulator 2), intended to supply a microcontroller, that also operates during load dump and thermal shutdown.

There is a power switch with protections, operated by an enable input.

The reset and ignition outputs can be used to interface by the microcontroller. The reset-signal can be used to call up the microcontroller and the ignition output indicates ignition voltage available.

Both supply pins can withstand load dump pulses and negative supply voltages.

Regulator 2 will be switched on at a supply voltage >6.5 V and off at a voltage of regulator 2 <1.9 V.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3604	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage					
	operating		9.75	14.4	25	V
	regulator 2 on	note 1	2.4	14.4	25	V
	jump start	$t \leq 10$ minutes	–	–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	–	50	V
I_q	total quiescent current	standby mode	–	400	500	µA
T_{vj}	operating virtual junction temperature		–	–	150	°C
Voltage regulators						
V_{REG1}	output voltage regulator 1	$0.5\ mA \leq I_{REG1} \leq 300\ mA$	8.65	9.0	9.35	V
V_{REG2}	output voltage regulator 2	$0.5\ mA \leq I_{REG2} \leq 30\ mA$; $V_P = 14.4\ V$	4.8	5.0	5.2	V
$V_{drop(REG1)}$	drop-out voltage	$I_{REG1} = 0.3\ A$; note 2	–	–	0.5	V
Power switch						
$V_{drop(sw)}$	drop-out voltage	$I_{sw} = 0.5\ A$; note 3	–	–	1.4	V
I_M	peak current	$t \leq 10$ ms	1.4	–	–	A

Notes

1. Minimum operating voltage, only if V_P has exceeded 6.5 V.
2. The drop-out voltage of regulator 1 is measured between V_P and $V_{REG\ 1}$.
3. The drop-out voltage of the power switch is measured between V_P and V_{sw}.

BLOCK DIAGRAM

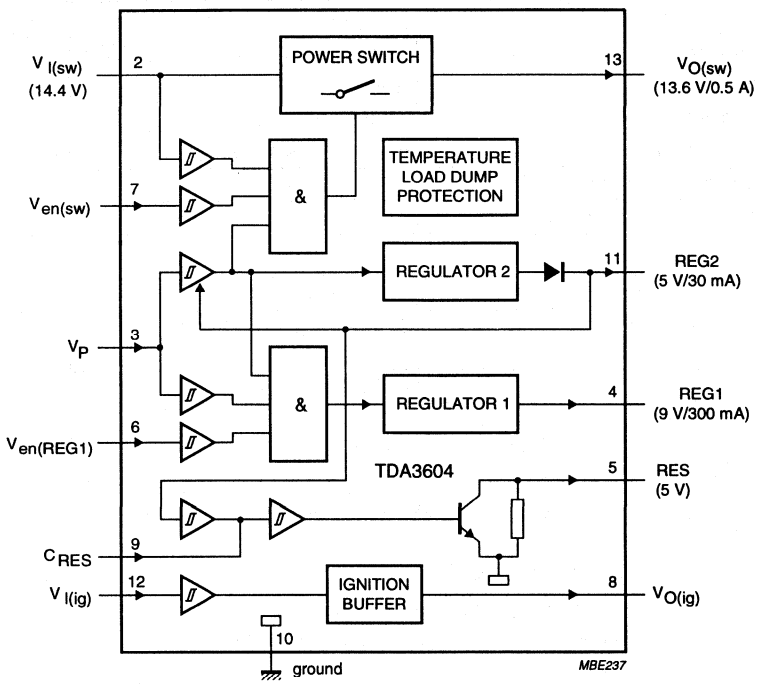


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
$V_{I(sw)}$	2	power switch input voltage
V_P	3	supply voltage
REG1	4	regulator 1 output
RES	5	reset output voltage (+5 V)
$V_{en(REG1)}$	6	regulator 1 enable input
$V_{en(sw)}$	7	power switch enable input voltage
$V_{O(ig)}$	8	ignition output voltage
C_{RES}	9	reset capacitor
GND	10	ground (0 V)
REG2	11	regulator 2 output
$V_{I(ig)}$	12	ignition input voltage
$V_{O(sw)}$	13	power switch output voltage

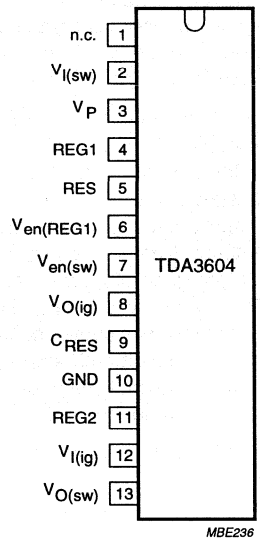


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA3604 is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller. Because of low-voltage operation of the car radio, low-voltage drop regulators are used.

Regulator 2 will switch on when the supply voltage exceeds 6.5 V for the first time and will switch off again when the output voltage of regulator 2 is below 1.9 V (this is below an engine start). When regulator 2 is switched on and the output voltage of this regulator is within its voltage range, the reset output will be enabled (reset will go HIGH via a pull-up resistor) to generate a reset to the microcontroller. The reset cycles can be extended by an external capacitor at pin 9). The above mentioned start-up feature is built in to secure a smooth start-up of the microcontroller at first connection, without uncontrolled switching of regulator 2 during the start-up sequence.

When both regulator 2 and the supply voltage ($V_P > 4.5$ V) are available, regulator 1 and the switch can be operated by enable inputs (pins 6 and 7 respectively).

All output pins are fully protected. The regulators are protected against load dump (regulator 1 will switch off at supply voltages higher than 25 V and short-circuit (foldback current protection).
The switch contains a current protection which is delayed for ≥10 ms (in short-circuit condition). During this time the current is limited to 1.4 A ($V_P \leq 18$ V).

At supply voltages over 16.9 V the switch is clamped at 15.0 V (to avoid externally connected circuitry being damaged by an overvoltage) and the switch will switch off at load dump.

Interfacing with the microcontroller can be accomplished by an ignition Schmitt-trigger and ignition output buffer, (simple full/semi on/off logic applications).

The total timing of a semi on/off logic set is shown Fig.3.

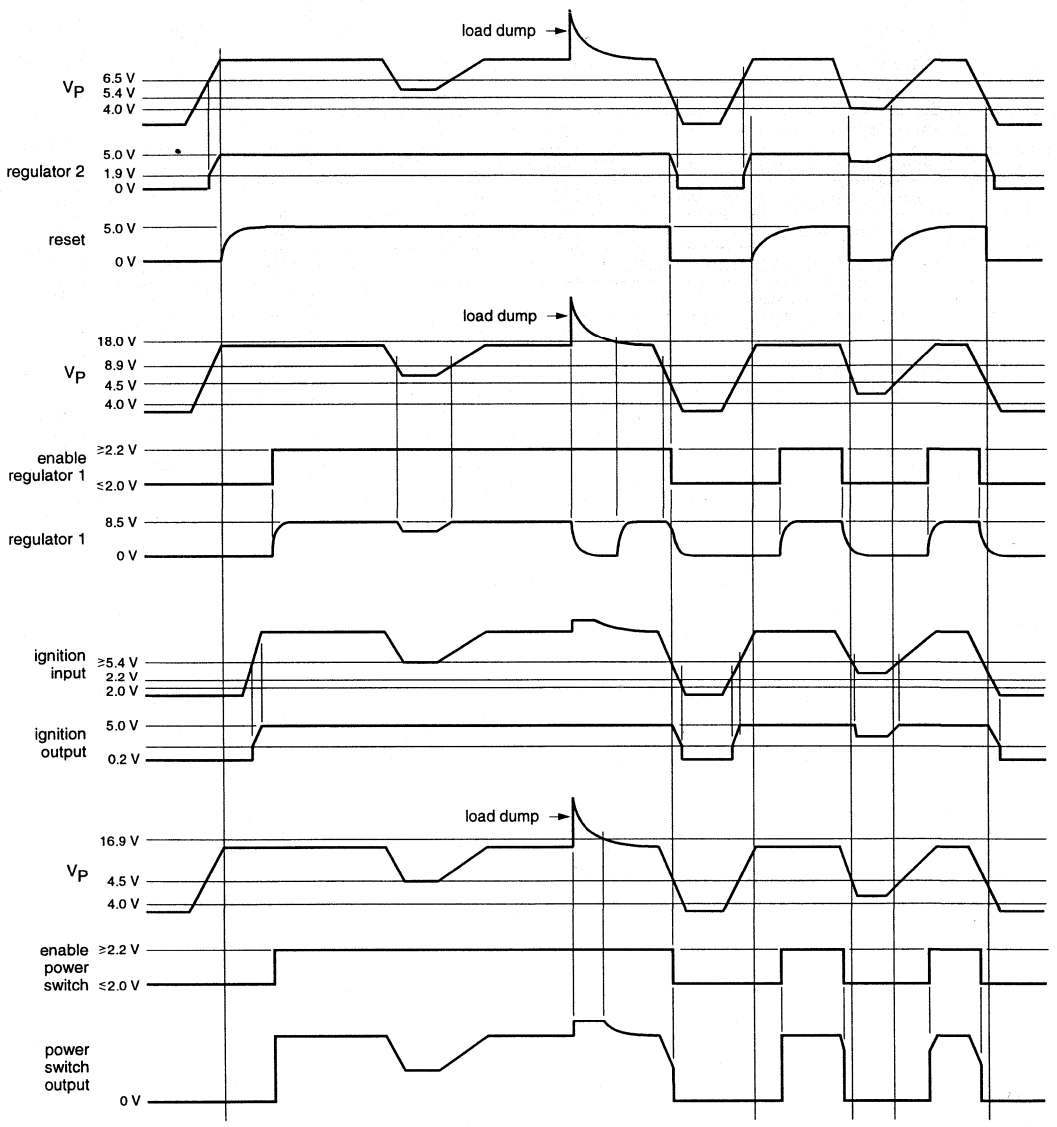


Fig.3 Timing diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage				
	operating		–	25	V
	jump start	$t \leq 10$ minutes	–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	50	V
V_P	reverse battery voltage	non-operating	–	–18	V
V_{ppi}	positive pulse voltage at ignition buffer	$V_P = 14.4$; $R_I = 1$ kΩ	–	50	V
V_{npi}	negative pulse voltage at ignition buffer	$V_P = 14.4$; $R_I = 1$ kΩ	–	–100	V
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{vj}	operating virtual junction temperature		–40	+150	°C
P_{tot}	total power dissipation		–	15.6	W

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	8	K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	50	K/W

CHARACTERISTICS

$V_P = V_{Psw} =$ 14.4 V; T_{amb} = 25 °C; see test Figs. 4 and 5 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage					
	operating		9.75	14.4	25	V
	Regulator 2 on	note 1	2.4	14.4	25	V
	jump start	t ≤10 minutes	–	–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	–	50	V
I_q	quiescent current	V_P = 12.4 V; note 2	–	400	500	µA
		V_P = 14.4 V; note 2	–	420	–	µA
Schmitt-trigger power supply for the power switch						
V_{thr}	rising voltage threshold		4.0	4.5	5.0	V
V_{thf}	falling voltage threshold		3.5	4.0	4.5	V
V_{hys}	hysteresis		–	0.5	–	V
Schmitt-trigger power supply for regulator 1						
V_{thr}	rising voltage threshold		4.0	4.5	5.0	V
V_{thf}	falling voltage threshold		3.5	4.0	4.5	V
V_{hys}	hysteresis		–	0.5	–	V
Schmitt-trigger power supply for regulator 2						
V_{thr}	rising voltage threshold		6.0	6.5	7.1	V
V_{thf}	falling voltage threshold		1.7	1.9	2.2	V
V_{hys}	hysteresis		–	4.7	–	V
Schmitt-trigger for enable input						
V_{thr}	rising voltage threshold		1.7	2.2	2.7	V
V_{thf}	falling voltage threshold		1.5	2.0	2.5	V
V_{hys}	hysteresis		–	0.2	–	V
Schmitt-trigger for reset buffer						
$V_{r(REG2)}$	rising voltage of regulator 2	note 3	–	$V_{REG2} - 0.15$	–	V
$V_{f(REG2)}$	falling voltage of regulator 2	note 3	–	$V_{REG2} - 0.25$	–	V
V_{spread}	voltage spread on tracking	note 4	–	10	–	mV
Schmitt-trigger for ignition buffer						
V_{thr}	rising voltage threshold		1.7	2.2	2.7	V
V_{thf}	falling voltage threshold		1.5	2.0	2.5	V
V_{hys}	hysteresis		–	0.2	–	V
Reset buffer						
I_{sink}	LOW-level sink current	$V_{RES} \leq 0.8$ V	15	20	–	mA
I_{leak}	leakage current	V_P = 14.4 V; V_{RES} = 5 V	25	50	100	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ignition buffer						
V_{OL}	LOW-level output voltage	I_{OL} = 0 mA	0	0.2	0.8	V
V_{OH}	HIGH-level output voltage	note 5	–	5.0	5.2	V
I_{OL}	LOW-level output current	$V_{OL} \leq 0.8$ V	0.3	0.8	–	mA
I_{OH}	HIGH-level output current	$V_{OH} \geq 3$ V	0.3	2.0	–	mA
Regulator 1 (note 6)						
V_{REG1}	output voltage off		–	1	400	mV
V_{REG1}	output voltage	0.5 mA $\leq I_{REG1} \leq$ 300 mA	8.65	9.0	9.35	V
		10 V $\leq V_P \leq$ 18 V	8.65	9.0	9.35	V
ΔV_{REG1}	line regulation	10 V $\leq V_P \leq$ 18 V	–	–	50	mV
ΔV_{REGL1}	load regulation	0.5 mA $\leq I_{REG1} \leq$ 300 mA	–	–	70	mV
SVRR1	supply voltage ripple rejection	f_i = 200 Hz; V_I = 2 V (p-p)	60	–	–	dB
V_{REGd1}	drop-out voltage	I_{REG1} = 300 mA; note 7	–	0.4	0.5	V
I_{REGm1}	current limit	V_{REG1} > 7 V; note 8	0.45	–	1.2	A
I_{REGsc1}	short-circuit current	$R_L \leq 0.5\ \Omega$; note 9	50	300	–	mA
α_{ct}	cross talk	note 10	–	50	–	dB
Regulator 2 (note 11)						
V_{REG2}	output voltage	0.5 mA $\leq I_{REG2} \leq$ 30 mA	4.8	5.0	5.2	V
		7 V $\leq V_P \leq$ 18 V	4.8	5.0	5.2	V
		18 V $\leq V_P \leq$ 50 V	4.75	5.0	5.25	V
ΔV_{REG2}	line regulation	7 V $\leq V_P \leq$ 18 V	–	–	50	mV
ΔV_{REGL2}	load regulation	0.5 mA $\leq I_{REG1} \leq$ 30 mA	–	–	50	mV
SVRR2	supply voltage ripple rejection	f_i = 200 Hz; V_I = 2 V (p-p)	60	–	–	dB
V_{REGd2}	drop-out voltage	I_{REG2} = 30 mA; note 12	–	0.3	0.4	V
I_{REGm2}	current limit	V_{REG2} > 4.5 V; note 8	0.1	–	0.5	A
I_{REGsc2}	short-circuit current	$R_L \leq 0.5\ \Omega$; note 9	–	50	–	mA
α_{ct}	cross talk	note 13	–	50	–	dB
Power switch						
V_{swd}	drop-out voltage	I_{sw} = 0.4 A; note 14	–	0.8	1.4	V
I_{swcc}	continuous current		0.5	–	–	A
V_{swcl}	clamping voltage	$V_P \geq 16.9$ V	–	15.0	16.2	V
I_M	peak current	$t \leq 10$ ms	1.4	–	–	A
V_{swfb}	fly back voltage behaviour	I_{sw} = –200 mA	–	–	20	V
$I_{lim(sw)}$	current limit	V_P = 14.4 V; V_{sw} = 10 V; note 8	0.6	–	1.0	A
Reset delay						
I_O	output current		–	3	–	µA
V_{thr}	rising voltage threshold		2.7	3.0	3.3	V
t_d	delay time	C_I = 47 nF; note 15	25	50	100	ms

Notes to the characteristics

1. Minimum operating voltage, only if V_P has exceeded 6.5 V.
2. Enable inputs of regulator 1, ignition and switch are low. Regulator 2 is unloaded.
3. Voltage drop due to load condition.
4. The spread on tracking is one sigma value.
5. Ignition output voltage will be less than or equal to the output voltage of regulator 2.
6. I_{REG1} = 5 mA.
7. The drop-out voltage of regulator 1 is measured between V_P and V_{REG1}.
8. At current limit, I_{REGm} is held constant (behaviour in accordance with the broken line in Fig. 4.
9. The foldback current protection limits the dissipated power at short circuit (see Figs 4 and 5).
10. The cross talk of regulator 1 is measured with an I_{REG2} = 0.5 mA up to 30 mA with an input frequency of f_i = 100 kHz.
11. I_{REG2} = 5 mA.
12. The drop-out voltage of regulator 2 is measured between V_P and V_{REG2}.
13. The cross talk of regulator 2 is measured with an I_{REG1} = 0.5 mA up to 100 mA with an input frequency of f_i = 100 kHz.
14. The drop-out voltage of the power switch is measured between V_P and V_{sw}.
15. The delay time depends on the value of the capacitor

$$t_d = \frac{C}{I} \times V_{thrC} = C \times 2.5 \times 10^6$$

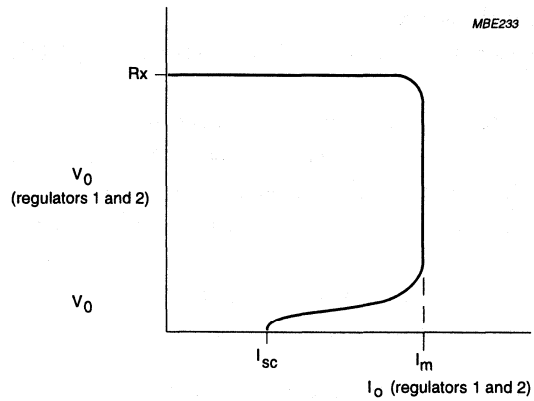


Fig.4 Foldback current protection of the regulators.

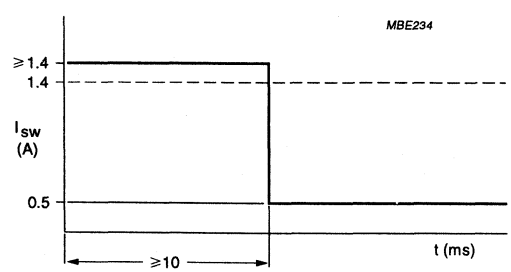
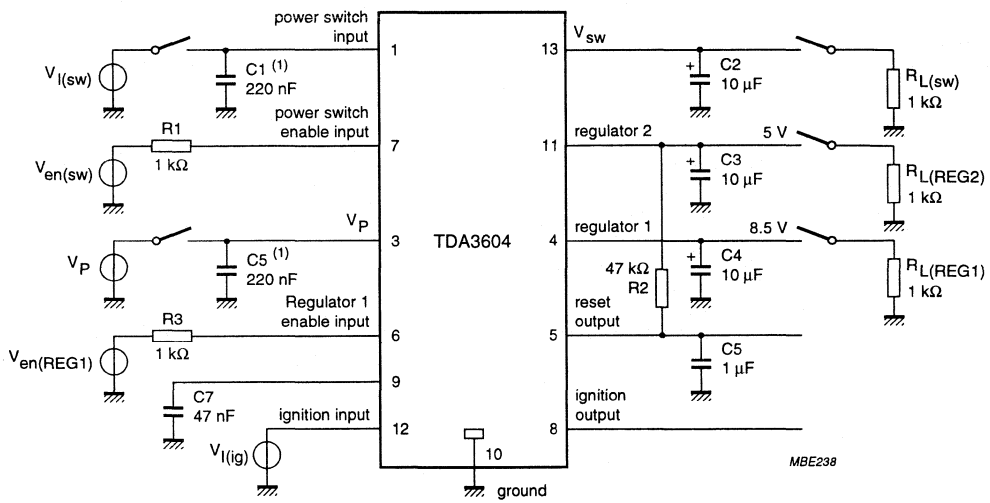


Fig.5 Foldback current protection of the power switch.

TEST AND APPLICATION INFORMATION



(1) Capacitor not required for stability.

Fig.6 Test circuit.

Noise information

The noise at the output of the regulators depends on the bandwidth of the regulators, which can be adjusted by the output capacitors. Table 1 shows the noise figures.

Although stability is guaranteed when C_L is higher than 10 µF (over temperature range) with tan (ϕ) = 1 in the frequency range 1 to 10 kHz, however, for low noise, a 47 µF load capacitor is required.

The noise on the supply line depends on the value of the supply capacitor and is caused by a current noise (output noise of the regulators is translated into a current noise by the output capacitors). When a high frequency capacitor of 220 nF with an electrolytic capacitor of 100 µF in parallel is placed directly over pins 3 and 10 (supply and ground) the noise is minimized.

Table 1 Noise figures

REGULATOR	NOISE (µV)(1)	OUTPUT CAPACITOR (µF)
1	tbf	10
	150	47
	tbf	100
	tbf	220
2	tbf	10
	100	47
	tbf	100
	tbf	220

Note

1. Bandwidth of 100 kHz.

CAR STEREO KITS

CCR520S V1.5

Application report ERA/AN93008

This Outline Specification is valid for CCR520S software release V1.5 masked in P83CE528EFB/002.

Modifications with respect to the application note "Outline Specification of Computer Controlled Car Radio System CCR520S", report number ERA/AN93001 :

1. Security Code programming mode included.
2. Pin option test (OPTROW) moved from pin 25 to pin 40.
3. Method of source switching factory selectable by means of an option diode.

CCR520S V1.5

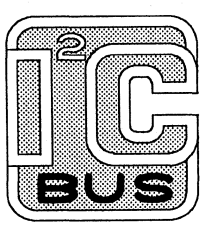
Application report
ERA/AN93008

SUMMARY:

CCR520 is a computer controlled high-end AM/FM car radio system with RDS decoding. It is based on a single 8051 family microcontroller (P83CE528) and various I²C-bus controlled peripherals.

The system contains functions such as PLL tuning, IF control, stereo decoding, RDS+EON decoding, IAC, sound switching, sound fader control, LCD display, cassette interface, external audio input jack and a detachable front.

Radio control and RDS+EON processing are combined in a single microcontroller.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

TABLE OF CONTENTS:

LIST OF FIGURES

1 INTRODUCTION.

CCR520 is a computer controlled high-end AM/FM car radio system with RDS (Radio Data System), EON (Enhanced Other Network information) and I²C-bus controlled radio ICs. CCR520S is the controlling microprocessor. It is based on the 8051 family microcontroller P83CE528 and takes care of all radio control functions as well as RDS and EON decoding.

Features:

- Digital PLL tuning for FM, MW and LW bands, (factory selectable FM only/LW disable).
- Manual Tuning.
- Search Tuning and Local/DX handling.
- Frequency Scan (Continuous Search, pausing 6 seconds on every station).
- Automatic Store Tuning (AST).
- Search for Traffic Programmes (TP) or specific Program Types (PTY).
- Presets: 6 in each of the bands: FM1, FM2, FM-AST, MW, MW-AST, LW.
- RDS functions:
  - PS — Programme Service name.
  - PI — Programme Identification code.
  - AF — Alternative Frequency List / Automatic Following.
  - TP / TA — Traffic Programme / Traffic Announcement.
  - PTY — Programme TYpe selection and display.
  - EON — Enhanced Other Networks information.
- Sound control: volume, bass, treble, balance, fader, loudness and mute via I²C-bus or potentiometers.
- Non Volatile Memory for last sound control settings, last band, last frequency for each band, Presets, PS names (RDS), AF lists (RDS), etc.
- 120 or 144 segment LCD display (I²C bus controlled) displaying:
  - system status (band / frequency / preset number / modes).
  - RDS Programme Service name (PS).
  - RDS Programme Type (PTY).
  - Sound control settings (Bass, Treble, Balance, Fader).
- Security code:
  - enable/disable by the user.
  - preprogrammable in the factory by means of a service mode.
- Power stabilizer control.
- User control up to 27 keys with either a fixed keyboard, a keyboard on a detachable front or a combination of both.
- User programmable customization options.
- Cassette Interface including ME/CR, Dolby and AMS control.
- Input jack for external audio source (e.g. CD player).

2 BLOCK DIAGRAM OF THE SYSTEM.

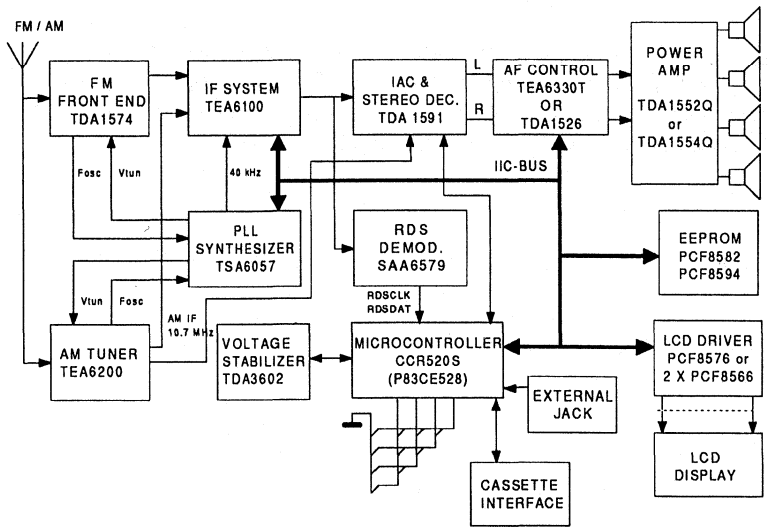


Figure 1 Block diagram of CCR520 with fixed keyboard

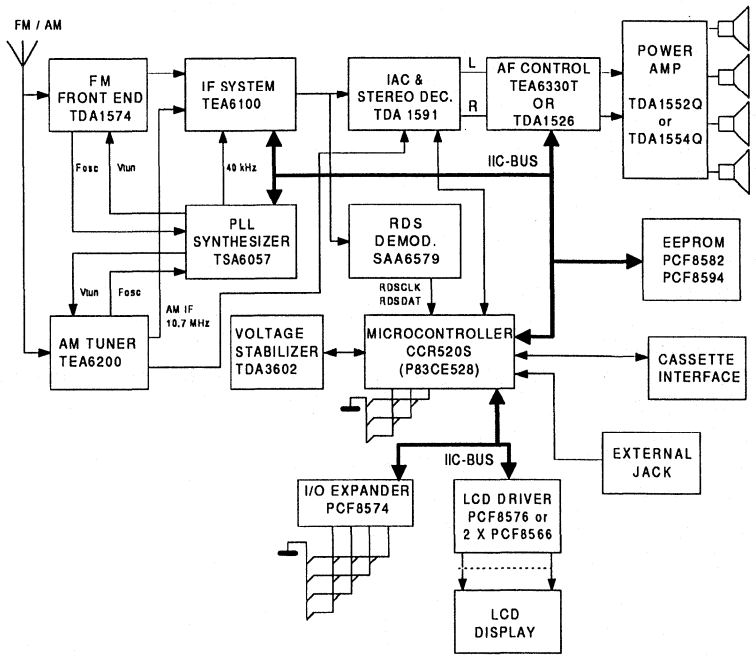


Figure 2 Block diagram of CCR520 with detachable keyboard

3 I.C. DESCRIPTION.

- TDA1574;T — Performs all the FM front-end functions, except the R.F. pre-amplifier stage. Incorporates an FM/IF pre-amplifier.

- TEA6200 — AM tuner, up-conversion system. Does not need an aerial tuned circuit. I.F. frequency 10.7 MHz. No alignments needed.

- TEA6100 — Integrated FM/IF system including a digital AM/FM tuning interface for microcomputer controlled radios with an I^2C-bus.

- TSA6057;T — PLL synthesizer with separate prescalers for AM and FM and loop filter outputs. I^2C-bus controlled.

- TDA1591;T — System combination of adjustment free PLL stereo decoder with de-emphasis control and an Interference Absorption Circuit (IAC) with low component count. Specially designed for car radios.

- TEA6330T or
- TDA1526 — I^2C-bus (TEA6330) or potentiometer (TDA1526) controlled AF pre-amplifier in SO package for car and home receivers. Includes volume, balance, bass, treble, fader (TEA6330) control and mute (TEA6330).

- CCR520S — The microcontroller, based on a P83CE528EFB. It is a 8051 derivative with an 8-bit CPU, 32 Kbytes ROM, 512 bytes RAM and four 8-bits I/O ports in a 44-pin QFP package.

- TDA3602 — Supply voltage stabilizer in SIL package with three output voltages (2 x 5V and 8.5V). Two outputs are switchable by external controls.

- TDA1552Q
  TDA1554Q — Class-B audio power amplifiers in SIL plastic package with 4 identical amplifiers. The TDA1552Q can deliver 2 x 22 W in BTL configuration, the TDA1554Q can deliver either 4 x 11 W or 2 X 22 W.

- SAA6579;T — RDS demodulator with onboard 57 kHz bandpass filter and a digital demodulator. Outputs a digital data signal and a clock signal for further processing.

- PCF8566T
  PCF8576T — LCD display drivers that interface to almost any liquid crystal display (LCD) having low multiplex rates. They generate the drive signals for any static or multiplexed LCD with up to four backplanes and up to 24 (PCF8566) or 40 (PCF8676) segment lines and can easily be cascaded for larger LCD applications. I^2C-bus controlled.

- PCF8582/94E-2P/T
  256/512 byte 5V electrically erasable programmable read only memories (EEPROM) that can be 100,000 times re-written.

4 SPECIFICATION OF THE SYSTEM.

Tuning:

- Frequency bands:

FM:	87.50	-	108.00	MHz	(50 kHz steps)
MW:	522	-	1611	kHz	(1 kHz steps)
LW:	144	-	288	kHz	(1 kHz steps)

- PLL tuning principle

- Manual tuning up / down
  Initially slow / fine grid. After 2.5 sec. fast / coarse grid.

- Local/DX switching. The Local/DX feature controls the search sensitivity. If the tuner has an input attenuator, the Local/DX switch controls the attenuator during search. If not, it controls the signal level threshold during search. Default after switching on is always DX mode.

- Search tuning up / down
  Sensitivity is controlled by Local/DX. If after one complete band sweep in local mode no station is found, the radio switches automatically to DX. Automatic muting and display of running frequency.

- Frequency Scan
  Continuous automatic search tuning, pausing for 6 seconds on every station.

- AST (Automatic Store Tuning) for FM and MW band.
  AST switches to FM-AST or MW-AST band, searches for the 6 strongest transmitters and stores them in the AST programme preset memory. In FM, duplication of PI codes will be avoided.

- Programme preset memory
  For each band (FM1, FM2, MW, LW, AST-FM and AST-MW) 6 programme presets and a "manual" frequency are stored. In FM, additional RDS information is stored: PI code (Programme Identification), AF list (Alternative Frequencies) and AF follow mode on/off.
  After band switching, the radio reverts to the latest frequency used in the new band (Either preset or a manually tuned frequency).

- Programme preset up / down control
  Programme presets can be recalled/stored by two key control (up and down) or by 6 separate preset keys.

- AF follow mode.
  If AF follow mode is on, the set will regularly measure the signal strength on alternative frequencies and compare it with the current station. If an alternative frequency offers better quality, the radio will switch over, and update the alternative frequency list. The measuring scheme is designed to cause minimum noticeable disturbance for the listener. The interval time between two measurements depends on the signal quality.

- Intelligent preset programme recall.
  If an FM programme preset with a known PI code is recalled, the primary frequency and all alternative frequencies stored in the programme preset memory are examined. The frequency with the highest signal strength that broadcasts the correct PI code will be selected. Only when the programme is not found on one of the AFs, a search is started after 6 seconds for a station with the proper PI code.

- TA mode
  In TA mode the radio only searches for transmitters that transmit the RDS traffic programme on the same station or linked via EON.
  The radio will automatically start a search when switching TA mode on and the current station is not a traffic station.

- PTY mode
  In PTY mode the radio only searches for transmitters that transmit the user-selected PTY code.
  The radio will automatically start a search when switching PTY mode on and the current station transmits no or the wrong PTY code.

- Last status memory: band, frequency, PI code, AF follow mode on/off status and TA mode on/off status are stored in memory. This status is recalled during switch on.

RDS:

- Bit, block and group synchronisation

- Data decoding and collection of:
  - PI, Programme Identification code
  - AF, Alternative Frequencies
  - TP, Traffic Programme
  - TA, Traffic Announcement
  - PS, Programme Service name
  - PTY, Programme TYpe
  - EON, Enhanced Other Networks information.

- AF follow mode using PI and AF (see also Tuning)

- Display of the programme service name in 8 alpha-numeric characters (PS name)

- Display of TP status

- Display of PTY status

- EON functions:
  - Switches temporarily to an other station if EON information indicates a traffic announcement on that other network.
  - Updates lists of alternative frequencies of other stations stored in preset memory with information received via the EON data.

- Break-in of traffic announcements and PTY alarm messages when the radio is muted or in cassette / external mode.

Detachable front:

- Optionally, the keyboard and the LCD display unit can be placed on a detachable front controlled by a 2nd I^2C bus. Only 5 contacts are required to connect the detachable front (6 if it hosts also the power key). No extra hardware is required to detect its presence.

Control:

- Up to 27 local control keys on either a fixed, a detachable keyboard or a combination.
  Triangular matrix using 7 lines.

Display:

- 120 Segment LCD or 144 Segment LCD with Umlaut (ü) and Accent (á) characters, 1:3 multiplexed.

- 8 Alphanumeric characters + decimal point are used for display of:
  - Band and frequency (Example: "FM 103.50")
  - Indication "BALANCE", "FADER", "TREBLE", "BASS" and their position (either analog bar or digital).
  - The entered security code
  - RDS programme service name (PS) in 8 alphanumeric characters.
  - RDS programme type (PTY):
    "NEWS", "AFFAIRS", "INFO", "SPORT", "EDUCATE", "DRAMA", "CULTURE", "SCIENCE", "VARIED", "POP M", "ROCK M", "M.O.R. M", "LIGHT M", "CLASSICS", "OTHER M", "ALARM"
  - "MUTE", in case the user mutes the radio, cassette or external
  - Cassette mode function such as "PLAY ->", "CAS WIND", etc.

- 7 Segment display for the current programme preset number.

- 8 Icons for display of:
  - STEREO — On when stereo pilot signal is detected, off when forced mono is selected.
  - AST — On when AST band selected, flashes when AST search/programming is busy.
  - AF — On when AF follow mode is enabled (see also Tuning). Flashes if no RDS data received.
  - TA — On in TA mode and flashing during a traffic announcement in progress.
  - TP — On when a traffic station is received, flashing when the station is is not a traffic station in TA mode.
  - PTY — On when PTY mode enabled, flashing when no or the wrong PTY code is received.
  - DOLBY ▯▯ — On in cassette mode when dolby selected.
  - ME/CR — On in cassette mode when ME/CR selected.

Non Volatile Memory:

Either 256 or 512 bytes. The amount of memory determines the maximum number of alternative frequencies to be stored per preset (5/9 AF's for 256/512 bytes EEPROM).

The next information is stored in NVM:

- System status e.g.: band, audio source (radio / cassette / external), selected PTY code.
- For each band (FM1, FM2, FM-AST, MW, MW-AST, LW): six preset frequencies and one non-preset frequency, last used preset.
- For each stored FM frequency:
  - PI-code;
  - PS Name (512 byte EEPROM only);
  - AF List, AF follow mode on/off.
- Audio controls: volume, balance, fader, treble, bass and loudness.
- Four digit security code (0000 - 9999).
  - Security code can be preprogrammed with the keyboard by means of a service mode, or a preprogrammed EEPROM has to be used.
  - Security code can not be changed by the user. The security code can be enabled or disabled by the user; enable/disable status is stored in EEPROM.
  - Must be entered each time the main supply line has been interrupted or the radio has been removed from the retrack.

Sound:

- Volume, balance, fader, treble and bass control with vol-up/down keys.
- Analog control select key to cycle through balance, fader, treble and bass.
- Mute key
- Automatic muting during tuning and AST search (silent tuning).
- Break-in of traffic announcements (in TA mode) and PTY-alarm messages when the radio is muted or in cassette / external mode.
- Loudness switching
- Sound settings are stored at switch-off and recalled at switch-on.
- "Bleep" tone to confirm user actions such as storing a programme preset, entering AST mode, etc.
- Mono / Stereo key
- Output pins for mute, loudness and traffic announcement, for use with conventional audio control circuitry.

Power-amplifier:

- Conventional power-amplifiers can be used such as two TDA1552Q (4 x 22 Watt), one TDA1554Q (4 x 11 Watt or 6 Watt in 2 Ohm or respectively 4 Ohm loudspeakers) or one TDA1552Q (2 x 22 Watt) in a BTL stereo configuration.

Options: Diode programmable
- Detachable front
- No LW band
- FM only
- No security code
- Static on/off switch
- Method of source switching

User programmable
- 2 / 4 Loudspeakers
- Bar / digital sound control display
- Loudness on/off
- Security code enable/disable

Automatically detected
- Digital sound control chip or conventional controls
- 120 / 144 segment LCD display
- 256 or 512 bytes EEPROM
- Loudness
- Local/DX FM Tuner Control
- AMS)
- Dolby) Cassette deck functions
- ME/CR)

Power connections:

- Continues power supply input. Normally connected directly to the car battery. All supply power is drawn from this input.

- Ignition key input. Normally connected to the accessory contact of the ignition switch. Used only for switching the radio on/off.
  This input is also used when the static on/off switch option is chosen instead of the momentary on/off key.

Switching-on/off:

- Recall of last system status (e.g.: frequency, band, sound control settings, RDS status and last selected audio source).

- Switch on by:
  - Power key, can be static or momentary.
  - Ignition contact (after the set was switched off by turning the ignition off).

- Switch off by:
  - Power key, can be static or momentary.
  - Ignition contact.
  - Removal of detachable keyboard.
  - Opening of the security contact.

- When switched on while the ignition contact is (and remains) off, the set will automatically switch off after 30 minutes.

- The radio will switch on again when switched off by means of a power voltage dip during engine start.

Cassette:
- Automatically switches to cassette mode after insertion of a cassette
- Interfaces with a mechanically controlled cassette deck
- Play/wind mode detection
- Play direction detection for auto-reverse cassette decks
- Radio reception during wind mode
- Cassette/Radio mode key
- Metal/Chromium tape on/off key
- DOLBY system on/off key
- AMS (Auto Music Search) on/off key
- Optional source switching to external mode (cd plug is in) or always to radio mode (option diode D6 is in) when the cassette is ejected.

External audio input:

- Automatically switches to external audio source when a connector is inserted.
- External/radio mode key.
- Optional source switching to cassette mode (cassette is in) or always to radio mode (option diode D6 is in) when the external plug is removed.

5 TARGET CHARACTERISTICS OF THE RADIO.

General

Supply voltage range		10.2	to	16	V
Quiescent current,	power off			2	mA (typ.)
	power on			520	mA (typ.)
Operating ambient temperature		-30	to	75	°C
FM frequency range		87.5	to	108	MHz
AM frequency range,	LW	144	to	288	kHz
	MW	522	to	1611	kHz
IF-frequency (AM and FM)				10.7	MHz

FM characteristics

V_{supply} = 14.4 V, T_{amb} = 25 °C, f_o = 98 MHz, f_{dev} = 22.5 kHz, f_{mod} = 1 kHz unless otherwise specified.
Dummy aerial as shown in Figure 3.

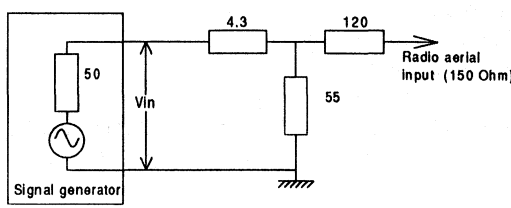


Figure 3 Dummy aerial to test the FM mode

Aerial input voltage (Vin), for -3 dB limiting (adjustable)			5 -	20	µV
for (S+N)/N = 26 dB				3	µV
for 10 dB crosstalk (stereo)				150	µV
Signal-to-noise ratio over most of the signal range				60	dB
RF signal handling capability for THD < 2% at 75kHz dev.			>	2	V
AF output over most of the signal range					
measured at pin 11 of IF module TEA6100.				150	mV
AM suppression over most of the signal range			>	50	dB
Total Harmonic Distortion over most of the signal range. 75 kHz dev.				0.5	% (typ.)
Adjacent signal selectivity (two signal method) S_{300}			>	64	dB
IF bandwidth 3dB bandwidth				170	kHz
IF suppression			>	85	dB
Search sensitivity		Vin	>	12	µV
RDS sensitivity:	Traffic Announcement	Vin	>	12	µV
	Programme Identification	Vin	>	15	µV
Frequency counter resolution				6.4	kHz
Frequency grid	Search Tuning			100	kHz
	Manual Tuning			50	kHz

AM characteristics

V_{supply} = 14.4 V, T_{amb} = 25 °C, f_o = 999 kHz, m = 0.3, f_{mod} = 1 kHz unless otherwise specified.
Dummy aerial as shown in Figure 4.

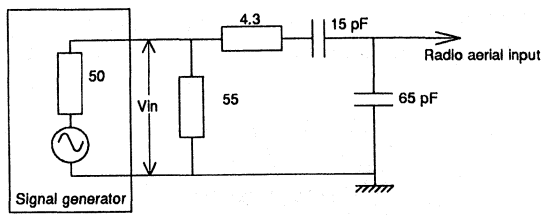


Figure 4 Dummy aerial to test the AM mode

Aerial input voltage (Vin), for (S+N)/N = 26 dB	MW		70	µV
	LW		140	µV
Signal-to-noise ratio for Vin = 1 mV		>	45	dB
AGC range Vin/500 mW for 10 dB variation of AF output			90	dB
RF signal handling capability for THD < 10 % at m = 0.8			1.4	V
Total Harmonic Distortion over most of the AGC range, m = 0.8, fmod = 400 Hz		<	2	%
Total bandwidth B 3dB			5	kHz
Fidelity (-3 dB)			30 Hz - 2	kHz
IF suppression tuned frequency 1400 kHz, Vin = 20 µV			62	dB
Image rejection tuned frequency 1400 kHz, Vin = 20 µV			76	dB
IF selectivity	S_9		36	dB
	S_{20}		66	dB
Frequency counter resolution			500	Hz
Frequency grid,				
LW (search and manual tuning)			1	kHz
MW (search tuning)			9	kHz
MW (manual tuning)			1	kHz
Search sensitivity	Vin	>	45	µV

6 MICROCONTROLLER AND PIN ASSIGNMENTS.

CCR520S is based on a P83CE528 microcontroller. It is single-chip microcontroller, manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family.

The pin assignments for CCR520S are given in Figure 5 and Figure 7.
Figure 6 and Figure 8 show the keyboard configurations for the fixed and detachable front respectively.

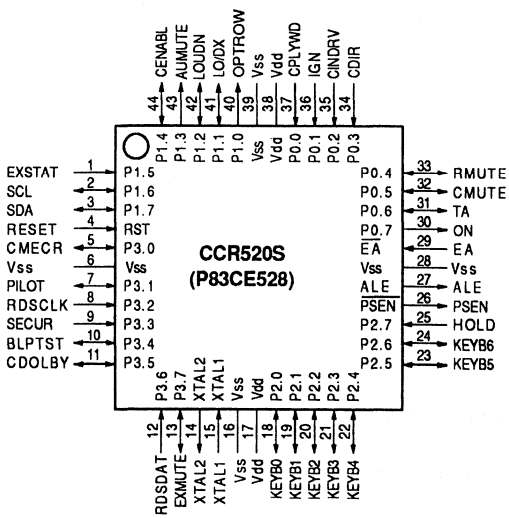


Figure 5 Pinning of CCR520S for fixed front

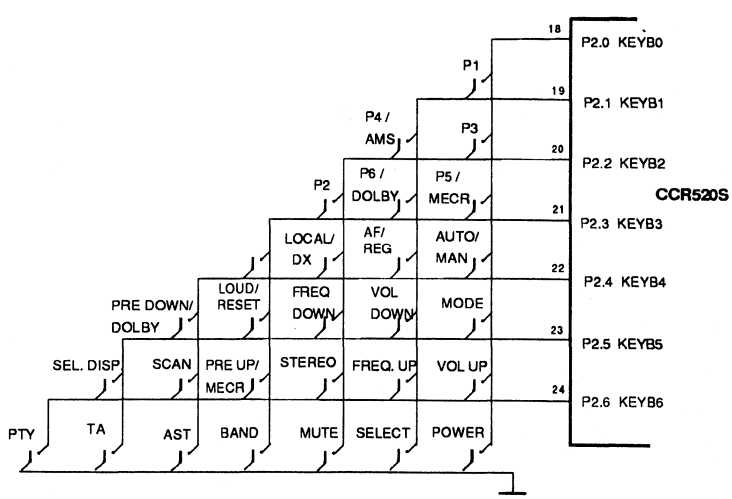


Figure 6 Keyboard configuration for fixed front

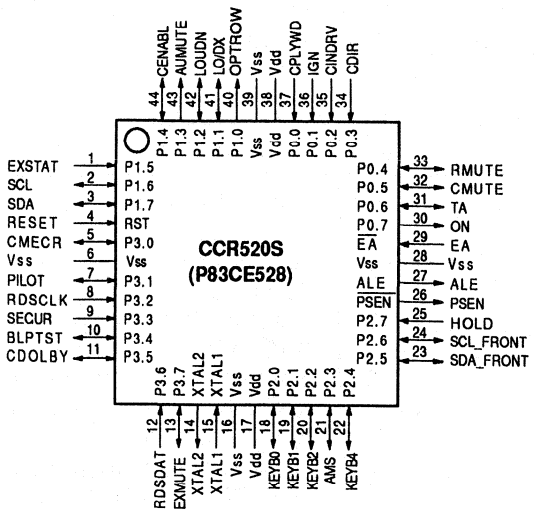


Figure 7 Pinning of CCR520S for detachable front

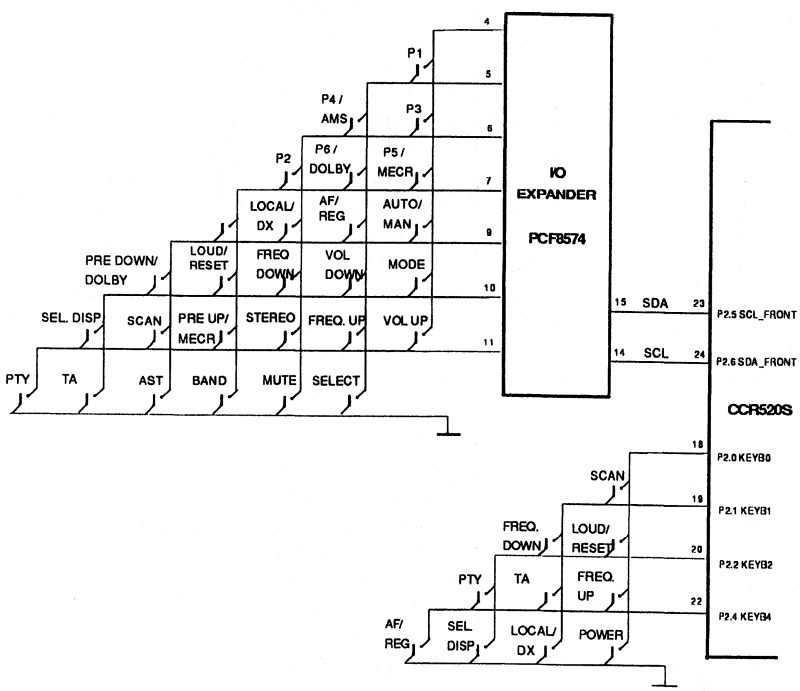


Figure 8 Keyboard configuration for detachable front

When the detachable keyboard option is chosen it is not necessary to use all the keys in the small fixed keyboard. At least the power key should be mounted when is chosen for the momentary on/off key. (Static on/off switch option disabled)

The following table gives a short description of all pins.

PIN	NAME	I/O	DESCRIPTION
1	EXSTAT	I	Status of external audio jack
2	SCL	I/O	I^2C Bus Clock line
3	SDA	I/O	I^2C Bus Data line
4	RESET	I	Device reset
5	CMECR	I/O	Cassette ME/CR select
6+16+28+39	Vss		GROUND
7	PILOT	I/O	Stereo indication / mono/stereo control
8	RDSCLK	I	RDS Clock from RDS demodulator
9	SECUR	I	Security contact
10	BLPTST	I/O	Bleep output / Test input (service mode)
11	CDOLBY	I/O	Cassette dolby select
12	RDSDAT	I	RDS Data from RDS demodulator
13	EXMUTE	O	Mute external audio source
14	XTAL2	O	Oscillator output
15	XTAL1	I	Oscillator input
17+38	Vdd		+ 5 V supply voltage
18	KEYB0	I/O	Keyboard matrix line 0
19	KEYB1	I/O	Keyboard matrix line 1
20	KEYB2	I/O	Keyboard matrix line 2
21	KEYB3	I/O	Keyboard matrix line 3 / AMS select
22	KEYB4	I/O	Keyboard matric line 4
23	KEYB5	I/O	Keyboard matric line 5 / detach. I^2C Data
24	KEYB6	I/O	Keyboard matric line 6 / detach. I^2C Clock
25	HOLD	I	Power supply OK in
26	/PSEN	O	Program Store Enable (n.c.)
27	ALE	O	Address Latch Enable (n.c.) (disabled)
29	/EA	I	External Access (connect pull-up)
30	ON	O	Power supply on control
31	TA	O	Traffic announcement in progress
32	CMUTE	O	Cassette mute
33	RMUTE	O	Radio mute
34	CDIR	I	Cassette direction (forward/reverse)
35	CINDRV	I	Cassette In drive
36	IGN	I	Ignition contact status or static on/off switch
37	CPLYWD	I	Cassette play/wind mode
40	OPTROW	O	Option row output
41	LO/DX	I/O	Local / DX control
42	LOUDN	I/O	Loudness
43	AUMUTE	O	General audio mute
44	CENABL	O	Cassette enable

7 KEYBOARD.

The keyboard consists of a 7-line triangular matrix connected to the microcontroller or the I/O expander PCF8574. The following table lists the available keys.

NAME	DESCRIPTION
P 1	Preset-1
P 2	Preset-2
P 3	Preset-3
P 4 / AMS	Preset-4 / Auto Music Search on/off (cassette)
P 5 / ME/CR	Preset-5 / Metal/Chromium on/off (cassette)
P 6 / dolby	Preset-6 / dolby on/off (cassette)
POWER	Power on/off (momentary on/off key)
VOL-UP	Analog sound setting up
VOL-DOWN	Analog sound setting down
SELECT	Select analog function for update
MUTE	Mute on/off
FREQ-UP	Manual / search tuning upward
FREQ-DOWN	Manual / search tuning downward
AUTO/MANUAL	Switch between manual / search tuning
BAND	Cycle through bands
AST	Automatic search tuning band select and programming
AF / REG	RDS AF follow mode on/off / regional mode on/off
TA	RDS traffic information mode on/off
PTY	RDS PTY mode on/off
LOUD / RESET	Loudness on/off / Sound settings reset
MODE	Radio / cassette / external selection
LOCAL / DX	Local / DX selection
STEREO	Suppress/enable stereo mode
PRE-UP / ME/CR	Programme preset up / Metal/Chromium on/off (cassette)
PRE-DOWN / dolby	Programme preset down / Dolby on/off (cassette)
SCAN	Automatic frequency scan
DISPLAY	Select display (PTY / frequency / PS name)

8 OPTION DIODES.

Diode	Description
D1	Detachable front
D2	FM Only
D3	No LW band
D4	No security
D5	Static on/off switch
D6	Method of source switching

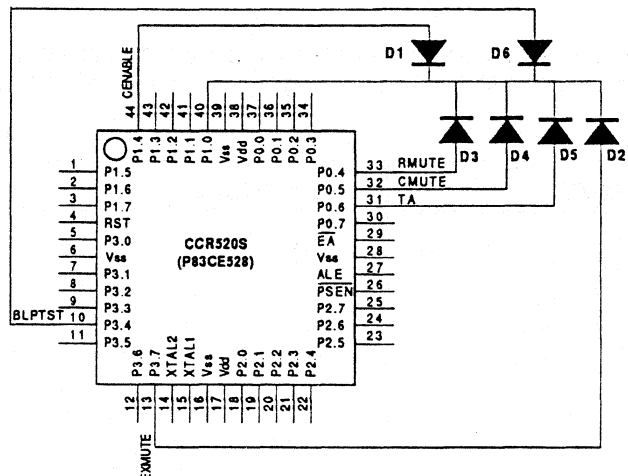


Figure 9 Location of option diodes

9 LCD DISPLAY.

The Liquid Crystal Display (LCD) is driven by either one PCF8576 or two PCF8566's. Figure 10 shows all the segments of the display. To support the RDS programme service name (PS) feature, the display is equipped with 8 alpha numeric characters. With 13 segments per character, display is possible of all required RDS characters (capitals only); with 16 segments per character, umlauts and the accent can be displayed as well.
Both displays operate in 1:3 multiplex mode.

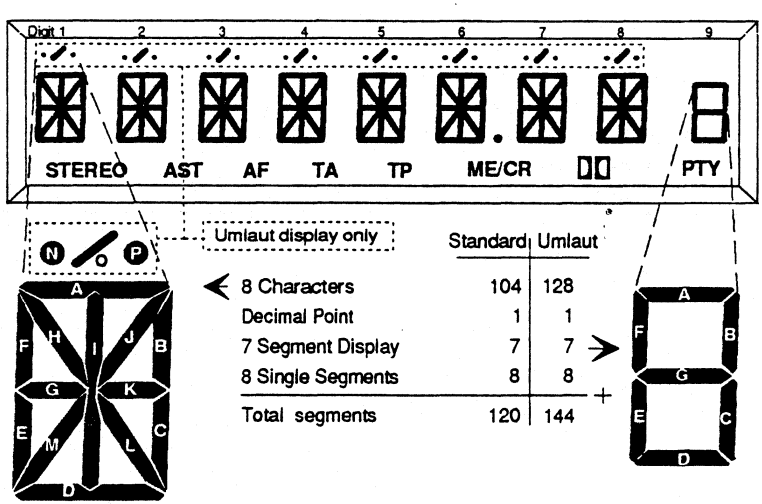


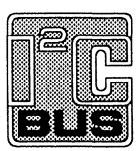
Figure 10 Liquid Crystal Display (LCD) layout

CCR610S Application report AN95080

Abstract

CCR610 is a computer controlled high-end AM/FM car radio system with R(B)DS EON decoding. It is based on a single 8051 family microcontroller (P83CE528), ICE (TEA6811 / TEA6822), SOFAC (TEA6320) and additional I²C-bus controlled peripherals.

"The purchase of Philips' complete set of Integrated Circuits as specified in this Outline Specification for manufacture of a radio system conforming the relevant specification as herein given, secures immunity from suit on unauthorized use of those Philips' patent rights, which specifically relate to automatic broadcast station storage (AST) and/or radio data system (RDS) features."



Purchase of Philips I²C components conveys a license under the I²C patent to use the components in the I²C system, provided the system conforms to the I²C specifications defined by Philips.

CCR610S Application report AN95080

Summary

CCR610 is a computer controlled high-end AM/FM car radio system with RDS decoding. It is based on a single 8051 family microcontroller (P83CE528) and various I^2C-bus controlled peripherals.

The system contains functions such as PLL tuning, IF control, stereo decoding, R(B)DS+EON decoding, IAC, source switching, sound fader control, LCD display, cassette interface, external audio input jack and a detachable front.

Radio control and R(B)DS+EON processing are combined in a single microcontroller.

CONTENTS

REVISION HISTORY

Version	Remarks
Version 0.1	First release report number ERA94001
Version 0.2	Report number AN94064 Modifications with respect to version 0.1: 1. AMS function fully implemented by solenoid and AMS pause control. 2. Option D4 moved to KEYB1 line. 3. Option D7 added. Band limits and tuning grid for different parts of the word. 4. RBDS decoding added.
Version 0.3	Modifications with respect to version 0.2: 1. Manual tuning algorithm changed. 2. For MW band only tuning on grid is possible. 3. Search tuning grid for USA option changed from 100 kHz to 200 kHz. 4. Manual tuning grid for USA option changed from 50 kHz to 100 kHz. 5. TEA6821 replaced by TEA6822. 6. Frequency counter resolution for FM changed from 5 kHz to 6.25 kHz. 7. PTY search algorithm changed. 8. Pin 9 of the microcontroller (SECUR) not used any more. (Security functionality stays the same.) 9. Input added for "Phone mute" detection.

1. INTRODUCTION

CCR610 is a computer controlled high-end AM/FM car radio system with R(B)DS (Radio Broadcasting Data System), EON (Enhanced Other Network information) and I²C-bus controlled radio IC's. CCR610S is the controlling microprocessor. It is based on the 8051 family microcontroller P83CE528 and takes care of all radio control functions as well as R(B)DS and EON decoding.

Features:

- Digital PLL tuning for FM, MW, LW and SW (49m) bands, (factory selectable MW, LW and SW disable).
- Factory option for application in different parts of the world (e.g. USA / Europe) concerning the band limits, tuning grid and PTY code table.
- Manual Tuning.
- Search Tuning and Local/Dx handling.
- Frequency Scan (Continuous Search, pausing 6 seconds on every station).
- Automatic Store Tuning (AST).
- Search for Traffic Programmes (TP) or specific Program Types (PTY).
- Presets: 6 in each of the bands: FM1, FM2, FM-AST, MW, MW-AST, LW and SW (49m).
- R(B)DS functions:
  - PS — Programme Service name.
  - PI — Programme Identification code.
  - AF — Alternative Frequency / Automatic Following.
  - TP / TA — Traffic Programme / Traffic Announcement.
  - PTY — Programme TYpe selection and display. (In four languages: English, German, Swedish and French.) PTY Code table for both RDS and RBDS.
  - EON — Enhanced Other Networks information.
- Sound control: volume, bass, treble, balance, fader, loudness and mute via I²C-bus or potentiometers.
- Non Volatile Memory for last sound control settings, last band, last frequency for each band, Presets, PS names (RDS), AF lists (RDS), etc.
- LCD display (I²C bus controlled) displaying:
  - system status (band / frequency / preset number / modes).
  - RDS Programme Service name (PS).
  - RDS Programme Type (PTY).
  - Sound control settings (Bass, Treble, Balance, Fader).
- Security code:
  - enable/disable by the user.
  - programmable in the factory by means of a service mode.
- Power stabilizer control with diagnostic functions.
- User control up to 27 keys with either a fixed keyboard, a keyboard on a detachable front panel or a combination of both.
- User programmable customization options.
- Cassette Interface including MTL, Dolby, AMS (Automatic Music Search) and Solenoid control.
- Input jack for external audio source (e.g. CD player).
- Input for phone mute detection.

2. BLOCK DIAGRAM OF THE SYSTEM

The block diagram of the realisation with a fixed keyboard is shown in Fig.1 . Fig.2 shows the block diagram in case a detachable keyboard is used.

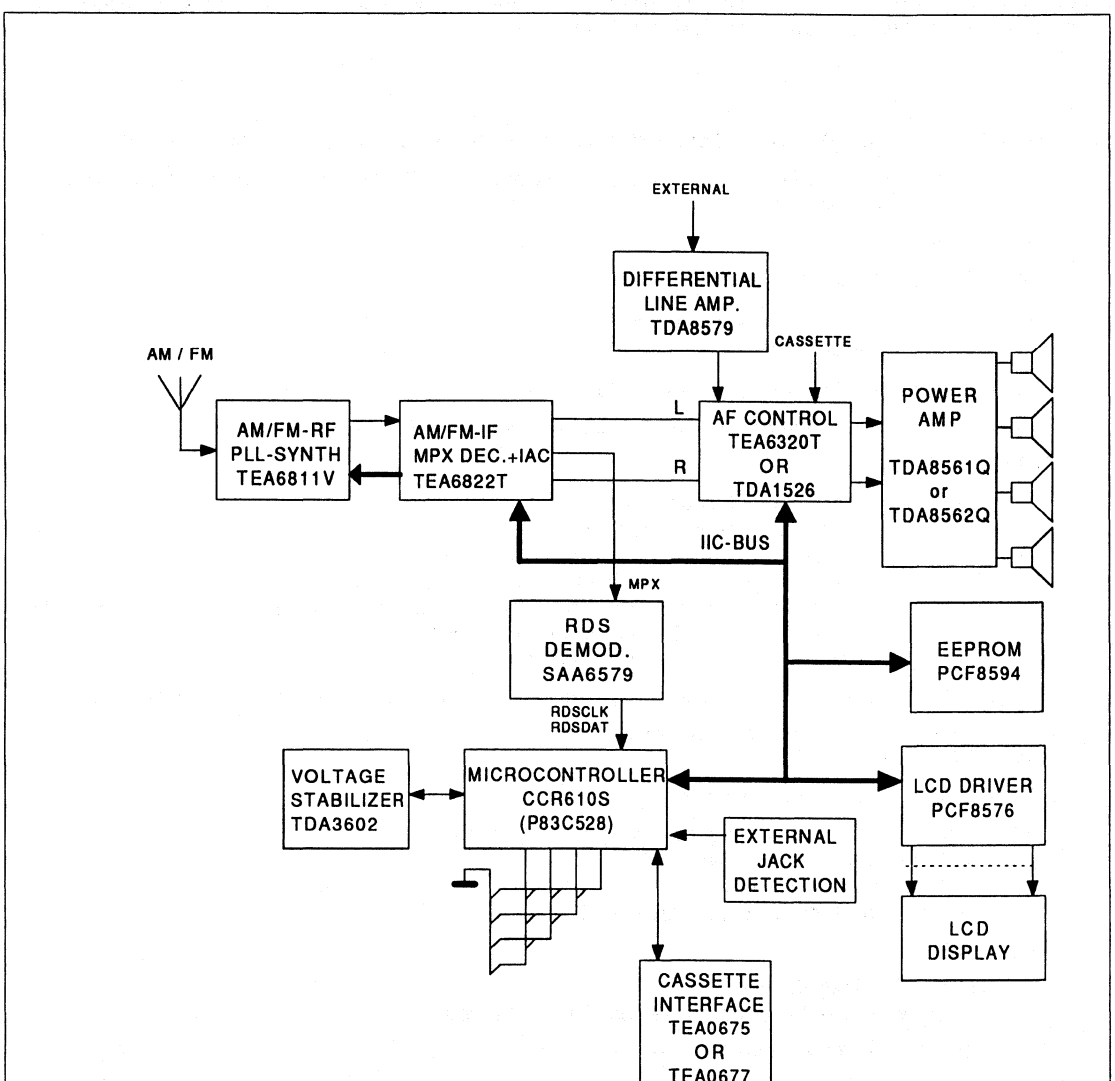


Fig.1 Block diagram of CCR610 with fixed keyboard

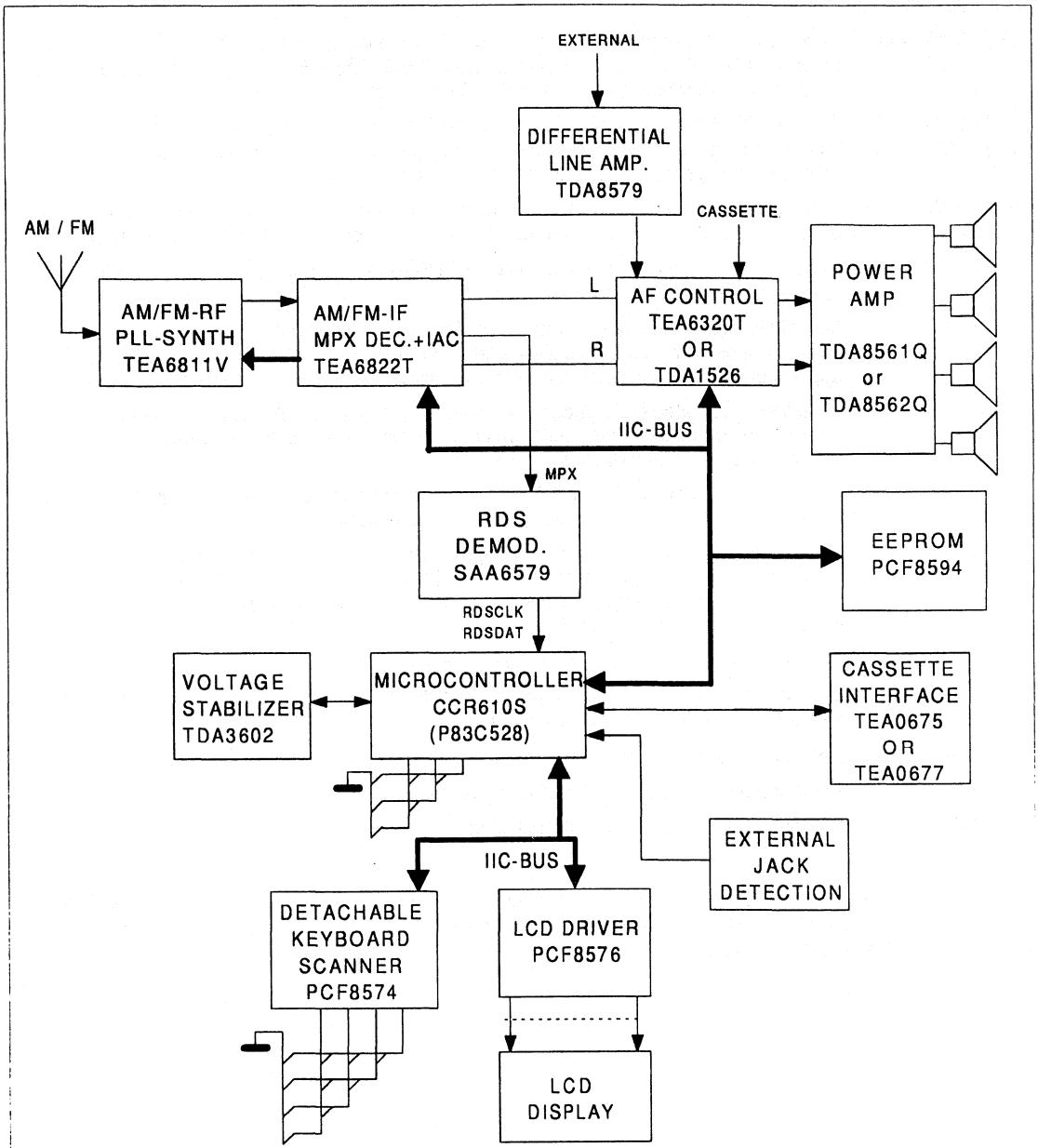


Fig.2 Block diagram of CCR610 with detachable keyboard

3. I.C. DESCRIPTION

- TEA6811V and TEA6822T — Two chip I²C-bus controlled radio concept. It incorporates an AM + FM tuner, an AM/FM RF-PLL synthesizer, an AM/FM IF (including IF detector) and FM stereo decoder and an Interference Absorption Circuit (IAC).
- TEA6320T or TDA1526 — I²C-bus (TEA6320) or potentiometer (TDA1526) controlled AF pre-amplifier for car and home receivers. Includes volume, balance, bass and treble control. The TEA6320 incorporates also fader control and mute.
- CCR610S — The microcontroller, based on a P83CE528EFB. It is a 8051 derivative with an 8-bit CPU, 32 Kbytes ROM, 512 bytes RAM and four 8-bits I/O ports in a 44-pin QFP package.
- TDA3602 — Supply voltage stabilizer in SIL package with three output voltages (2 × 5V and 8.5V). Two outputs are switchable by external controls.
- TDA8561Q — Monolithic integrated class-B output amplifier in a 17-lead single-in-line (SIL) plastic package. It contains 4 × 7W single-ended amplifiers or 2 × 24W amplifiers in a bridged application (4Ω load). Incorporates dynamic distortion detection and diagnostic function.
- TDA8562Q — Monolithic integrated class-B output amplifier in a 17-lead single-in-line (SIL) plastic package. It contains 4 × 7W single-ended amplifiers (4Ω load). Incorporates dynamic distortion detection and diagnostic function.
- SAA6579(T) — RDS demodulator with on chip 57 kHz bandpass filter and a digital demodulator. Outputs a digital data signal and a clock signal for further processing.
- PCF8576T — LCD display driver capable of interfacing to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD with up to four backplanes and up to 40 segment lines and can easily be cascaded for larger LCD applications. I²C-bus controlled.
- PCF8574(T) — Detachable keyboard scanner. I²C-bus controlled.
- PCF8594E-2P/T — 512 byte 5V electrically erasable programmable read only memory (EEPROM) that can be 100,000 times re-written. I²C-bus controlled.
- TEA0675(T) — Head amplifier with Dolby* B-type noise reduction and AMS processor.
- TEA0677(T) — Head amplifier. (without AMS and Dolby noise reduction).
- TDA8579(T) — Differential line amplifier for external input.

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, USA, from whom licensing and application information must be obtained. Dolby is a registered trade mark of Dolby Laboratories Licensing Corporation.

4. SPECIFICATION OF THE SYSTEM

Tuning:

- Frequency bands:

  The following frequency bands are used depending on the factory option USA / Europe:

FM:	87.50	- 108.00	MHz	(50 / 100 kHz steps)	}	
MW:	531	- 1629	kHz	(9 kHz steps)	}	For application
LW:	144	- 288	kHz	(1 kHz steps)	}	in Europe
SW:	5.9	- 6.2	MHz	(1 kHz steps)	}	

FM:	87.90	- 107.90	MHz	(100 / 200 kHz steps)	}	
MW:	530	- 1710	kHz	(10 kHz steps)	}	For application
SW:	5.9	- 6.2	MHz	(1 kHz steps)	}	in USA

- PLL tuning principle

- Manual tuning up / down

  First one step, next after 0.5 seconds. Fast repetition at 12.5 times per second.

- Local/Dx switching

  The Local/DX feature controls the search sensitivity. In the TEA6811 a tuner attenuator for the FM-band is incorporated. After power on the setting defaults to Dx.

- Search tuning up / down

  Sensitivity is controlled by Local/Dx. If after one complete band sweep in Local mode no station is found, the radio switches automatically to Dx. During search tuning the running frequency is displayed and the radio is muted.

- Frequency Scan

  Continuous automatic search tuning, pausing for 6 seconds on every station.

- AST (Automatic Store Tuning) for FM and MW band

  AST switches to FM-AST or MW-AST band, searches for the 6 strongest transmitters in the band and stores them in the AST programme preset memory. In FM, duplication of PI codes will be avoided.

- Programme preset memory

  For each band (FM1, FM2, MW, LW, SW (49m), FM-AST and MW-AST) 6 programme presets and a "manual" frequency are stored. In FM, additional RDS information is stored: PI code (Programme Identification), PS name (Programme Service), AF list (Alternative Frequencies) and AF follow mode on/off.

  Whenever another band is selected, the radio reverts to the last frequency tuned to in the new band (this can be either a preset frequency or a manually tuned frequency).

- Programme preset up / down control

  Programme presets can be stored and recalled by two key control (up and down) or by 6 separate preset keys.

- AF follow mode

  When AF follow mode is on, the set will regularly measure the signal strength of alternative frequencies and compare it with the current station. If an alternative frequency offers better quality, the radio will switch over and update the alternative frequency list. The measuring scheme is designed to cause minimum noticeable disturbance for the listener. The interval time between two measurements depends on the signal quality.

- Intelligent preset programme recall

  If an FM programme preset with a known PI code is recalled, the primary frequency and all alternative frequencies stored in the programme preset memory are examined. The frequency with the highest signal strength broadcasting the correct PI code will be selected. If the correct programme is not found on one of the AFs then after 6 seconds a search is started for a station with a correct PI code.

- TA mode

  In TA mode the radio only searches for transmitters that transmit the RDS traffic programme on the same station or linked via EON. The radio will automatically start a search when switching on TA mode and the current station is not a traffic station.

- PTY scan mode

  In PTY scan mode the radio searches for transmitters that transmit the user-selected PTY code. Dependent on the factory option USA/Europe the RBDS PTY-table or the RDS PTY-table is used. The user can select from four different languages in which the PTY code is displayed (English, German, Swedish and French). In case of RBDS (application USA) the PTY language is english and can not be changed.

- Last status memory: band, frequency, PI code, AF follow mode on/off status and TA mode on/off status are stored in memory. This status is recalled during switch on.

R(B)DS:

- Bit, block and group synchronisation
- Data collection and decoding of:
  - PI, Programme Identification code
  - AF, Alternative Frequencies
  - TP, Traffic Programme
  - TA, Traffic Announcement
  - PS, Programme Service name
  - PTY, Programme TYpe
  - EON, Enhanced Other Network
- AF follow mode using PI and AF (see also Tuning).
- Display of the programme service name in 8 alpha-numeric characters (PS name).
- Display of AF, TP, TA, PTY, EON and Regional mode status.
- Regional mode on/off switching. When Regional mode is on, the radio will, during AF switching, only switch over to stations with exactly the same PI-code. When Regional mode is off, the radio will also switch over to stations broadcasting regional variants off the original station. (so called "generic" or "family" PI codes)
- Break-in of traffic announcements and PTY alarm messages even when the radio is muted or in cassette / external mode.

EON:

- Switch temporarily to an other station if EON information indicates a traffic announcement on an other network even when the radio is muted or in cassette / external mode.
- Update lists of alternative frequencies of other stations stored in preset memory with information received via EON.
- Display by means of an icon whether EON data is received or not and whether an EON traffic announcement is broadcast.

Detachable front:

- Optionally, the keyboard and the LCD display unit can be placed on a detachable front controlled by a 2nd I^{2}C bus. Only 5 contacts are required to connect the detachable front (6 if it also hosts the power key). No extra hardware is required to detect its presence.

Control:

- Up to 27 Local control keys on either a fixed, a detachable keyboard or a combination.
  Triangular matrix using 7 lines.

Display:

- 143 Segment LCD with Umlaut (ü) characters, 1:4 multiplexed divided into:

  - 8 Alphanumeric characters + decimal point are used to display:
    - Band and frequency (Example: "FM 103.50")
    - Indication "BALANCE", "FADER", "TREBLE", "BASS" and their position (either analog bar or digital).
    - The security code being entered.
    - RDS programme service name (PS) in 8 alphanumeric characters.
    - RDS programme type (PTY)
    - "MUTE", in case the user mutes the radio, cassette or external.
    - Cassette mode function such as "PLAY >", "CAS WIND", etc.

  - 7 Segment display for the current programme preset number.

  - 15 Icons for display of:
    - ST — On when stereo pilot signal is detected and the radio is not in forced mono mode.
    - AST — On when AST band is selected.
    - SCAN — On when in Frequency scan mode.
    - AF — On when AF follow mode is enabled (see also Tuning), flashing if no RDS data received.
    - TA — On in TA mode and flashing during a traffic announcement in progress.
    - TP — On when a traffic station is received, flashing when the station is not a traffic station and TA mode is on.
    - PTY — On when a PTY code is received, flashing during PTY search.
    - DOLBY ▯▯ — On in cassette mode when dolby is on.
    - MTL — On in cassette mode when metal/chrome is on.
    - AMS — On in cassette mode when AMS is on.
    - REG — On when the radio is in regional mode (see also RDS)
    - EON — On when EON data is received, flashing during an EON traffic announcement.
    - LOC — On when the radio is in Local mode (see also Tuning)
    - LOUD — On when Loudness is on.
    - CLIP — On when clipping is detected and clipping control is active.

Non Volatile Memory:

512 bytes EEPROM. The following information is stored in NVM:

- System status e.g.: band, audio source (radio / cassette / external).
- For each band FM1, FM2, FM-AST, MW, MW-AST, LW, SW(49m) : 6 preset frequencies, one non-preset frequency and the last used preset number.
- For each FM preset:
  - PI-code
  - PS Name
  - AF List (9 AF's)
  - AF follow mode on/off.
- Audio controls: volume, bass, treble, balance, fader and loudness.
- Four digit security code (0000 - 9999).
  - Security code can be programmed with the keyboard by means of a service mode, otherwise a preprogrammed EEPROM is to be used.
  - Security code can not be changed by the user. The security code can be enabled or disabled by the user; enable/disable status is stored in NVM.
  - If enabled, the security code must be entered each time the main supply line has been interrupted or the radio has been removed from the retrack.
- At power-on the contents of the NVM is checked, when a non-initialized EEPROM is detected, the EEPROM will be programmed with default values.

Sound:

- Volume, bass, treble, balance and fader control with vol-up/down keys.
- Analog control select key to cycle through bass, treble, balance and fader.
- Mute key.
- Automatic muting during tuning and AST search (silent tuning).
- Break-in of traffic announcements and PTY-alarm messages (at increased volume level) when the radio is muted or in cassette / external mode.
- Loudness switching.
- Sound settings are stored at switch-off and recalled at switch-on.
- "Bleep" tone to confirm user actions such as storing a programme preset, entering AST mode, etc.
- Mono / stereo key.

- Output pins for mute, loudness and traffic announcement, for use with conventional audio control circuitry.
- Automatic mute of the radio during "Phone mute" detection.

Power-amplifier:

- Power-amplifiers with diagnostic facilities
  * 1 × TDA8561Q amplifier for 4 × 7 W or 2 × 24 W (both at 4Ω load)
  * 1 × TDA8562Q amplifier for 4 × 7 W (4Ω load)
  * 2 × TDA8561Q amplifier for 4 × 24 W (4Ω load)

  - Diagnostic control:
    * short-circuit or too high temperature detection, display an error message
    * signal clipping, via an icon and stepwise decrease of bass and or volume
- Optional conventional power-amplifiers (without diagnostics) can be used such as two TDA1552Q for 4 × 22 W, one TDA1554Q for 4 × 11 W (2Ω load) or 4 × 6 W (4Ω load) or one TDA1552Q 2 × 22 W in a BTL stereo configuration.

Options:

Diode programmable

- Detachable front
- Available frequency bands
- No security code
- Static on/off switch
- Method of source switching
- Frequency band limits and tuning grid

User programmable

- 2 / 4 Loudspeakers
- Bar / digital sound control display
- Loudness on / off
- Preferred PTY language (English, German, Swedish and French)
- Security code enable / disable
- TA volume level

Automatically detected

- Digital sound control chip or conventional audio control circuitry

- Loudness
- AMS)
- Dolby) Cassette deck functions
- ME/CR)
- Availability of power amplifier with diagnostics facility

Power connections:

- Continuous power supply input. Normally connected directly to the car battery. All supply power is drawn from this supply.

- Ignition key input. Normally connected to the accessory contact of the ignition switch. Used only for switching the radio on/off.

  This input is also used when the static on/off switch option is chosen instead of the momentary on/off key.

Switching on/off:

- Recall of last system status (e.g.: frequency, band, sound control settings, RDS status and last selected audio source).

- Switch on by:
  - Power key, can be static or momentary.
  - Ignition contact (after switched off by turning the ignition contact off).

- Switch off by:
  - Power key, can be static or momentary.
  - Ignition contact.
  - Removal of detachable keyboard.
  - Wrong security code entered (after 30 to 40 seconds).

- When switched on while the ignition contact is (and remains) off, the set will automatically switch off after 30 minutes.

- The radio will switch on again when switched off by means of a power voltage dip during engine start.

Cassette:

- Automatically switches to cassette mode after insertion of a cassette
- Interfaces with a mechanically controlled cassette deck
- Play/wind mode detection
- Play direction detection for auto-reverse cassette decks
- Cassette solenoid control
- AMS pause detection for full AMS control
- Radio sound during cassette winding
- ME/CR on/off key
- DOLBY on/off key
- AMS on/off key
- Radio/Cassette/External mode key
- Optional source switching to external mode (external plug is in) or always to radio mode (option diode D6 is present) when the cassette is ejected.

External audio input:

- Automatically switches to external audio source when an external source is inserted.
- Radio/Cassette/External mode key.
- Optional source switching to cassette mode (cassette is in) or always to radio mode (option diode D6 is present) when the external plug is removed.

5. TARGET CHARACTERISTICS OF THE RADIO

General

Supply voltage range		10.2	to	16	V
Quiescent current:	power off		<	2	mA (typ.)
	power on			550	mA (typ.)
Operating ambient temperature		-30	to	80	°C
FM frequency range:	Europe	87.5	to	108	MHz
	USA	87.9	to	107.9	MHz
AM frequency range:	Europe	144	to	288	kHz (LW)
		531	to	1629	kHz (MW)
		5900	to	6200	kHz (SW)
	USA	530	to	1710	kHz (MW)
		5900	to	6200	kHz (SW)
IF-frequency double conversion:	FM-IF1/IF2	72.2 MHz / 10.7 MHz			
	AM-IF1/IF2	10.7 MHz / 450 kHz			

FM characteristics

V_{supply} = 14.4 V, T_{amb} = 25 °C, f_o = 98 MHz, f_{dev} = 22.5 kHz, f_{mod} = 1 kHz unless otherwise specified. Dummy aerial as shown in Fig.3 .

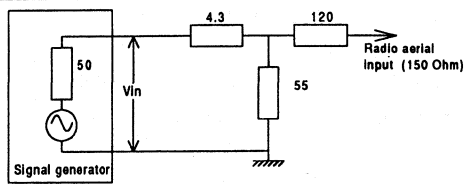


Fig.3 Dummy aerial to test the FM mode

Aerial input voltage (Vin), for -3 dB limiting (adjustable)				3 - 20	µV
for (S+N)/N = 26 dB				2.7	µV
for 10 dB crosstalk (stereo)				70	µV
Signal-to-noise ratio over most of the signal range				64	dB
RF signal handling capability for THD < 2% at 75kHz dev.			>	2	V
MPX output (RMS value) at pin 47 of the TEA6822				200	mV
AM suppression over most of the signal range			>	55	dB
Total Harmonic Distortion over most of the signal range. 75 kHz dev.				0.5	% (typ.)
Adjacent signal selectivity (two signal method) S_{200}			>	45	dB
IF suppression:	IF1 (72.2 MHz)		>	70	dB
	IF2 (10.7 MHz)		>	90	dB
Search sensitivity (adjustable)		Vin	>	4	µV
RDS sensitivity:	Traffic Announcement	Vin	>	12	µV
	Programme Identification	Vin	>	15	µV
Frequency counter resolution				6.25	kHz
Frequency grid (Europe):	Search Tuning			100	kHz
	Manual Tuning			50	kHz
	Repetitive Manual tuning (after .5s)			100	kHz
Frequency grid (USA):	Search Tuning			200	kHz
	Manual Tuning			100	kHz
	Repetitive Manual tuning (after .5s)			200	kHz

AM characteristics

V_{supply} = 14.4 V, T_{amb} = 25 °C, f_o = 999 kHz, m = 0.3, f_{mod} = 1 kHz unless otherwise specified. Dummy aerial as shown in Fig.4 .

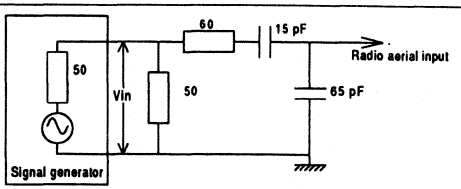


Fig.4 Dummy aerial to test the AM mode

Aerial input voltage (Vin),				
for (S+N)/N = 26 dB	MW		55	µV
	LW		80	µV
	SW		t.b.f.	
Signal-to-noise ratio for Vin = 1 mV		>	55	dB
AGC range 5 mV/Vin for 10 dB variation of AF output		>	60	dB
RF signal handling capability for THD < 10 % at m = 0.8		>	3	V
Total Harmonic Distortion over most of the AGC range, m = 0.8, fmod = 1 kHz		<	2	%
Total bandwidth B 3dB			4.5	kHz
Fidelity (-3 dB)			10 Hz - 2 kHz	
IF suppression	IF1 (10.7 MHz)	>	70	dB
	IF2 (450 KHz)	>	100	dB
IF selectivity	S_9	>	55	dB
	S_{18}	>	60	dB
Frequency counter resolution			250	Hz

Frequency grid	Europe		
LW (search and manual tuning)		1	kHz
MW (search and manual tuning)		9	kHz
SW (search and manual tuning)		1	kHz
	USA		
MW (search and manual tuning)		10	kHz
SW (search and manual tuning)		1	kHz
Search sensitivity (adjustable)		> 20	µV

6. MICROCONTROLLER AND PIN ASSIGNMENTS

CCR610S is based on a P83CE528 microcontroller. It is single-chip microcontroller, manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family.

The pin assignment for CCR610S is given in Fig.5 .

Fig.6 and Fig.7 show the keyboard configurations for the fixed and detachable front respectively.

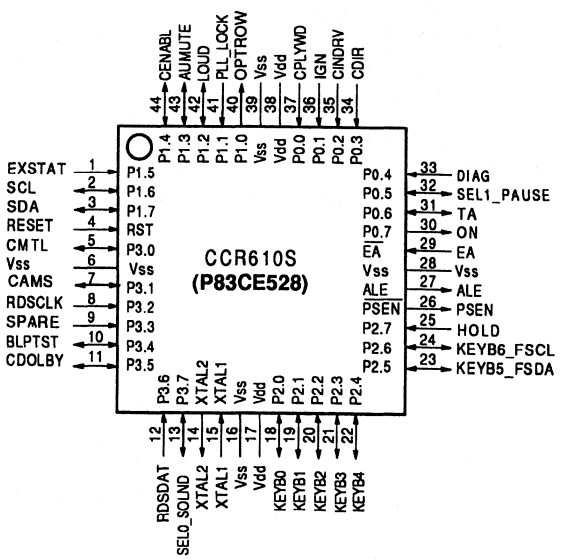


Fig.5 Pinning of CCR610S

If the radio is equipped with a detachable keyboard, pins KEYB5_FSDA & KEYB6_FSCL (pins 23 & 24) are used as I^2C-bus lines to the detachable keyboard. Otherwise pin 23 and pin 24 are used as scan lines for the fixed keyboard.

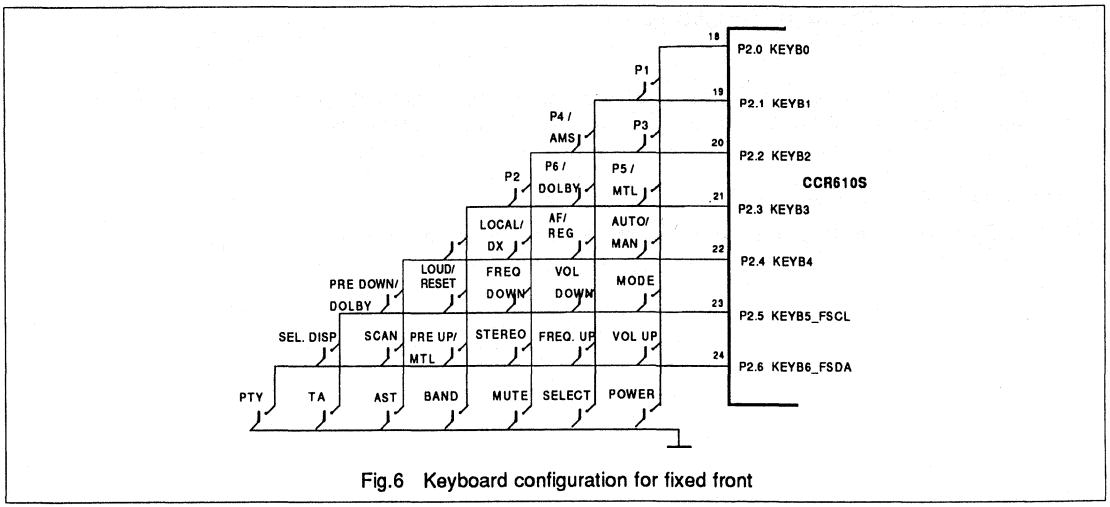


Fig.6 Keyboard configuration for fixed front

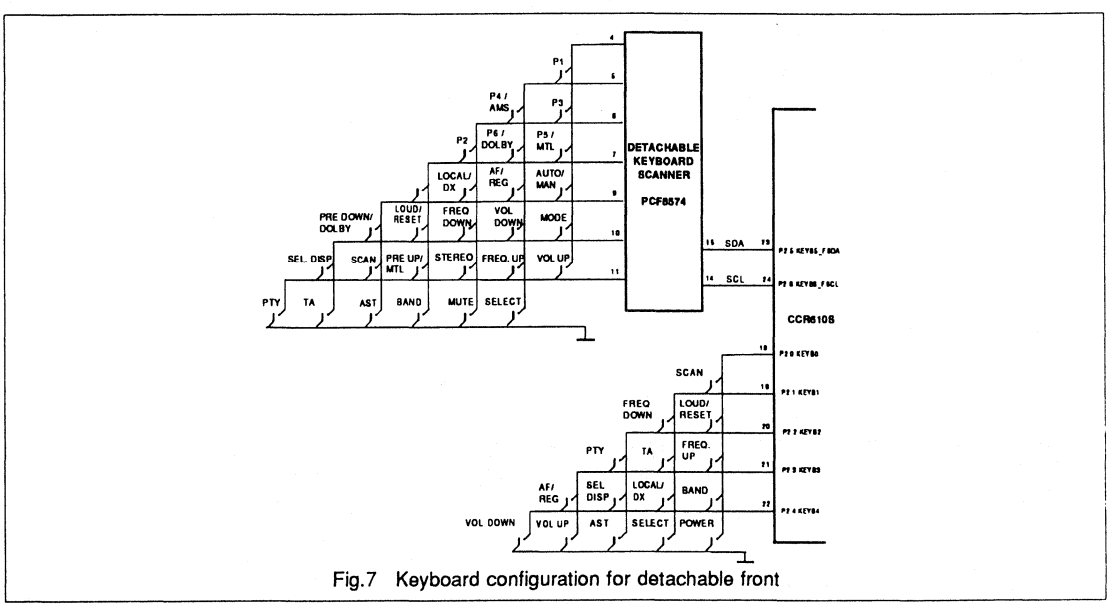


Fig.7 Keyboard configuration for detachable front

If the detachable keyboard option is chosen it is not necessary to mount all the keys on the small fixed keyboard. At least the power key should be mounted if a choice is made for the momentary on/off key. (Static on/off key option disabled) The following table gives a short description of all pins.

TABLE Pinning CCR610S

PIN	NAME	I/O	DESCRIPTION
1	EXSTAT	I	Status of external audio jack
2	SCL	I/O	I^2C Bus Clock line
3	SDA	I/O	I^2C Bus Data line
4	RESET	I	Device reset
5	CMTL	I/O	Cassette Metal (versus Chrome/Ferro) select
6+16+28+39	Vss		GROUND
7	CAMS	I/O	Cassette AMS select
8	RDSCLK	I	RDS Clock from RDS demodulator
9	SPARE		
10	BLPTST	I/O	Bleep output / Test input (service mode)
11	CDOLBY	I/O	Cassette dolby select
12	RDSDAT	I	RDS Data from RDS demodulator
13	SEL0_SOLND	O	Audio source selector pin 0 (potentiometer control) Cassette solenoid control
14	XTAL2	O	Oscillator output
15	XTAL1	I	Oscillator input
17+39	Vdd		+ 5 V supply voltage
18	KEYB0	I/O	Keyboard matrix line 0
19	KEYB1	I/O	Keyboard matrix line 1
20	KEYB2	I/O	Keyboard matrix line 2
21	KEYB3	I/O	Keyboard matrix line 3
22	KEYB4	I/O	Keyboard matrix line 4
23	KEYB5_FSDA	I/O	Keyboard matrix line 5 / detach. I^2C Data
24	KEYB6_FSCL	I/O	Keyboard matrix line 6 / detach. I^2C Clock
25	HOLD	I	Power supply OK in
26	/PSEN	O	Program Store Enable (n.c.)
27	ALE	O	Address Latch Enable (n.c.) (disabled)
29	/EA	I	External Access (connect pull-up)
30	ON	O	Power supply on control
31	TA	O	Traffic announcement in progress
32	SEL1_PAUSE	O I	Audio source selector pin 1 (potentiometer control) AMS pause input
33	DIAG	I	Diagnostic input (power amplifier)
34	CDIR	I	Cassette direction (forward/reverse)
35	CINDRV	I	Cassette In drive

TABLE Pinning CCR610S

PIN	NAME	I/O	DESCRIPTION
36	IGN	I	Ignition contact status or static on/off switch
37	CPLYWD	I	Cassette play/wind mode
40	OPTROW	O	Option row output
41	PLL_LOCK	I	Tuner in-lock detection.
42	LOUD	I/O	Loudness
43	AUMUTE	I/O	General audio mute output / Phone Mute input
44	CENABL	O	Cassette enable

In case of conventional audio sound control circuitry, pin SEL0_SOLND and SEL1_PAUSE are used to select between the various audio sources (radio, cassette, external) by means of a dual 4 channel analogue multiplexer (e.g. HEF4052B). If a Sofac is installed these pins will be used for respectively solenoid control and AMS pause input control.

7. KEYBOARD

The keyboard consists of a 7-line triangular matrix connected to the microcontroller or the I/O expander PCF8574. The following table lists the available keys.

TABLE Keyboard keys

NAME	DESCRIPTION	
P1	Radio mode:	Preset-1
P2	Radio mode:	Preset-2
P3	Radio mode:	Preset-3
P4	Radio mode:	Preset-4
AMS	Cassette mode:	Auto Music Search on/off
P 5	Radio mode:	Preset-5
MTL	Cassette mode:	MTL on/off
P 6	Radio mode:	Preset-6
DOLBY	Cassette mode:	Dolby on/off
POWER	Power on/off (momentary on/off key)	
VOL-UP	Analog sound setting up	
VOL-DOWN	Analog sound setting down	
SELECT	Select analog sound function for update	
MUTE	Mute on/off	
FREQ-UP	Radio mode:	Manual / search tuning upward
FREQ-DOWN	Radio mode:	Manual / search tuning downward
AUTO/MANUAL	Radio mode:	Switch between manual / search tuning
BAND	Cycle through bands	
AST	Automatic search tuning band select and programming	
AF	RDS AF follow mode on/off when pressed short.	
REGIONAL	When pressed long, regional mode on/off	
TA	RDS traffic information mode on/off	
PTY	Display current PTY and enter PTY programming mode	
LOUD	Loudness on/off	
RESET	When pressed long, reset sound settings	
MODE	Select next audio source: Radio / Cassette / External	
LOCAL/DX	Local / DX selection	

TABLE Keyboard keys

NAME	DESCRIPTION	
STEREO	Suppress/enable stereo mode	
PRE-UP	Radio mode:	Preset up
MTL	Cassette mode:	MTL on/off
PRE-DOWN	Radio mode:	Preset down
DOLBY	Cassette mode:	Dolby on/off
SCAN	Radio mode:	Automatic frequency scan
DISPLAY	Radio mode:	Select display (PTY / frequency / PS name)

8. OPTION DIODES

The circuit involved in selecting certain options is presented in Fig.8 . The two tables show the available options and the way to select them.

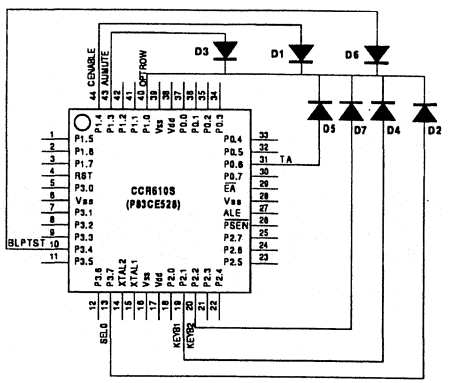


Fig.8 Location of option diodes

TABLE Available options

Diode	Description
D1	Detachable front
D2	Available bands 0
D3	Available bands 1
D4	No security
D5	Static on/off switch
D6	Method of source switching
D7	Tuning grid and band limitations for USA application are selected

TABLE Band selection with D2 and D3

Diode D2	Diode D3	Available bands
Not present	Not present	FM, MW, LW
Present	Not present	FM
Not present	Present	FM, MW
Present	Present	FM, MW, LW, SW(49m)

9. LCD DISPLAY

The Liquid Crystal Display (LCD) is driven by one PCF8576. Fig.9 shows all the segments of the display. To support the RDS programme service name (PS) feature, the display is equipped with 8 alpha numeric characters. For each character umlaut display is possible.

The display operates in 1:4 multiplex mode.

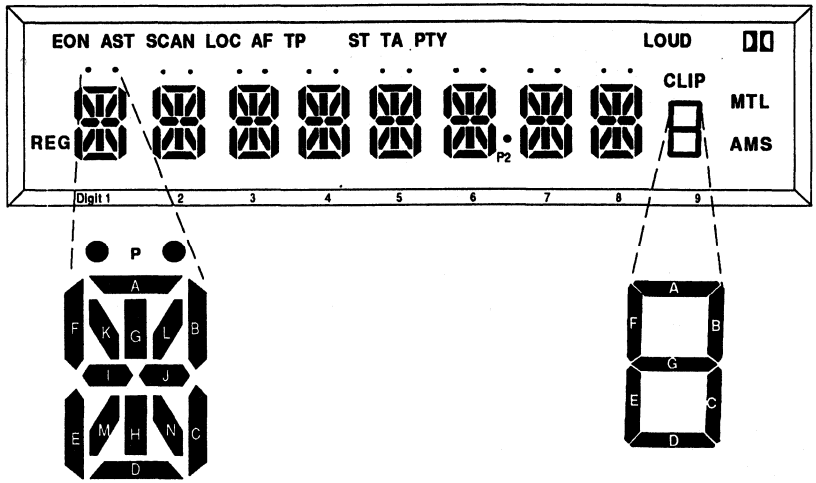


Fig.9 Liquid Crystal Display (LCD) layout

DISPLAY/GAUGE DRIVERS

Differential air-core meter driver SA5775

DESCRIPTION

The SA5775 is a monolithic driver for controlling air-core (or differential) meters typically used in automotive instrument cluster applications. The circuit interfaces with a microprocessor through a serial bus and directly drives the air-core meter. The SA5775 has 10-bit resolution (0.35 degree) and is guaranteed to be monotonic. Data can be shifted through the part, allowing several SA5775s to be cascaded with only one chip-select line. On-chip current shut down logic protects the circuit from external faults.

FEATURES

- 10-Bit resolution (0.35 degrees)
- Exceptional accuracy (0.25 degrees, typical)
- High-torque capability
- Active differential drivers eliminate back-EMF issues
- No RFI/EMI generation issues
- Simple serial interface
- Simple cascading capability for multiple meters
- Internal fault protection
- Only one external component required (bypass capacitor)

PIN CONFIGURATION

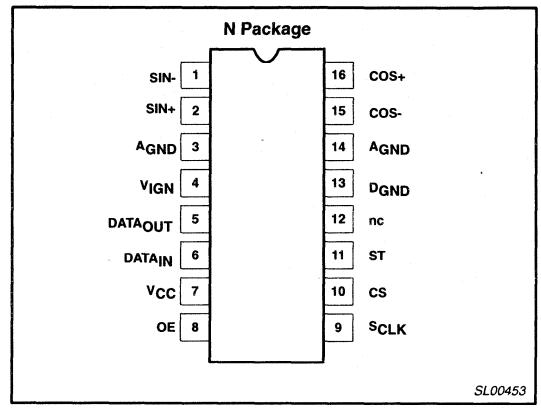


Figure 1. Pin Configuration

APPLICATION

- Instrumentation utilizing air-core meters

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5775N	SOT38-4

BLOCK DIAGRAM

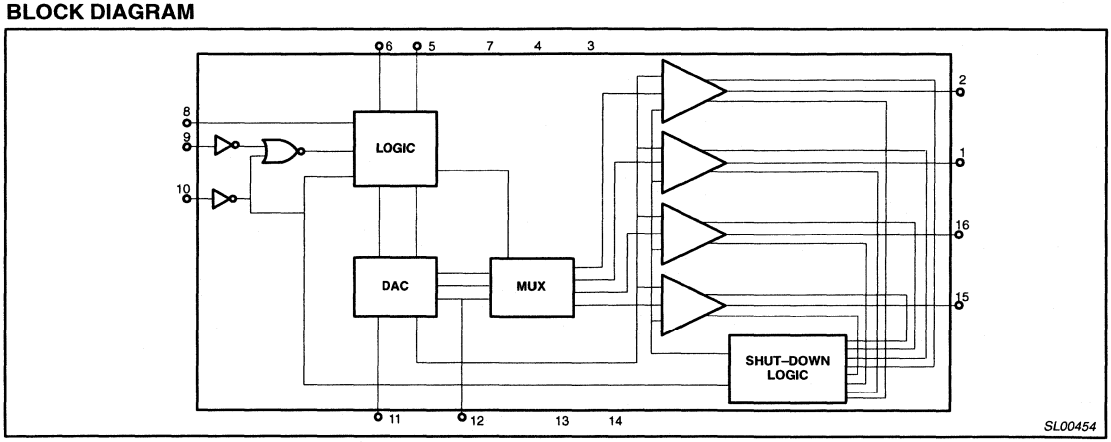


Figure 2. Block Diagram

Table 1. SA5775 Pin Descriptions

Pin #	Name	Function
1	SIN–	Negative output connection to the SIN coil of the gauge.
2	SIN+	Positive output connection to the SIN coil of the gauge.
3	A_{GND}	Ground for V_{IGN} supply. Pins 3, 13 and 14 connected on the circuit board.
4	V_{BB}	Analog supply. Nominally 14.0V.
5	$DATA_{OUT}$	Serial data output. Output of the internal shift register. When a new data word is shifted in, the old word is shifted out the $DATA_{OUT}$ pin.
6	$DATA_{IN}$	Serial data input. A new data word is serially shifted into the part on the rising edge of S_{CLK}. The data is shifted in MSB first.
7	V_{CC}	5V logic supply. The internal latches and registers are set to zero on the rising edge of this signal.
8	OE	Output drivers are turned off when this input is low. Current draw is minimized.
9	S_{CLK}	Serial clock input. Data is loaded into the part on the rising edge of S_{CLK}.
10	CS	Active high chip select input. When CS is high, the part is enabled to receive a new serial input word. The high-to-low transition of CS loads the new 10-bit word into the DAC registers and updates the output.
11	ST	Status output from this IC to indicate that the outputs have been disabled. The outputs may be disabled due to shorted outputs, over temperature conditions, power up reset, or output enable control pin. This output is an open drain output. Multiple status outputs may be wire OR'ed together. This output is low when the outputs are disabled due to a fault condition.
12	nc	Not connected
13	D_{GND}	Ground for V_{CC} supply. Connect to Pins 3 and 14.
14	A_{GND}	Ground for V_{BB} supply. Connect to Pins 3 and 13.
15	COS–	Negative output connection to the COS coil of the gauge.
16	COS+	Positive output connection to the COS coil of the gauge.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{IGN}	Analog supply	-1 to +19	V
V_{CC}	Digital supply	-1 to +6	V
D_{GND} to A_{GND}	Ground difference	-0.3 to +0.3	V
V_{IN}	Digital input voltage, Data In, OE, CS, S_{CLK}	-1 to +7	V
P_D	Power dissipation (T_A = 25°C)[1] N package	1500	mW
T_A	Ambient operating temperature	–40 to +85	°C
T_J	Junction temperature	150	°C
θ_{JA}		90	°C/W

NOTE:
1. For power dissipation ratings in still air, derate above 25°C at the following rates:
N package at 12mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{IGN} = 7.5 to 18V; V_{CC} = 4.5 to 5.5V; T_A = –40 to +85°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{IGN}	Ignition supply voltage		7.5		18	V
I_{IGN}	Ignition supply current	V_{IGN} = 18V no load R_{LC}, R_{LS} = R_{LMIN}[1,2]			25 130	mA mA
I_{CC}	Logic supply current	V_{CC} = 5.5V			1	mA
V_{OH}	Output high voltage	Data out I_{OH} = 300µA	V_{CC} – 0.8			
V_{OL}	Output low voltage	Data out I_{OL} = 1.5mA			0.4	V
V_{OL} Status		I_{OL} = 2.8mA			0.8	V
I_{OH} Status		ST, V_{CC} = 5V			25	µA
V_{IH}	Input high voltage	CS, S_{CLK}, $DATA_{IN}$	0.7 x V_{CC}			V
V_{IL}	Input low voltage	CS, S_{CLK}, $DATA_{IN}$			0.3 x V_{CC}	V
I_{IH}	Input high current	CS, S_{CLK}, $DATA_{IN}$, V_{IN} = 0.7 x V_{CC}			10	µA
I_{IL}	Input low current	CS, S_{CLK}, $DATA_{IN}$, V_{IN} = 0.3 x V_{CC}			10	µA
A_{CC}	Output function accuracy[3]	R_{LC}, R_{LS} = R_{LMIN}	–0.5		0.5	Degree
I_{SD}	Output shut-down current	COS+, COS–, SIN+, SIN– I_{SINK} V_{IGN} = $V_{IGN\ (MAX)}$ V_{IGN} = $V_{IGN\ (MIN)}$ I_{SOURCE} V_{IGN} = $V_{IGN\ (MAX)}$ V_{IGN} = $V_{IGN\ (MIN)}$	 85 43 85 43		 450 300 350 150	 mA mA mA mA
V_{DRIVE}	Coil drive voltage	V_{IGN} = $V_{IGN\ (MAX)}$ V_{IGN} = $V_{IGN\ (MIN)}$	68		78	%V_{IGN}
R_{LMIN}	Minimum load resistance	T_A = 85°C T_A = 25°C T_A = –40°C	300 245 180			Ω Ω Ω

NOTE:
1. See Test Circuit.
2. Maximum current is when output is 45 degrees; T_A = –40°C, and R_L = 180Ω.
3. See Table below:

Ideal	Nominal	Input Code
0	0.176	0
45	45.176	128
90	90.176	256
135	135.176	384
180	180.176	512
225	225.176	640
270	270.176	768
360	359.820	1023
N = Binary Input Code **Equation for Output Angle (θ) vs Output Voltage**		
Quadrant	**Equation**	
I	$\theta = \tan^{-1} \mid [(SIN+) - (SIN-)] / [(COS+) - (COS-)] \mid$	
II	$\theta = 180° - \tan^{-1} \mid [(SIN+) - (SIN-)] / [(COS+) - (COS-)] \mid$	
III	$\theta = 180° - \tan^{-1} \mid [(SIN+) - (SIN-)] / [(COS+) - (COS-)] \mid$	
IV	$\theta = 360° - \tan^{-1} \mid [(SIN+) - (SIN-)] / [(COS+) - (COS-)] \mid$	

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 7.5 to 18V; V_{CC} = 4.5 to 5.5V; T_A = –40 to +85°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
FS_{CLK}	Input frequency				1.6	MHz
TS_{CLKH}	S_{CLK} high time		175			ns
TS_{CLKL}	S_{CLK} low time	V_{CC} = 5.5V	175			ns
TRO	Output rise time DO	0.75 to V_{CC} –1.2V, C_L = 90pF			75	ns
TFO	Output fall time DO	V_{CC} –1.2V to 0.75, C_L = 90pF			75	ns
TSU	DI set-up time		75			ns
THI	DI hold time		75			ns

TYPICAL APPLICATION

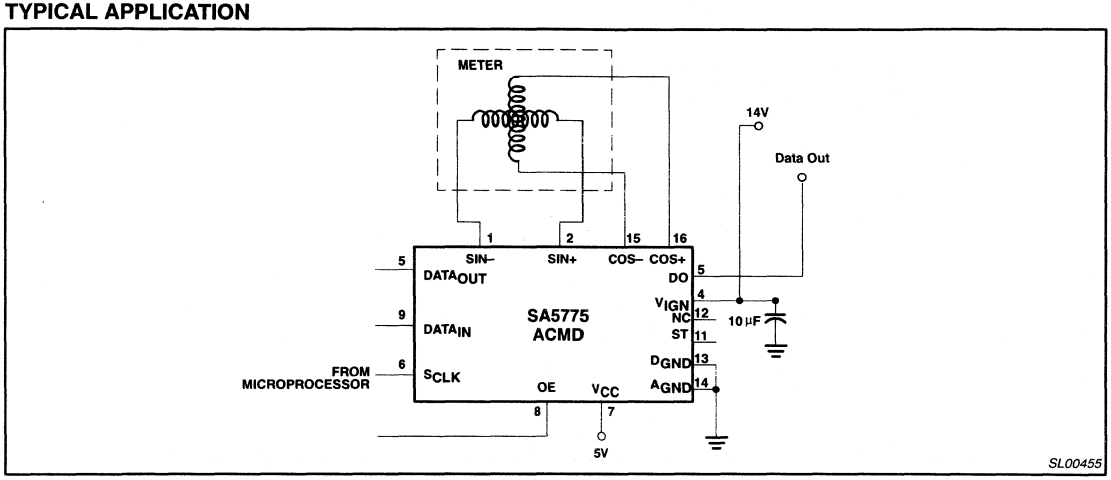


Figure 3. Typical Application

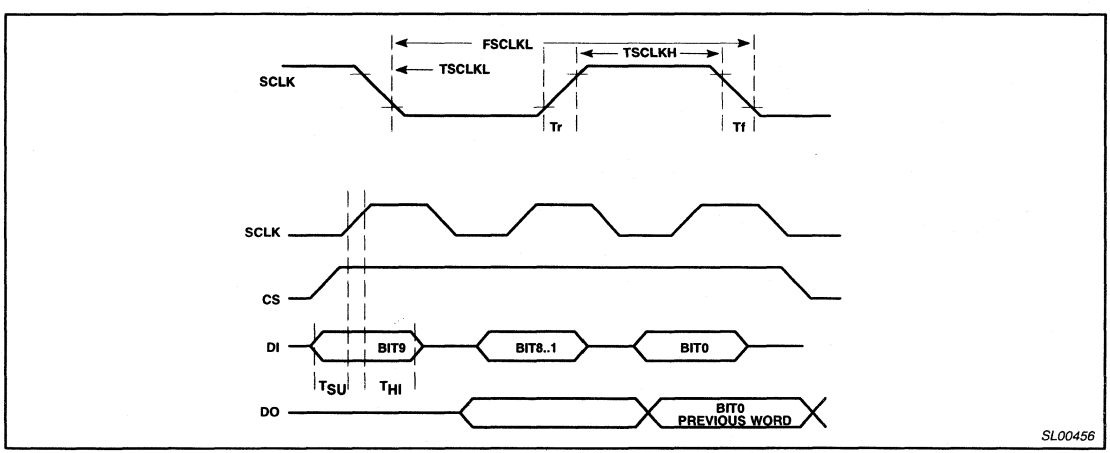


Figure 4. Serial Interface Timing

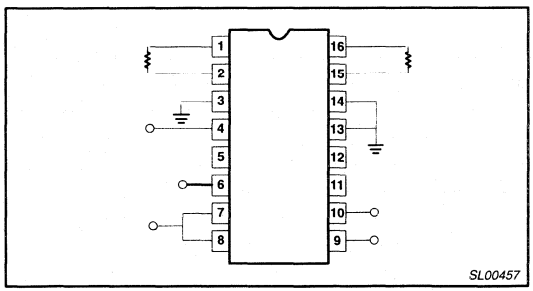


Figure 5. SA5775 Test Circuit

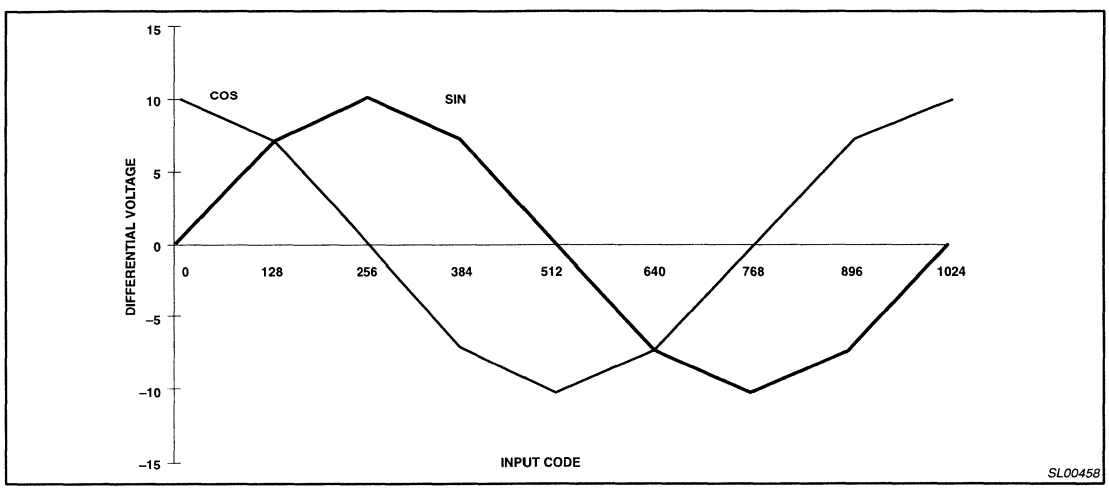


Figure 6. SA5775 Output Voltages (V_{IGN} = 14V)

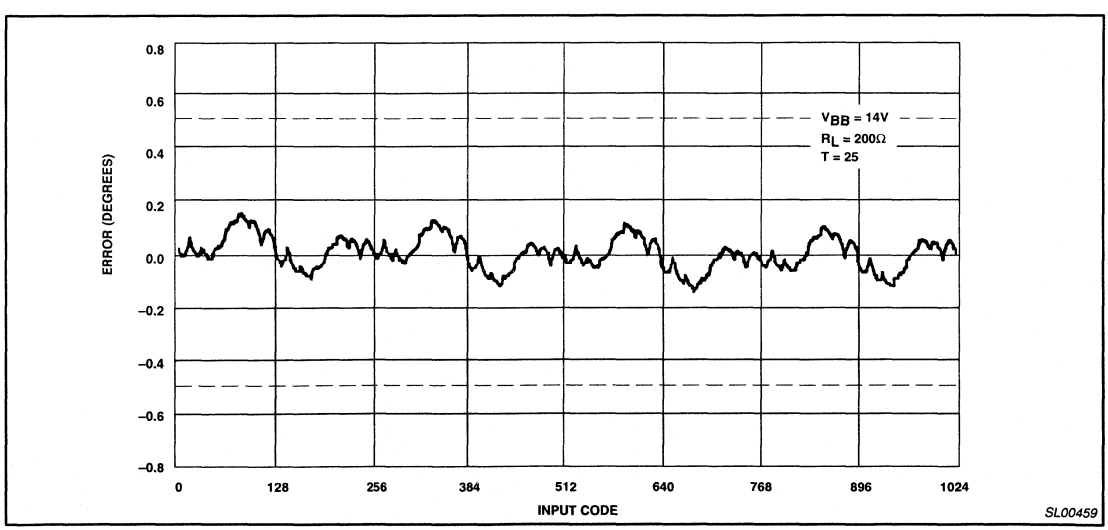


Figure 7. Error Graph

Controlling air core meters with the 87C751 and SA5775

Application report
AN426

INTRODUCTION

Often, certain classes of microcontroller applications surface where large amounts of on-chip resources such as a large program memory space and numerous I/O pins are not required. These applications are typically cost sensitive and desirable attributes of the MCU include low cost and modest on-chip resources such as program and data memory, I/O, and timer-counters. Substantial benefits of reduced design cycle time can be realized by using an industry-standard architecture having software compatibility with existing popular microcontrollers.

THE 87C751

The Philips 87C751 is one such microcontroller that easily meets these requirements. This device, shown in Figure 1, has a 2k x 8 program memory, 64 bytes of RAM, 19 parallel I/O lines, and a 16-bit autoreload timer-counter. It also includes an I^2C serial interface and a fixed rate timer. The 87C751 is based on the 80C51 core and thus uses an industry-standard architecture and instruction set. The device is available in both ROM (83C751) and EPROM (87C751) versions. The EPROM version is available in both UV erasable and OTP packages. References to the 87C751 in this document also apply to the 83C751, unless explicitly stated.

TYPICAL APPLICATION

A typical example of such an application is the interface between the 87C751 and the Philips SA5775 Serial Gauge Driver, SGD, shown in Figure 2. This circuit includes the 87C751 microcontroller, the SA5775 Serial Gauge Driver, an NE555 timer, and discrete support components.

An air core meter differs from a conventional (d'Arsonval) meter movement in that it has no spring to return the needle to a predetermined position, no zeroing adjustment, and no permanent magnet in the classical sense. Instead, it consists of two coils of wire wound in quadrature with each other around a central core in which there is a disc magnetized along its diameter. A shaft is placed through the center of this disc so that the shaft rotates with the disc. An indicating needle attached to this shaft will rotate with it.

SA5775 Serial Gauge Driver

The SA5775 is a monolithic driver for controlling air core meters typically used in automotive instrument clusters and is shown in Figure 3. The SA5775 receives a 10-bit serial word and converts that word to four voltage outputs that appear at the SINE+, SINE–, COSINE+, and COSINE– outputs. The differential voltage at the SINE outputs are applied to one coil of the meter and the COSINE outputs are applied to the other coil of the meter.

The currents through these coils produce a resultant magnetic force which is the vector sum of the magnetic forces produced by each of the two coils. Since the currents through the coils are bidirectional this magnetic vector can rotate through a full 360 degrees. The magnetized disc within the air core meter will follow the rotating vector and the needle will indicate the vector's current position. Since 10 bits are used, there are 1024 discrete words available resulting in an angular displacement of 0.3516 degrees per bit. This is small enough to provide an apparently smooth movement of the needle. The smoothness of the motion will depend greatly on the damping factor of the meter movement.

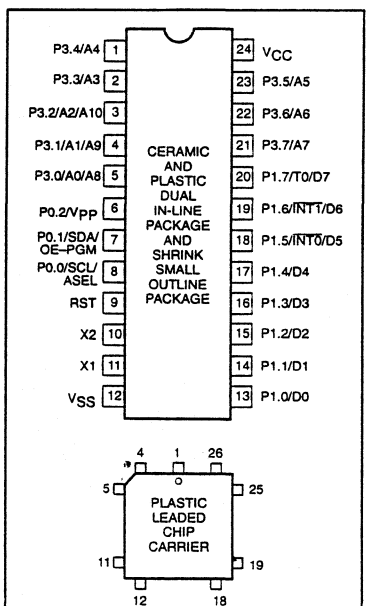
A simplified block diagram of the SA5775 is shown in Figure 4. This device consists of a serial-in/parallel-out shift register, a data latch, a D/A converter, a multiplexer, and output buffers.

A logic high must be present on the chip select (CS) input to clock in the data. Data appearing on the data input (DI) pin is clocked into the shift register on the rising edge of the clock (CLK) input. The data output (DO) pin is the overflow from the shift register, allowing the user to daisy chain multiple SA5775 devices. Note that data is clocked out of this pin on the falling edge of the clock. The CS pin is also used to latch the parallel outputs of the shift register into the data latch. The outputs of the data latch feed the inputs to the D/A converter. The D/A converter outputs are buffered to form the drive signals for the meter coils.

The D/A converter circuits, multiplexer and associated output buffers are purposely designed such that the span of these circuits do not include the power supply rails. This is to avoid inaccuracies that would otherwise occur if the output were to become very close to either supply rail. With a supply voltage of 14 volts (VIGN), the outputs will span a range of approximately 1 to 11 volts. The SA5775 is designed to drive air core meters having a minimum winding impedance of 180Ω at –40°C.

The clock high and low time requirements are 175ns minimum and the maximum data rate is 1.6 megabits per second. At this rate it would require approximately 6.4ms to ramp from zero to full scale if all binary codes were loaded into the SA5775. However, the air core meter cannot respond to such data rates. Both inertia of the movement and damping build into the design of typical air core meter movements limit their response speed.

A high on the output enable input pin (OE) is required to permit the SA5775 to drive the air core gauge. In Figure , OE is held low while the microcontroller is being reset to prevent the gauge from being driven.



Pin	Function	Pin	Function
1	P3.4/A4	15	P1.0/D0
2	P3.3/A3	16	P1.1/D1
3	P3.2/A2/A10	17	P1.2/D2
4	P3.1/A1/A9	18	P1.3/D3
5	N.C.	19	P1.4/D4
6	P3.0/A0/A8	20	P1.5/INT0/D5
7	P0.2/VPP	21	N.C.
8	P0.1/SDA/OE-PGM	22	N.C.
9	P0.0//SCLASEL	23	P1.6/INT1/D6
10	N.C.	24	P1.7/T0/D7
11	RST	25	P3.7/A7
12	X2	26	P3.6/A6
13	X1	27	P3.5/A5
14	VSS	28	VCC

Figure 1. Pin Configuration

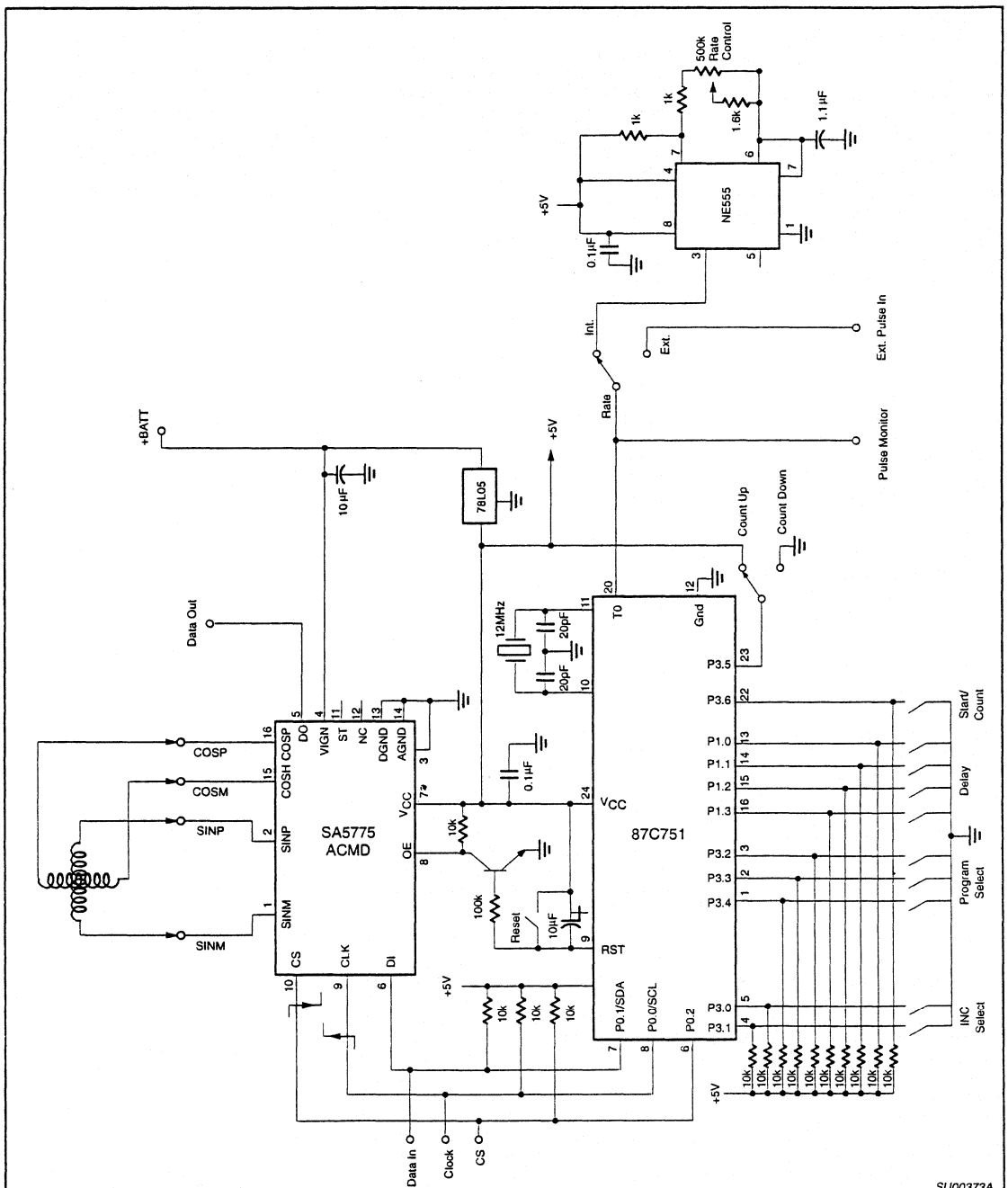


Figure 2. Interface Between the 87C751 and the Philips SA5775

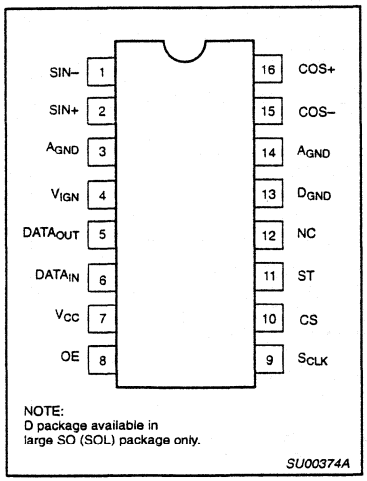


Figure 3. D and N Packages

87C751 Microcontroller

The 87C751 microcontroller provides all of the intelligence in this application. It samples various input ports to determine which demonstration programs to run, the incremental step sizes for angular displacement of the meter core, and the time delay between increments. In one of the demonstration modes, it also samples a variable frequency input and positions the meter core in response to the frequency of that input. The 87C751 also transmits the 10-bit serial data to the SA5775. Data input (DI), Clock (CLK), and Chip Select (CS) lines are driven from the 87C751.

Port 0 of the 87C751 is a 3-bit wide port and is used for communicating data to the SGD. Data is transmitted, MSB first, in a serial stream clocked into the DI of the SA5775 on the rising edge of the clock. In order to clock in data, the CS pin of the SA5775 must be high. The data in the input register is shifted into a latch that drives the DAC on the high to low transition of the CS line. As data is shifted into the SGD, it overflows through the Data Out (DO) pin on the falling edge of the clock. With this facility, multiple SGDs can be daisy-drained with DO of one SGD being connected to DI of the next one, and common clock and chip select lines may be used. This simplifies the interfacing to multiple meter drivers.

The 78L05 regulator (Q2) provides 5 Volt power for the board so that single supply of +14 volts can be applied to the board.

Three rotary switches are used on this board. The PROGRAM SELECT switch (S3) is used to select the program routine that is executed, the INC SELECT (S2) switch selects the incremental step sizes of two of the routines, and the DELAY switch (S4) is used to set the delay between successive word transmissions in one of the routines.

The START/COUNT button (S5) is used to begin execution of a routine, and to cause the next incremental step in Routine #1.

The COUNT UP/DOWN switch (S6) is used in Routine #1 to determine whether the count is increased or decreased with transmission of successive words.

NE555 Timer

The NE555 timer shown in this application example is used as a free running squarewave generator used to simulate sensor inputs such as those which might be found in an automobile, etc. The NE555 timer (U4) operates in the astable mode to produce an output frequency that can be varied from about 1Hz to about 200 Hz. Three of the program routines measure the input period and produce an output code that is proportional to the frequency present at pin 20 (TO) of the microcontroller. A RATE switch (S7) is used to select between the on board oscillator or an external source.

The program listing is included at the end of this application note.

Program Entry

The program starts at address 030(hex) on line 21 of the program listing. The first task is to write 1's to all pins of each port.

Lines 25 and 26 clear registers 6 and 7. These registers are used in this program only to hold the data that is sent out to the SGD. The registers are cleared to be sure that the starting value is zero.

At line 27 the program waits until the START/COUNT button (S5) is depressed before continuing. Lines 28 and 29 set the timer to overflow after 10ms. This is done by setting the timer registers for a count of 10,000 microseconds less than full scale. When the timer counter overflows the timer flag is set, and the timer is reloaded with the value in the timer register. By examining the timer flag we know when 10ms has expired.

Line 30 calls subroutine RPS (Read Port Selected), which reads Port 3 to determine which routine has been selected. Since the PROGRAM SELECT switch (S3) is connected to port pins P3.2 through P3.4, subroutine RPS (lines 507 through 511 at the end of the program) first reads Port 3 into the accumulator, then complements it because the switches used are complementary binary. The reading is then rotated right once and the upper nibble and the LSB (least significant bit) are masked off, leaving twice the value of the port selected in the accumulator. Twice the read value is needed for the next few main program lines that determine which routine to execute.

Line 31 moves the address of label JMPTBL (Jump Table) to the 16-bit Data Pointer (DPTR) register. Line 32 causes a program jump to the address that is the sum of the value in the accumulator (two times the routine number selected) plus the DPTR register. Since each of the commands on lines 33 through 40 are two byte commands, these addresses are all separated by two bytes; hence, the need for the accumulator to contain a number that is twice the number of the selected routine.

Routine 0

This routine begins on line 41 by incrementing the 10-bit word in registers 7 and 6 by the amount indicated by the setting of the INCREMENT SELECT switch, then sending that word to the SA5775. When a full scale overflow is detected, a full scale code (3FF hex) is sent out, followed by a delay of 500 ms, then successive output codes are sent out, decremented by an amount indicated by the INCREMENT SELECT switch. When an underflow is detected a code of zero scale is sent and the routine returns to the beginning of the program. This routine is implemented with a series of subroutine calls.

The SO subroutine begins on line 356 and starts by sending out whatever ten bits that in the two LSBs of register 7 (R7) plus the 8 bits of R6 by calling the SENDIT subroutine. Then it calls the UP subroutine, which increases the word value to be sent out. The program then jumps to the beginning of this subroutine, repeating the process of sending out a word and incrementing to the next word until an overflow from the tenth bit (bit 2 of R7) is detected at line 362.

The SENDIT subroutine (beginning on line 476) brings the CS line high, sets a bit counter (R1) to 2 (to send out two bits of R7), brings the value of R7 to the accumulator, rotates the accumulator to the right three times through the carry bit to bring the two LSBs to the position of the two MSBs, calls the SEND1 routine, which sends the number of bits in the accumulator, starting with the MSB, indicated by R1. Counter R1 is then set to 8 to send out all 8 bit of R6 and the accumulator is loaded with the contents of R6. The SEND1 routine is again called to send out the final 8 bits, and, on line 491, the CS line is brought low, loading the SA5775 internal parallel latch with the contents of the input shift register.

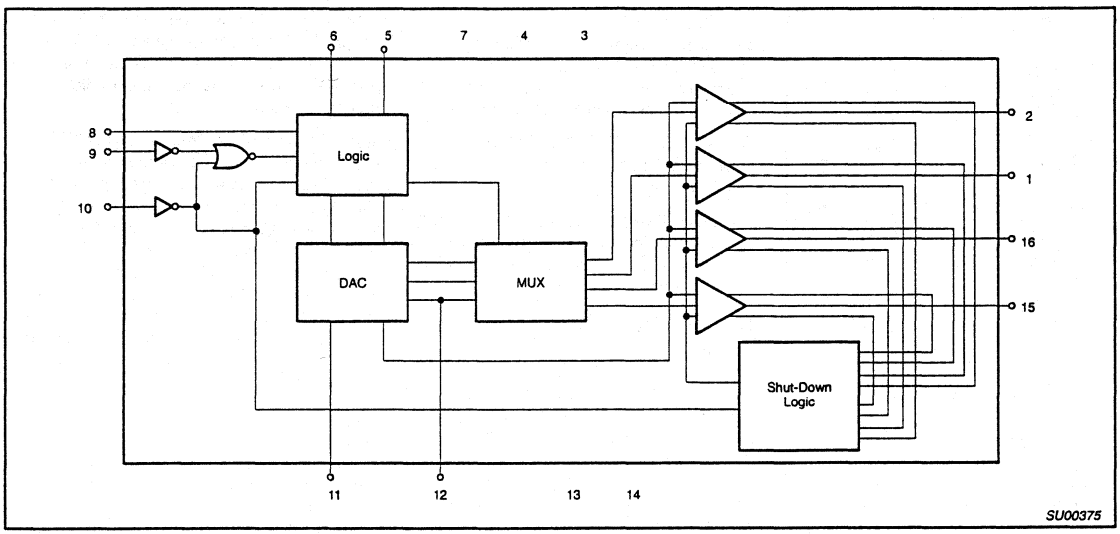


Figure 4. Block Diagram of the SA5775

The SEND1 routine rotates the accumulator left through the carry bit, moves the value of the carry bit to port pin PO.1 (SDA—Serial Data pin), waits to provide a setup time, brings the clock low, waits, brings the clock high, waits, then decrements bit counter sends the next bit if the counter is not zero. A return is executed when the counter becomes zero.

The UP subroutine, beginning at line 364, reads the delay selected by switch S4 at port pin P1, complements it (again, because the rotary switches are complementary binary), masks off the upper four bits (because the delay switch has just four positions and is connected to the lower four bits of the port), multiplies it by 4 (rotates left twice), then moves the result to R1. If R1 is not zero, the program jumps around line 376 and calls a 10ms delay (subroutine DLY10MS) the number of times entered into R1.

The 10ms delay subroutine (starting at line 436) sets the timer for 10ms, waits at line 446 for the timer flag to be set, clears the timer flag, stops the timer, and returns, in this case, to line 379, where the program decrements R1 and repeats the 10ms delay until R1 is zero.

If the selected delay was zero, the program jumps from line 376 to line 380 and reads port 3 to determine the amount the sent out word is to change from the value previously sent out. The accumulator is complemented and the upper 6 bits masked off to recover only the two bits of the selected increment amount. Since increments of 1, 2, 3, or 4 LSBs are hardly noticeable, the program then multiplies the result by 8 (rotate left three times). To insure a minimum change amount, the accumulator is increment by one at line 386. This all means that the increment amounts that can be selected are 1, 9, 17, or 25 LSBs. This amount is added, in lines 387 through 391, to the word previously send out and we return from this subroutine.

After calling the S0 subroutine, PR0GO call the FULLSC (full scale) subroutine, which sends out the full scale code of 3E8(hex). Although a 10-bit full scale code would be 3FF(hex), going only to 3E8 allows an easy distinction between zero scale and full scale when looking at the display. The FULLSC subroutine is found at line 352.

After advancing to full scale, there is a 500ms delay, found at line 464 and called from line 48, then 49 calls the S0D subroutine to send out decreasing word values.

The S0D subroutine begins at line 393 and begins by sending out the current word in R7 and R6 from line 398, then calling subroutine DOWN, which calculates the next (decreasing) word to send out. DOWN begins at line 402. It essentially does the same thing as the UP subroutine, but subtracts the INCREMENT SELECT value from the previously sent word rather than adding to it.

At line 50 subroutine ZEROSC is called to send a zero scale code to the SA5775, then the program branches back to the beginning.

Routine 1

This routine is selected with the PROGRAM SELECT switch is in position 1 or position 9. Routine 1 (PROG1) increments or decrements the word send out, depending upon the setting of the COUNT UP/COUNT DOWN switch, S6. The amount of change is determined by the setting of the INC SELECT switch, S2.

At line 63, the program examines S6 at port pin P3.6 and jumps to the decrement portion of the routine if the pin is low. If this pin is high, the UP subroutine is called from line 64 to increase the R7/R6 word value. The UP subroutine was previously described.

If pin P3.6 is low, the DOWN subroutine (line 402) decreases the previous word sent out by the amount determined from the INC SELECT switch setting.

To insure enough delay to allow the user time to release the START/COUNT button (S5), a delay of 200ms is included at line 66 before jumping to line 27, where another depression of the START/COUNT button is awaited. If S3 (PROGRAM SELECT) is still set to 1 or 9, depression of S5 will cause a jump back to line 52. If another program is selected, the program will jump to the selected routine.

Holding down S5 with PROGRAM SELECT set at position 1 or 9 will cause increasing or decreasing word values to be sent to the SA5775.

Routine 2
PROG2 is the most complex of all these routines. The purpose of this routine is to cause the air core meter deflection to represent the frequency presented at the timer/counter input to the microcontroller. This is done by measuring the period of the input square wave and taking the inverse of the period. The input here must be a square wave because a slow rise and fall time at this input will cause fluctuating readings. To determine the frequency by counting pulses for a time would require a much longer time and, therefore, is impractical.

The MEAS (measure) subroutine is called at line 79 to measure the period of the input waveform and the CALC (calculate) subroutine is called at line 80 to calculate the code to send to the SA5775. The SENDIT subroutine is then called to send the word to the SA5775 and the program jumps back to line 28.

The MEAS subroutine begins at line 83 by being sure the timer is not running and clearing the timer (overflow) flag, then entering zero into both high and low bytes of the timer and the timer register. The carry bit is then cleared (line 90) and the timer started and the timer interrupt enabled.

Lines 93 and 94 form a short loop that waits until either the carry bit is set or until the TO input is low. The carry bit is set when the timer has gone beyond one second. This is done by the timer interrupt subroutine, found at lines 16 through 19. If the TO input never goes low, we know the frequency is at or near zero and the program jumps to GZS (line 108) where R3 is loaded with a 1F (hex) to cause the CALC subroutine to load zero scale into R7/R6.

When (and if) TO is found to be low, the program jumps to line 95 and waits for that input to go high. Time out process is the same as above.

Now that the TO input is found high (if is is before the one second time out), the timer and carry bit are cleared in lines 97 through 100 (R3 is an extension of the timer).

At lines 101 through 107 we wait for one complete cycle at the TO input, with the timer/counter measuring that period, then return to line 80, where the CALC subroutine is called.

The CALC subroutine, starting at line 113, begins by initializing the word to send out (R7/R6) to zero, clearing the carry bit, checking to see if R3 indicates a time above one second, returning to line 81 if it does. Otherwise the program continues at line 26, where the program checks to see if the input frequency is beyond full scale (timer reading above 00 12 88 hex). If it is, R7/R6 is loaded with 12 88 hex (full scale of decimal 1,000). This value was chosen because it is sufficiently far from zero scale that it is easily discerned from zero scale on the display.

If the result is not to be full scale or zero scale, the program continues at line 140 with a shift and subtract divide routine. The dividend would be 1,000,000 (decimal) to convert back to frequency in Hertz (period measurements is in microseconds), but that would provide a maximum count of 200 at 200Hz, only one fifth of the full scale desired of 1,000. So we made the dividend to be 5,000,000 decimal, or 4C 4B 40 hex.

This algorithm is found in lines 156 through 192 and works as follows:

1. Clear a counter.
2. Rotate dividend until the first one is in the second MSB position. Since a code of 4C has already provides that, no shifting is necessary.
3. Rotate the divisor (the period in microseconds in this case) left until the first one is in the second MSB position, but the first byte is LESS THAN the first byte of the dividend. Increment the counter each time the divisor is rotated.
4. Initialize a counter to zero.
5. Rotate the quotient (answer) and dividend one bit left.
6. If first byte of quotient is smaller than the first byte of the quotient, jump to step 8.
7. Add one to the quotient and subtract the divisor from the dividend.
8. Decrement the counter and go to step 5 if it is not zero.

Once the CALC subroutine is completed, the program calls SENDIT from line 81 and jumps, ultimately, to the selected routine.

Routine 3
PROG3, beginning at line 194, measures the input period four times, then calculates the code to display that is the average of these four readings.

It starts by setting a counter for three readings, taking those three readings and storing them in memory, beginning at RAM address 20 hex, using register RO as an index register.

At line 212 the program takes a fourth reading, then adds the three previous readings to it in lines 213 through 227; and divides the sum by four (rotates right twice) in lines 229 through 239. The word to send out is then calculated from line 240 and sent to the SGD, after which the program then looks for and jumps to the selected routine.

Routine 4
PROG4 begins at line 243 and displays the average of the current and last three words sent out.

RAM space used is first initialized to zero and a new reading is taken and a new word is calculated and saved. At lines 264 through 284, the new word is added to the last three readings and the average calculated and stored in RAM locations 28 and 29 (hex), and the average word is sent out.

At line 286, the program reads for the program selected and jumps to line 254 if this routine is selected, otherwise it goes to line 28.

Routine 5
PROG5 begins at line 293 and, very simply, send in sequence the codes for 1/8 through full scale in 1/8 scale steps, with 500ms between steps. It then steps down to zero scale in 1/8 scale steps, then returns to line 28.

Routine 6
PROG6 begins at line 314 and does the same as PROG5, but steps in 1/4 scale increments.

Routine 7
PROG7 loads the code for 3/8 scale into R7/R6, sends it, waits 500ms, changes r& for 5/8 scale, sends it, waits for 500ms, then repeats this sequence 9 more times (for a total of ten times), waits 500ms, then returns the output to zero scale and the program jumps to line 28.

```
                    1  ;                                SGD V3 DEMO                TT.20
                    2  ;                             PROCESSOR:  87C751
                    3  ;                                                        7-29-89
                    4  ;
                    5  ;   The purpose of this program is to drive version 3 of the SGD (SA5775)
                    6  ;   demonstration board.  The PROGRAM SELECT switch is used to select from
                    7  ;   a choice of four routines.  Registers R7 and R6 contain the 10-bit word
                    8  ;   that is send to the SA5775.
                    9  ;
                   10  $MOD751
0000                11          ORG     0
                   12  ;
0000 B02E          13          SJMP    START               ;RESET VECTOR
                   14  ;
000B               15          ORG     00BH                ;TIMER/COUNTER INTERRUPT ROUTINE
000B 0B            16          INC     R3                  ;INCREMENT R3 (3rd BYTE OF TIMER)
000C 740F          17          MOV     A,#0FH              ;TEST FOR TIME OUT (R3 > 0F)
000E 9B            18          SUBB    A,R3                ;IF R3 > 0F, CARRY IS SET
000F 32            19          RETI
                   20  ;
0030               21          ORG     30H                 ;START OF PROGRAM
0030 7580FF        22  START:  MOV     P0,#0FFH            ;SET PORTS HIGH
0033 7590FF        23          MOV     P1,#0FFH
0036 75B0FF        24          MOV     P3,#0FFH
0039 7F00          25          MOV     R7,#0               ;CLEAR WORD TO SEND OUT
003B 7E00          26          MOV     R6,#0
003D 20B6FD        27  W:      JB      P3.6,W              ;WAIT FOR START BUTTON DEPRESS
0040 758BF0        28  READY:  MOV     RTL,#LOW(0-10000) ;SET TIMER REGISTER
0043 758DD8        29          MOV     RTH,#HIGH(0-10000);FOR 10ms TIME
0046 51D2          30          ACALL   RPS                 ;READ PORT 3 FOR PROG SELECT
0048 90004C        31          MOV     DPTR,#JMPTBL        ;JMP ADDRESS TO DATA POINTER
004B 73            32          JMP     @A+DPTR             ;GOTO APPROPRIATE ROUTINE
004C 015C          33  JMPTBL: AJMP    PROG0               ;RAMP UP AND BACK DOWN
004E 0168          34          AJMP    PROG1               ;STEP UP/DOWN W/ start PRESS
0050 017A          35          AJMP    PROG2               ;READ & DISPLAY SPEED
0052 2145          36          AJMP    PROG3               ;DISPLAY AVERAGE OF 4 NEW READINGS
0054 2186          37          AJMP    PROG4               ;DISPLAY AVERAGE OF LAST 4 READINGS
0056 21D3          38          AJMP    PROG5               ;ADVANCE TO FULL SCALE AND BACK IN 45 DEGREE STEPS
0058 21F3          39          AJMP    PROG6               ;ADVANCE TO FULL SCALE AND BACK IN 90 DEGREE STEPS
005A 4107          40          AJMP    PROG7               ;ALTERNATE DISPLAY BETWEEN 3/8 AND 5/8 SCALE TEN TIMES
005C               41  PROG0:
                   42  ;   This routine increases word sent at the selected step size (INCREMENT SELECT)
                   43  ;   and delay time (DELAY), up to full scale, waits 500ms, then decreases the
                   44  ;   word sent at the selected step size and delay times until zero scale is reached.
                   45
005C 5128          46          ACALL   SO                  ;SEND OUT INCREASING WORDS
005E 5121          47          ACALL   FULLSC              ;SET TO FULL SCALE
0060 51A5          48          ACALL   DLY500              ;WAIT 500ms
0062 5152          49          ACALL   SOD                 ;SEND OUT DECREASING WORDS
0064 511B          50          ACALL   ZEROSC              ;RESET TO ZERO SCALE
0066 0130          51          AJMP    START               ;GO TO BEGINNING OF PROGRAM
006B               52  PROG1:
                   53  ;
                   54  ;         MANUAL INCREMENT/DECREMENT ROUTINE
                   55  ;
                   56  ;   This routine increases or decreases the sent out word, depending upon
                   57  ;   the setting of the UP/DOWN switch, by an amount set by the INCREMENT
                   58  ;   SELECT switch.  There is a wait of 200ms before again looking for
                   59  ;   depression of the START/COUNT button to allow time to release this
                   60  ;   button and switch bounce to settle.  The program then looks to see which
                   61  ;   routine is selected and goes to that routine.
                   62  ;
0068 30B50B        63          JNB     P3.5,DCX            ;GO AND COUNT DOWN IF SELECTED
006B 5130          64          ACALL   UP                  ;INCREASE WORD
006D 51B5          65  DP1:    ACALL   SENDIT              ;SEND THE WORD
006F 519D          66          ACALL   DLY200              ;WAIT 200ms
0071 013D          67          AJMP    W                   ;WAIT FOR COUNT BUTTON DEPRESS & SELECTED ROUTINE
0073 20B5F2        68  DCX:    JB      P3.5,PROG1          ;GO AND COUNT UP IF SELECTED
0076 515A          69          ACALL   DOWN                ;DECREASE WORD
```

```
0078 80F3      70          SJMP   DP1
007A           71   PROG2:
               72   ;
               73   ;        READ TIME INPUT AND DISPLAY "SPEED"
               74   ;
               75   ;   This routine measures the period of the square wave at the T0 input and
               76   ;   sends out a word that is inversely proportional to 5 times that period,
               77   ;   providing a display proportional to frequency.
               78   ;
007A 1182      79          ACALL  MEAS            ;MEASURE THE INPUT PERIOD
007C 11C5      80          ACALL  CALC            ;CALCULATE THE WORD TO SEND
007E 51B5      81          ACALL  SENDIT          ;SEND OUT THE WORD
0080 0140      82          AJMP   READY
0082 C28C      83   MEAS:  CLR    TR              ;HALT TIMER
0084 C28D      84          CLR    TF              ;CLEAR TIMER FLAG
0086 758B00    85          MOV    RTL,#0          ;SET TIMER REGISTERS
0089 758D00    86          MOV    RTH,#0
008C 758A00    87          MOV    TL,#0           ;SET TIMER
008F 758C00    88          MOV    TH,#0
0092 7B00      89          MOV    R3,#0           ;CLEAR TIMER 3RD BYTE
0094 C3        90          CLR    C
0095 D28C      91          SETB   TR              ;START TIMER
0097 75A882    92          MOV    IE,#82H         ;ENABLE TIMER INTERRUPT
009A 4021      93   W20:   JC     GZS             ;JUMP IF R3 > 0F
009C 2097FB    94          JB     P1.7,W20        ;WAIT FOR T0 INPUT LOW
009F 401C      95   W21:   JC     GZS             ;JUMP IF R3 > 0F
00A1 3097FB    96          JNB    P1.7,W21        ;WAIT FOR T0 INPUT HIGH
00A4 758A00    97          MOV    TL,#0           ;RESET TIMER
00A7 758C00    98          MOV    TH,#0
00AA 7B00      99          MOV    R3,#0
00AC C3       100          CLR    C               ;CLEAR CARRY/BORROW
00AD 4008     101   W22:   JC     HT              ;JUMP IF TIME UP (CARRY SET)
00AF 2097FB   102          JB     P1.7,W22        ;WAIT FOR T0 LOW
00B2 4003     103   W23:   JC     HT              ;JUMP IF TIME UP (CARRY SET)
00B4 3097FB   104          JNB    P1.7,W23        ;WAIT FOR T0 HIGH AGAIN
00B7 C28C     105   HT:    CLR    TR              ;HALT TIMER
00B9 75A800   106          MOV    IE,#0           ;DISABLE ALL INTERRUPTS
00BC 22       107          RET
00BD 7B1F     108   GZS:   MOV    R3,#1FH         ;SET FOR ZERO SCALE
00BF 22       109          RET
00C0 7F03     110   GFS:   MOV    R7,#03
00C2 7EE8     111          MOV    R6,#0E8H
00C4 22       112          RET
00C5          113   CALC:
              114   ;
              115   ;   This subroutine calculates the 10-bit word to send as a function fo what
              116   ;   is in R3, TH & TL.  The 10-bit word is developed and left in registers
              117   ;   R7 and R6 for use by SENDIT subroutine.
              118   ;
00C5 7F00     119          MOV    R7,#0           ;INITIALIZE QUOTIENT
00C7 7E00     120          MOV    R6,#0
00C9 C3       121          CLR    C               ;CLEAR CARRY/BORROW
00CA 740F     122          MOV    A,#0FH          ;CHECK FOR ZERO SCALE
00CC 9B       123          SUBB   A,R3
00CD 5001     124          JNC    NZS             ;JUMP IF NOT ZERO SCALE
00CF 22       125          RET
00D0 E58A     126   NZS:   MOV    A,TL            ;CHECK FOR FULL SCALE
00D2 9488     127          SUBB   A,#88H
00D4 E58C     128          MOV    A,TH
00D6 9413     129          SUBB   A,#13H
00D8 EB       130          MOV    A,R3
00D9 9400     131          SUBB   A,#0
00DB 40E3     132          JC     GFS
00DD 752E4C   133          MOV    2EH,#4CH        ;SET DIVIDEND TO 5,000,000
00E0 752F4B   134          MOV    2FH,#4BH
00E3 753040   135          MOV    30H,#40H
00E6 7C00     136          MOV    R4,#0           ;CLEAR DIVIDE COUNTER
00E8 8B2B     137          MOV    2BH,R3          ;MOVE READING TO MEMORY (DIVISOR)
00EA 858C2C   138          MOV    2CH,TH
```

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00ED 858A2D  139          MOV    2DH,TL
00F0 C3      140  ROTL:    CLR    C                ;BRING DIVISOR BE JUST LESS THAN DIVIDEND
00F1 E52E    141          MOV    A,2EH
00F3 952B    142          SUBB   A,2BH
00F5 4014    143          JC     DIV24            ;JUMP IF SHIFTING WOULD MAKE DIVISOR > DIVIDEND
00F7 6012    144          JZ     DIV24            ;JUMP IF DIVISOR & DIVIDEND MS BYTES EQUAL BEFORE SHIFT
00F9 E52D    145          MOV    A,2DH            ;SHIFT DIVISOR TO LEFT
00FB 33      146          RLC    A
00FC F52D    147          MOV    2DH,A
00FE E52C    148          MOV    A,2CH
0100 33      149          RLC    A
0101 F52C    150          MOV    2CH,A
0103 E52B    151          MOV    A,2BH
0105 33      152          RLC    A
0106 F52B    153          MOV    2BH,A
0108 0C      154          INC    R4
0109 80E5    155          SJMP   ROTL
010B C3      156  DIV24:   CLR    C
010C EE      157          MOV    A,R6             ;ROTATE QUOTIENT LEFT
010D 33      158          RLC    A
010E FE      159          MOV    R6,A
010F EF      160          MOV    A,R7
0110 33      161          RLC    A
0111 FF      162          MOV    R7,A
0112 C3      163          CLR    C                ;ROTATE DIVIDEND LEFT
0113 E530    164          MOV    A,30H
0115 33      165          RLC    A
0116 F530    166          MOV    30H,A
0118 E52F    167          MOV    A,2FH
011A 33      168          RLC    A
011B F52F    169          MOV    2FH,A
011D E52E    170          MOV    A,2EH
011F 33      171          RLC    A
0120 F52E    172          MOV    2EH,A
0122 C3      173          CLR    C                ;TEST SUBTRACT MOST SIGNIFICANT BYTES
0123 952B    174          SUBB   A,2BH
0125 401B    175          JC     ZERO             ;JUMP IF QUOTIENT MS BYTE < DIVISOR MS BYTE
0127 7401    176          MOV    A,#1             ;ADD 1 TO QUOTIENT
0129 2E      177          ADD    A,R6
012A FE      178          MOV    R6,A
012B EF      179          MOV    A,R7
012C 3400    180          ADDC   A,#0
012E FF      181          MOV    R7,A
012F C3      182          CLR    C                ;SUBTRACT DIVISOR FROM DIVIDEND
0130 E530    183          MOV    A,30H
0132 952D    184          SUBB   A,2DH
0134 F530    185          MOV    30H,A
0136 E52F    186          MOV    A,2FH
0138 952C    187          SUBB   A,2CH
013A F52F    188          MOV    2FH,A
013C E52E    189          MOV    A,2EH
013E 952B    190          SUBB   A,2BH
0140 F52E    191          MOV    2EH,A
0142 DCC7    192  ZERO:    DJNZ   R4,DIV24
0144 22      193          RET
0145         194  PROG3:
             195  ;
             196  ;              DISPLAY AVERAGE OF FOUR NEW READINGS
             197  ;
             198  ;    This routine reads the period of the T0 input four times, then displays the
             199  ;    "speed" corresponding to the average of these four readings.
             200  ;
0145 7903    201          MOV    R1,#3            ;SET FOR 3 READINGS
0147 7820    202          MOV    R0,#20H          ;SET INDEX REGISTER FOR BOTTOM
0149 1182    203  P30:    ACALL  MEAS             ;TAKE 3 READINGS AND SAVE THEM
014B EB      204          MOV    A,R3
014C F6      205          MOV    @R0,A
014D 08      206          INC    R0
014E A68C    207          MOV    @R0,TH
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0150 08       208           INC    R0
0151 A68A     209           MOV    @R0,TL
0153 08       210           INC    R0
0154 D9F3     211           DJNZ   R1,P30
0156 1182     212           ACALL  MEAS              ;TAKE A 4TH READING, LEAVING IN R3,TH,TL
0158 7828     213           MOV    R0,#28H           ;SET INDEX REGISTER FOR TOP
015A 7903     214           MOV    R1,#3             ;SET COUNTER TO ADD FIRST 3 READINGS TO LAST ONE
015C E58A     215   P31:    MOV    A,TL              ;ADD FIRST THREE READINGS TO THE LAST ONE
015E 26       216           ADD    A,@R0
015F F58A     217           MOV    TL,A
0161 18       218           DEC    R0
0162 E58C     219           MOV    A,TH
0164 36       220           ADDC   A,@R0
0165 F58C     221           MOV    TH,A
0167 18       222           DEC    R0
0168 EB       223           MOV    A,R3
0169 36       224           ADDC   A,@R0
016A FB       225           MOV    R3,A
016B 18       226           DEC    R0
016C D9EE     227           DJNZ   R1,P31
016E 7902     228           MOV    R1,#2
0170 EB       229   P32:    MOV    A,R3              ;DIVIDE BY 4 (ROTATE RIGHT TWICE) FOR AVERAGE
0171 C3       230           CLR    C
0172 13       231           RRC    A
0173 FB       232           MOV    R3,A
0174 E58C     233           MOV    A,TH
0176 13       234           RRC    A
0177 F58C     235           MOV    TH,A
0179 E58A     236           MOV    A,TL
017B 13       237           RRC    A
017C F58A     238           MOV    TL,A
017E D9F0     239           DJNZ   R1,P32
0180 11C5     240           ACALL  CALC              ;CALCULATE THE WORD
0182 51B5     241           ACALL  SENDIT            ;SEND OUT THE WORD
0184 0140     242           AJMP   READY             ;GO TO SELECTED ROUTINE
0186          243   PROG4:
              244   ;
              245   ;        DISPLAY AVERAGE OF LAST FOUR WORDS SENT OUT
              246   ;
              247   ;   This routine sends out the average of the last four readings sent out.
              248   ;
0186 7827     249           MOV    R0,#27H
0188 7600     250   P4:     MOV    @R0,#0
018A 18       251           DEC    R0
018B B81FFA   252           CJNE   R0,#1FH,P4
018E 7820     253   P4A:    MOV    R0,#20H
0190 1182     254   P40:    ACALL  MEAS              ;MEASURE PERIOD
0192 11C5     255           ACALL  CALC              ;CALCULATE THE CODE
0194 EF       256           MOV    A,R7              ;SAVE THE CODE
0195 F6       257           MOV    @R0,A
0196 08       258           INC    R0
0197 EE       259           MOV    A,R6
0198 F6       260           MOV    @R0,A
0199 752800   261           MOV    28H,#0            ;INITIALIZE THE WORD TO SEND
019C 752900   262           MOV    29H,#0
019F 7927     263           MOV    R1,#27H
01A1 E529     264   P41:    MOV    A,29H             ;ADD TOGETHER LAST 4 RESULTS
01A3 C3       265           CLR    C
01A4 27       266           ADD    A,@R1
01A5 F529     267           MOV    29H,A
01A7 E528     268           MOV    A,28H
01A9 19       269           DEC    R1
01AA 37       270           ADDC   A,@R1
01AB F528     271           MOV    28H,A
01AD 19       272           DEC    R1
01AE B91FF0   273           CJNE   R1,#1FH,P41
01B1 7902     274           MOV    R1,#2
01B3 C3       275   P42:    CLR    C
01B4 E528     276           MOV    A,28H
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01B6 13       277          RRC    A
01B7 F528     278          MOV    28H,A
01B9 E529     279          MOV    A,29H
01BB 13       280          RRC    A
01BC F529     281          MOV    29H,A
01BE D9F3     282          DJNZ   R1,P42
01C0 AF28     283          MOV    R7,28H
01C2 AE29     284          MOV    R6,29H
01C4 51B5     285          ACALL  SENDIT          ;SEND OUT THE WORD
01C6 51D2     286          ACALL  RPS             ;READ PROGRAM SELECT
01C8 B40806   287          CJNE   A,#8,N4         ;JUMP TO N4 (& "READY") IF PROGRAM 4 NOT SELECTED
01CB 08       288          INC    R0
01CC B828C1   289          CJNE   R0,#28H,P40     ;GOTO P40 IF R0 NOT 28 (HEX)
01CF 80BD     290          SJMP   P4A
01D1 0140     291   N4:    AJMP   READY
              292   ;
              293   PROG5:
              294   ;
              295   ;   This routine advances the display in 45 degree steps to full scale, then steps down
              296   ;   to zero in 45 degree steps.  There is a 500ms delay between steps.
              297   ;
01D3 7F00     298          MOV    R7,#0
01D5 7E7F     299   P5:    MOV    R6,#07FH
01D7 51B1     300          ACALL  SD500           ;SEND THE WORD AND WAIT 500ms
01D9 7EFF     301          MOV    R6,#0FFH
01DB 51B1     302          ACALL  SD500           ;SEND THE WORD AND WAIT 500ms
01DD 0F       303          INC    R7
01DE BF04F4   304          CJNE   R7,#4,P5
01E1 7F03     305          MOV    R7,#3
01E3 7EFF     306   LP5:   MOV    R6,#0FFH
01E5 51B1     307          ACALL  SD500           ;SEND THE WORD AND WAIT 500ms
01E7 7E7F     308          MOV    R6,#7FH
01E9 51B1     309          ACALL  SD500
01EB 1F       310          DEC    R7
01EC BFFFF4   311          CJNE   R7,#0FFH,LP5
01EF 511B     312          ACALL  ZEROSC          ;RETURN TO ZERO
01F1 013D     313          AJMP   W               ;WAIT FOR KEY PRESS
01F3          314   PROG6:
              315   ;
              316   ;   This routine advances the display in 90 degree steps to full scale, then steps down
              317   ;   to zero in 90 degree steps.  There is a 500ms delay between steps.
              318   ;
01F3 7EFF     319          MOV    R6,#0FFH
01F5 7F00     320          MOV    R7,#0
01F7 51B1     321   LP6:   ACALL  SD500           ;SEND THE WORD AND WAIT 500ms
01F9 0F       322          INC    R7
01FA BF04FA   323          CJNE   R7,#4,LP6
01FD 1F       324   LP6A:  DEC    R7
01FE 51B1     325          ACALL  SD500           ;SEND THE WORD AND WAIT 500ms
0200 BF00FA   326          CJNE   R7,#0,LP6A
0203 511B     327          ACALL  ZEROSC          ;RETURN TO ZERO
0205 013D     328          AJMP   W               ;WAIT FOR KEY PRESS
0207          329   PROG7:
              330   ;
              331   :   This routine alternates between 3/8 and 5/8 scale ten times with 300ms delay
              332   ;   between steps, then waits 500ms before returning display to zero scale.
              333   ;
0207 7A0A     334          MOV    R2,#10          ;SET COUNTER
0209 7E7F     335   PR7:   MOV    R6,#07FH
020B 7F01     336          MOV    R7,#1
020D 51AD     337          ACALL  SD300           ;SEND OUT THE WORD AND WAIT 300ms
020F 7F02     338          MOV    R7,#2
0211 51AD     339          ACALL  SD300           ;SEND OUT THE WORD AND WAIT 300ms
0213 DAF4     340          DJNZ   R2,PR7          ;DO IT 10 TIMES
0215 51A5     341          ACALL  DLY500          ;WAIT 500ms
0217 511B     342          ACALL  ZEROSC          ;RESET TO ZERO SCALE
0219 0130     343          AJMP   START           ;LOOK FOR VALID PROGRAM
              344   ;
              345   ;
```

```
                346  ;               SUBROUTINES
                347  ;
                348  ;
021B 7F00       349  ZEROSC: MOV     R7,#0           ;RESET METER TO ZERO SCALE
021D 7E00       350         MOV     R6,#0
021F 4125       351         AJMP    RST
0221 7F03       352  FULLSC: MOV     R7,#03H         ;SET METER TO FULL SCALE
0223 7EFF       353         MOV     R6,#0FFH
0225 51B5       354  RST:    ACALL   SENDIT
0227 22         355
0228            356  SO:
                357  ;
                358  ;   This subroutine sends increasing 10-bit words in registers R7 & R6 to the SGD.
                359  ;
0228 51B5       360         ACALL   SENDIT          ;WRITE THE 10-BIT WORD TO SGD
022A 5130       361         ACALL   UP              ;INCREASE THE WORD VALUE
022C 30E2F9     362         JNB     ACC.2,SO        ;JUMP IF BIT 2 NOT SET
022F 22         363         RET
0230            364  UP:
                365  ;
                366  ;   This subroutine waits for a period of time = 10ms X DELAY read un, then
                367  ;   increases the 10-bit word by the INCREMENT SELECT amount.
                368  ;
0230 E590       369         MOV     A,P1            ;READ DELEY
0232 F4         370         CPL     A               ;COMPLEMENT ACC
0233 540F       371         ANL     A,#0FH          ;MASK OFF UPPER 4 BITS
0235 23         372         RL      A
0236 23         373         RL      A
0237 F9         374         MOV     R1,A
0238 B90002     375         CJNE    R1,#0,D10       ;JUMP IF DELAY SET FOR ZERO
023B 8006       376         SJMP    NODLY
023D 7B01       377  D10:    MOV     R3,#1           ;SET FOR 1 X 10ms DELAY
023F 5195       378  D10A:   ACALL   DLY10MS        ;DELAY 10MS x DELAY
0241 D9FC       379         DJNZ    R1,D10A
0243 E5B0       380  NODLY: MOV     A,P3            ;READ INCREMENT SELECT
0245 F4         381         CPL     A               ;COMPLEMENT ACC
0246 5403       382         ANL     A,#3            ;MASK OFF UPPER 6 BITS
0248 23         383         RL      A
0249 23         384         RL      A
024A 23         385         RL      A
024B 04         386         INC     A
024C 2E         387         ADD     A,R6            ;ADD INCREMENT TO R6
024D FE         388         MOV     R6,A            ;SAVE IT
024E E4         389         CLR     A
024F 3F         390         ADDC    A,R7            ;ADD CARRY TO R7
0250 FF         391         MOV     R7,A            ;SAVE IT
0251 22         392         RET
0252            393  SOD:
                394  ;
                395  ;   This subroutine sends out decreasing words at the rate set by DELAY and
                396  ;   step size determined by INCREMENT SELECT.
                397  ;
0252 51B5       398         ACALL   SENDIT          ;SEND OUT THE PRESENT WORD
0254 515A       399         ACALL   DOWN            ;DECREASE THE WORD
0256 50FA       400         JNC     SOD             ;DO IT AGAIN IF CARRY NOT SET
0258 411B       401         AJMP    ZEROSC
025A            402  DOWN:
                403  ;
                404  ;   Waits for 10ms x DELAY pot setting, then sends out decreasing values of words
                405  ;   in step sizes of 8 x INCREMENT SELECT + 1.
                406  ;
025A E590       407         MOV     A,P1            ;READ DELAY
025C F4         408         CPL     A               ;COMPLEMENT ACC
025D 540F       409         ANL     A,#0FH          ;MASK OFF UPPER FOUR BITS
025F 23         410         RL      A
0260 23         411         RL      A
0261 F9         412         MOV     R1,A            ;SAVE DELAY
0262 B90002     413         CJNE    R1,#0,D10S      ;JUMP IF DELAY SET FOR ZERO
0265 8004       414         SJMP    NDD
```

```
0267 5195    415  D10S:   ACALL  DLY10MS          ;DELAY 10ms x (DELAY +1)
0269 D9FC    416          DJNZ   R1,D10S
026B E5B0    417  NDD:    MOV    A,P3              ;READ INCREMENT SELECT
026D F4      418          CPL    A                 ;COMPLEMENT ACC
026E 5403    419          ANL    A,#3              ;MASK OFF UPPER 6 BITS
0270 23      420          RL     A                 ;MULTIPLY BY 8
0271 23      421          RL     A
0272 23      422          RL     A
0273 04      423          INC    A                 ;INSURE MINIMUM STEP
0274 C3      424          CLR    C                 ;CLEAR CARRY FOR SUBTRACTION
0275 CE      425          XCH    A,R6
0276 9E      426          SUBB   A,R6              ;SUBTRACT INCREMENT FROM R6
0277 CE      427          XCH    A,R6              ;SAVE IT
0278 E4      428          CLR    A                 ;CLEAR ACCUM FOR SUBTRACTION
0279 CF      429          XCH    A,R7
027A 9F      430          SUBB   A,R7              ;SUBTRACT BORROW FROM R7
027B 5403    431          ANL    A,#3              ;INSURE MAXIMUM WORD
027D CF      432          XCH    A,R7              ;SAVE IT
027E 22      433          RET
027F 00      434  DELAY:  NOP                      ;3us DELAY
0280 22      435          RET
0281         436  DMS10:
             437  ;
             438  ;   Produces a delay of 10ms x the value in R3.
             439  ;   Destroys R3 and timer readings.
             440  ;
             441  ;
0281 758AF0  442          MOV    TL,#LOW,(0-10000) ;LOAD TIMER FOR 10ms DELAY
0284 758CD8  443          MOV    TH,#HIGH(0-10000)
0287 C28D    444          CLR    TF                ;CLEAR TIMER FLAG
0289 D28C    445          SETB   TR                ;START TIMER
028B 308DFD  446  MS10W:  JNB    TF,MS10W          ;WAIT FOR TIMER FLAG TO BE SET
028E C28D    447          CLR    TF                ;CLEAR TIMER FLAG
0290 DBF9    448          DJNZ   R3,MS10W          ;WAIT RS x 10ms
0292 C28C    449          CLR    TR                ;STOP TIMER
0294 22      450          RET
             451  ;
0295 7B01    452  DLY10MS: MOV   R3,#1             ;SET R3 FOR 10ms WAIT
0297 80EB    453          SJMP   DMS10             ;WAIT 10ms
             454  ;
0299 7B0A    455  DLY100:  MOV   R3,#10            ;SET R3 FOR 100ms WAIT
029B 80E4    456          SJMP   DMS10             ;WAIT 100ms
             457  ;
029D 7B14    458  DLY200:  MOV   R3,#20            ;SET R3 FOR 200ms WAIT
029F 80E0    459          SJMP   DMS10             ;WAIT 200ms
             460  ;
02A1 7B1E    461  DLY300:  MOV   R3,#30            ;SET R3 FOR 300ms WAIT
02A3 80DC    462          SJMP   DMS10             ;WAIT 300ms
             463  ;
02A5 7B32    464  DLY500:  MOV   R3,#50            ;SET R3 FOR 500ms WAIT
02A7 80D8    465          SJMP   DMS10             ;WAIT 500ms
             466  ;
02A9 51B5    467  SD200:   ACALL  SENDIT           ;SEND THE WORD
02AB 80F0    468          SJMP   DLY200            ;WAIT 200ms
             469  ;
02AD 51B5    470  SD300:   ACALL  SENDIT           ;SEND THE WORD
02AF 80F0    471          SJMP   DLY300            ;WAIT 200ms
             472  ;
02B1 51B5    473  SD500:   ACALL  SENDIT           ;SEND THE WORD
02B3 80F0    474          SJMP   DLY500            ;WAIT 500ms
             475  ;
02B5         476  SENDIT:
             477  ;
             478  ;   This subroutine sends out a single word locate4d in R7 and R6.
             479  ;   Accumulator, R0 and R1 are destroyed.
             480  ;
02B5 D282    481          SETB   P0.2              ;SET CS HIGH
02B7 7902    482          MOV    R1,#02            ;SET COUNTER FOR 2 BITS OF R7
02B9 EF      483          MOV    A,R7              ;MOVE R7 TO A FOR SEND OUT
```

```
02BA 13      484          RRC    A                ;ALIGN R7 FOR SEND OUT
02BB 13      485          RRC    A
02BC 13      486          RRC    A
02BD 51C7    487          ACALL  SEND1            ;SEND OUT UPPER TWO BITS
02BF 7908    488          MOV    R1,#8            ;SET COUNTER FOR R6 SEND OUT
02C1 EE      489          MOV    A,R6             ;MOVE R6 TO ACCUM
02C2 51C7    490          ACALL  SEND1            ;SEND OUT LOWER 8 BITS
02C4 C282    491          CLR    P0.2             ;LOAD SGD
02C6 22      492          RET
02C7         493   SEND1:
             494   ;
             495   ;   This subroutine sends [R1] number of bits of the accumulator, starting
             496   ;   with the MSB over the IIC port.
             497   ;   Accumulator, R0 and R1 are destroyed.
             498   ;
02C7 33      499          RLC    A                ;ROTATE BIT TO CARRY
02C8 9281    500          MOV    P0.1,C           ;MOVE CARRY TO DATA OUT
02CA C280    501          CLR    P0.0             ;CLOCK LOW
02CC 00      502          NOP
02CD D280    503          SETB   P0.0             ;CLOCK HIGH
02CF D9F6    504          DJNZ   R1,SEND1         ;SEND NEXT BIT TILL DONE
02D1 22      505          RET
             506   ;
02D2 E5B0    507   RPS:   MOV    A,P3             ;READ PORT 3 FOR PROGRAM SELECT
02D4 F4      508          CPL    A                ;COMPLEMENT ACC
02D5 03      509          RR     A                ;ROTATE TO LSB's & MULT BY 2
02D6 540E    510          ANL    A,#0EH           ;MASK FOR PROGRAM SELECT * 2
02D8 DD      511          RET
             512   END

ASSEMBLY COMPLETE, 0 ERRORS FOUND
```

```
ACC ..... D ADDR   00E0H     PREDEFINED
CALC ..... C ADDR   00C5H
D10 ..... C ADDR   023DH
D10A ..... C ADDR   023FH
D10S ..... C ADDR   0267H
DCX ..... C ADDR   0073H
DELAY ..... C ADDR   027FH     NOT USED
DIV24 ..... C ADDR   010BH
DLY100 ..... C ADDR   0299H     NOT USED
DLY10MS ..... C ADDR   0295H
DLY200 ..... C ADDR   029DH
DLY300 ..... C ADDR   02A1H
DLY500 ..... C ADDR   02A5H
DMS10 ..... C ADDR   0281H
DOWN ..... C ADDR   025AH
DP1 ..... C ADDR   006DH
FULLSC ..... C ADDR   0221H
GFS ..... C ADDR   00C0H
GZS ..... C ADDR   00BDH
HT ..... C ADDR   00B7H
IE ..... D ADDR   00A8H     PREDEFINED
JMPTBL ..... C ADDR   004CH
LP5 ..... C ADDR   01E3H
LP6 ..... C ADDR   01F7H
LP6A ..... C ADDR   01FDH
MEAS ..... C ADDR   0082H
MS10W ..... C ADDR   028BH
N4 ..... C ADDR   01D1H
NDD ..... C ADDR   026BH
NODLY ..... C ADDR   0243H
NZS ..... C ADDR   00D0H
P0 ..... D ADDR   0080H     PREDEFINED
P1 ..... D ADDR   0090H     PREDEFINED
P3 ..... D ADDR   00B0H     PREDEFINED
P30 ..... C ADDR   0149H
P31 ..... C ADDR   015CH
P32 ..... C ADDR   0170H
P4 ..... C ADDR   0188H
P40 ..... C ADDR   0190H
P41 ..... C ADDR   01A1H
P42 ..... C ADDR   01B3H
P4A ..... C ADDR   018EH
P5 ..... C ADDR   01D5H
PR7 ..... C ADDR   0209H
PROG0 ..... C ADDR   005CH
PROG1 ..... C ADDR   0068H
PROG2 ..... C ADDR   007AH
PROG3 ..... C ADDR   0145H
PROG4 ..... C ADDR   0186H
PROG5 ..... C ADDR   01D3H
PROG6 ..... C ADDR   01F3H
PROG7 ..... C ADDR   0207H
READY ..... C ADDR   0040H
ROTL ..... C ADDR   00F0H
RPS ..... C ADDR   02D2H
RST ..... C ADDR   0225H
RTH ..... D ADDR   008DH     PREDEFINED
RTL ..... D ADDR   008BH     PREDEFINED
SD200 ..... C ADDR   02A9H     NOT USED
SD300 ..... C ADDR   02ADH
SD500 ..... C ADDR   02B1H
SEND1 ..... C ADDR   02C7H
SENDIT ..... C ADDR   02B5H
SO ..... C ADDR   0228H
SOD ..... C ADDR   0252H
START ..... C ADDR   0030H
TF ..... B ADDR   008DH     PREDEFINED
TH ..... D ADDR   008CH     PREDEFINED
TL ..... D ADDR   008AH     PREDEFINED
TR ..... B ADDR   008CH     PREDEFINED
UP ..... C ADDR   0230H
W ..... C ADDR   003DH
W20 ..... C ADDR   009AH
W21 ..... C ADDR   009FH
W22 ..... C ADDR   00ADH
W23 ..... C ADDR   00B2H
ZERO ..... C ADDR   0142H
ZEROSC ..... C ADDR   021BH
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Using the NE/SA5234 amplifier

Application report AN1651

Author: L. Hadley

I. SUMMARY

The NE/SA5234 is a unique low-voltage quad operational amplifier specifically designed to operate in a broadly diverse environment. It is an enhanced pin-for-pin replacement for the LM324 category of devices. Supply conditions can range from 1.8V to 6.0V with a resultant current drain of 2.8mA,-700μA per op amp.

Most notable are the input and output dynamic range characteristics of the individual op amps. The common-mode input voltage can actually exceed the positive and negative supply rails by 250mV with no danger of output latching or polarity reversal. In addition, the output of each op amp will swing to within 50mV of the supply rails over the full supply range.

The frequency related characteristics are also above average for low voltage devices in this class. Internal unity gain compensation makes the NE5234 very resistant to any tendency to oscillate in low closed-loop gain configurations. Even so, a unity-gain bandwidth of 2.5MHz is retained. Slew rate is 0.8V/μs and each op amp will settle to a 1% of nominal level within 1.4μs.

II. DETAILED DESCRIPTION

Input Stage

The input differential amplifier consists of a compound transistor structure of parallel NPN and PNP transistors which account for the unique over-drive characteristics of the NE5234. Referring to Figure 1, it is seen that the NPN pair, Q1 and Q2, allow the input to operate in the common-mode input voltage range of 1V above V_{EE}. This region is designated the N-mode region in Figure 3a. Operation in the common-mode range below 1V transfers the input stage into the P-mode of operation.

In the N-mode operating condition, collector current from Q1 and Q2 is summed in the output emitter node of Q10 and Q12 respectively. Q1's base is the non-inverting input and Q2's base the inverting input node for the amplifier.

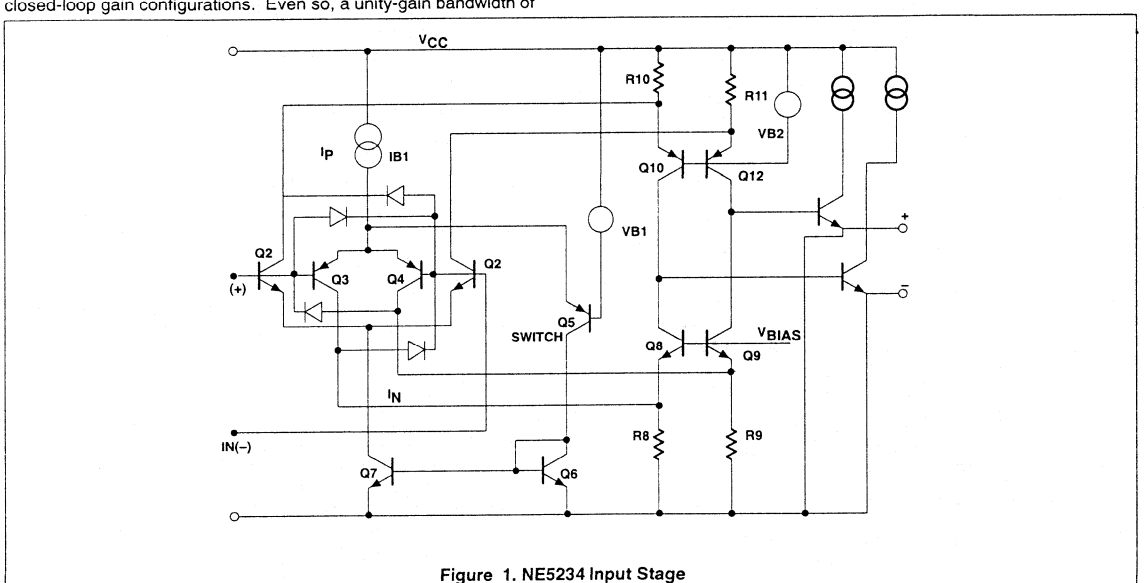


Figure 1. NE5234 Input Stage

Linear operation between the two modes is governed by a current steering circuit consisting of Q5,6 and 7 in conjunction with voltage reference VB1. Operation in the

N-region of the common-mode range will automatically cause Q5 to transfer the IB1 current source to Q7 and the NPN transistor pair Q1 and Q2. Operation below the 1V level at the inputs allows the current from IB1 to be fed directly to Q3 and Q4 emitters giving them priority in processing the signal and linearizing their transfer function. (The sum of the NPN and PNP input pair currents remain constant.)

Operation in the common-mode range near the positive supply rail would normally cause the input stage NPN transistor's base collector junction to become forward biased (base current flow directly to the collector circuit) reversing the collector current flow direction. In a conventional op amp, this would have the adverse effect of reversing the output signal polarity as the operating region is traversed by the input signal. (see Figure 2)

To prevent this from occurring, large geometry diode-connected transistors are cross-connected to the opposite NPN collector, (Q1, Q2). This current, in turn, is summed at the emitter of Q12 pulling it above the V_{CC} rail voltage and preventing polarity reversal. The inverse condition occurs when Q2 is driven above the positive rail, with Q10 emitter being pulled up and signal polarity preserved. (See Figure 1)

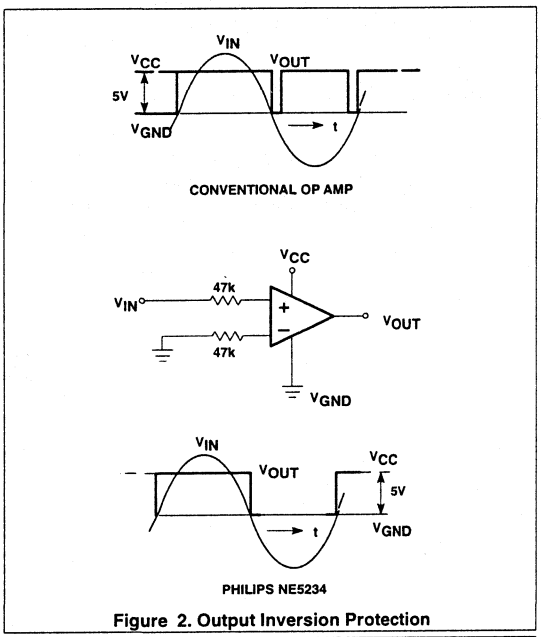
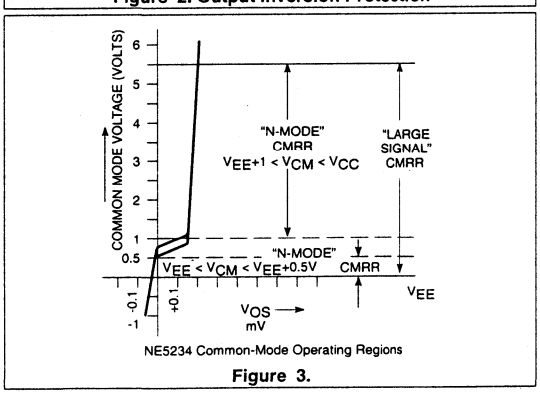


Figure 2. Output Inversion Protection



NE5234 Common-Mode Operating Regions

Figure 3.

For negative going input signals, which drive the inputs toward the V_{EE} rail and below, another set of diode-connected transistors come into operation. These steer the current from the input into Q8 or Q9 emitter circuits again preventing the reversal effect.

Figure 3 shows graphically how the N and P mode transitions relate to the common-mode input voltage and the offset voltage V_{OS}.

Intermediate Amplifier and Output Stage (Figure 4)

The intermediate stage is isolated from the input amplifier by emitter followers
to prevent any adverse loading effect. This stage adds gain to the over all amplifier and translates levels for the following class-AB current-control driver. Note that I_2 is the inverting input and I_1 the non-inverting input. The output is taken from multiple collectors on the non-inverting side and provides matching for the following stage.

Class-AB control of the output stage is achieved by Q61 and Q62 with the associated output current regulators. These act to monitor the smallest current of the non-load supporting output transistor to keep it in conduction. Thus, neither Q71 or Q81 is allowed to cutoff but is forced to remain in the proper Class-AB region.

Overload protection is provided by monitor circuits consisting of R76-D2 for sinking and R86-D3 for sourcing condition at the output. When the output current, source or sink, reaches 15 milliamperes, drive current to the stage is shunted away from current sources IB6 or IB9 reducing base current to driver transistors Q72 and Q82 respectively.

The prevention of saturation in the output stage is achieved by saturation detectors Q78 and Q88. When either Q71 or Q81 approaches saturation, current is shunted away from the driver transistors, Q72 or Q83 respectively.

III. CHARACTERISTICS

Internal Frequency Compensation

The use of nested Miller capacitors C2 through C6, in the intermediate and output sections, provides the overall frequency compensation for the amplifier. The dominant pole setting capacitor, C2, provides a constant 6dB/octave roll-off to below the unity gain frequency of 2.5MHz. Figure 5 shows the measured frequency response plot for various values of closed-loop gains.

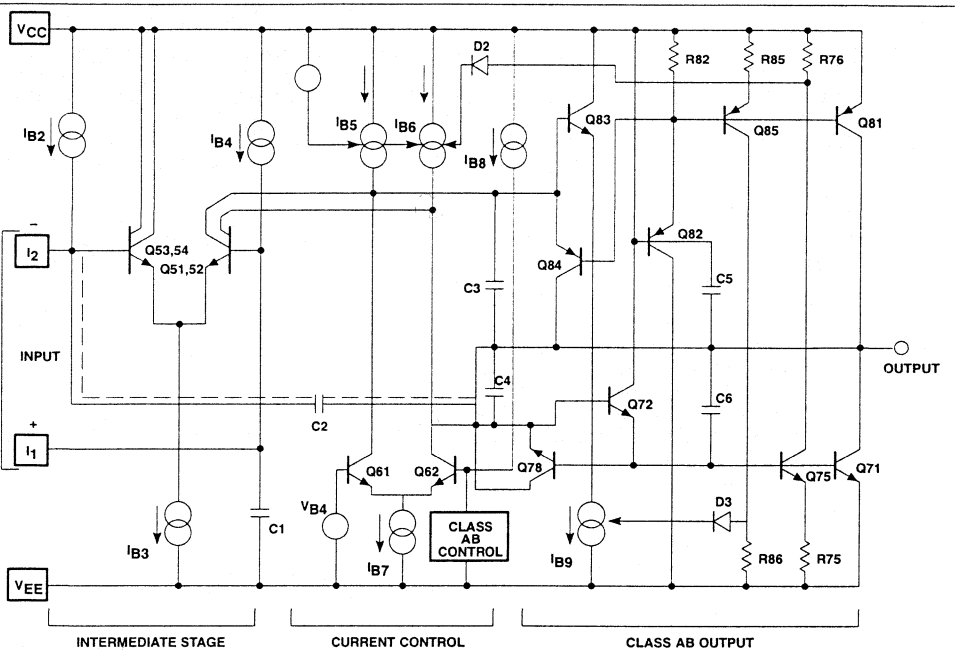


Figure 4.

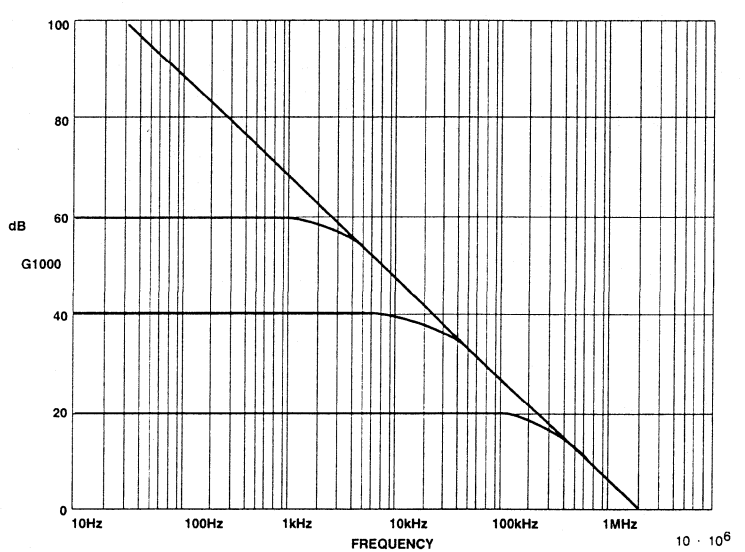


Figure 5. NE5234 Closed Loop Gain vs Frequency

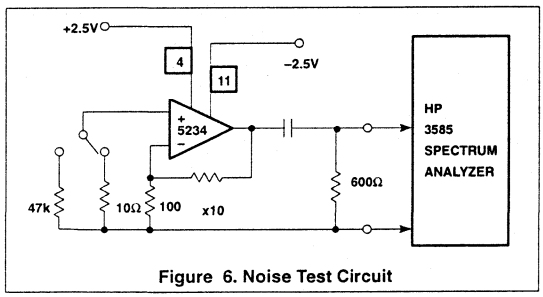


Figure 6. Noise Test Circuit

IV. NOISE REFERRED TO THE INPUT

The typical spectral voltage noise referred to each of the op amps in the NE/SA5234 is specified to be 25nV/√Hz. Current noise is not specified. In the interest of providing a balance of information on the device parameters, a small sample of the standard NE5234s, were tested for input noise current. While this data does not represent a specification, it will give the designer a ball park figure to work with when beginning a particular design with the device. For completeness I have provided the corresponding spectral noise voltage data for the same sample. The data was taken using an HP3585A spectrum analyzer which has the capability of reading noise in nV/√Hz.

The test circuit is shown in Figure 6. As is typical for such measurements the amplifier under test is terminated at its input first with a very low resistance, for the voltage noise reading, followed by the same test with a high value of resistance to register the effect of current noise. The amplifier is set to a non-inverting closed-loop gain of 20dB. Dual supply operation was chosen to allow direct termination of the input resistors to ground.

The measurements were made over the range from 200Hz to 2kHz. Each sample is measured at 200Hz, 500Hz, 1kHz and 2kHz. The data is averaged for each frequency and then the small sample distribution is derived statistically giving the standard deviation relative to the mean.

Referring to the graph in Figure 7a, the equivalent voltage noise is seen to average 18 nV/√Hz. The 95% confidence interval is determined to be approximately one nV/√Hz. The majority of the errors which contribute to this measurement are due to the thermal noise of the parallel combination of the feedback resistor network, in addition to the 10Ω termination resistor on the non-inverting input. At 300° Kelvin a 10Ω resistor generates 0.4 nV/√Hz and the feedback network's equivalent resistance of 90Ω generates 1.2nV/√Hz. Their order-of-magnitude difference from the main noise sources allows them to be neglected in the overall calculation of total stage noise.

Noise current is measured across a 47kΩ resistor and averaged in the same manner. The thermal noise generated by this large resistance is not insignificant. At room temperature it is 28nV/√Hz and must be subtracted from the total noise as measured at the output of the op amp in order to arrive at the equivalent current generated noise voltage. Figure 7b shows the derived current noise distribution for the small sample of 10 NE5234 devices. The result shows that noise current in the 200Hz to 2kHz frequency is typically 0.2pA/√Hz. The 1/f region was not determined for either current or voltage noise.

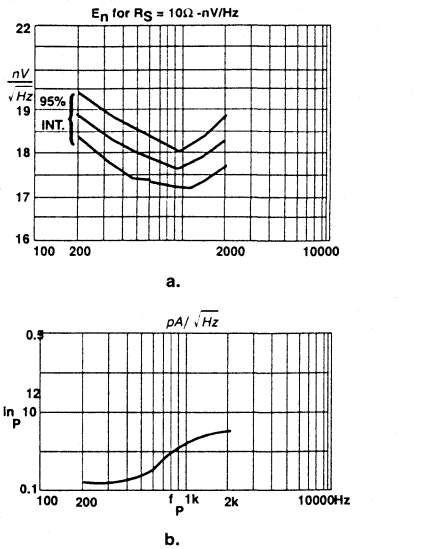


Figure 7. Typical Noise Current and Voltage vs Frequency

V. GUIDE LINES FOR MINIMIZING NOISE

When designing a circuit where noise must be kept to a minimum, the source resistances should be kept low to limit thermally generated degradation in the overall output response. Orders-of-magnitude should be kept in mind when evaluating noise performance of a particular circuit or in planning a new design. For instance, a transducer with a 10kΩ source resistance will generate 2μV of RMS noise over a 20kHz bandwidth. Using the graphical data above, total noise from a gain stage may be calculated.-

Amplifier Noise Voltage (EQ. 1.)

$$25nV/\sqrt{Hz} \cdot \sqrt{BW} = 3.5\mu V_{RMS}$$
$$BW = 10kHz$$

Noise from source 10kΩ Resistance –

Noise Voltage from source resistance (EQ. 2.)

$$14nV/\sqrt{Hz} \cdot \sqrt{BW} = 20\mu V_{RMS}$$

Current generated noise (EQ. 3.)

$$0.2pA/\sqrt{Hz} \cdot 10^3 \cdot \sqrt{BW} = 0.28\mu V_{RMS}$$

The total noise is the root-to-sum-of-the-squares of the individual noise voltages –

$$En = \sqrt{(3.5)^2 + (2.0)^2 + (0.28)^2} \quad \text{(EQ. 4.)}$$
$$= 4.04\mu V_{RMS}$$

To determine the signal-to-noise ratio of the stage we must first choose a stage gain, make it 40dB, and a signal voltage magnitude from the transducer which we will set at $10mV_{RMS}$. The resulting signal-to-noise ratio at the output of this stage is determined by first multiplying the gain times the signal which gives $1V_{RMS}$ with a

resultant noise of 400mV$_{RMS}$. The signal-to-noise ratio is calculated as

$$S/N \quad 20\log_{10}(1.0/4x10^{-4}) = 68dB \qquad \text{(EQ. 5.)}$$

This is quite adequate for good quality audio applications.

Next assume that the bandwidth is cut to 3.0kHz with an input of 1mV$_{RMS}$. The RMS noise is modified by the ratio of the root of the noise channel bandwidths.

$$\left[\frac{\sqrt{3x10^3}}{\sqrt{20x10^3}}\right] \cdot EN = 1.6\mu V_{RMS} \qquad \text{(EQ. 6.)}$$

Amplified Noise = 160μV$_{RMS}$

$$S/N \quad 20\log_{10}\left[\frac{100x10^{-3}}{1.6x10^{-4}}\right] \qquad \text{(EQ. 7.)}$$

$$= 56dB$$

A 56dB S/N will provide superior voice channel communications .

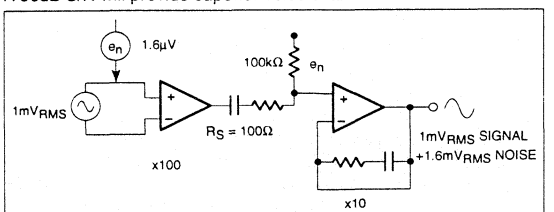


Figure 8.

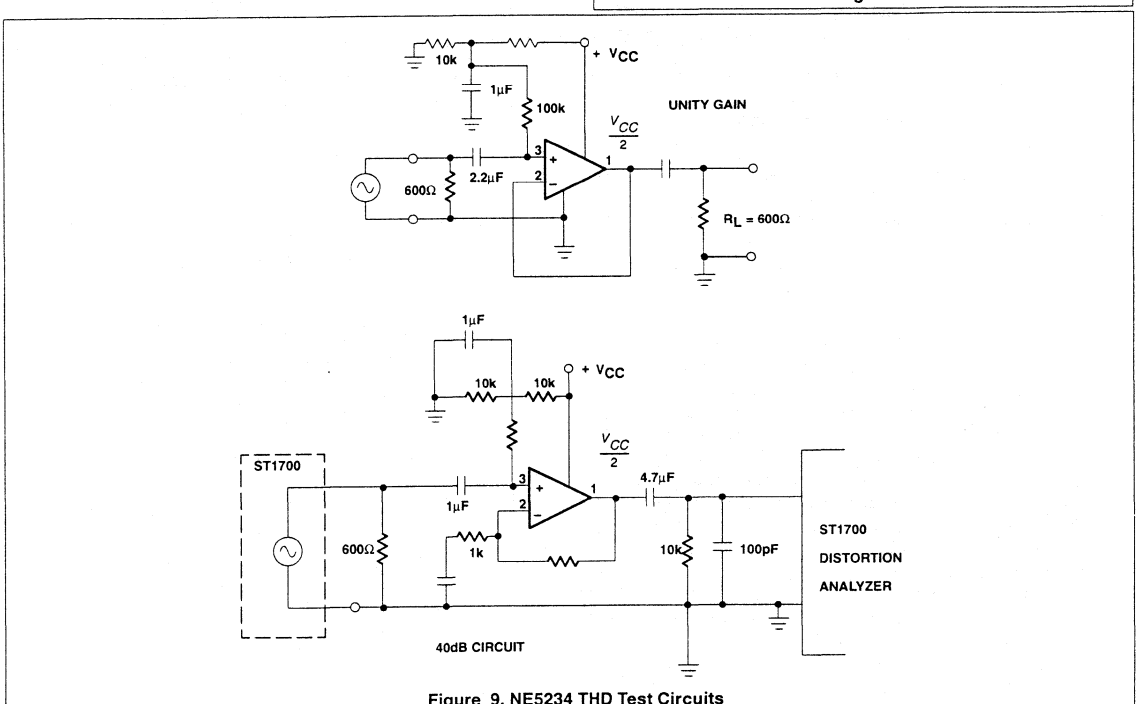


Figure 9. NE5234 THD Test Circuits

VI. MULTIPLE STAGE CONSIDERATIONS

Since multiple noise generators are non-coherent, their total effect is the root-of-the-sum-of-the-squares of the various noise generators at a given amplifier input.

This makes orders-of-magnitude lower noise sources less important than the higher magnitude source. Therefore, when considering the combined signal-to-noise of multiple stages of gain, the first stage in a chain dominates making its design parameters the most critical. For this reason it is good practice to make the preamp stage gain as high as practical to boost signal levels to the second stage allowing at least an order-of-magnitude above the second-stage noise. For instance, a signal input which exceeds the input noise of the following stage by a factor of 10:1 will only be degraded by 0.5% or -46dB, neglecting the first-stage noise. If we use the preceding example with a first-stage output signal of 100mV$_{RMS}$ and a 56dB S/N, and an output noise of 0.16mV. Following this with a 10kHz band limited gain-of-10 second-stage, with a 100kΩ noise source at the non-inverting input, the combined S/N is calculated as follows: (assume a 100Ω source resistance from amplifier #1)

The Second stage output noise is:

$$\left[\sqrt{(0.163x10^{-3})^2 + \left(\sqrt{4KT \cdot 100 \cdot 10,000}\right)^2}\right] \cdot 10 \qquad \text{(EQ. 8.)}$$

$$= 1.6mV$$

$$K = \text{Boltzman'sConstant} = 1.38\times10^{-23}\ \frac{\text{Joule}}{\text{DegKelvin}} \qquad \text{(EQ. 9.)}$$

$$T = 300^{\circ}K\ ;\ BW = 10kHz$$

The amplified output signal = $1V_{RMS}$

$$S/N = 20\log_{10}\left(\frac{1}{1.6\times10^{-3}}\right) \qquad \text{(EQ. 10.)}$$

$$= 56dB$$

Note that there is no effect from the second-stage thermally generated resistor noise due to the dominating effect of the first-stage amplified noise being much greater than the input noise of the second-stage. In addition the equivalent noise resistance of the second-stage is essentially the output resistance of the first-stage plus any series resistance used in coupling the two. This is the parallel combination of source resistance with input terminating or biasing resistance.

VII. LOW HARMONIC DISTORTION

The NE/SA5234 is extremely well adapted to reducing harmonic distortion as it relates to signal level and head room in audio and instrumentation circuits. Its unique internal design limits overdrive induced distortion to a level much below that experienced with other low voltage devices. As will be shown, the device is capable of operating over a wide supply range without causing the typical clipping distortion prevalent in companion operational amplifiers of this class.

A series of tests are shown to allow you to see just how resistant this device is to generating clipping distortion. Two different gain configurations were chosen to demonstrate this particular feature: unity gain non-inverting and 40dB non-inverting. The test set-up was as shown in Figure 9. The Harmonic Distortion analyzer used to make the measurements was a Storage Technology ST1700. The test frequency is 1kHz. For single supply operation, as previously covered, the amplifier should be biased to half the supply voltage to minimize distortion. Operation with dual supplies is simpler from a parts count standpoint as isolation capacitors are not required. Also the time constants associated with charging and discharging these is eliminated . Figure 10a,b and c shows the total harmonic distortion in percent versus input voltage level at 1kHz in V_{RMS} for a non-inverting, unity gain NE5234. The load on the amplifier output is 10kΩ. Beginning with a supply voltage of 1.8V and an input level of $0.1V_{RMS}$, distortion is well below 0.2% ad remains there up to an input level just over $0.5V_{RMS}$ ($1.4V_{P-P}$) and increases to 0.4% for for $0.6V_{RMS}$ ($1.7V_{P-P}$).

For a 2V supply, the input levels increase to $0.65V_{RMS}$ and $0.7V_{RMS}$, respectively for similar levels of distortion. With a supply voltage of 3.0V the input may be increased to $1V_{RMS}$ before THD rises to 0.2% and $1.1V_{RMS}$ for only 0.8% THD. Operation with a 600Ω load will only raise the THD figures slightly . By way of comparison, Figure 10c shows the greatly reduced dynamic range experienced when an LM324 is plugged into the test socket in place of the NE5234. Note that The THD is completely off scale for the case of 1.8 and 2.0V supply, then is barely usable for the low level end of the 3.0V supply example. Figure 11a, b, and c demonstrates the effect on harmonic distortion when closed loop gain is increased to 40dB in the non-inverting mode. It is evident that little increase in THD levels result. The graphs for the 2.0 and 3.0V supply case also include additional information on the effect of a 600Ω load on distortion.

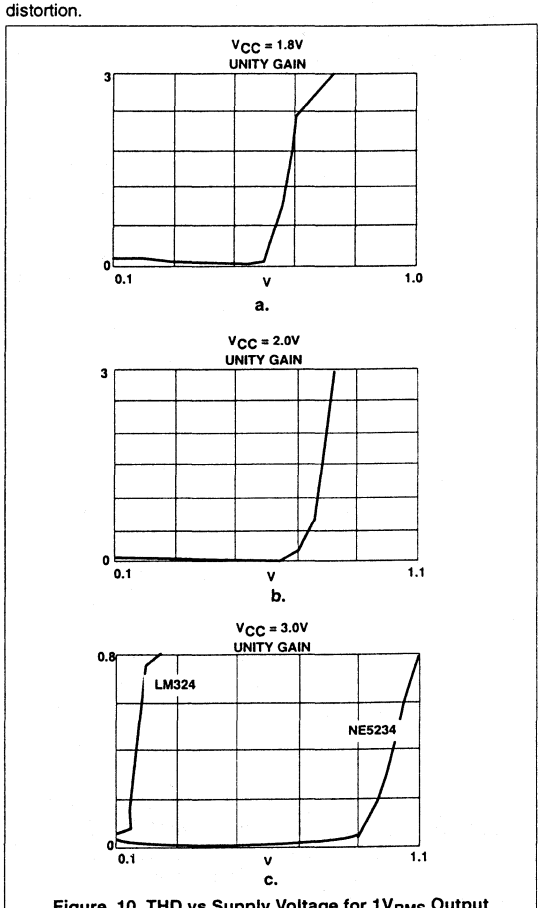


Figure 10. THD vs Supply Voltage for $1V_{RMS}$ Output

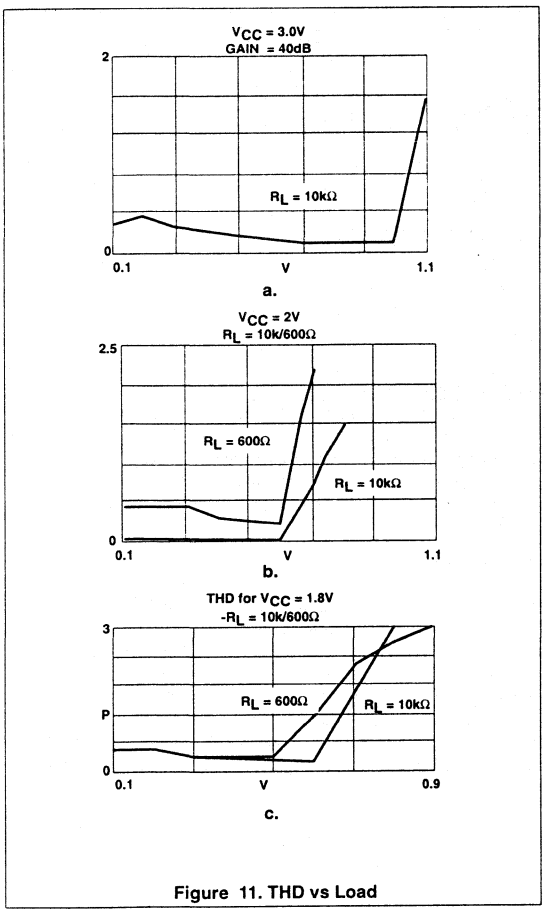


Figure 11. THD vs Load

VIII. GAIN-BANDWIDTH VS CLOSED LOOP FREQUENCY RESPONSE

Figure 5 shows the small signal frequency response of the NE5234 versus closed-loop gain in dB. The test circuit is shown in Figure 6. The plot is taken from measured data and thus shows how each value of closed-loop gain coincides with the open-loop response curve. The NE/SA5234's open-loop gain response has a uniform 6dB/octave roll-off which continues beyond 2.5MHz. This factor guarantees each op amp in the IC a high stability in virtually any gain configuration. In making these measurements, dual supplies of ±2.5V were used in order to allow a grounded reference plane and no coupling capacitors which might cause frequency related errors.

A critical parameter which affects the reproduction quality of complex waveforms is the gain-bandwidth-product of the operational amplifier. Essentially, this is a measure of the maximum frequency handling characteristics of any operational amplifier for a given closed-loop gain. As is evident from the graph, the NE/SA5234 has a 2.5MHz unity gain cross-over frequency — much higher than most other low voltage op amps. For comparison, the μA741 has a gain-bandwidth-product of 1MHz, as do the LM324 and the MC3403.

IX. LOOP-GAIN

The dynamic signal response of any closed-loop amplifier stage is a function of the Loop-gain of that particular stage. Loop-gain is equal to the open-loop gain in dB, at a given frequency, minus the closed-loop gain of the stage. The greater the Loop-gain, the lower the transfer function error of the device. Essentially, any parametric error is reduced by the factor of the Loop-gain. This includes output resistance and output signal voltage accuracy. It is good practice then to maximize Loop-gain to the degree that stage gain may be sacrificed for bandwidth. In some cases it is actually better to use two stages of gain in order to preserve signal quality than to use one high gain stage. Of course, there is a trade-off between the aforementioned factors that affect the signal-to-noise ratio of the stage and optimizing the Loop-gain. For example, a voice-band audio stage which requires 3kHz bandwidth, should be limited to a closed-loop gain of 40dB for lowest distortion in the output signal. For higher quality audio applications requiring a 20kHz bandwidth, the closed-loop gain must be limited to 20dB. This results in a Loop-gain of 20dB at the highest signal frequency.

A second consideration in the list of frequency dependent parameters is the effect of amplifier slew rate. Not only is it frequency dependent but it is also a function of signal amplitude, as we shall see in the next section.

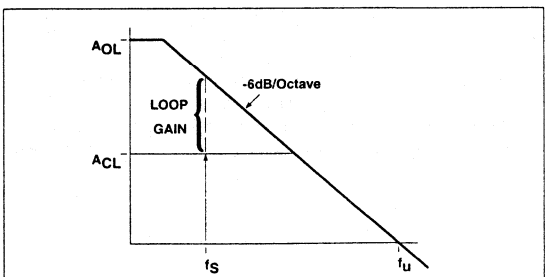


Figure 12.

X. SLEW RATE RESPONSE

The slew rate of an operational amplifier determines how fast it can respond to a signal, and is measured in volts-per-microsecond. The NE5234 has a typical slew rate of 0.8V/μs. Let us see just what this means in terms of signal handling capability. If a sinusoidal input signal, V_S, is used as reference, it is specified by its frequency and peak amplitude, V_P as follows:

$$V_S = V_P \sin (2\pi f t) \qquad \text{(EQ. 11.)}$$

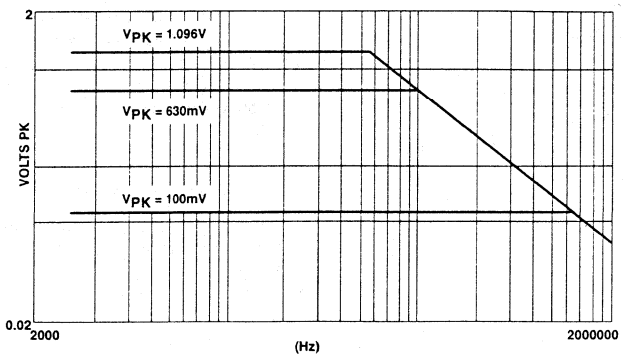


Figure 13. Slew Rate Limiting Amplitude vs Frequency

Slew Rate (SR) is the time-rate-of-change of the signal voltage during any complete cycle, that is over the range of 0 to 2π. This amounts to taking the time derivative of the sine wave which results in multiplying the cosine by the factor '2πf'.

An example of the trade off between signal amplitude and frequency is shown below for the NE5234 slew rate of 0.8V/μs. As shown in Figure 13, the maximum allowable amplitude signal which can be reproduced is determined by the slew rate response line which gives peak output volts versus frequency in Hertz.

Mathematically, slew rate is determined, by the equation below, as the derivative of the sine wave signal. The resultant slew rate function changes with both frequency and amplitude.

Slew Rate $= V_P\ (2\pi\ f)\ \cos\ (2\pi\ f\ t)$

Note that maximum slew rate occurs where the input sine wave signal crosses the values of 0, π, and 2π on the radian axis. To get a feel for what this means in regards to the typical low voltage circuit, let us consider a $1V_{RMS}$ sinusoidal input to a unity gain amplifier. The peak voltage in the above equation is 1.414V. One can then calculate the required slew rate to faithfully reproduce this signal for various signal frequencies. Or with a given slew rate and a required peak signal amplitude, the maximum frequency before slew rate limiting occurs may be determined. For example using the above amplitude of $1V_{RMS}$, and the slew rate of the NE5234 which is 800,000V/sec, one determines that the highest frequency component which may be reproduced before slew rate distortion occurs is:

800,000 V/sec / 2π • 1.414 volts peak = 90,090Hz. A graphical representation of this relationship is shown in Figure 13. By using this graph along with the information in the preceding Figure 10 and Figure 11, which relate usable signal levels versus power supply voltage, the dynamic behavior of a particular design may be predicted. For instance, given a single supply configuration operating at 2.0V, Figure 10b shows an upper limit to input amplitude of $0.7V_{RMS}$, or about 1V peak for 1% THD. Using this level with the data in Figure 13 leads to a figure of 116kHz as an upper frequency limit for a unity gain amplifier stage operating at 2V DC.

$$\frac{dV_S}{d\,t} = V_P\ \omega \cos\ \omega t = \text{Slew Rate} \qquad \text{(EQ. 12.)}$$

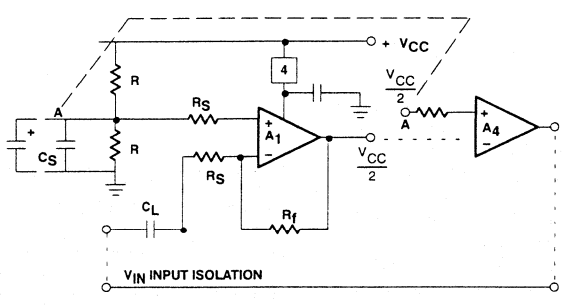


Figure 14. Single Supply Biasing in Cascade

XI. PROCEDURES

Single Supply Operation

When the NE/SA5234 is used in an application where a single supply is necessary, input common-mode biasing to half the supply is recommended for best signal reproduction, Referring to Figure 14, a simplified inverting amplifier input stage is shown with the simplest form of resistive divider biasing. The value of the divider resistance R is not critical and may be increased above the 10kΩ value shown as long as the bias current does not interfere with accuracy due to DC loading error. However the divider junction must be kept at a low AC impedance This is the purpose of bypass

capacitor C_S. Its use provides transient suppression for signals coming from the supply bus. A low cost 0.1μF ceramic disk or chip capacitor is recommended for suppressing fast transients in the microsecond and sub-microsecond region.
Foil capacitors are simply too inductive for any high frequency bypass application and should be avoided. If low frequency noise such as 60Hz or 120Hz ripple is present on the supply bus, an electrolytic capacitor is added in parallel as shown. The common-mode input source resistance, R_S, should also be matched within a reasonable tolerance for maximizing the rejection of induced AC noise.

The output of the first stage is now fixed at the common mode bias voltage and the amplified AC signal is referenced to this constant value. Capacitive coupling to the inverting input is of course required to prevent the bias voltage from being multiplied by the stage gain. Second stage biasing may now be provided by the output voltage of the first stage if non-inverting operation is used in the former. For lowest noise in a high gain input stage, the magnitude of the input source resistance is critical; low values of resistance are preferred over high values to minimize thermally generated noise.

Non-Inverting Stage Biasing

Non-inverting operation of an amplifier stage with single supply is similar to the previous example but the bias resistor R_S must now be sufficiently high to allow the signal to pass
without significant attenuation. The input source resistance reflects the output resistance of the preceding stage or other sourcing device such as a bridge circuit of relatively high impedance. A simple rule of thumb is to make the bias resistor an order of magnitude larger than the generator resistance. Again the feed back network must be terminated capacitively. In this case R1 and the generator resistance should be matched and then R_S is matched to the feedback resistance ,R_F.

In all cases proper bypassing of the NE5234 supply leads (Pins 4 and 11) is very important particularly in a high noise environment. Bypass capacitors must be of ceramic construction with the shortest possible leads to keep inductance low. Chip capacitors are superior in this respect complimenting the increased use of surface mounted integrated devices. Note that both the NE5234D and the automotive grade SA5234D are available and are the surface mount versions of the device.

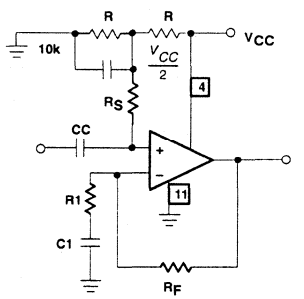


Figure 15. Non-Inverting Biasing

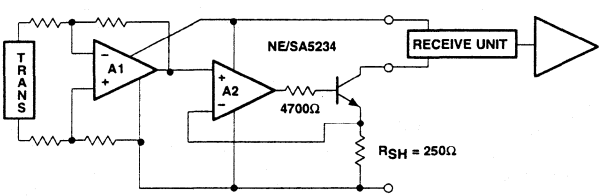
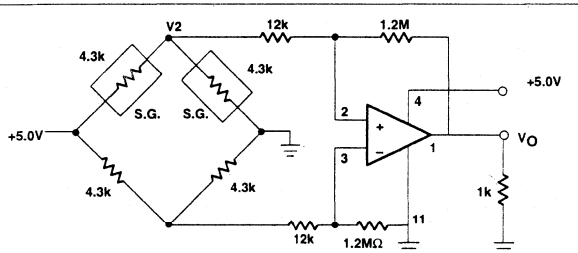


Figure 16. A 4-20mA Current Loop



$\lvert V_2 - V_1 \rvert$	V_O
5.9mV	0.5V
25.6mV	2.50V
46.6mV	4.63V

S.G.: Matched Strain Gauge elements

Figure 17. Strain Gauge Amplifier

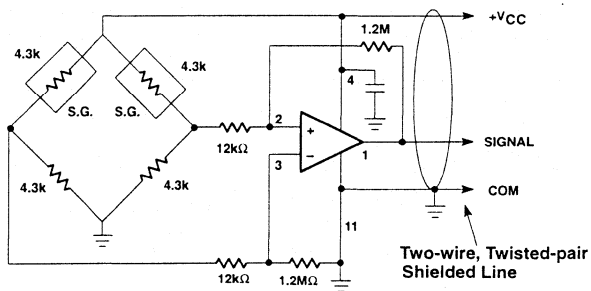


Figure 18. Remote Strain Gauge

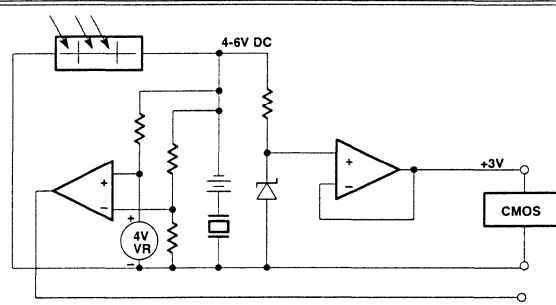


Figure 19. Solar Regulator

APPLICATIONS EXAMPLES

Instrumentation

Strain Gauge Bridge Amplifier

The circuit below shows a simple strain gauge circuit with a gain of 100 (40dB) and operated from a single supply. The chart illustrates the transfer function of the circuit for a single order-of-magnitude signal differential range from the bridge beginning with 5mV up to 50mV. The circuit is operated from a single 5V supply, but could equally as well be configured to use a dual balanced supply. It is immediately evident that the wide common-mode output range of the NE5234 is very advantageous in handling this wide range of signals with good linearity due to this feature.

A variation on this particular idea is the remote strain gauge circuit operating from a three wire line, one of which is the shield. This full-differential input circuit has balanced

input resistance to afford good common-mode noise rejection characteristics. Resistors are metal film or deposited carbon. Supply leads must be carefully bypassed close to the NE/SA5234 with ceramic or chip monolithic capacitors to give optimum noise performance. As shown, an auxiliary sub-regulator may be added to improve the overall DC stability of the bridge signal voltage. A regulator capable of providing the necessary few milliamperes at somewhat reduced voltage for the transducer is shown in one of the following examples. This makes use of one of the op amps in the same device package to provide the voltage regulation. Note that the use of multiple op amps within a single package minimizes the possibility of thermal drift and mismatched response from various DC parameters.

Multiple sets of transducers may be constructed from The NE/SA5234 or the NE5234D surface mount device to form a compact and stable instrumentation package. This is useful for transducer applications in

the measurement of pressure, strain, position and temperature, which have similar circuit configurations. First order temperature compensation of the transducers such as semiconductor strain gauges, or resistive units may be achieved by using one of the gauges as a reference device only. It is thermally coupled to the same member as the active gauge, as shown in the example. (Figure 18)

A 4 to 20mA Current Loop

Some instrumentation installations require the 4-20mA current loop. This addition to the above bridge transducer circuit examples is demonstrated in Figure 16.

This circuit makes use of the remote transducer bridge previously described and adds current loop signaling capability. The voltage-to-current converter consists of an additional op amp from the same NE/SA5234 package combined with a single transistor to drive the current loop. The sensitivity is actually in mA/V, or transconductance, which is equal to $1/R_{SH}$. This sensitivity in this particular example is set to 4mA/V. Thus, with a bridge amplifier having a differential gain of 100, an input of 10mV will produce a 4mA output current and 50mV will produce a 20mA output. Of course the line resistance plus receiver resistance must be within the voltage compliance range of the supply voltage to guarantee linear operation over the total range. A negative supply may be used if it is preferred to have the current loop referenced to ground.

DC Regulators and Servos

Closely related to DC and low frequency AC linear transducers are DC regulators and servo circuits. The proliferation of many battery, and solar powered remote instrumentation packages results in a need for adaptable circuits which may readily be made up from existing stock ICs. The examples given here are quite simple, but can be very useful to the designer when economy and size are at a premium.

Solar Regulator for 3-Volt CMOS

Working with small instrumentation packages which are to operate from solar photovoltaic cells may bring a need for simple sub-regulators for MOS circuits requiring only a few milliamperes of drain current. Figure 19 shows a simple low voltage regulator making use of the particularly excellent DC characteristics of the NE/SA5234. The regulator becomes an integral part of any functional analog signal processing package such as an environmental data instrumentation unit. The low current drain of the the typical 3V or 5V MOS digital IC allows one sub regulator to serve up to 10 or more such devices. If the instrument package is to be subjected to wide temperature variations, the SA5234 is recommended. A second op amp in the package may serve as a low battery alarm with tone modulator as in radio links, or simple logic level comparator. Overcurrent protection is easily added within the regulator loop to detect short circuit failures and automatically limit the current.

DC Servo-amps

Servo control systems for low voltage motor drives require high gain-accuracy and good DC stability for many applications. Applications such as the position control of air flow vanes, servo valves, and optical lenses or apertures, are typical examples. Figure 20 demonstrates one simple DC motor servo application with position control feedback. The motor is a 3V permanent magnet rotor type used in micro-position applications and is adaptable to battery supply environments.

Position information is received from a multi-turn potentiometer to give adequate resolution. The input voltage may be generated from another potentiometer which is remote from the motor drive unit proper, or from a D/A converter output for micro processor controlled systems. The input voltage range is 1.0 to 3.0V and the supply voltage is 4.5V.

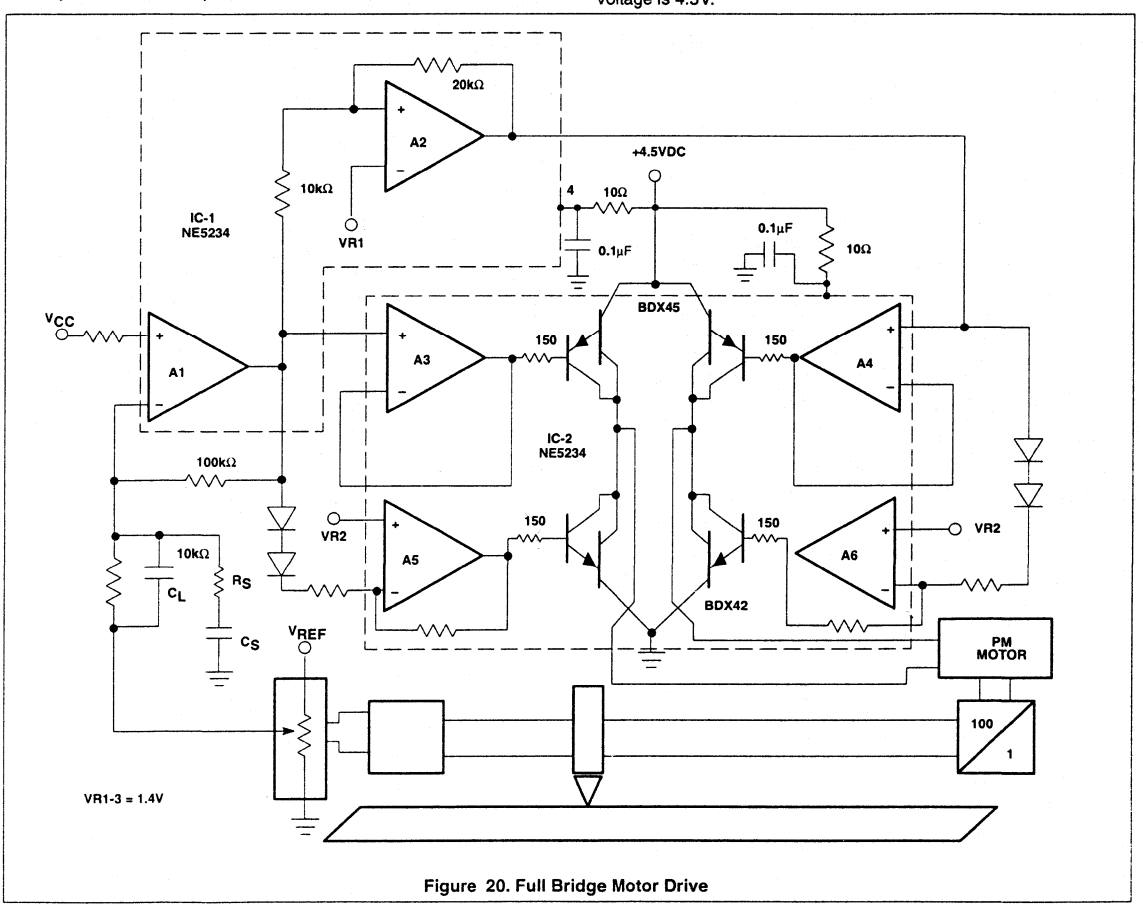


Figure 20. Full Bridge Motor Drive

Active filters

The NE5234 is easily adapted to use in a variety of active filter applications. Its high open-loop gain and excellent unity gain stability make it ideal for high-pass, band-pass and low-pass configurations operated with low voltage single supplies. Its low output impedance also makes it capable of obtaining low noise operation without resorting to separate high current buffers.

Figure 21a shows the circuit for a VCVS low-pass filter with dual supply biasing and 600Ω output termination. Figure 21b is a band-pass filter with AC coupled gain network for single supply operation.

Communications and Audio

Stereo Bridge Amplifier

Figure 22 shows two NE5234 ICs in a bridge amplifier application. The choice of split supplies allows DC coupling, both from the input signal source and to the load. The gain is set to a nominal 20dB. Either inverting or non-inverting operation is available. The inverting input impedance is chosen as 600Ω in order to match standard audio impedance lines within a system. The use of two such amplifiers will provide stereo operation to +10dBm for a 600Ω load.

Voice Operated Microphone

The processing of voice transmissions for communications channels is generally coupled with the need for keeping the signal-to-noise ratio high and the intelligibility optimized for a given channel bandwidth. In addition, when a circuit is battery operated and portable, the requirement to obtain maximum battery life becomes important. The circuit example shown here is aimed at filling the need for a portable voice operated transmitter, cordless phone, or tape recorder. It utilizes the Philips Semiconductors NE5234 quad op amp in conjunction with the new low-voltage NE578 compandor to create an audio processor capable of operating in just such an environment. Both devices are operational to a low battery voltage of 2.0V. In addition the design further conserves current by automatically shifting the NE578 compandor to standby during the period when no transmissions are being made. Total current consumption at 3.0V is 2.8mA for the NE5234. In the active mode the NE578 draws 1.4mA and this drops to 170μA in the standby mode. This amounts to reducing the supply current demand by approximately 25% in the 'listen mode'.

Figure 23 shows the VOX audio circuit example. A description of its operation for voice activated transmission follows.

Audio generated by the electret microphone is fed into the non-inverting input of preamp A1 and the signal amplified by 12dB. The biasing is accomplished by the resistive divider which provides a level of half the supply voltage which is connected through a 100k resistor to the non-inverting terminal of A1. This automatically provides ratiometric common mode biasing set at $V_{CC}/2$ for the device. This level is then transferred directly to the following amplifier, A2, setting its DC operating point. The DC gain of both stage A1 and A2 are unity so the cumulative DC error is not multiplied by stage gain. The peak voice level is approximately $100mV_{RMS}$ at the input to A1 from the microphone and this is boosted to $400mV_{RMS}$. The feedback network gain has a low frequency corner at 160Hz and is flat up to the intersection of the closed loop gain with the open loop gain curve at nearly 500kHz. This would increase the noise bandwidth to an excessive degree unnecessary for voice channel communication. A band limiting network is, therefore, inserted across the feedback resistor to limit response to a nominal 5kHz.

Amplifier stage A2 is used to provide high level audio to the rectifier-filter stage for the rapid generation of a DC control signal for operating the voice activated switch function. Stage A2 gain is set to 20dB in order to allow activation of the voice channel on the rising edge of the first voice syllable. An attack time of 20ms is implemented by adjusting the input charging impedance (R_S) between the rectifier and the A2 amplifier output. AC coupling must be used to isolate the DC common-mode voltage of the amplifier from the rectifier/storage capacitor and to allow only audio frequencies to drive the switching circuit. Amplifier A3 provides a high impedance unity gain buffer to allow a very slow decay rate to be applied to the time constant capacitor, C_T. The output of the storage capacitor reaches approximately 3.2V for a 250ms duration 600Hz burst signal. Diode D1 (1N914) provides a negative clamp action which forces the full peak-to-peak voltage from A2 to charge the storage capacitor. D2 then acts to charge the capacitor to the peak input voltage minus one diode drop, 0.7V. Finally, the buffered DC control signal is fed to A4 which acts as a threshold comparator with extremely high gain and controlled hysteresis. This provides a positive going signal for releasing the NE578 from its inhibit mode when voice input is present. The NE578 is switched from standby mode when voice input is present. The NE578 is switched from standby mode to the active state by raising the voltage on Pin 8 of the device above 2V. Shutting the audio channel off requires this pin to be driven below 100mV. This demands the extremely wide output voltage swing of the NE5234 in order to reach this near to the negative rail voltage. The voltage threshold of the comparator, A4, is adjustable by use of the sensitivity control, R_S. It is used to allow the activation level to be raised or lowered depending upon the ambient audio level in the transmitter vicinity.

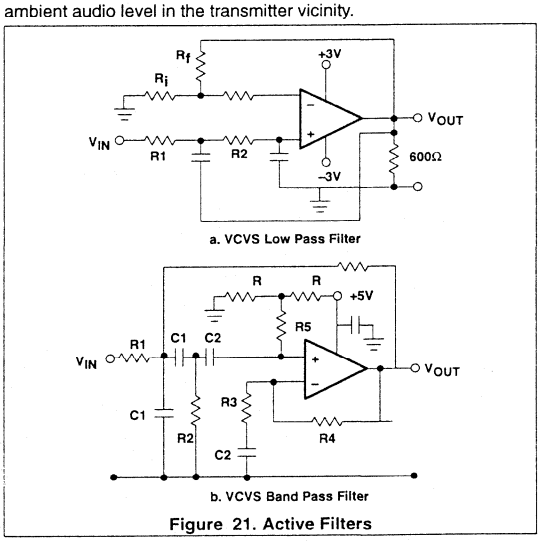


Figure 21. Active Filters

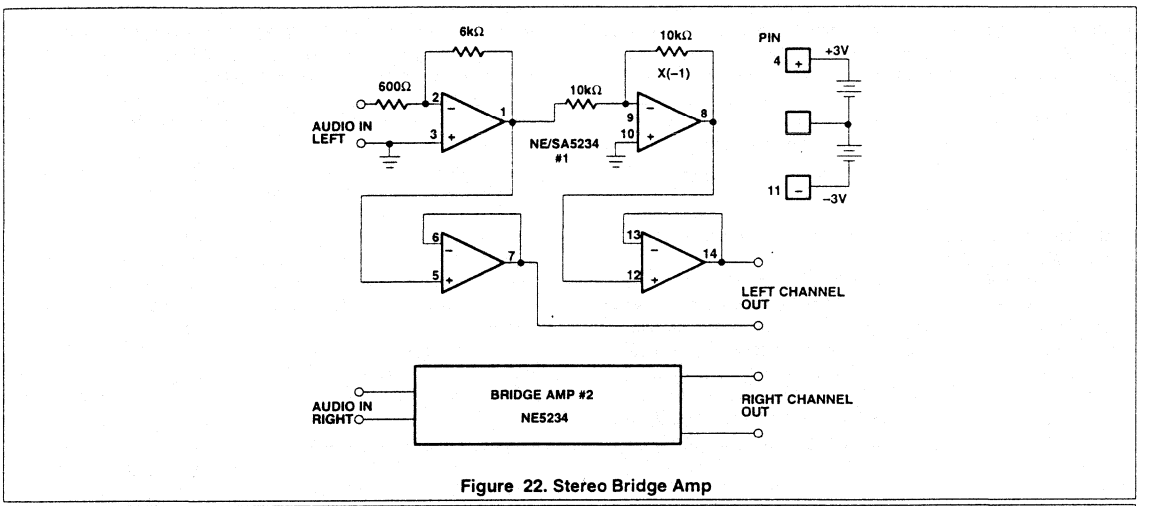


Figure 22. Stereo Bridge Amp

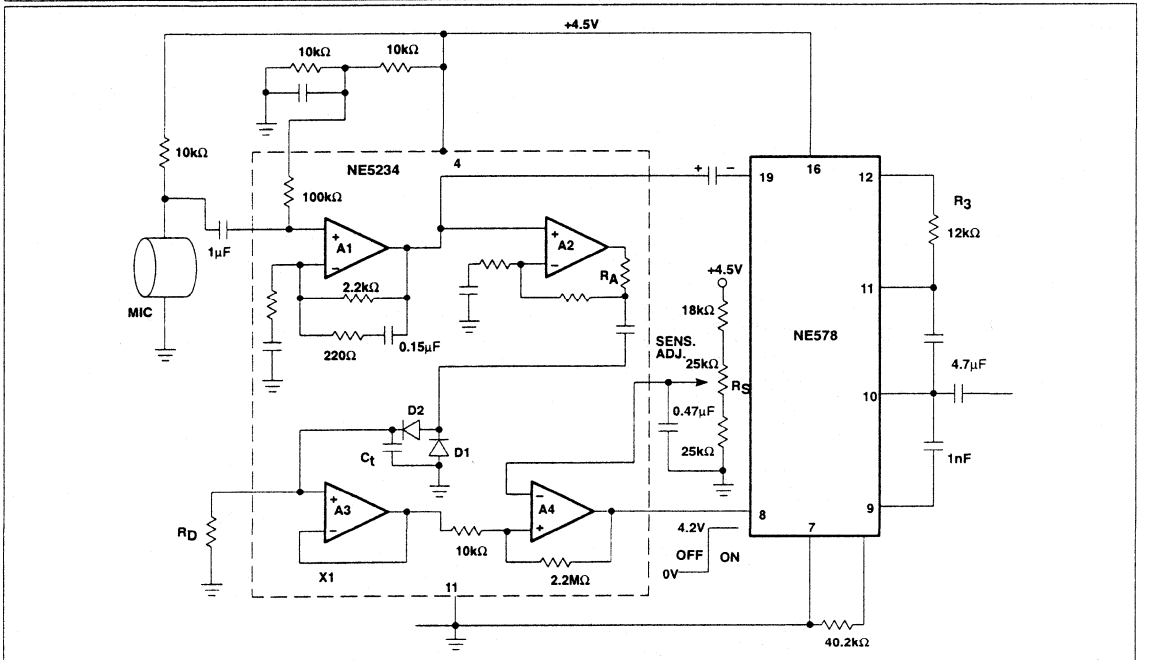


Figure 23. VOX Audio System

Other critical parameters in this type of circuit are the attack and decay times of the RC network which controls the operation of the voice operated switch. Attack time determines how quickly the circuit activates after a quiet period, and the decay time sets how long the transmitter channel stays active between words. It is important to reach an optimum balance between the two time constants in order to allow unbroken transmissions of good quality and no lost syllables. A 100 to 1 attack/decay ratio is used in this particular application and this is primarily set by the value of R_A and R_D. A typical delay of two seconds is easily accomplished. Due to extremely high input impedance of the buffer stage A3, R_D may be in the 1 to 2MΩ range allowing a reasonable value of storage capacitor to be used.

The Audio Channel

Audio input from the preamplifier, A1, is fed directly to Pin 14 of the NE578 compandor. Referring to Figure 24, which shows the

internal diagram of the device, it can be seen that this is the compressor portion of the NE578. There is the option in this system to operate either in a 2:1 compressor mode or an automatic level control mode, (ALC). The compressor mode simply makes a 2:1 reduction in the amplitude dynamic range of the input signal and brings it up to the chosen nominal 0dB output level which is programmable from $10mV_{RMS}$ to $1V_{RMS}$. In this particular example it is programmed for a 0dB level of $0.42V_{RMS}$ which is approximately $1V_{P-P}$. This allows for a standardized output level with good characteristics for FM modulation where peak deviation must be controlled. Figure 25 shows the input-output characteristics of the compressor and ALC.

The compressor also has an attack time determined by capacitor C6 on Pin 11. Attack time is 10k * C6, decay time equals four times this value. An auxiliary amplifier stage is used following the NE578 in order to allow bandwidth and special forms of equalization to be implemented. Note that 2:1 compression in a transmission will enhance the channel dynamic range and may be used with no further processing at the receiver, but feeding the received signal through the complimentary 2:1 expandor will achieve even greater enhancement of the recovered audio. The NE578 contains both operations in the same package. Please refer to Philips Semiconductors applications note AN1762 by Alvin K. Wong for complete information on these compandor circuits using the NE578.

Fiber Optic Receiver for Low Frequency Data (Figure 26)

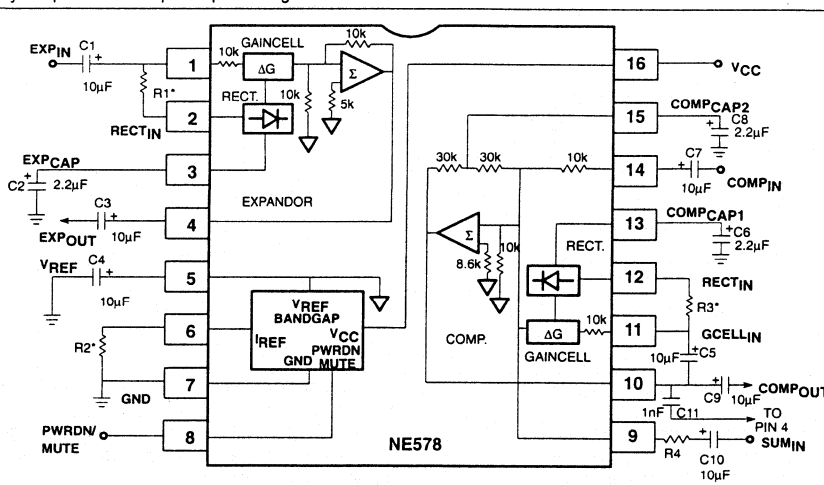
This application makes use of the NE/SA5234 to detect photo-optic signals from either fiber or air transmitted IR (Infra-red) pulses. The signal is digitally encoded for the highest signal-to-noise ratio. The received signal is sensed by an IR photo diode which has its cathode biased to half the supply voltage (2.5V). The first gain stage is configured as a transimpedance amplifier to allow conversion from the microampere diode current signals to a voltage output of approximately $10mV_{0-P}$. The second stage provides a gain-of-ten amplifier to raise this signal level to 1V peak amplitude. This stage is directly coupled from the preamplifier stage in order to provide the necessary common-mode voltage of 2.5V. Its gain control network is capacitively coupled to prevent DC gain as is required in single supply configurations. Since this is essentially a pulse gain stage, low frequency gain below the signal repetition rate is not needed. The third stage acts in a limiting amplifier configuration and its output is squared to swing approximately 5V, the standard TTL level. Again common-mode biasing is passed along from each of the stages up to the last in order minimize parts and simplify circuit layout. The final stage is a simple buffer amplifier to allow the receiver to drive a low impedance long wire line of 600Ω to 900Ω resistance. Some rise time response adjustment may be required. This is easily achieved following stage three by using R_T-C_T to limit the rate of change of the signal voltage prior to the buffer. Note that the last stage acts as a zero-crossing detector. This maximizes noise immunity by allowing a transition only after the third stage output voltage has risen above $2/3V_{CC}$. Phase inversion may be accomplished, if the logic level signals are polarity reversed, by making stage 3 inverting and AC coupling the input signal with a sufficiently large capacitor to reduce droop. Stage 3 must then be biased by connecting its non-inverting node to bias point 'A'. This provides a 2.5V threshold for the proper switching operation of the stage. However, care must be taken not allow the network's time constant to become code dependent as to the average low frequency signal components or errors will result in the output signal.

The advantage of this particular circuit is that it has the simplicity of single supply operation along with the capability of a large output swing making it fully TTL compatible

REFERENCES:

Philips Semiconductors. Linear Data Manual, Volume 2 : Industrial. Sunnyvale: 1988.

Wong, Alvin K. Companding with the NE577 and NE578..Philips Semiconductors Applications Note AN1762 : September 1990.



*R1, R2 and R3 are 1% resistors.

Figure 24. Block Diagram of NE578 Test and Application Circuit

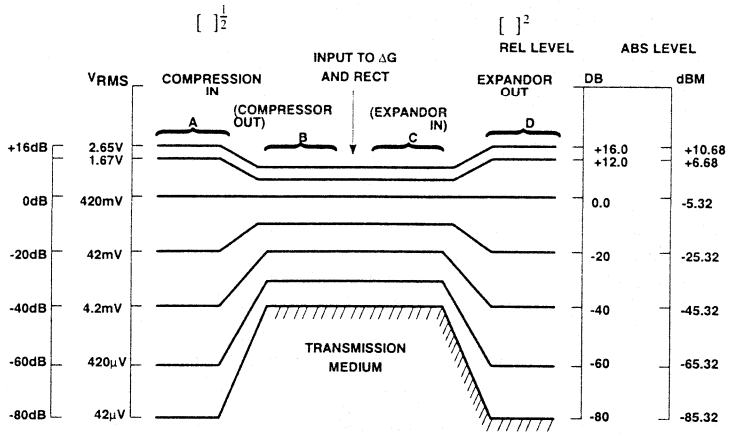


Figure 25. NE570/571/SA571 System Level

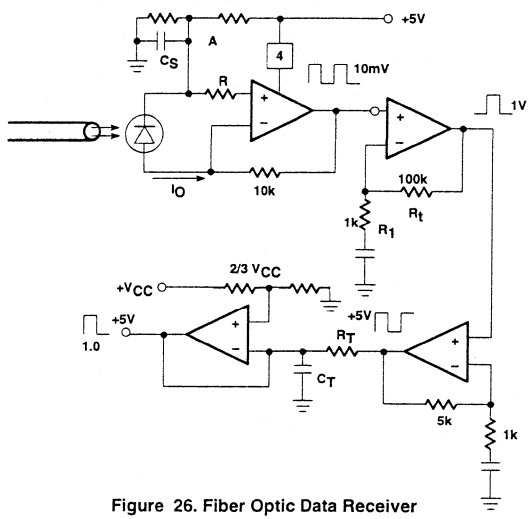


Figure 26. Fiber Optic Data Receiver

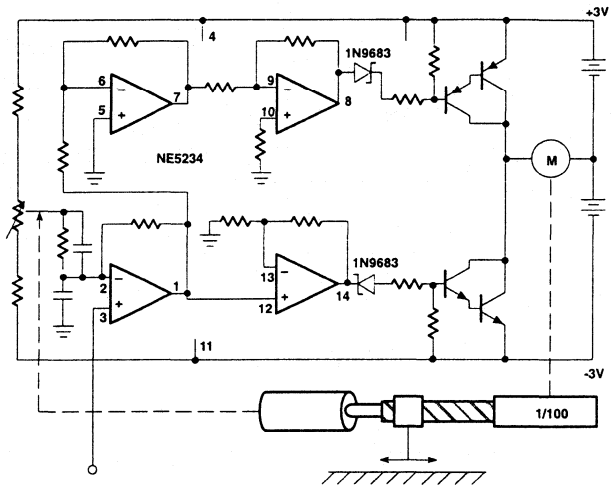


Figure 27. Half Bridge Servo

SA5775 air core meter driver — Application report AN1761

INTRODUCTION

The SA5775 is a monolithic Serial Gauge Driver (SGD) which can be used to directly drive Air Core Meters (ACM), typically used in automobile dashboards (Figure 1). The circuit interfaces with the serial bus of a microprocessor, has 10-bit resolution (0.35 degrees) and is guaranteed to be monotonic. Data can be shifted through the part so that several SA5775s can be cascaded with only one chip select line. On-board circuitry protects the circuit from external faults.

PRINCIPLES OF AIR CORE METERS

In many meter applications hitherto, D'Arsonval type of movements have been used. In this, a field coil is used along with a permanent magnet. When a current passes through the field coil, it generates a magnetic field. The magnetic field, due to the field coil, interacts with that due to the permanent magnet producing a resultant force that causes a needle to deflect, the deflection being controlled by a spring. Calibration of the current results in known deflections of the needle which is used to indicate the desired reading. While the advantage of such a system lies in its low cost and well-known behavior, there are also a number of disadvantages.

1. The strength of the mechanical spring degrades with age and with temperature cycling.
2. The permanent magnet ages with a lessening of the magnetic field. This makes it harder for it to pull the needle against the spring.
3. The mechanism is prone to damage due to vibrations from handling and other causes.

To overcome some of these problems, Air Core Meters have been used quite successfully. In this type of movement, there are two coils which are wound at 90° from one another (see Figures 2 and 3). A needle is attached to a magnetized disk that is positioned between the two coils. When currents 90° out-of-phase with each other pass through the two coils, the resultant magnetic fields produce a force which moves the disk. The position of the disk is dependent upon the ratio of the currents in the two coils. By varying this ratio, the disk and hence the needle position can be varied.

The advantage of such a type of movement lies in the fact that:

1. There are no springs
2. Only effect of magnetic strength degradation with age is in slowing of mechanical response time
3. Accuracy does not degrade with age
4. Not prone to damage due to vibration/handling on account of rugged sleeve bearings
5. Built-in damping

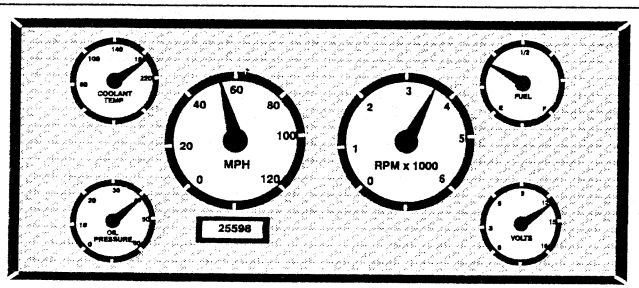
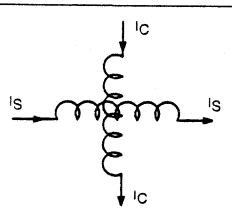
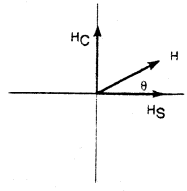


Figure 1. Analog Instrument Cluster



(a)



(b)

Figure 2.

THEORY OF OPERATION

In a solenoid, the strength of the magnetic field produced is given by

$$H = nI$$

where n = number of turns
I = current through the coil

When two coils are placed at right angles as shown in Figure 3 with the currents through the two coils being I_C and I_S, the resultant magnetic fields are

$$H_C = n\,I_C \quad (1a)$$

$$H_S = n\,I_S \quad (1b)$$

Then the magnitude of the resultant magentic field H is given by the vector sum of H_C and H_S, namely

$$|H| = \sqrt{H_C^2 + H_S^2} \quad (2)$$

and the angle of the magnetic field is

$$\angle H = Arc\ \tan\left(\frac{H_S}{H_C}\right) \quad (3)$$

The currents I_C and I_S have the form and relationship as shown in Figure 4, so that

$$I_C = I\ Cos\left(\frac{360^o}{1024}\ Code\right) \quad (4a)$$

$$I_S = I\ Sin\left(\frac{360^o}{1024}\ Code\right) \quad (4b)$$

as 2^{10} bits are used for resolution of 360° and where code is the input code.

Substituting 4a and 4b in (1), (2) and (3) yields

$$|H| = n\,I \quad (5)$$

and

$$\angle H = Arc\ \tan\left(\frac{Sin\ \theta}{Cos\ \theta}\right) = \theta$$

where

$$\theta = \left(\frac{360^o}{1024}\ Code\right) \quad (6)$$

From Equations (5) and (6), it is clear that the torque which is dependent upon |H| is a constant if I is constant and θ is linearly dependent upon the input code.

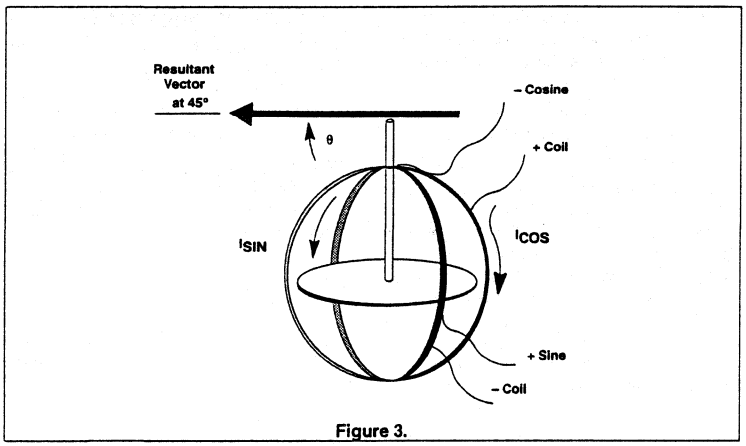


Figure 3.

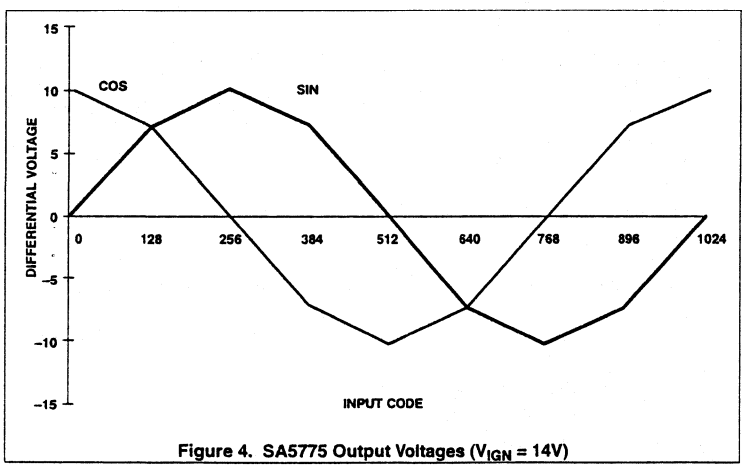


Figure 4. SA5775 Output Voltages (V_{IGN} = 14V)

In actuality, a voltage V is used to drive the coils so that

$$I = \frac{V}{R} \quad (7)$$

where R is the resistance of the coil and in this case, it is assumed that both coils have the same resistance. Thus

$$|H| = \frac{n\,V}{R} \quad (8)$$

Voltage drive has advantages over current drive since there is

1. No back EMF problem
2. No headroom problem
3. Better precision
4. Ratiometric drive

BLOCK DIAGRAM DESCRIPTION

The logic block contains the 10-bit input shift register and a 10-bit parallel latch for the DAC. The DAC generates two output voltages that are offset within the supply rails to give the output buffers enough headroom to operate. With a 14V supply, the typical output swing is from 1V to 11V. V1 and V2 are the DAC outputs that provide the relationnship between the SIN coil voltage and COS coil voltage to create the desired display pointer deflection. The MUX generates all four quadrants by switching the

90 degree data from the DAC to the appropriate output buffer. The output buffers provide the necessary current to drive the air core gauge. The output buffers are always connected to the coils and can sink and source sufficient current so that inductive kickback is eliminated during normal operation.

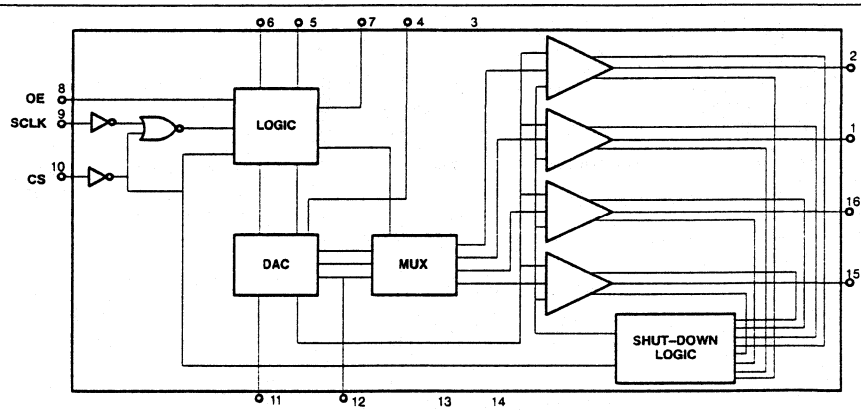


Figure 5. SA5775 Block Diagram

The primary function of the SGD IC is to generate the transfer function that maps an input code into the correct voltages for linearly controlling the SIN and COS coils of an air core display. This circuit receives commands via an internal serial data interface port which is SPI compatible. The parts can be serially cascaded to minimize the necessary interface signals in multi-chip systems. The SGD has 10-bit resolution (0.35 degrees) and is guaranteed to be monotonic. The input data is directly proportional to the displayed angle in degrees. An input code of all 0's gives an output angle of 0.176 degrees; all 1's will generate a full-scale output of 359.82 degrees (see Table 2). The SGD output buffers are capable of sourcing up to 80mA per differential driver to control a single air core display directly.

FUNCTIONAL DESCRIPTION

The SA5775 which is housed in a 16-Pin package has terminal connections as shown in Figure 6. The function of each pin is described in Table 1.

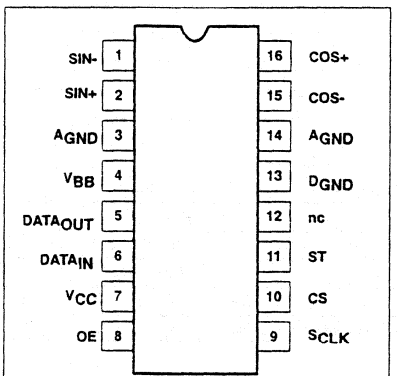


Figure 6. Pin Configuration

Table 1. SA5775 Pin Descriptions

Pin #	Name	Function
1	SIN–	Negative output connection to the SIN coil of the gauge.
2	SIN+	Positive output connection to the SIN coil of the gauge.
3	A_{GND}	Ground for V_{IGN} supply. Pins 3, 13 and 14 connected on the ckt board.
4	V_{BB}	Analog supply. Nominally 14.0V.
5	$DATA_{OUT}$	Serial data output. Output of the internal shift register. When a new data word is shifted in, the old word is shifted out the $DATA_{OUT}$ pin.
6	$DATA_{IN}$	Serial data input. A new data word is serially shifted into the part on the rising edge of S_{CLK}. The data is shifted in MSB first.
7	V_{CC}	5V logic supply. The internal latches and registers are set to zero on the rising edge of this signal.
8	OE	Output drivers are turned off when this input is low. Current draw is minimized.
9	S_{CLK}	Serial clock input. Data is loaded into the part on the rising edge of S_{CLK}.
10	CS	Active high chip select input. When CS is high, the part is enabled to receive a new serial input word. The high-to-low transition of CS loads the new 10-bit word into the DAC registers and updates the output.
11	ST	Status output from this IC to indicate that the outputs have been disabled. The outputs may be disabled due to shorted outputs, over temperature conditions, power up reset, or output enable control pin. This output is an open drain output. Multiple status outputs may be wire OR'ed together. This output is low when the outputs are disabled due to a fault condition.
12	nc	Not connected
13	D_{GND}	Ground for V_{CC} supply. Connect to Pins 3 and 14.
14	A_{GND}	Ground for V_{BB} supply. Connect to Pins 3 and 13.
15	COS–	Negative output connection to the COS coil of the gauge.
16	COS+	Positive output connection to the COS coil of the gauge.

Table 2.

Ideal	Nominal	Input Code
0	0.176	0
45	45.176	128
90	90.176	256
135	135.176	384
180	180.176	512
225	225.176	640
270	270.176	768
360	359.820	1023
N = Binary Input Code Equation for Output Angle (θ) vs Output Voltage		
Quadrant	Equation	
I	$\theta = \tan^{-1} \mid [(SIN+) - (SIN-)] / [(COS+) - (COS-)] \mid$	
II	$\theta = 180° - \tan^{-1} \mid [(SIN+) - (SIN-)] / [(COS+) - (COS-)] \mid$	
III	$\theta = 180° - \tan^{-1} \mid [(SIN+) - (SIN-)] / [(COS+) - (COS-)] \mid$	
IV	$\theta = 360° - \tan^{-1} \mid [(SIN+) - (SIN-)] / [(COS+) - (COS-)] \mid$	

SERIAL INTERFACE

The SGD is controlled through a serial interface with the following control functions:

S_{CLK}

Serial input clock. When CS is high, the rising edge of S_{CLK} shifts a new data bit into the SGD.

CS

Active high chip select. Enables the SGD to receive serial input data. The falling edge of CS loads a new 10-bit data word into the internal DAC register which updates the output.

DI

Serial data input. The data at this pin is shifted into the internal shift register on the rising edge of S_{CLK}. Data is shifted in MSB first.

DO

Serial data output. This pin is the output of the internal shift register. The data output on this pin is the input data from DI pin delayed by 11 clock cycles. This pin can be used to cascade several SGDs with one CS line to load all of the SGDs concurrently.

Power Moding

This device has a power on reset. On the rising edge of V_{CC} the internal latches and registers are set to zero and the outputs are disabled.

Output Driver Control

Directed control of the outputs can happen in one of several ways:

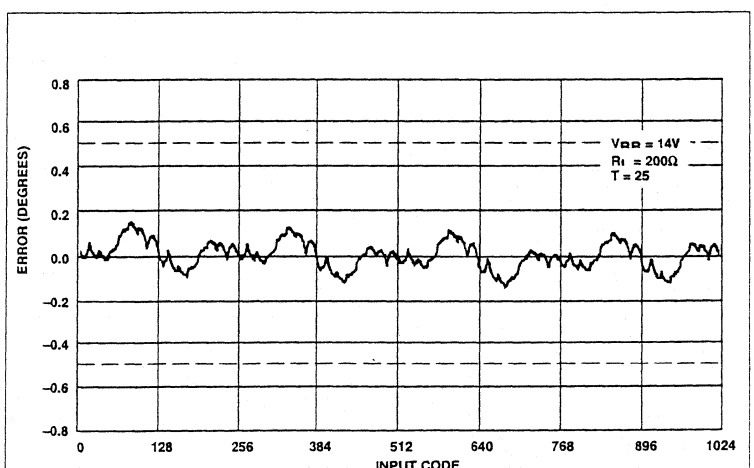


Figure 7. Error Graph

1. The outputs are disabled with the rising edge of V_{CC}.
2. The outputs are disabled when OE is taken low or held low. The data registers for the outputs can still be updated while OE is low. When OE is taken high, the current output data value is displayed. A falling edge on CS will be required to activate outputs if a fault condition has occurred prior to the OE going high.
3. The outputs are disabled if an overcurrent condition exists on either of the coil output buffers. The coil output buffers will be enabled after the next CS high-to-low transition; assuming OE is high. If the overcurrent condition has not been removed, the outputs will immediately return to their disabled condition. The ST pin will indicate status of the coil outputs.
4. The outputs will be disabled by thermal shut-down circuitry if there is excessive power dissipation. The die temperature must go below 140°C before a falling edge on the CS pin will clear this fault condition and allow the coil outputs to go active.

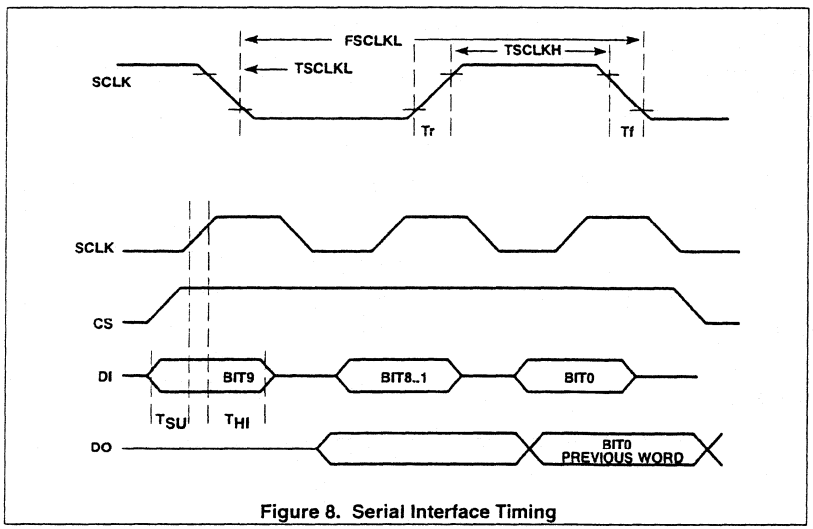


Figure 8. Serial Interface Timing

Dual air-core gauge driver SA5777

DESCRIPTION

The SA5777 is a monolithic driver for controlling air-core (or differential) meters typically used in automotive instrument cluster applications. The circuit interfaces with a microprocessor through a serial bus and directly drives the air-core meter. The SA5777 has 10-bit resolution (0.35 degree) and is guaranteed to be monotonic. Data can be shifted through the part, allowing several SA5777s to be cascaded with only one chip-select line. On-chip current shut down logic protects the circuit from external faults.

FEATURES

- 10-Bit resolution (0.35 degrees)
- Exceptional accuracy (0.5 degrees, typical)
- High-torque capability
- Active differential drivers eliminate back-EMF issues
- No RFI/EMI generation issues
- Simple serial interface
- Simple cascading capability for multiple meters
- Internal fault protection
- Only one external component required (bypass capacitor)

PIN CONFIGURATION

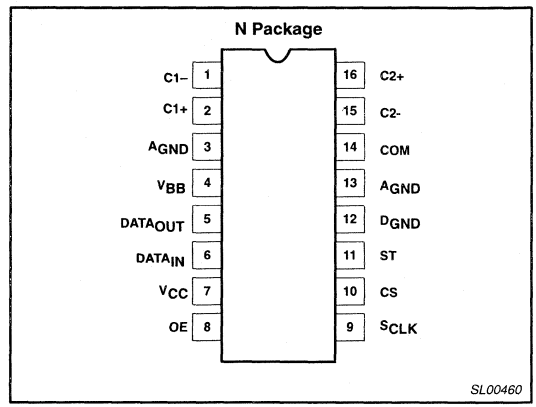


Figure 1. Pin Configuration

APPLICATION

- Instrumentation utilizing air-core meters

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5777N	SOT38-4

BLOCK DIAGRAM

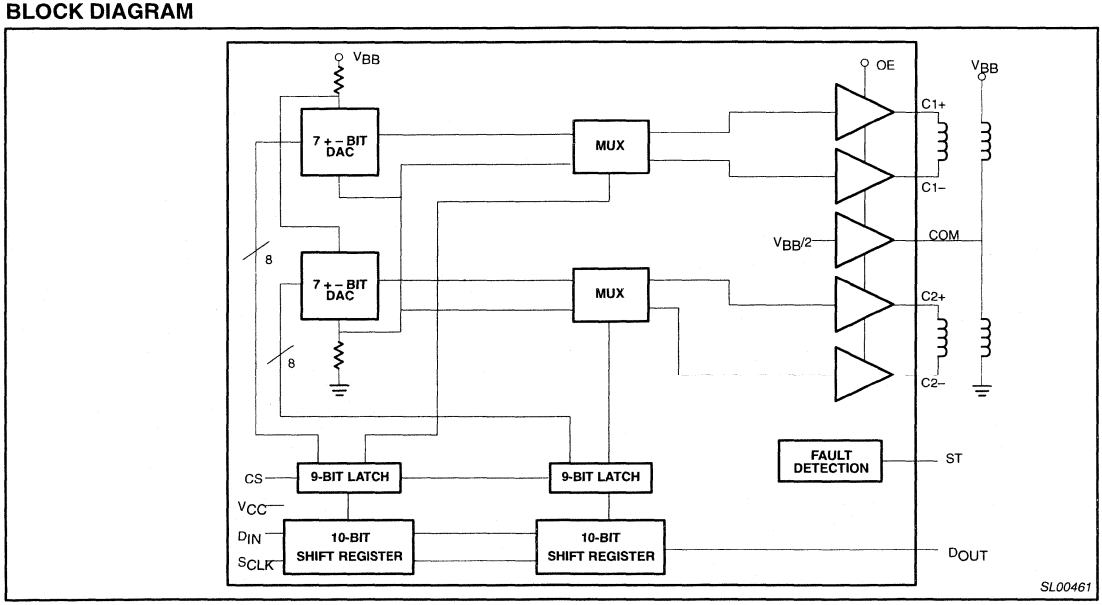


Figure 2. Block Diagram

Table 1. SA5777 Pin Descriptions

Pin #	Name	Function
1	C1–	Negative output connection to the TAN coil of meter #1.
2	C1+	Positive output connection to the TAN coil of meter #1.
3	A_{GND}	Ground for V_{BB} supply. Pins 3, 12 and 13 should be connected on the circuit board.
4	V_{BB}	Analog supply. Nominally 13.5V.
5	$DATA_{OUT}$	Serial data output. Output of the internal shift register. When a new data word is shifted in, the old word is shifted out the $DATA_{OUT}$ pin. $DATA_{OUT}$ output is always active.
6	$DATA_{IN}$	Serial data input. A new data word is serially shifted into the part on the rising edge of S_{CLK}. The data is shifted in MSB first, gauge 1 first.
7	V_{CC}	5V logic supply. The internal latches and registers are set to zero on the rising edge of this signal.
8	OE	Output drivers are turned off when this input is low.
9	S_{CLK}	Serial clock input. Data is loaded into the part on the rising edge of S_{CLK}. Data is shifted out of $DATA_{OUT}$ on the falling edge of S_{CLK}.
10	CS	Active high chip select input. When CS is high, the part is enabled to receive a new serial input word. The high-to-low transition of CS loads the new 20-bit word into the DAC registers and updates the output.
11	ST	Status output. This is an open drain output and goes low when the coil output buffers (C1+, C1–, C2+, C2–, COM) have been disabled. The coil outputs may be disabled due to shorted outputs, over-temperature conditions, power-on reset, or by the output enable (OE) pin. Multiple status outputs , ST, may be wire OR'ed together.
12	D_{GND}	Ground for V_{CC} supply. Connect to Pins 3 and 13.
13	A_{GND}	Ground for V_{BB} supply. Connect to Pins 3 and 12.
14	COM	Output drive for biased coils. This output will be 1/2 of V_{BB}.
15	C2–	Negative output connection to the TAN coil of meter #2.
16	C2+	Positive output connection to the TAN coil of meter #2.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{BB}	Analog supply	-1 to +20	V
V_{CC}	Digital supply	-1 to +6	V
V_{IN}	Digital input voltage, Data In, OE, CS, S_{CLK}	-1 to +6	V
D_{GND} to A_{GND}	Ground difference	±0.5	V
T_A	Ambient operating temperature	–40 to +85	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature	–65 to +150	°C
P_D	Power dissipation (T_A = 25°C)[1] N package	1500	mW
θ_{JA}		90	°C/W

NOTE:
1. For power dissipation ratings in still air, derate above 25°C at the following rates:
   N package at 12mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{BB} = 7.5 to 18V; V_{CC} = 4.5 to 5.5V; T_A = –40 to +85°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{BB}	Analog supply voltage		7.5		18	V
I_{IGN}	Analog supply current	V_{BB} = 18V no load $R_{C1} = R_{C2} = R_{LMIN}$			30 170	mA mA
I_{CC}	Logic supply current	V_{CC} = 5.5V			1.0	mA
V_{OH}	Output high voltage	Data out I_{OH} = 800µA	V_{CC} – 0.8			
V_{OL}	Output low voltage	Data out I_{OL} = 1.5mA			0.4	V
V_{OL} Status		ST, I_{OL} = 2.5mA			0.8	V
I_{OH} Status		ST, VO (ST) = V_{CC}			25	µA
V_{IH}	Input high voltage	CS, S_{CLK}, $DATA_{IN}$, OE	0.7 x V_{CC}			V
V_{IL}	Input low voltage	CS, S_{CLK}, $DATA_{IN}$, OE			0.3 x V_{CC}	V
I_{IH}	Input high current	CS, S_{CLK}, $DATA_{IN}$, V_{IN} = 0.7 x V_{CC}			1	µA
I_{IL}	Input low current	CS, S_{CLK}, $DATA_{IN}$, V_{IN} = 0.3 x V_{CC}			1	µA
A_{CC}	Output function accuracy[2]	$R_{C1} = R_{C2} = R_{LMIN}$			±1	Degree
I_{SD}	Output shut-down current	C1+, C1–, C2+, C2–, COM I_{SINK} $V_{BB} = V_{BB\ (MAX)}$ $V_{BB} = V_{BB\ (MIN)}$ I_{SOURCE} $V_{BB} = V_{BB\ (MAX)}$ $V_{BB} = V_{BB\ (MIN)}$	 85 43 85 43		 450 300 350 150	 mA mA mA mA
V_{DRIVE}	Differential coil drive voltage[1]	$V_{BB} = V_{BB\ (MAX)}$ $R_L = R_{L\ (MIN)}$	0.7 x V_{BB}		0.8 x V_{BB}	V
R_{LMIN}	Minimum load resistance	T_A = 85°C T_A = 25°C T_A = –40°C	305 245 180			Ω Ω Ω
V_{BIAS}	Bias voltage[3]	IOB (Source or Sink) $R_L = R_{L\ (MIN)}$	0.475 x V_{BB}		0.525 x V_{BB}	V

NOTE:

1. V_{DRIVE} is the maximum voltage that is applied across the coil, it is equal to (C1+) – (C1–) or (C2+) – (C2–).
2. In reference to nominal values in Figure 4. (Based on 7+ bit DAC).
3. Output Angle (0) $= \tan^{-1}\left[\frac{(C+) - (C-)}{V_{BB} - V_{BIAS}}\right] - \tan^{-1}\left[\frac{(C+) - (C-)}{V_{BB} - V_{BIAS}}\right]$ Data–in = 0

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 7.5 to 18V; V_{CC} = 4.5 to 5.5V; T_A = –40 to +85°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
FS_{CLK}	Input frequency				1.60	MHz
TS_{CLKH}	S_{CLK} high time		175			ns
TS_{CLKL}	S_{CLK} low time	V_{CC} = 5.5V	175			ns
TRO	Output rise time DO	0.75 to V_{CC} –1.2V, C_L = 90pF			75	ns
TFO	Output fall time DO	V_{CC} –1.2V to 0.75, C_L = 90pF			75	ns
TSU	DI set-up time		75			ns
THI	DI hold time		75			ns
T_{CSH}	Time before first S_{CLK} rising edge		75			ns
T_{CSL}	Time after last S_{CLK} falling edge		75			ns

FUNCTIONAL DESCRIPTION

The SA5777 dual air-core gauge driver logic Block Diagram shows the two 10-bit input shift registers and two 9-bit parallel latches, and two 7+-bit DACs. The MSB is a dummy bit required for compatibility with the SA5775. The DACs generate output voltages that are offset within the supply rails to give the output buffers enough headroom to operate. With a 14V supply, the typical output swing is from 1V to 11.5V. The MUX generates the two required quadrants by switching the 56° data from the DAC to the appropriate output buffer. The output buffers provide the necessary current to drive the air-core gauge. The output buffers are always connected to the coils and can sink and source sufficient current so that inductive kickback is eliminated during normal operation.

The primary function of the SA5777 IC is to generate the transfer function that maps an input code into the correct voltages for linearly controlling the coils of an air-core gauge display (Figure 3). The SA5777 has been implemented using the tangent drive algorithm. Therefore, one coil on each meter will be driven with an output approximating the tangent function, the other coils will be biased at $1/2V_{BB}$. The internal DAC is designed to operate over a 7+ bit (56°) data range. An extended range can be achieved by changing the relationship between the bias coil and the driver coil. As the current through the bias coil is reduced, the full scale deflection is increased. Theoretically, this deflection could approach 180°, but practical limitations of accuracy, resolution, and torque restrict the full scale range to approximately 112° (Figure 4). This full scale range corresponds to a bias coil voltage of 0.5 x V_{BB} and a full scale tangent voltage of 0.744 x V_{BB}. The DAC has been tailored to maintain the meter accuracy at this maximum deflection. The 0.5 x V_{BB} bias coil voltage is obtained by connecting the bias coils of the two meters in series across V_{BB}. This gives bias stability over temperature. The internal bias generator is used to offset any inaccuracies due to meter mismatches. This circuit receives commands via an internal serial data interface port which is SPI compatible. These parts can be serially cascaded with other SA5777 ICs and/or SA5775 ICs to interface signals in multi-chip systems. The SA5777 has a typical resolution of 0.35° over a full scale deflection of approximately 112° and is guaranteed to be monotonic. The input data is directly proportional to the displayed angle in degrees (Figure NO TAG). Input code 0 gives an output angle of 0°, code 319 (decimal) will generate a full scale output of 112.15°. Codes higher than decimal 319 will not be loaded into the DAC latches and will leave the coil output buffers unchanged. However, codes greater than 319 can be shifted through the SA5777 intact if other parts are cascaded. The SA5777 is capable of sourcing and sinking up to 100mA per differential driver to control either one or two air-core gauge displays directly.

On-chip overcurrent and thermal shut-down logic prevents the chip from overheating due to high current fault conditions. When a shut-down condition is detected, the protection circuit disables the coil output buffers (i.e., C1+, C1–, C2+, C2–, COM). The coil output buffers remain in this condition until the first falling edge of CS that occurs after the die temperature has decreased to about 140°C or the overcurrent condition has been removed. During shut-down, the digital portion of this IC continues to operate normally.

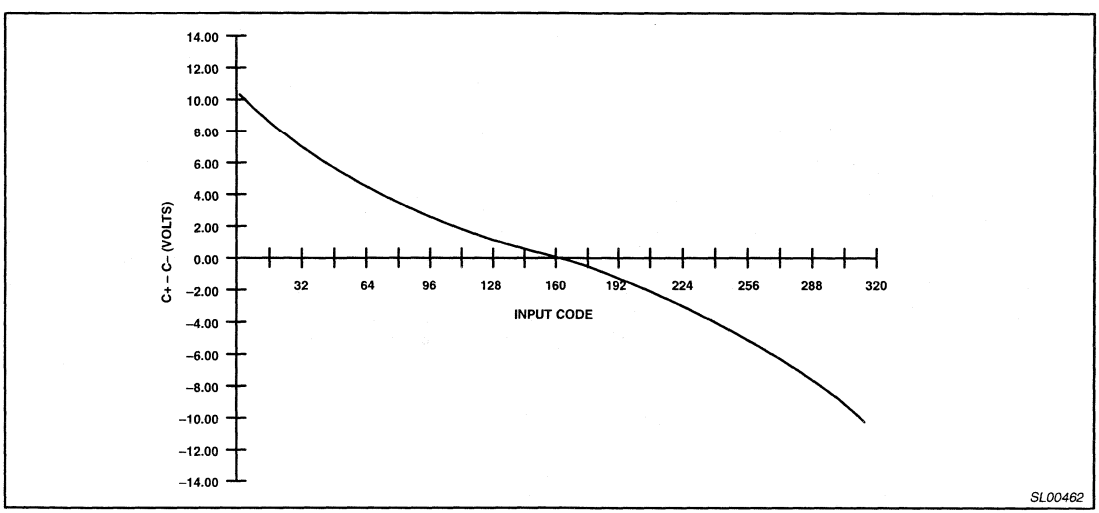


Figure 3. Typical Output Voltage vs Input Code (V_{BB} = 14V)

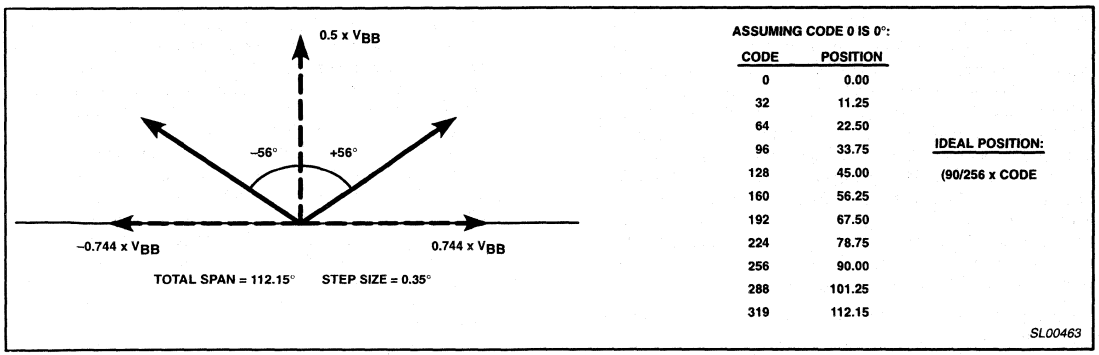


Figure 4. Total Span

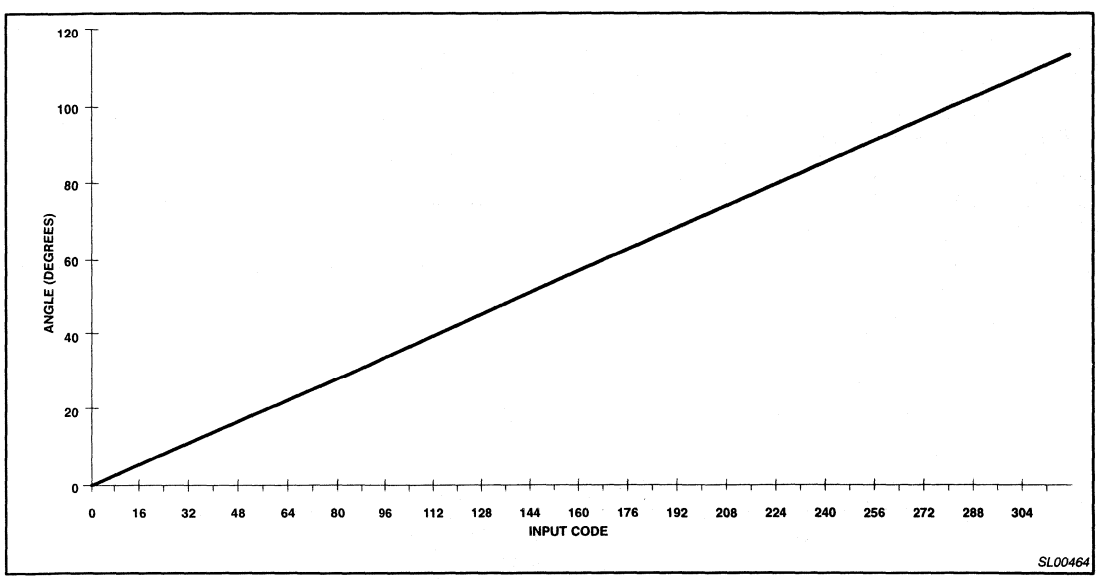


Figure 5. Meter Position (degrees) vs Input Code

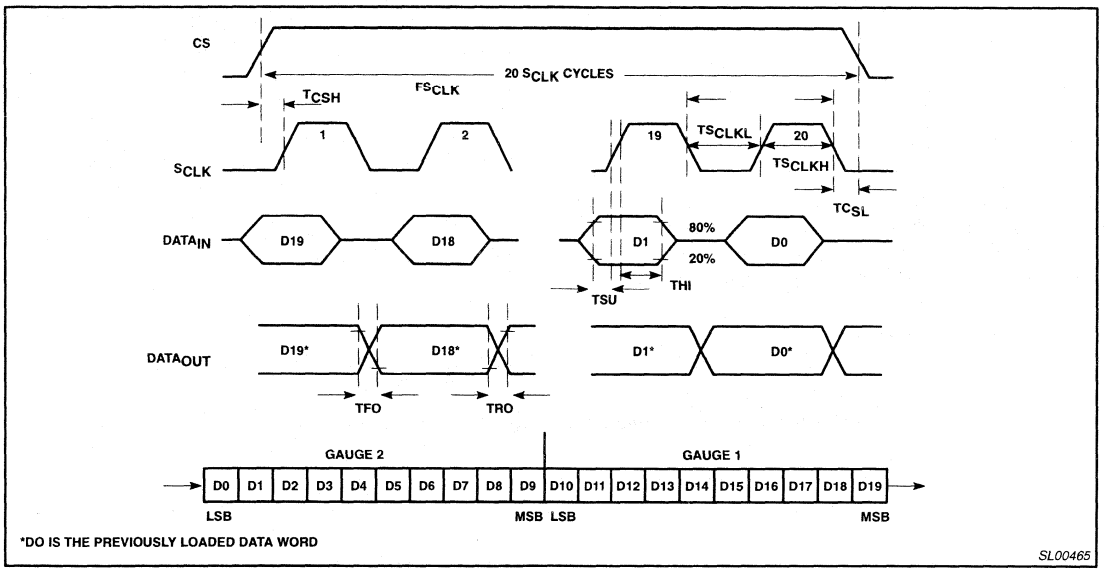


Figure 6. Serial Interface Timing

Serial Interface

The SA5777 is controlled through a serial interface with the following control functions (reference Figure 6):

S_{CLK}	Serial input clock. When CS is high, the rising edge of S_{CLK} shifts a new data bit into the SA5777 and the falling edge shifts the data out of $DATA_{OUT}$.
CS	Active high chip select. Enables the SA5777 to receive serial input data. The falling edge of CS loads a new 20-bit data word into the internal DAC registers which updates the tangent coil output buffers (C1+, C1–, C2+, C2–).
$DATA_{IN}$	Serial data input. The data at this pin is shifted into the internal shift register on the rising edge of S_{CLK}. Data is shifted in MSB first, gauge 1 first.
$DATA_{OUT}$	Serial data output. This pin is the output of the internal shift register. The data output on this pin is the input data from $DATA_{IN}$ pin delayed by 20 clock cycles. This pin can be used to cascade several SA5777s with one CS line to load all of the SA5777s concurrently.

Power Moding

The SA5777 has a power-on reset capability. On the rising edge of V_{CC}, the internal latches and registers are set to zero and the coil output buffers (C1+, C1–, C2+, C2–, COM) are disabled.

Coil Output Buffer Control

The coil buffers (C1+, C1–, C2+, C2–, COM) are disabled:

1. With the rising edge of V_{CC} (power-on reset).
2. When OE is taken low or held low. The data registers for the outputs can still be updated while OE is low. When OE is taken high, the current output data value is displayed. A falling edge on CS will be required to activate the outputs if a fault condition has occurred prior to the OE going high.
3. Due to an overcurrent condition on either of the coil output buffers. The coil output buffers will be enabled after the next CS high-to-low transition; assuming OE is high. If the overcurrent condition has not been removed, the outputs will immediately return to their disabled condition. The ST pin will indicate status of the coil outputs.
4. Due to excessive power dissipation (i.e., thermal shut-down). The die temperature must go below 140°C before a falling edge on the CS pin will clear this fault condition and allow the coil outputs to go active.

Application Notes

The air-core gauge is constructed of two coils would on a cavity at 90° to each other. Inside the cavity there is a disk which is magnetized on its diameter. The currents through the coils generate a resultant magnetic vector that causes the magnetic disc to move until the magnetic fields are aligned. If the ratio of the currents in the two coils follows the tangent function, then the transfer characteristic relating the input data to output angle is linear.

Maximum current is when output is at zero and full scale degrees, $T_A = -40°C$, and $R_L = 180$.

Copper wire has a typical temperature coefficient of 0.4%/C

8-stage shift-and-store register LED driver HEF4794B

APPLICATIONS

- Automotive
- Industrial.

GENERAL DESCRIPTION

The HEF4794B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel LED driver outputs O_0 to O_7. Data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the outputs whenever the output enable (EO) signal is HIGH.

Two serial outputs (O_S and O_S') are available for cascading a number of HEF4794B devices. Data is available at O_S on positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at O_S' on the next negative-going clock edge and provides cascading HEF4794B devices when the clock rise time is slow.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PIN POSITION	MATERIAL	CODE
HEF4794BT	16	SO16	plastic	SOT109-1
HEF4794BP	16	DIP16	plastic	SOT38-4

FUNCTIONAL DIAGRAM

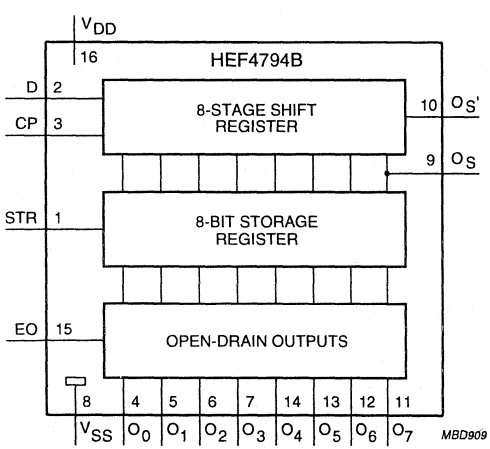


Fig.1 Functional diagram.

LOGIC DIAGRAMS

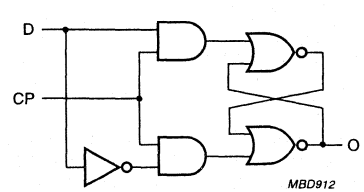


Fig.2 One D-latch.

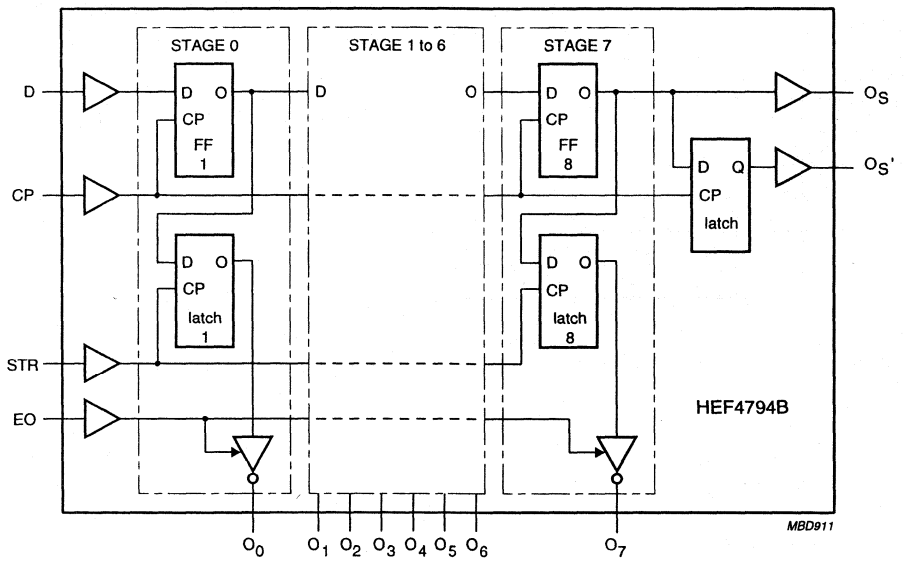


Fig.3 Logic diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
STR	1	strobe input
D	2	data input
CP	3	clock input
O_0 to O_3	4 to 7	parallel outputs 0 to 3 (open drain)
V_{SS}	8	ground
O_S, O_S'	9 and 10	serial outputs
O_7	11	parallel output 7 (open drain)
O_6	12	parallel output 6 (open drain)
O_5	13	parallel output 5 (open drain)
O_4	14	parallel output 4 (open drain)
EO	15	output enable input
V_{DD}	16	supply voltage

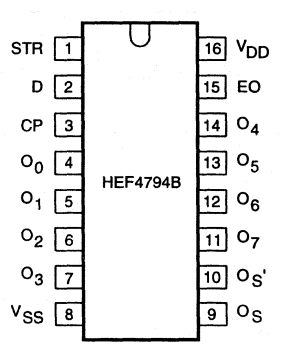


Fig.4 Pin configuration.

FUNCTIONAL DESCRIPTION

Table 1 Function table; note 1.

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	EO	STR	D	O_0	O_n	O_S	O_S'
↑	L	X	X	Z	Z	O_6'	nc
↓	L	X	X	Z	Z	nc	O_7
↑	H	L	X	nc	nc	O_6'	nc
↑	H	H	L	L	O_{n-1}	O_6'	nc
↑	H	H	H	H	O_{n-1}	O_6'	nc
↓	H	H	H	nc	nc	nc	O_7

Note

1. H = HIGH state;
   L = LOW state;
   X = don't care;
   ↑ = positive-going transition;
   ↓ = negative-going transition;
   Z = high-impedance OFF state;
   nc = no change;
   O_6' = the information in the seventh shift register stage.

   At the positive clock edge the information in the 7^{th} register stage is transferred to the 8^{th} register stage and the O_S output.

FAMILY DATA

See *"Family Specifications"* except for: rating for DC current into any open-drain output is 40 mA.

I_{DD} LIMITS CATEGORY MSI

See *"Family Specifications"* for ratings.

DC CHARACTERISTICS

V_{SS} = 0 V.

SYMBOL	PARAMETER	CONDITIONS	T_{amb} (°C)						UNIT
			−40		+25		+85		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{OL}	LOW level output voltage	V_I = V_{SS} or V_{DD}; $\|I_O\|$ < 20 mA; V_{DD} = 5 V	–	0.75	–	0.75	–	1.5	V
		V_I = V_{SS} or V_{DD}; $\|I_O\|$ < 20 mA; V_{DD} = 10 V	–	0.75	–	0.75	–	1.5	V
		V_I = V_{SS} or V_{DD}; $\|I_O\|$ < 20 mA; V_{DD} = 15 V	–	0.75	–	0.75	–	1.5	V
I_{OZH}	HIGH level output leakage current; 3-state	V_O = 15 V; V_{DD} = 5 V	–	2	–	2	–	15	μA
		V_O = 15 V; V_{DD} = 10 V	–	2	–	2	–	15	μA
		V_O = 15 V; V_{DD} = 15 V	–	2	–	2	–	15	μA

AC POWER CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL FORMULA FOR P (μW)[1]
P	dynamic power dissipation per package	V_{DD} = 5 V	$1200f_i + \Sigma(f_oC_L) \times V_{DD}^2$
		V_{DD} = 10 V	$5550f_i + \Sigma(f_oC_L) \times V_{DD}^2$
		V_{DD} = 15 V	$15000f_i + \Sigma(f_oC_L) \times V_{DD}^2$

Note

1. Where:
   $R_L = \infty$;
   f_i = input frequency (MHz);
   f_o = output frequency (MHz);
   C_L = load capacitance (pF);
   $\Sigma(f_oC_L)$ = sum of outputs;
   V_{DD} = supply voltage (V).

AC TIMING CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns; unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT	TYPICAL EXTRAPOLATION FORMULA
t_{PHL}	propagation delay time CP to O_S; HIGH-to-LOW	5	–	160	320	ns	132 ns + (0.55 ns/pF)C_L
		10	–	65	130	ns	53 ns + (0.23 ns/pF)C_L
		15	–	45	90	ns	37 ns + (0.16 ns/pF)C_L
t_{PLH}	propagation delay time CP to O_S; LOW-to-HIGH	5	–	130	260	ns	102 ns + (0.55 ns/pF)C_L
		10	–	55	110	ns	44 ns + (0.23 ns/pF)C_L
		15	–	40	80	ns	32 ns + (0.16 ns/pF)C_L
t_{PHL}	propagation delay time CP to O_S'; HIGH-to-LOW	5	–	120	240	ns	92 ns + (0.55 ns/pF)C_L
		10	–	50	100	ns	39 ns + (0.23 ns/pF)C_L
		15	–	40	80	ns	32 ns + (0.16 ns/pF)C_L
t_{PLH}	propagation delay time CP to O_S'; LOW-to-HIGH	5	–	130	260	ns	102 ns + (0.55 ns/pF)C_L
		10	–	60	120	ns	49 ns + (0.23 ns/pF)C_L
		15	–	45	90	ns	37 ns + (0.16 ns/pF)C_L
t_{PZL}	propagation delay time CP to O_n; OFF-to-LOW	5	–	240	480	ns	note 1
		10	–	80	160	ns	
		15	–	55	110	ns	
t_{PLZ}	propagation delay time CP to O_n; LOW-to-OFF	5	–	170	340	ns	note 1
		10	–	75	150	ns	
		15	–	60	120	ns	

SYMBOL	PARAMETER	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT	TYPICAL EXTRAPOLATION FORMULA
t_{PZL}	propagation delay time STR to O_n; OFF-to-LOW	5	–	140	280	ns	note 1
		10	–	70	140	ns	
		15	–	55	110	ns	
t_{PLZ}	propagation delay time STR to O_n; LOW-to-OFF	5	–	100	200	ns	note 1
		10	–	40	100	ns	
		15	–	35	70	ns	
t_{THL}	output transition time O_S and O_S'; HIGH-to-LOW	5	–	85	170	ns	35 ns + (1.0 ns/pF)C_L
		10	–	40	80	ns	19 ns + (0.42 ns/pF)C_L
		15	–	30	60	ns	16 ns + (0.28 ns/pF)C_L
t_{TLH}	output transition time O_S and O_S'; LOW-to-HIGH	5	–	85	170	ns	35 ns + (1.0 ns/pF)C_L
		10	–	40	80	ns	19 ns + (0.42 ns/pF)C_L
		15	–	30	60	ns	16 ns + (0.28 ns/pF)C_L
t_{PZL}	output enable time EO to O_n; OFF-to-LOW	5	–	100	200	ns	note 1
		10	–	55	110	ns	
		15	–	50	100	ns	
t_{PLZ}	output disable time EO to O_n; LOW-to-OFF	5	–	80	160	ns	note 1
		10	–	40	80	ns	
		15	–	30	60	ns	
t_{WCPL}	minimum clock pulse width LOW	5	60	30	–	ns	
		10	30	15	–	ns	
		15	24	12	–	ns	
t_{WSTRH}	minimum strobe pulse width HIGH	5	80	40	–	ns	
		10	60	30	–	ns	
		15	24	12	–	ns	
t_{su}	set-up time D to CP	5	60	30	–	ns	
		10	20	10	–	ns	
		15	15	5	–	ns	
t_h	hold time D to CP	5	+5	−15	–	ns	
		10	20	5	–	ns	
		15	20	5	–	ns	
$f_{clk(max)}$	maximum clock frequency	5	5	10	–	MHz	
		10	11	22	–	MHz	
		15	14	28	–	MHz	

Note

1. Definition of symbol equivalent to 3-state outputs.

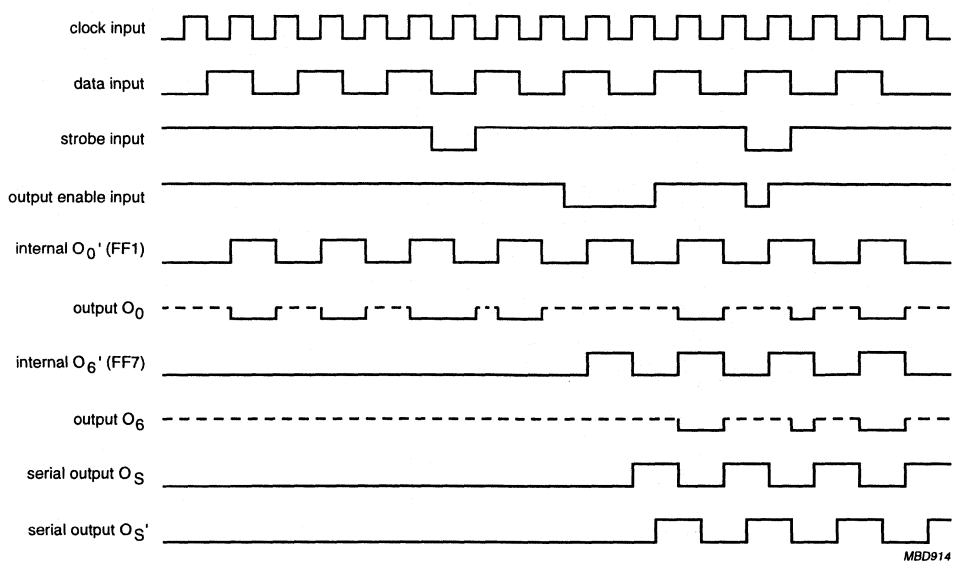


Fig.5 Timing diagram.

APPLICATION INFORMATION

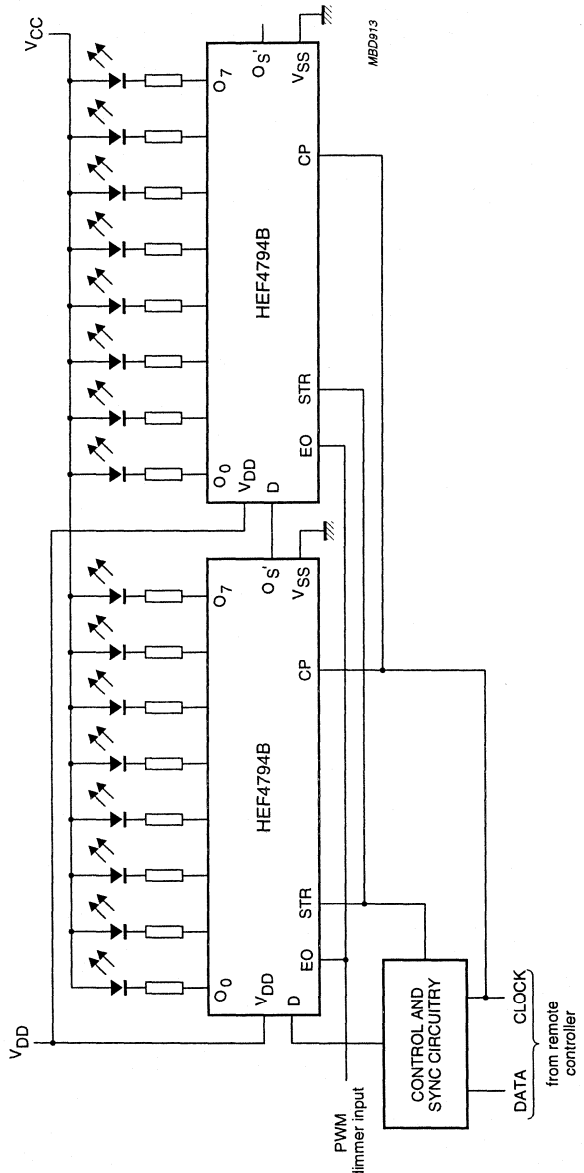


Fig.6 Application example: serial-to-parallel converting LED drivers.

12-stage shift-and-store register LED driver HEF4894B

APPLICATIONS

- **Automotive**
- **Industrial**

GENERAL DESCRIPTION

The HEF4894B is an 12 stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel LED driver outputs O_0 to O_{11}. Data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the outputs whenever the output enable (EO) signal is HIGH.

Two serial outputs (O_S and O_S') are available for cascading a number of HEF4894B devices. Data is available at O_S on positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at O_S' on the next negative-going clock edge and provides cascading HEF4894B devices when the clock rise time is slow.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PIN POSITION	MATERIAL	CODE
HEF4894BT	20	SO	plastic	SO20/SOT163-1
HEF4894BP	20	DIL	plastic	DIL20/SOT146-1

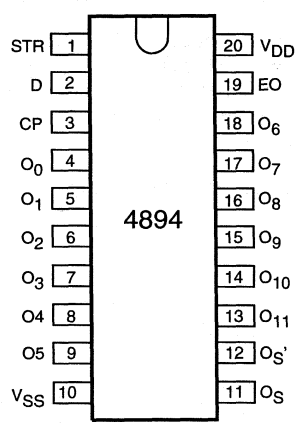
PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	STR	strobe input
2	D	data input
3	CP	clock input
4, 5, 6, 7, 8, 9, 18, 17, 16, 15, 14, 13	O_0 to O_{11}	parallel outputs (open drain)
10	V_{SS}	ground
11, 12	O_S, O_S'	serial outputs
19	EO	output enable input
20	V_{DD}	positive supply voltage

FAMILY DATA

See Family Specifications except for:
Rating for DC current into any open-drain output: 40 mA.

I_{DD} LIMITS category MSI: see Family Specifications.



Preliminary pin assignment.

Fig.1 Pinning diagram.

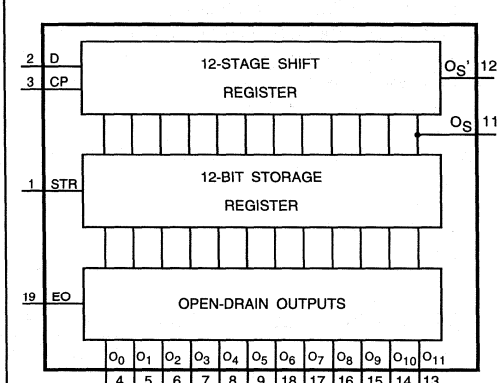


Fig.2 Functional diagram.

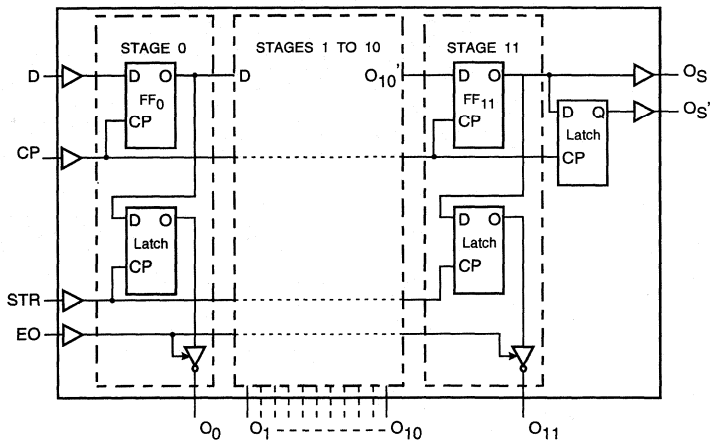


Fig.3 Logic diagram.

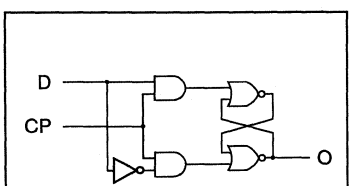


Fig.4 One D-latch.

FUNCTION TABLE

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	EO	STR	D	O_0	O_n	O_S	O_S'
↑	L	X	X	Z	Z	O_{10}'	nc
↓	L	X	X	Z	Z	nc	O_{11}
↑	H	L	X	nc	nc	O_{10}'	nc
↑	H	H	L	Z	$O_n - 1$	O_{10}'	nc
↑	H	H	H	L	$O_n - 1$	O_{10}'	nc
↓	H	H	H	nc	nc	nc	O_{11}

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
↑ = positive-going transition
↓ = negative-going transition

Z = high impedance OFF state
nc = no change
O_{11}' = the information in the twelfth shift register stage.

At the positive clock edge the information in the 10th register stage is transferred to the 11th register stage and the O_S output.

DC CHARACTERISTICS

V_{SS} = 0 V.

PARAMETER	V_{DD} (V)	SYMBOL	T_{amb} (°C)						UNIT	CONDITIONS
			−40		+25		+85			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
output voltage LOW; O_n	5	V_{OL}	−	0.75	−	0.75	−	1.5	V	V_I = V_{SS} or V_{DD}; $\|I_O\|$ < 20 mA
	10		−	0.75	−	0.75	−	1.5		
	15		−	0.75	−	0.75	−	1.5		
output leakage current; HIGH; O_n	5	I_{OZH}	−	2	−	2	−	15	µA	V_O = 15 V
	10		−	2	−	2	−	15		
	15		−	2	−	2	−	15		

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns.

PARAMETER	V_{DD} (V)	typical formula for P (µW)	where:
Dynamic power dissipation per package (P)	5	1200 f_i + $\Sigma(f_oC_L)$ x V_{DD}^2	R_{load} = ∞ f_i = input frequency (MHz), f_o = output frequency (MHz), C_L = load capacitance (pF), $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	5550 f_i + $\Sigma(f_oC_L)$ x V_{DD}^2	
	15	15000 f_i + $\Sigma(f_oC_L)$ x V_{DD}^2	

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns.

PARAMETER	V_{DD} (V)	SYMBOL	TYP.	MAX.	UNIT	TYPICAL EXTRAPOLATION FORMULA
Propagation delay CP to O_S HIGH to LOW	5	t_{PHL}	160	320	ns	132 ns + (0.55 ns/pF) C_L
	10		65	130		53 ns + (0.23 ns/pF) C_L
	15		45	90		37 ns + (0.16 ns/pF) C_L
Propagation delay CP to O_S LOW to HIGH	5	t_{PLH}	130	260	ns	102 ns + (0.55 ns/pF) C_L
	10		55	110		44 ns + (0.23 ns/pF) C_L
	15		40	80		32 ns + (0.16 ns/pF) C_L
Propagation delay CP to O_S' HIGH to LOW	5	t_{PHL}	120	240	ns	92 ns + (0.55 ns/pF) C_L
	10		50	100		39 ns + (0.23 ns/pF) C_L
	15		40	80		32 ns + (0.16 ns/pF) C_L
Propagation delay CP to O_S' LOW to HIGH	5	t_{PLH}	130	260	ns	102 ns + (0.55 ns/pF) C_L
	10		60	120		49 ns + (0.23 ns/pF) C_L
	15		45	90		37 ns + (0.16 ns/pF) C_L
Propagation delay CP to O_n OFF to LOW	5	t_{PZL}	240	480	ns	see note 1
	10		80	160		
	15		55	110		
Propagation delay CP to O_n LOW to OFF	5	t_{PLZ}	170	340	ns	see note 1
	10		75	150		
	15		60	120		
Propagation delay STR to O_n OFF to LOW	5	t_{PZL}	140	280	ns	see note 1
	10		70	140		
	15		55	110		
Propagation delay STR to O_n LOW to OFF	5	t_{PLZ}	100	200	ns	see note 1
	10		40	100		
	15		35	70		
Output transition time; O_s, O_s' HIGH to LOW	5	t_{THL}	85	170	ns	35 ns + (1.0 ns/pF) C_L
	10		40	80		19 ns + (0.42 ns/pF) C_L
	15		30	60		16 ns + (0.28 ns/pF) C_L
Output transition time; O_s, O_s' LOW to HIGH	5	t_{TLH}	85	170	ns	35 ns + (1.0 ns/pF) C_L
	10		40	80		19 ns + (0.42 ns/pF) C_L
	15		30	60		16 ns + (0.28 ns/pF) C_L

Note

1. Definition of symbol equivalent to 3-state outputs.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns.

PARAMETER	V_{DD} (V)	typical formula for P (µW)	where:
Dynamic power dissipation per package (P)	5	1200 f_i + $\Sigma(f_oC_L)$ x V_{DD}^2	R_{load} = ∞ f_i = input frequency (MHz), f_o = output frequency (MHz), C_L = load capacitance (pF), $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	5550 f_i + $\Sigma(f_oC_L)$ x V_{DD}^2	
	15	15000 f_i + $\Sigma(f_oC_L)$ x V_{DD}^2	

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns.

PARAMETER	V_{DD} (V)	SYMBOL	TYP.	MAX.	UNIT	TYPICAL EXTRAPOLATION FORMULA
Propagation delay CP to O_S HIGH to LOW	5	t_{PHL}	160	320	ns	132 ns + (0.55 ns/pF) C_L
	10		65	130		53 ns + (0.23 ns/pF) C_L
	15		45	90		37 ns + (0.16 ns/pF) C_L
Propagation delay CP to O_S LOW to HIGH	5	t_{PLH}	130	260	ns	102 ns + (0.55 ns/pF) C_L
	10		55	110		44 ns + (0.23 ns/pF) C_L
	15		40	80		32 ns + (0.16 ns/pF) C_L
Propagation delay CP to O_S' HIGH to LOW	5	t_{PHL}	120	240	ns	92 ns + (0.55 ns/pF) C_L
	10		50	100		39 ns + (0.23 ns/pF) C_L
	15		40	80		32 ns + (0.16 ns/pF) C_L
Propagation delay CP to O_S' LOW to HIGH	5	t_{PLH}	130	260	ns	102 ns + (0.55 ns/pF) C_L
	10		60	120		49 ns + (0.23 ns/pF) C_L
	15		45	90		37 ns + (0.16 ns/pF) C_L
Propagation delay CP to O_n OFF to LOW	5	t_{PZL}	240	480	ns	see note 1
	10		80	160		
	15		55	110		
Propagation delay CP to O_n LOW to OFF	5	t_{PLZ}	170	340	ns	see note 1
	10		75	150		
	15		60	120		
Propagation delay STR to O_n OFF to LOW	5	t_{PZL}	140	280	ns	see note 1
	10		70	140		
	15		55	110		
Propagation delay STR to O_n LOW to OFF	5	t_{PLZ}	100	200	ns	see note 1
	10		40	100		
	15		35	70		
Output transition time; O_s, O_s' HIGH to LOW	5	t_{THL}	85	170	ns	35 ns + (1.0 ns/pF) C_L
	10		40	80		19 ns + (0.42 ns/pF) C_L
	15		30	60		16 ns + (0.28 ns/pF) C_L
Output transition time; O_s, O_s' LOW to HIGH	5	t_{TLH}	85	170	ns	35 ns + (1.0 ns/pF) C_L
	10		40	80		19 ns + (0.42 ns/pF) C_L
	15		30	60		16 ns + (0.28 ns/pF) C_L

Note

1. Definition of symbol equivalent to 3-state outputs.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns.

PARAMETER	V_{DD} (V)	SYMBOL	MIN.	TYP.	MAX.	UNIT
output enable time EO to O_n OFF to LOW	5 10 15	t_{PZL}	– – –	100 55 50	200 110 100	ns
output disable time EO to O_n LOW to OFF	5 10 15	t_{PLZ}	– – –	80 40 30	160 80 60	ns
minimum clock pulse width LOW	5 10 15	t_{WCPL}	60 30 24	30 15 12	– – –	ns
minimum strobe pulse width HIGH	5 10 15	t_{WSTRH}	80 60 24	40 30 12	– – –	ns
set-up time D to CP	5 10 15	t_{su}	60 20 15	30 10 5	– – –	ns
hold time D to CP	5 10 15	t_{hold}	5 20 20	−15 5 5	– – –	ns
Maximum clock pulse frequency	5 10 15	f_{max}	5 11 14	10 22 28	– – –	MHz

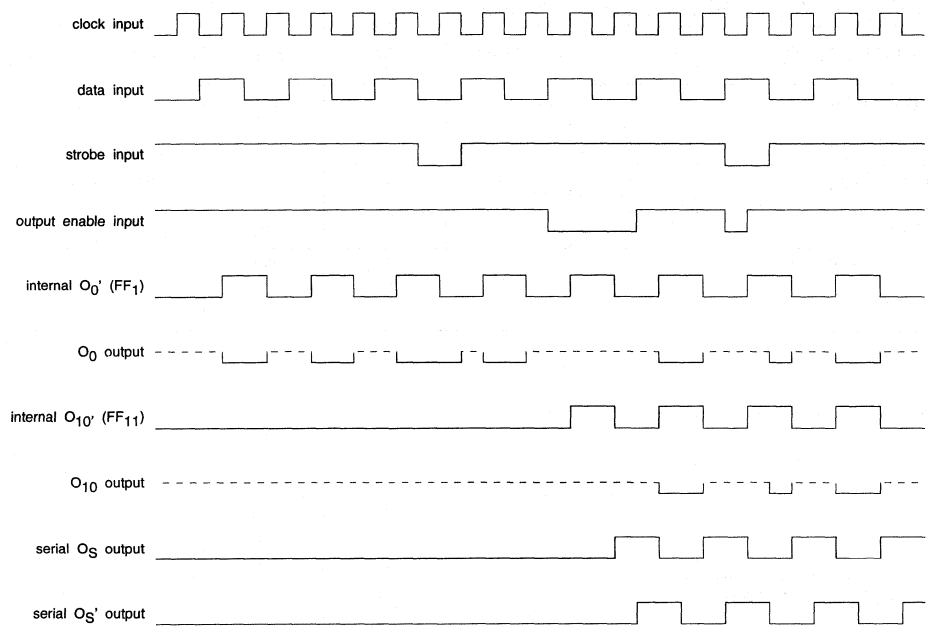


Fig.5 Timing diagram.

APPLICATION INFORMATION

An example of applications for the HEF4894B is:

- Serial-to-parallel converting LED driver

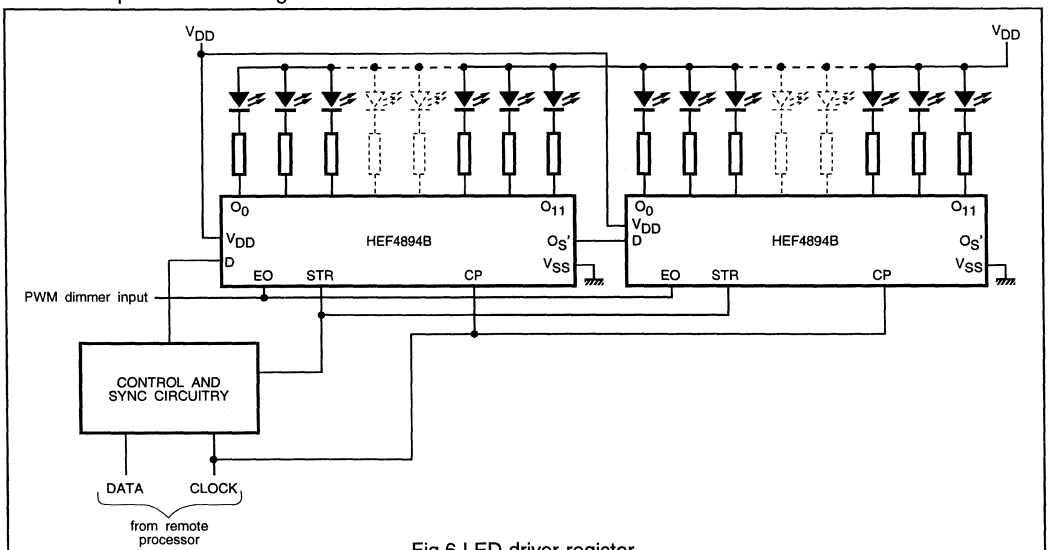


Fig.6 LED driver register.

AMPLIFIERS

Quad voltage comparator AU2901

DESCRIPTION

The AU2901 consists of four independent precision voltage comparators, with an offset voltage specification as low as 2.0mV max for each comparator, which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common–mode voltage range includes ground, even though they are operated from a single power supply voltage.

The AU2901 was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the AU2901 will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

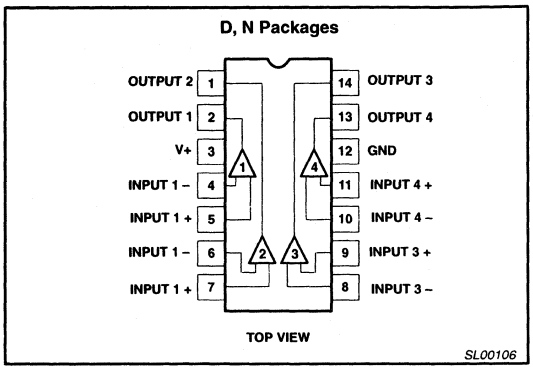
FEATURES

- Wide single supply voltage range 2.0VDC to 36VDC or dual supplies ±1.0VDC to ±18VDC
- Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/comparator at 5.0VDC)
- Low input biasing current 25nA
- Low input offset current ±5nA and offset voltage
- Input common–mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 250mV at 4mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

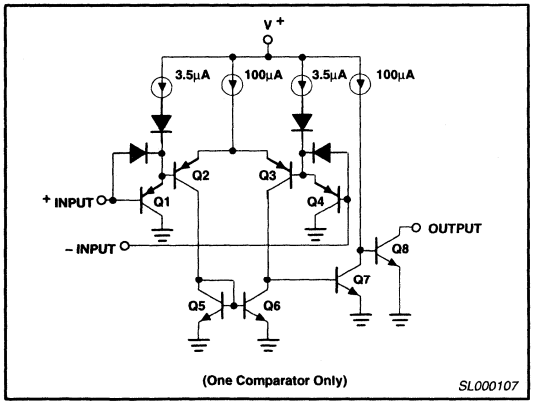
APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

PIN CONFIGURATION



EQUIVALENT CIRCUIT



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14–Pin Plastic Small Outline (SO) Package	–40°C to +125°C	AU2901D	SOT108-1
14–Pin Plastic Dual In-Line Package (DIP)	–40°C to +125°C	AU2901N	SOT27-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	V_{CC} supply voltage	36 or ±18	V_{DC}
V_{DIFF}	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	–0.3 to +36	V_{DC}
P_{DMAX}	Maximum power dissipation, T_A=25°C (still–air)[1]		
	N package	1420	mW
	D package	1040	mW
	Output short–circuit to ground[2]	Continuous	
I_{IN}	Input current (V_{IN}<–0.3V_{DC})[3]	50	mA
T_A	Operating temperature range		
	AU2901	–40 to +125	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C, at the following rates:
   N Package at 11.4mW/°C
   D Package at 8.3mW/°C
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector–base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which was negative, again returns to a value greater than –0.3V_{DC}.

ELECTRICAL CHARACTERISTICS

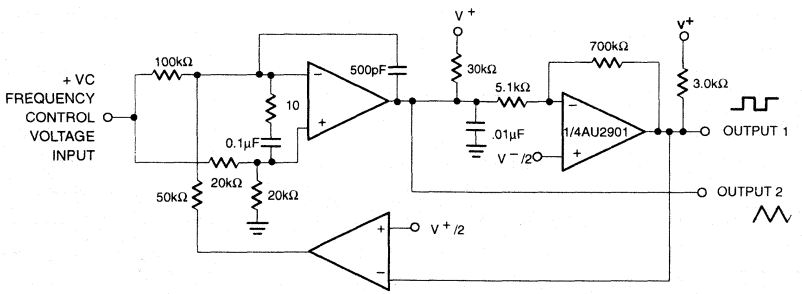
$V+=5V_{DC}$, AU2901: $-40°C$, $T_A \leq 125°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	AU2901			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage[2]	$T_A = 25°C$ Over temp.		±2.0 ±9	±7.0 ±15	mV
V_{CM}	Input common–mode voltage range[3]	$T_A = 25°C$ Over temp.	0 0		V+–1.5 V+–2.0	V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}[5] $\geq 0V_{DC}$ (or V– if need)			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		 25 200	 250 500	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		 ±5 ±50	 ±50 ±200	 nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN}(+) = 0$, $V_O \leq 1.5V_{DC}$, $T_A = 25°C$	6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1V_{DC}$, $V_{IN}(-) = 0$ $V_O = 5V_{DC}$, $T_A = 25°C$ $V_O = 30V_{DC}$, Over temp.		0.1	 1.0	nA µA
I_{CC}	Supply current	$R_L = \infty$ on comparators, $T_A = 25°C$ V+ = 30V		0.8 1.0	2.0 2.5	mA
A_V	Voltage gain	$R_L \geq 15k\Omega$, $V+ = 15V_{DC}$	25	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25°C$ Over temp.		 400	 400 700	mV
t_{LSR}	Large–signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4V_{DC}$, $V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300		ns
t_R	Response time[5]	$V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3		µs

NOTES:

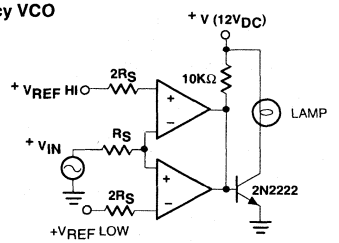
1. Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common–mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V_{DC}$ (or $0.3V_{DC}$ below the magnitude of the negative power supply, if used).
2. At output switch point, $V_O \approx 1.4V_{DC}$, R_S=0Ω with V+ from $5V_{DC}$ to $30V_{DC}$; and over the full input common–mode range ($0V_{DC}$ to $V+ - 1.5V_{DC}$).
3. The input common–mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common–mode voltage range is V+ – 1.5V, but either or both inputs can go to $30V_{DC}$ without damage.
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The response time specified is for a 100mV input step with a 5mV overdrive. For larger overdrive signals, 300ns can be obtained (see Typical Performance Characteristics section).

EQUIVALENT CIRCUIT

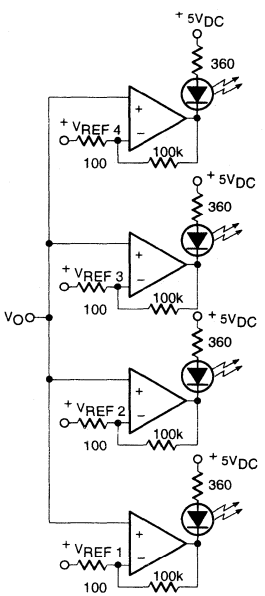


NOTES:
V+ = 30V$_{DC}$
+ 250m V$_{DC}$ ≤ V$_C$ ≤ 50V$_{DC}$
700H ≤ f$_O$ = 100kHz

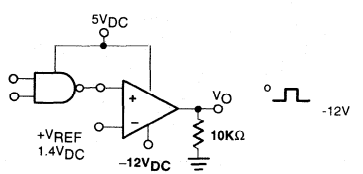
Two–Decade High–Frequency VCO



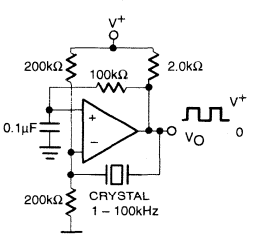
Limit Comparator



Visible Voltage Indicator



TTL–to–MOS Logic Converter



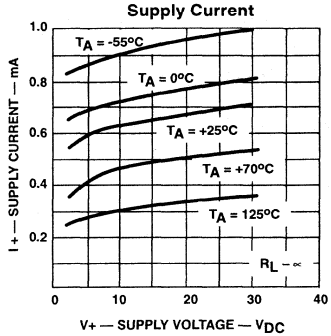
Crystal–Controlled Oscillator

NOTE:
Input of unused comparators should be grounded.

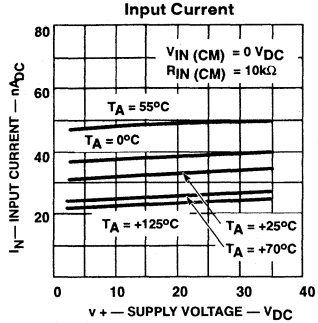
SL00108

TYPICAL PERFORMANCE CHARACTERISTICS

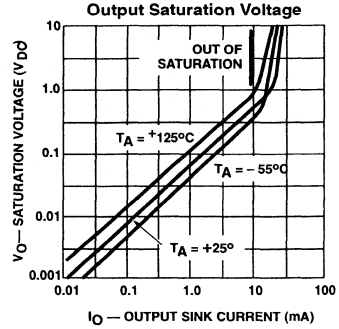
Supply Current



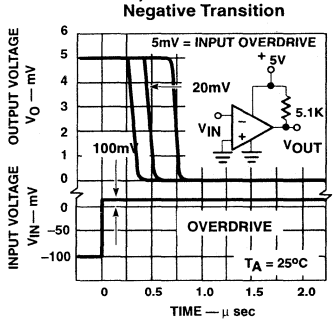
Input Current



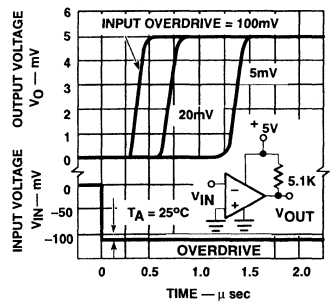
Output Saturation Voltage



Response Time for Various Input Overdrives — Negative Transition



Response Time for Various Input Overdrives — Positive Transition



SL00109

Low power quad operational amplifier AU2902

DESCRIPTION

The AU2902 consists of four independent, high-gain, internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages.

UNIQUE FEATURES

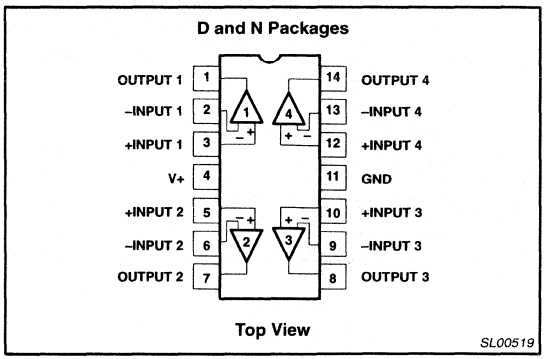
In the linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain crossover frequency and the input bias current are temperature-compensated.

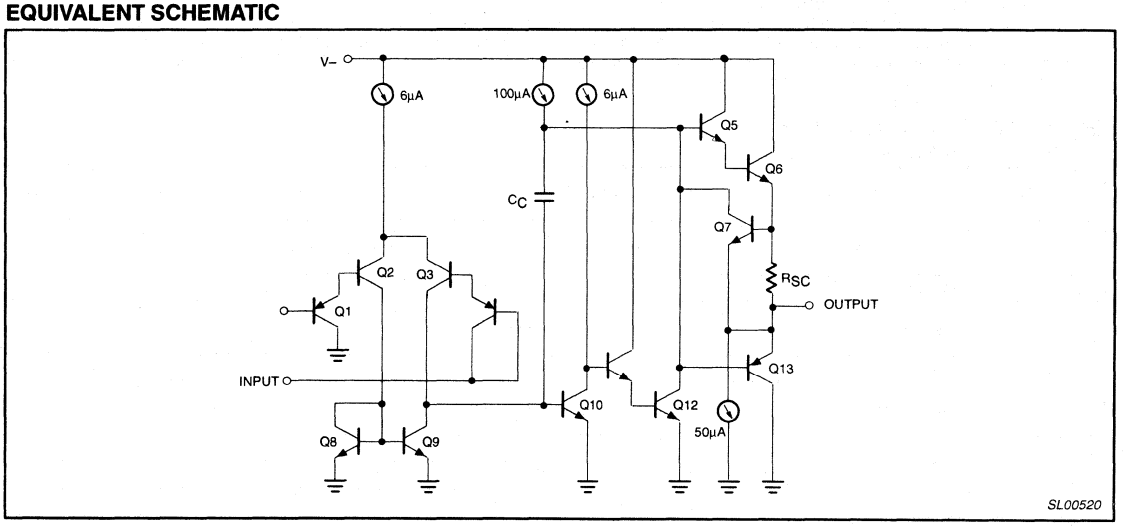
FEATURES

- Internally frequency-compensated for unity gain
- Large DC voltage gain: 100dB
- Wide bandwidth (unity gain): 1MHz (temperature-compensated)
- Wide power supply range Single supply: $3V_{DC}$ to $30V_{DC}$ or dual supplies: $\pm1.5V_{DC}$ to $\pm15V_{DC}$
- Very low supply current drain: essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)
- Low input bias current: $45nA_{DC}$ (temperature-compensated)
- Low input offset voltage: $2mV_{DC}$ and offset current: $5nA_{DC}$
- Differential input voltage range equal to the power supply voltage
- Large output voltage: $0V_{DC}$ to V_{CC}-$1.5V_{DC}$ swing

PIN CONFIGURATION



EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	-40 to +125°C	AU2902N	SOT27-1
14-Pin Plastic Small Outline (SO) Package	-40 to +125°C	AU2902D	SOT108-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	32 or ±16	V_{DC}
V_{IN}	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	–0.3 to +32	V_{DC}
P_{DMAX}	Maximum power dissipation, T_A=25°C(still–air)[1]		
	N package	1420	mW
	D package	1040	mW
	Output short–circuit to GND one amplifier V_{CC}<15V_{DC} and T_A=25°C	Continuous	
I_{IN}	Input current (V_{IN}<–0.3V)[3]	50	mA
T_A	Operating ambient temperature range		
	AU2902	–40 to +125	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. Derate above 25°C at the following rates:
   N package at 11.4mW/°C
   D package at 8.3mW/°C
2. Short–circuits from the output to V_{CC}+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA, independent of the magnitude of V_{CC}. At values of supply voltage in excess of +15V_{DC} continuous short–circuits can exceed the power dissipation ratings and cause eventual destruction.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector–base junction of the input PNP transistors becoming forward biased and thereby acting as input bias clamps. In addition, there is also lateral NPN parasitic transistor action on the IC chip. This action can cause the output voltages of the op amps to go to the V+ rail (or to ground for a large overdrive) during the time that the input is driven negative.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=5V, T_A=25°C unless otherwise specified.

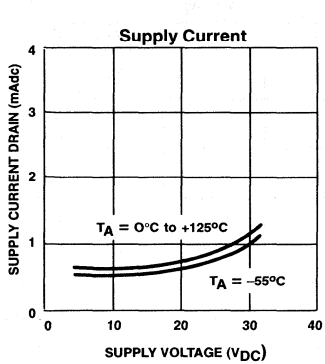
SYMBOL	PARAMETER	TEST CONDITIONS	AU2902			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω		±2	±7	mV
		R_S=0Ω, over temp.			±9	
$\Delta V_{OS}/\Delta T$	Temperature drift	R_S=0Ω, over temp.		7		µV/°C
I_{BIAS}	Input current[2]	I_{IN}(+) or I_{IN}(–)		45	250	nA
		I_{IN}(+) or I_{IN}(–), over temp.		40	500	
$\Delta I_{BIAS}/\Delta T$	Temperature drift	Over temp.		50		pA/°C
I_{OS}	Offset current	I_{IN}(+)–I_{IN}(–)		±5	±50	nA
		I_{IN}(+)–I_{IN}(–), over temp.			±150	
$\Delta I_{OS}/\Delta T$	Temperature drift	Over temp.		10		pA/°C
V_{CM}	Common–mode voltage range[3]	V_{CC}≤30V	0		V_{CC}–1.5	V
		V_{CC}≤30V, over temp.	0		V_{CC}–2	V
CMRR	Common–mode rejection ratio	V_{CC}=30V	65	70		dB
V_{OUT}	Output voltage swing	R_L=2kΩ, V_{CC}=30V, over temp.	26			V
V_{OH}	Output voltage high	R_L≥10kΩ, V_{CC}=30V, over temp.	27	28		V

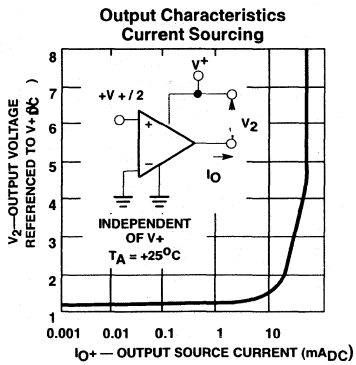
DC ELECTRICAL CHARACTERISTICS (Continued)

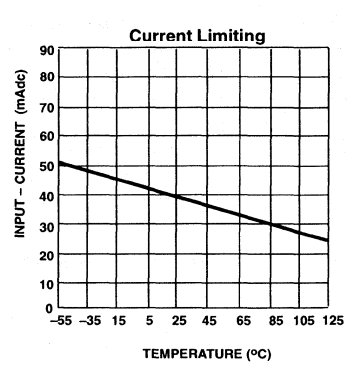
SYMBOL	PARAMETER	TEST CONDITIONS	AU2902			UNIT
			Min	Typ	Max	
V_{OL}	Output voltage low	$R_L \leq 10k\Omega$, V_{CC}=5V, over temp.		5	20	mV
I_{CC}	Supply current	$R_L=\infty$, V_{CC}=30V, over temp.		1.5	3	mA
		$R_L=\infty$, V_{CC}=5V, over temp.		0.7	1.2	
A_{VOL}	Large–signal voltage gain	V_{CC}=15V (for large V_O swing), $R_L \geq 2k\Omega$	25	100		V/mV
		V_{CC}=15V (for large V_O swing), $R_L \geq 2k\Omega$, over temp.	15			
	Amplifier–to–amplifier coupling[5]	f=1kHz to 20kHz, input referred		–120		dB
PSRR	Power supply rejection ratio	R_S=0Ω	65	100		dB
I_{OUT}	Output current Source	V_{IN}+=+1V, V_{IN}–=0V, V_{CC}=15V	20	40		mA
		V_{IN}+=+1V, V_{IN}–=0V, V_{CC}=15V, over temp.	10	20		
	Output current Sink	V_{IN}–=+1V, V_{IN}+=0V, V+=15V	10	20		
		V_{IN}–=+1V, V_{IN}+=0V, V_{CC}=15V, over temp.	5	8		
		V_{IN}–=+1V, V_{IN}+=0V, V_O=200mV	12	50		µA
I_{SC}	Short–circuit current[4]		10	40	60	mA
V_{DIFF}	Differential input voltage[3]				V_{CC}	V
GBW	Unity gain bandwidth			1		MHz
SR	Slew rate			0.3		V/µs
V_{NOISE}	Input noise voltage	f=1kHz		40		nV/√Hz

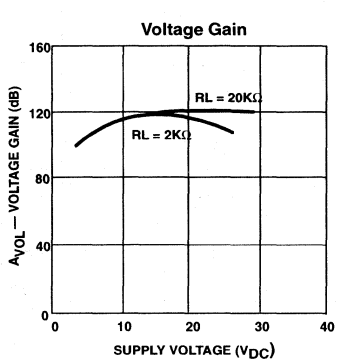
NOTES:
1. $V_O \approx 1.4V_{DC}$, R_S=0Ω with V_{CC} from 5V to 30V and over full input common–mode range ($0V_{DC}$+ to V_{CC} –1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common–mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common–mode voltage range is V_{CC} –1.5, but either or both inputs can go to +32V without damage.
4. Short–circuits from the output to V_{CC} can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V_{CC}. At values of supply voltage in excess of $+15V_{DC}$, continuous short–circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of coupling increases at higher frequencies.

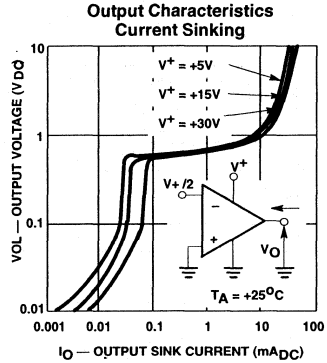
TYPICAL PERFORMANCE CHARACTERISTICS

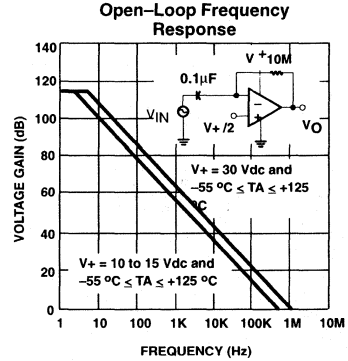

Supply Current
SUPPLY CURRENT DRAIN (mAdc)
T_A = O°C to +125°C
T_A = –55°C
SUPPLY VOLTAGE (V_{DC})

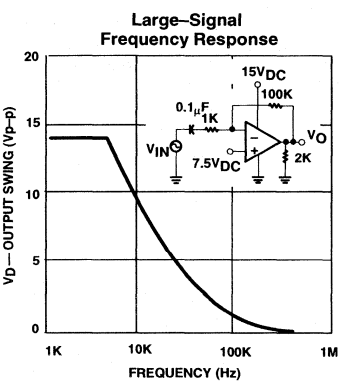

Output Characteristics
Current Sourcing
V_2—OUTPUT VOLTAGE REFERENCED TO V+ (V)
+V + / 2
V_2
I_O
INDEPENDENT OF V+
T_A = +25°C
I_{O+} — OUTPUT SOURCE CURRENT (mA_{DC})

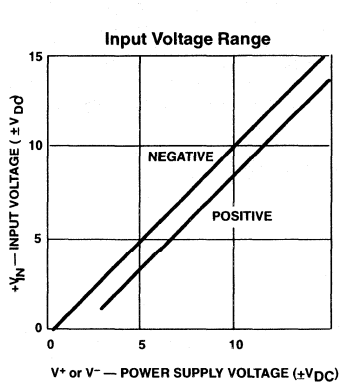

Current Limiting
INPUT – CURRENT (mAdc)
TEMPERATURE (°C)

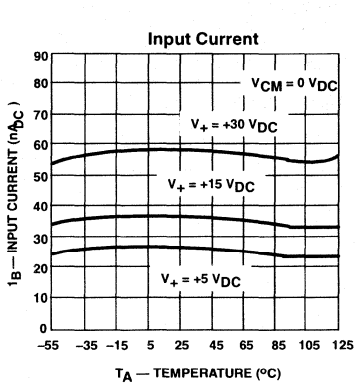

Voltage Gain
A_{VOL} — VOLTAGE GAIN (dB)
RL = 20KΩ
RL = 2KΩ
SUPPLY VOLTAGE (V_{DC})


Output Characteristics
Current Sinking
VOL — OUTPUT VOLTAGE (V DC)
V+ = +5V
V+ = +15V
V+ = +30V
V+ /2
V_O
T_A = +25°C
I_O — OUTPUT SINK CURRENT (mA_{DC})


Open–Loop Frequency
Response
VOLTAGE GAIN (dB)
V +10M
0.1μF
V_{IN}
V+ /2
V_O
V+ = 30 Vdc and
–55 °C ≤ TA ≤ +125 °C
V+ = 10 to 15 Vdc and
–55 °C ≤ TA ≤ +125 °C
FREQUENCY (Hz)

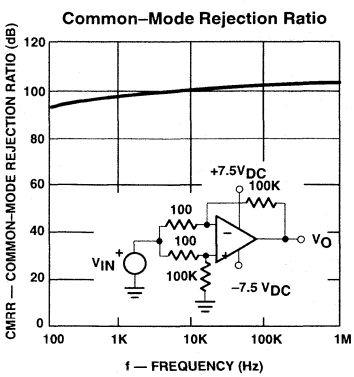

Large–Signal
Frequency Response
V_O — OUTPUT SWING (Vp-p)
15V_{DC}
100K
0.1μF
1K
V_{IN}
V_O
7.5V_{DC}
2K
FREQUENCY (Hz)

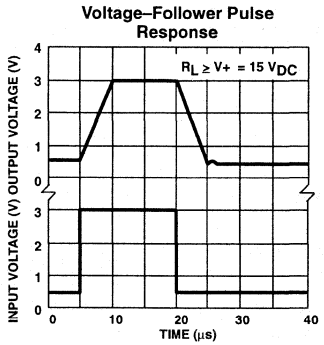

Input Voltage Range
$+V_{IN}$ — INPUT VOLTAGE (± V DC)
NEGATIVE
POSITIVE
V+ or V– — POWER SUPPLY VOLTAGE (±V_{DC})

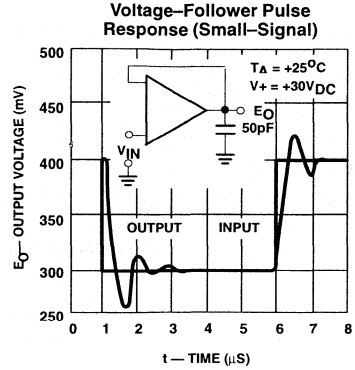

Input Current
I_B — INPUT CURRENT (nA DC)
V_{CM} = 0 V_{DC}
V_+ = +30 V_{DC}
V_+ = +15 V_{DC}
V_+ = +5 V_{DC}
T_A — TEMPERATURE (°C)

SL00521

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

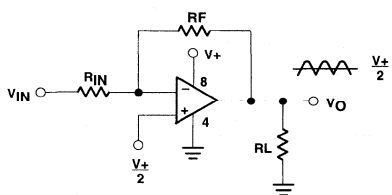




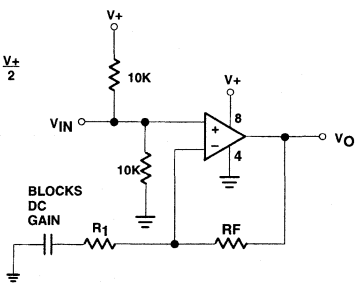


SL00522

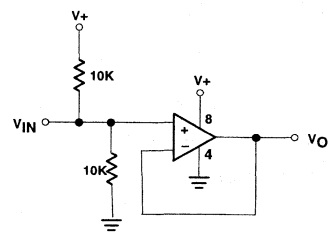
TYPICAL APPLICATIONS



Single Supply Inverting Amplifier



Non–Inverting Amplifier



Output Biasing Voltage–Follower

SL00523

Low power dual voltage comparator AU2903

DESCRIPTION

The AU2903 consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0mV max. for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

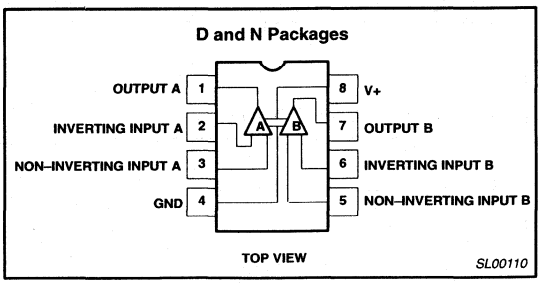
FEATURES

- Wide single supply voltage range 2.0V_{DC} to 36V_{DC} or dual supplies ±1.0V_{DC}, to ±18V_{DC}
- Very low supply current drain (0.8mA) independent of supply voltage (2.0mW/comparator at 5.0V_{DC})
- Low input biasing current 25nA
- Low input offset current ±5nA and offset voltage ±2mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 250mV at 4mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

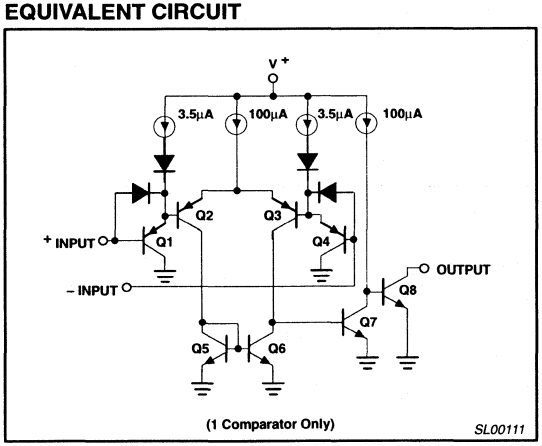
APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

PIN CONFIGURATION



EQUIVALENT CIRCUIT



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	-40°C to +125°C	AU2903D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +125°C	AU2903N	SOT97-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	36 or ±18	V_{DC}
	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	-0.3 to +36	V_{DC}
P_{DMAX}	Maximum power dissipation, T_A=25°C (still-air)[3]		
	N package	1160	mW
	D package	780	mW
	Output short-circuit to ground[1]	Continuous	
I_{IN}	Input current (V_{IN}<-0.3V_{DC})[2]	50	mA
T_A	Operating temperature range		
	AU2903	-40 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V_{DC}.
3. Derate above 25°C, at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C

DC AND AC ELECTRICAL CHARACTERISTICS

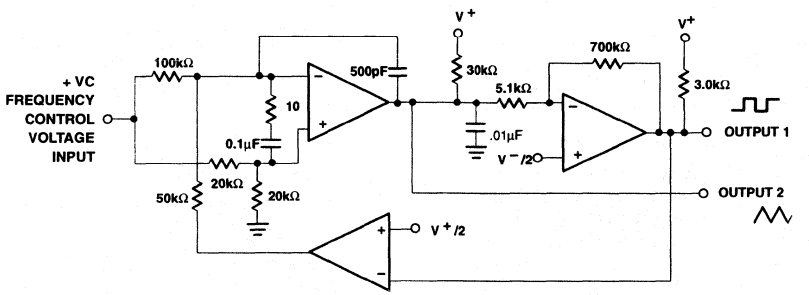
V+=5V_{DC}, AU2903; -40°C, T_A ≤ +125°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	AU2903			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage[2]	T_A = 25°C Over temp.		±2.0 ±9	±7.0 ±15	mV
V_{CM}	Input common-mode voltage range[3, 6]	T_A = 25°C Over temp.	0 0		V+-1.5 V+-2.0	V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}s ≥ 0V_{DC} (or V- if need)			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A=25°C Over temp.		 25 200	 250 500	nA
I_{OS}	Input offset current	$I_{IN(+)}$ - $I_{IN(-)}$ T_A = 25°C Over temp.		 ±5 ±50	 ±50 ±200	 nA nA
I_{OL}	Output sink current	$V_{IN(-)}$ ≥ 1V_{DC}, $V_{IN(+)}$ = 0, V_O ≤ 1.5V_{DC} T_A = 25°C	6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)}$ ≥ 1V_{DC}, $V_{IN(-)}$ = 0 V_O = 5V_{DC}, T_A = 25°C V_O = 30V_{DC}, over temp.		 0.1 	 1.0	 nA µA
I_{CC}	Supply current	R_L = ∞ on both comparators. T_A = 25°C V+ = 30V, over temp.		 0.8 1	 1 2.5	mA
A_V	Voltage gain	R_L ≥ 15kΩ, V+ = 15V_{DC}, T_A = 25°C	25	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)}$ ≥ 1V_{DC}, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4mA T_A = 25°C Over temp.		 400 	 400 700	mV
t_{LSR}	Large-signal response time	V_{IN} = TTL logic swing, V_{REF} = 1.4V_{DC} V_{RL} = 5V_{DC}, R_L = 5.1kΩ, T_A = 25°C		300		ns
t_R	Response time[5]	V_{RL} = 5V_{DC}, R_L = 5.1kΩ T_A = 25°C		1.3		µs

NOTES:

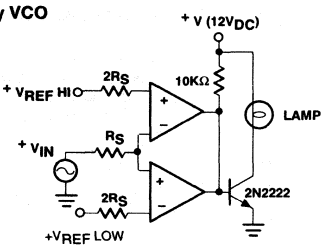
1. Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3V_{DC} (V_{DC} below the magnitude of the negative power supply, if used).
2. At output switch point, V_O ≈ 1.4V_{DC}, R_S = 0Ω with V+ from 5V_{DC} to 30V_{DC} and over the full input common-mode range (0V_{DC} to V+-1.5V_{DC}).
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+-1.5V, but either or both inputs can go to 30V_{DC} without damage.
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The response time specified is for a 100mV input step with a 5mV overdrive.
6. For input signals that exceed V_{CC}, only the over-driven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

TYPICAL APPLICATIONS

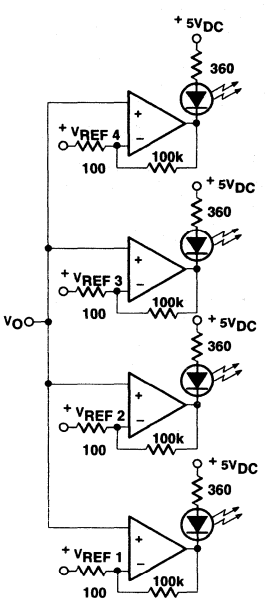


NOTES:
V+ = $30V_{DC}$
+ 250m $V_{DC} \leq V_C = 50V_{DC}$
$700H \leq f_O = 100kHz$

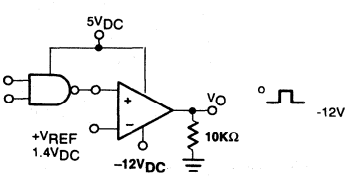
Two–Decade High–Frequency VCO



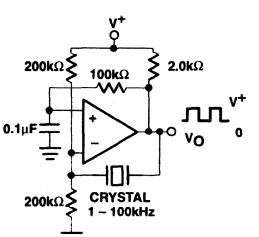
Limit Comparator



Visible Voltage Indicator



TTL–to–MOS Logic Converter

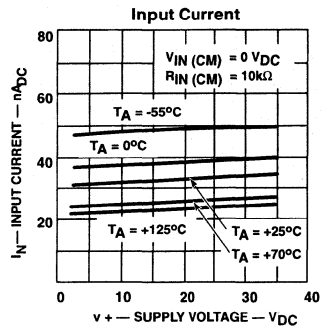


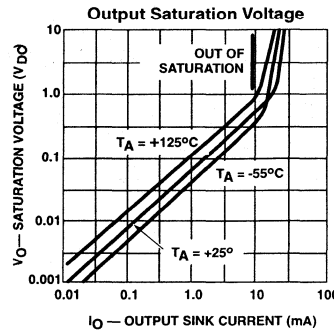
Crystal–Controlled Oscillator

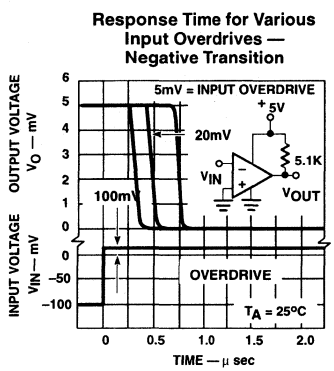
NOTE:
Input of unused comparators should be grounded.

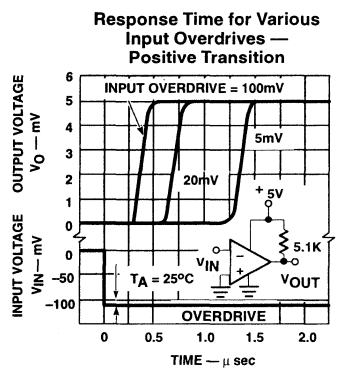
SL00112

TYPICAL PERFORMANCE CHARACTERISTICS









SL00113

Low power dual operational amplifier AU2904

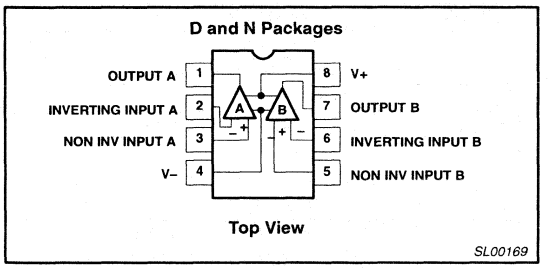
DESCRIPTION

The AU2904 consists of two independent, high-gain, internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible, and the low power supply current drain is independent of the magnitude of the power supply voltage.

FEATURES

- Internally frequency-compensated for unity gain
- Large DC voltage gain: 100dB
- Wide bandwidth (unity gain): 1MHz (temperature-compensated)
- Wide power supply range Single supply: $3V_{DC}$ to $30V_{DC}$ or dual supplies: $\pm1.5V_{DC}$ to $\pm15V_{DC}$
- Very low supply current drain (400μA): essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)
- Low input bias current: $45nA_{DC}$ (temperature-compensated)
- Low input offset voltage: $2mV_{DC}$ and offset current: $5nA_{DC}$
- Differential input voltage range equal to the power supply voltage
- Large output voltage: $0V_{DC}$ to V+-$1.5V_{DC}$ swing

PIN CONFIGURATION



UNIQUE FEATURES

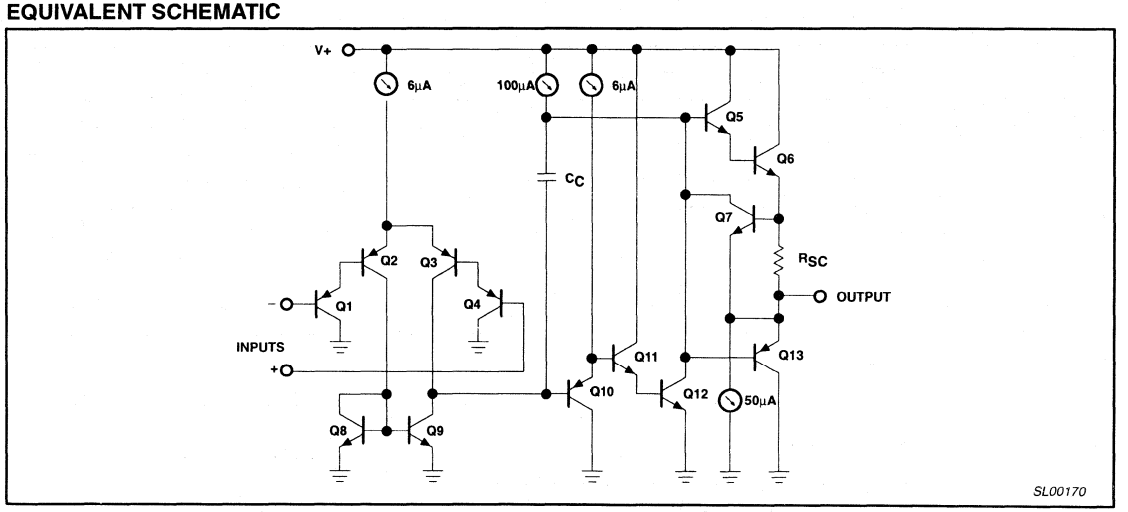
In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain crossover frequency and the input bias current are temperature-compensated.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +125°C	AU2904N	SOT97-1
8-Pin Plastic Small Outline (SO) Package	-40 to +125°C	AU2904D	SOT96-1

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage V+	32 or ±16	V_{DC}
	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	-0.3 to +32	V_{DC}
P_{DMAX}	Maximum power dissipation, T_A=25°C(still-air)[1]		
	N package	1160	mW
	D package	780	mW
	Output short-circuit to GND[5] V+<15V_{DC} and T_A=25°C	Continuous	
T_A	Operating ambient temperature range AU2904	-40 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. Derate above 25°C at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=25°C V+ =+5V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	AU2904			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω		±2	±7	mV
		R_S=0Ω, over temp.			±9	
V_{OS}	Drift	R_S=0Ω, over temp.		7		µV/°C
I_{OS}	Offset current	$I_{IN}(+)-I_{IN}(-)$		±5	±50	nA
		Over temp.			±150	nA
I_{OS}	Drift	Over temp.		10		pA/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	250	nA
		Over temp., $I_{IN}(+)$ or $I_{IN}(-)$		40	500	
I_{BIAS}	Drift	Over temp.		50		pA/°C
V_{CM}	Common-mode voltage range[3]	V+=30V	0		V+-1.5	V
		Over temp., V+=30V	0		V+-2.0	V
CMRR	Common-mode rejection ratio	V+=30V	65	70		dB
V_{OH}	Output voltage swing	R_L≥2kΩ, V+=30V, over temp.	26			V
		R_L≥10kΩ, V+=30V, over temp.	27	26		
V_{OL}	Output voltage swing	R_L≥10kΩ, Over temp.		5	20	mV
I_{CC}	Supply current	R_L=∞, V+=30V		0.5	1.0	mA
		R_L=∞ on all amplifiers, Over temp., V+=30V		0.6	1.2	mA
A_{VOL}	Large-signal voltage gain	R_L≥2kΩ, V_{OUT} ±10V, V+=15V	25	100		V/mV
		Over temp.	15			
PSRR	Supply voltage rejection ratio	R_S=0Ω	65	100		dB
	Amplifier-to-amplifier coupling[4]	f=1kHz to 20kHz (input referred)		-120		dB
I_{OUT}	Output current source	V_{IN+}=+1V_{DC}, V_{IN-}=0V_{DC}, V+=15V_{DC}	20	40		mA
		Over temp.	10	20		

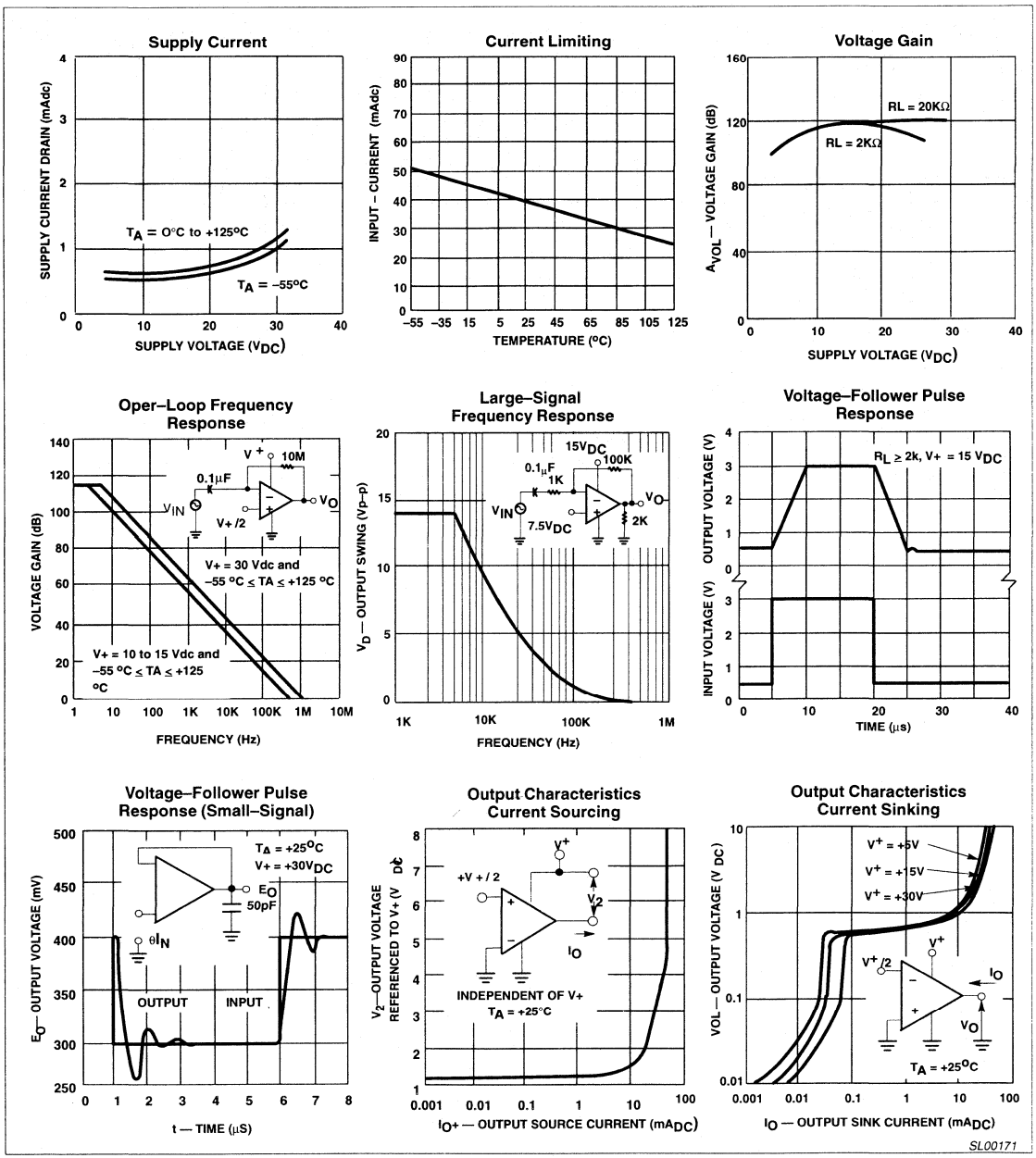
DC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	AU2904			UNIT
			Min	Typ	Max	
I_{OUT}	Output current					
	Sink	V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC}	10	20		mA
		V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC}, over temp.	5	8		mA
		V_{IN+}=0V, V_{IN-}=+1V_{DC}, V_O=200mV	12	50		µA
I_{SC}	Short circuit current[5]			40	60	mA
	Differential input voltage[3]				V+	V
GBW	Unity gain bandwidth	T_A=25°C		1		MHz
SR	Slew rate	T_A=25°C		0.3		V/µs
V_{NOISE}	Input noise voltage	T_A=25°C f=1kHz		40		nV/√Hz

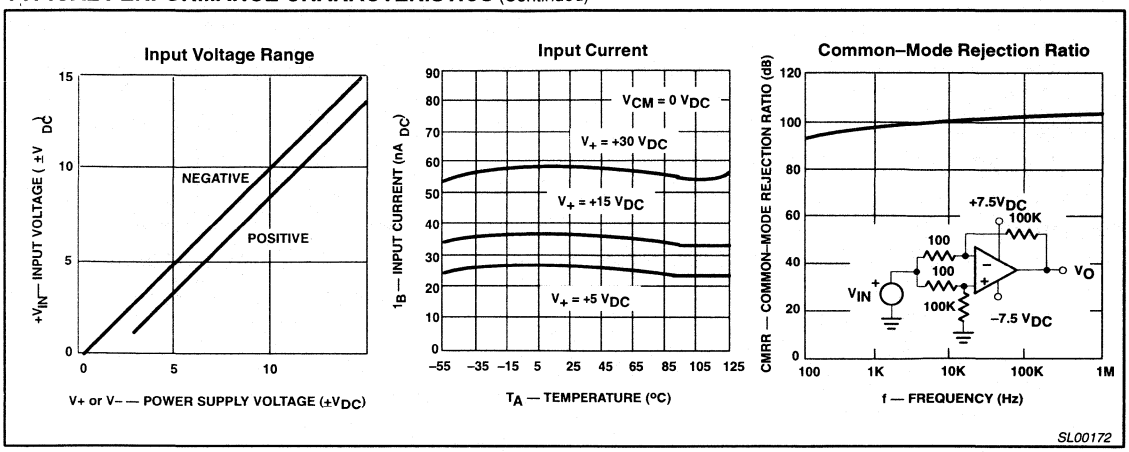
NOTES:

1. $V_O \approx$ 1.4V, R_S=0Ω with V_{CC} from 5V to 30V and over full input common-mode range (0V_{DC}+ to V_{CC}-1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+-1.5, but either or both inputs can go to +32V without damage.
4. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of coupling increases at higher frequencies.
5. Short-circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.

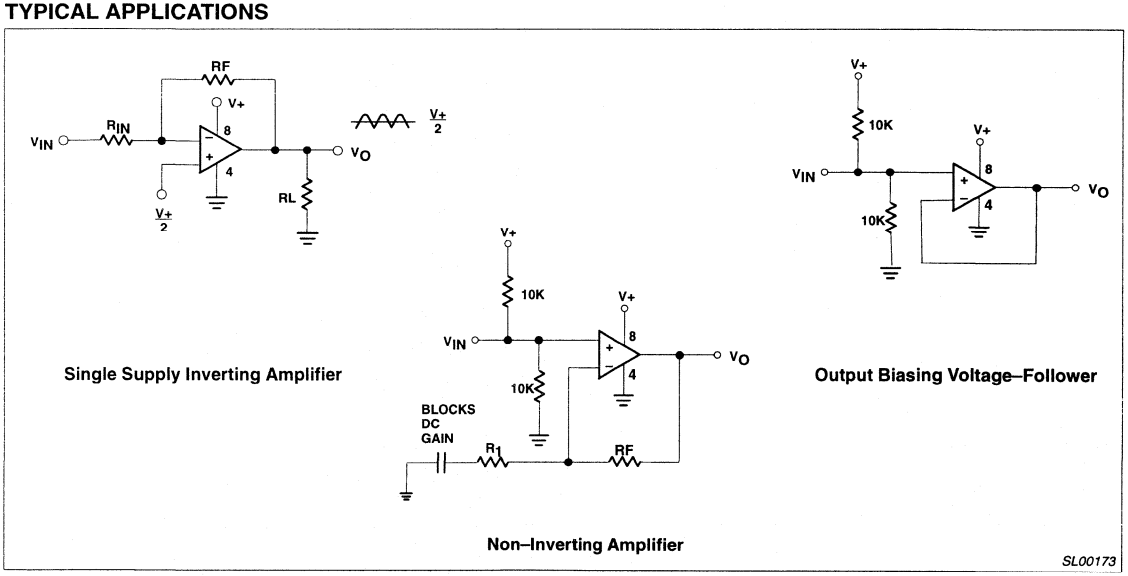
TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TYPICAL APPLICATIONS



Matched quad high-performance low-voltage operational amplifier

NE/SA5234

DESCRIPTION

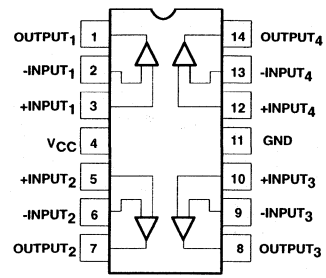
The NE/SA5234 is a matched, low voltage, high performance quad operational amplifier. Among its unique input and output characteristics is the capability for both input and output rail-to-rail operation, particularly critical in low voltage applications. The output swings to less than 50mV of both rails across the entire power supply range. The NE/SA5234 is capable of delivering 5.5V peak-to-peak across a 600Ω load and will typically draw only 700μA per amplifier. The bandwidth is 2.5MHz and the 1% settling time is 1.4μs.

FEATURES

- Wide common-mode input voltage range: 250mV beyond both rails
- Output swing within 50mV of both rails
- Functionality to 1.8V typical
- Low current consumption: 700μA per amplifier
- ±15mA output current capability
- Unity gain bandwidth: 2.5MHz
- Slew rate: 0.8V/μs
- Low noise: 25nV/√Hz
- Electrostatic discharge protection
- Short-circuit protection
- Output inversion prevention

PIN CONFIGURATION

N, and D PACKAGES



SL00568

APPLICATIONS

- Automotive electronics
- Signal conditioning and sensing amplification
- Portable instrumentation
  - Test and measurement
  - Medical monitors and diagnostics
  - Remote meters
- Audio equipment
- Security systems
- Communications
  - Pagers
  - Cellular telephone
  - LAN
  - 5V Datacom bus
- Error amplifier in motor drives
- Transducer buffer amplifier

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5234D	SOT108-1
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5234N	SOT27-1
14-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5234D	SOT108-1
14-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5234N	SOT27-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
V_{ESD}	ESD protection voltage at any pin[5] human body model robot model	 2000 200	 V V
V_S	Dual supply voltage	±3.5	V
V_{DP}	Voltage at any device pin[1]	$V_S \pm 0.5$	V
I_{DP}	Current into any device pin[1]	± 50	mA
V_{IN}	Differential input voltage[2]	0.5	V
V_{CM}	Common-mode input voltage (positive)	V_{CC} + 0.5	V
V_{CM}	Common-mode input voltage (negative)	V_{EE} - 0.5	V
P_D	Power dissipation[3]	500	mW
T_J	Operating junction temperature[3]	+150	°C
V_{SC}	Supply voltage allowing indefinite output short circuit to either rail[3,4]	7	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C
θ_{JA}	Thermal impedance 14 pin Plastic DIP 14 pin Plastic SO	 80 115	 °C/W °C/W

NOTES:
1. Each pin is protected by ESD diodes. The voltage at any pin is limited by the ESD diodes.
2. The differential input of each amplifier is limited by two internal diodes, connected in parallel and opposite to each other. For more differential input range, use differential resistors in series with the input pins.
3. The maximum operating junction temperature is +150°C. At elevated temperatures, devices must be derated according to the package thermal resistance and device mounting conditions. Derates above +25°C: F package at 6.7mW/°C; N package at 9.5mW/°C; D package at 6.25mW/°C.
4. Simultaneous short circuits of two or more amplifiers to the positive or negative rail can exceed the power dissipation ratings and cause eventual destruction of the device.
5. Guaranteed by design.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	+2 to +5.5	V
V_S	Dual supply voltage	±1 to ±2.75	V
V_{CM}	Common-mode input voltage (positive)	V_{CC} + 0.25	V
V_{CM}	Common-mode input voltage (negative)	V_{EE} - 0.25	V
T_A	Temperature NE SA	 0 to +70 -40 to +85	 °C °C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2 to 5.5V, V_{EE} = 0V, T_A = 25°C; $V_{EE} < V_{CM} < V_{CC}$; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234			SA5234			
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_{CC} = 5.5V		2.8	4.0		2.8	4.0	mA
		V_{CC} = 5.5V over full temperature range		3.0	4.6		3.2	4.8	
V_{OS}	Offset voltage			±0.2	±4		±0.2	±4	mV
		Over full temperature range		±0.4	±5		±0.6	±5	
$\Delta V_{OS}/\Delta T$	Offset voltage drift with temperature			4			4		µV/°C
ΔV_{OS}	Offset voltage difference between any amplifiers in the same package at the same common mode level[1]			0.4	3		0.4	3	mV
		Over full temperature range		0.8	4		1.2	4	
I_{OS}	Offset current			±3	±20		±3	±30	nA
		Over full temperature range		±4	±30		±6	±60	
$\Delta I_{OS}/\Delta T$	Offset current drift with temperature			0.02	±.3		0.03	±.3	nA/°C
I_B	Input bias current[1]	$V_{EE} < V_{CM} < V_{EE}$ +0.5V	-200	-90		-200	-90		nA
		Over full temperature range	-225	-100		-250	-150		
		V_{EE} +1V < V_{CM} < V_{CC}		25	70		25	75	
		Over full temperature range		35	100		35	120	
$\Delta I_B/\Delta T$	Input bias current drift with temperature			0.5			0.5		nA/°C
ΔI_B	Input bias current difference between any amplifier in the same package at the same common mode level.	$V_{EE} < V_{CM} < V_{EE}$ +0.5V		10	30		10	30	nA
		Over full temperature range		25	50		50	70	
		V_{EE} +1V < V_{CM} < V_{CC}		5	20		5	20	
		Over full temperature range		15	30		25	50	
V_{CM}	Common-mode input range	$V_{OS} \leq$ 6mV	V_{EE}-0.25		V_{CC}+0.25	V_{EE}-0.25		V_{CC}+0.25	V
		$V_{OS} \leq$ 6mV over full temperature range	V_{EE}-0.1		V_{CC}+0.1	V_{EE}-0.1		V_{CC}+0.1	
CMRR	Common-mode rejection ratio, small signal	$V_{EE} < V_{CM} < V_{EE}$+0.5V, V_{EE}+1V < V_{CM} < V_{CC}		100		90	100		dB
		Over full temperature range		100		80	90		
	Common-mode rejection ratio, large signal	$V_{EE} < V_{CM} < V_{CC}$		90			100		
		Over full temperature range		80			90		
PSRR	Power supply rejection ratio	$V_{EE} < V_{CM} < V_{CC}$	80	100		80	100		dB
		Over full temperature range	80	90		80	90		

DC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234			SA5234			
			MIN	TYP	MAX	MIN	TYP	MAX	
I_L	Peak load current, sink and source		10	12		10	12		mA
		Over full temperature range	5	8		5	8		
A_{VOL}	Open-loop voltage gain		90	110		90	110		dB
		Over full temperature range		90			90		
V_{OUT}	Output voltage swing	I_{PEAK} = 0.1mA	V_{EE}+0.05		V_{CC}-0.05	V_{EE}+0.1		V_{CC}-0.1	V
		I_{PEAK} = 10mA	V_{EE}+0.25		V_{CC}-0.25	V_{EE}+0.25		V_{CC}-0.25	
		I_{PEAK} = 5mA over full temp range	V_{EE}+0.2		V_{CC}-0.2	V_{EE}+0.2		V_{CC}-0.2	
	Output voltage swing for V_{CC} = 2.75V, V_{EE} = -2.75V	R_L = 2kΩ	V_{EE}+0.2		V_{CC}-0.2	V_{EE}+0.2		V_{CC}-0.2	V
		R_L = 600Ω,	V_{EE}+0.25		V_{CC}-0.25	V_{EE}+0.25		V_{CC}-0.25	

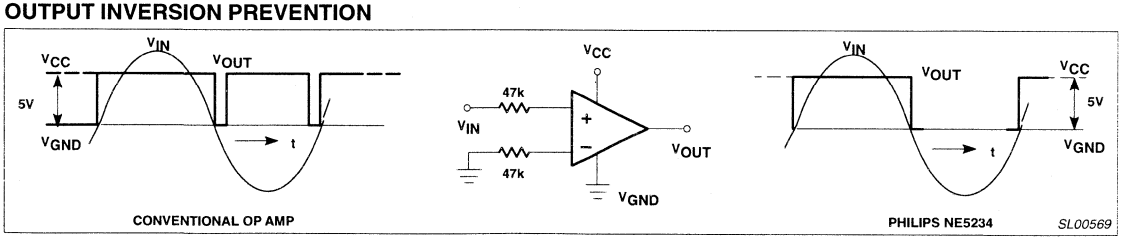
NOTES:
1. These parameters are measured for $V_{EE} < V_{CM} < V_{EE}$+.5V and for V_{EE}+1V < $V_{CM} < V_{CC}$. By design these parameters are intermediate for common mode ranges between the measured regions.

AC ELECTRICAL CHARACTERISTICS

T_A = +25°C; V_{CC} = 2 to 5.5V; R_L = 10k; C_L = 100pF; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234			SA/SE5234			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	Over full temperature range	0.5	0.8		0.5	0.8		V/µs
BW	Unity gain bandwidth: -3dB	Over full temperature range	2	2.5	4.0	2	2.5	4.0	MHz
θ_M	Phase Margin	C_L = 50pF		55			55		deg
t_S	1% settling time	A_V = 1, 1V step		1.4			1.4		µs
V_N	Input referred voltage noise	A_V = 1, R_S = 0Ω, at 1kHz		25			25		nV/Hz 1/2
THD	Total harmonic distortion	10kHz, $1V_{P-P}$, A_V = 1		0.1			0.1		%

OUTPUT INVERSION PREVENTION



PACKAGE INFORMATION

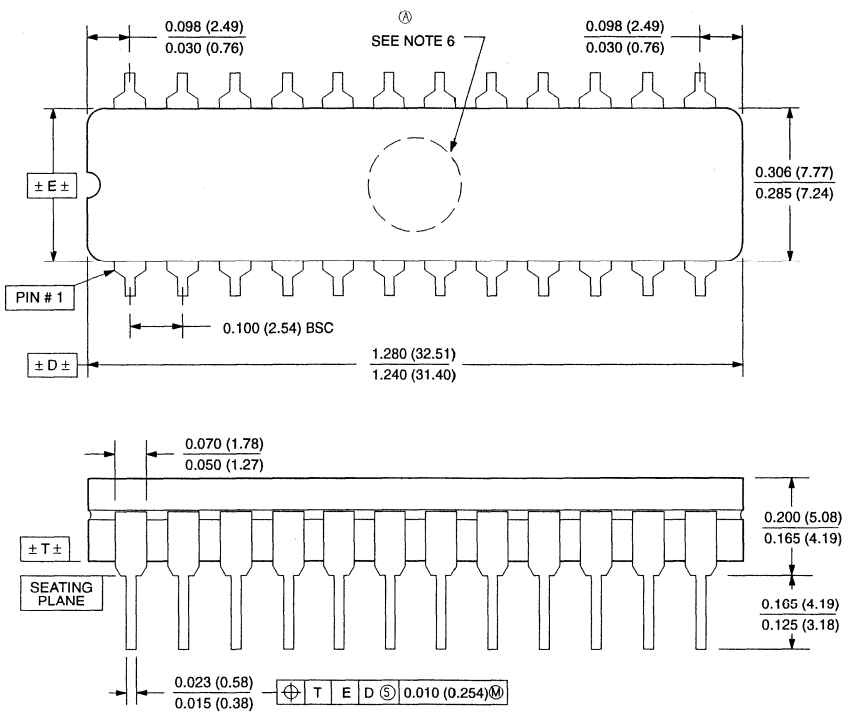
INDEX

Package information — Package outlines

NAME	DESCRIPTION	VERSION	PAGE
SO (small outline)			
SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1	1466
SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1	1467
SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1	1468
SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1	1469
SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1	1470
SSOP (shrink small outline package)			
SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1	1471
SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1	1472

CDIP

CDIP24: ceramic dual in-line (F) package (with window (FA) package); 24 leads (300 mil) 0586B

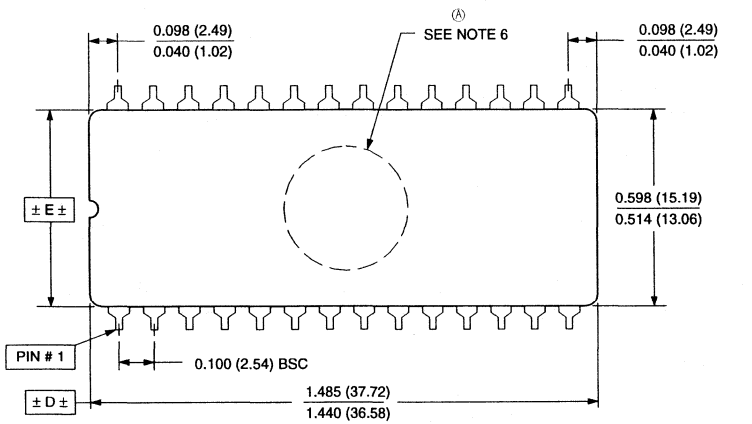


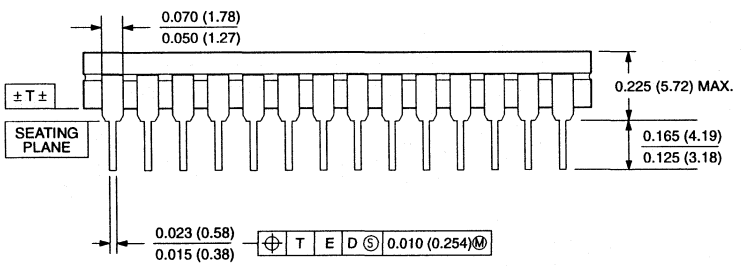
NOTES:

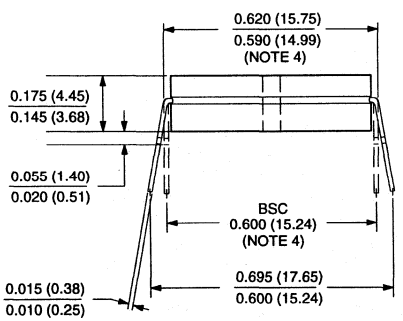
1. Controlling dimension: Inches. Millimeters are shown in parentheses.
2. Dimension and tolerancing per ANSI Y14. 5M-1982.
3. ™TÍ, ™DÍ, and ™EÍ are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #24 when viewed from the top.

Ⓐ 6. Denotes window location for EPROM products.

CDIP28: ceramic dual in-line (F) package (with window (FA) package); 28 leads (600 mil) **0589B**





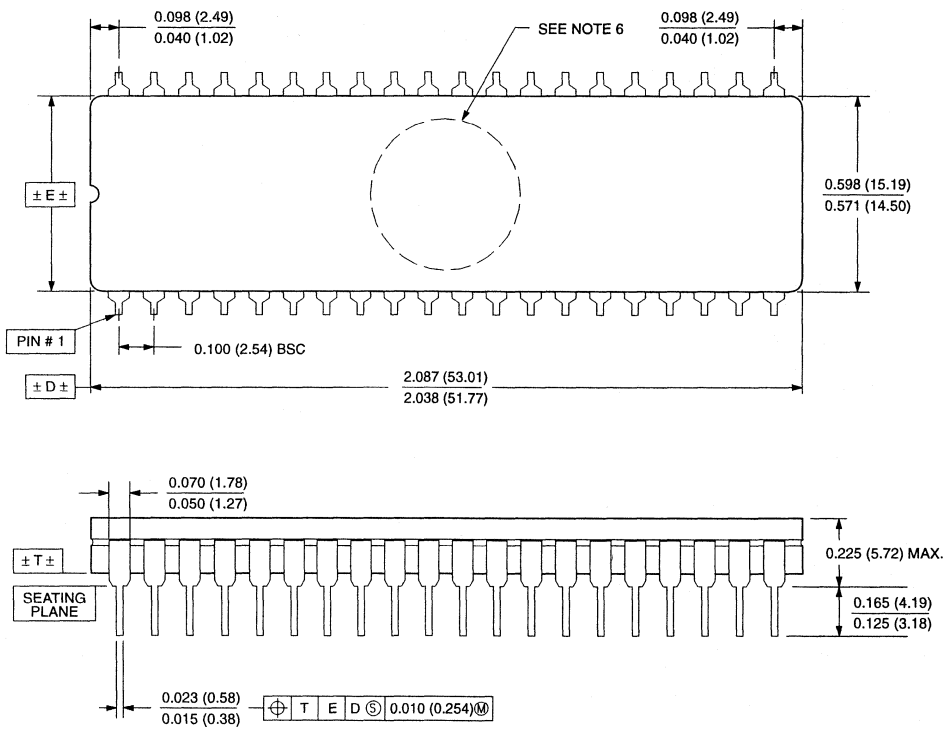


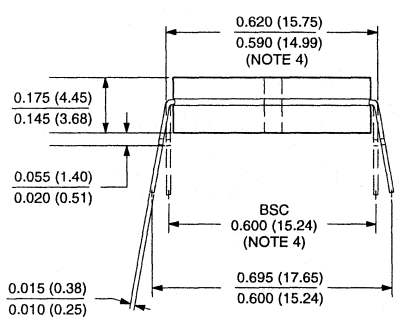
NOTES:

1. Controlling dimension: Inches. Millimeters are shown in parentheses.
2. Dimension and tolerancing per ANSI Y14. 5M-1982.
3. ™T∫, ™D∫, and ™E∫ are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #28 when viewed from the top.

Ⓐ 6. Denotes window location for EPROM products.

CDIP40: ceramic dual in-line (F) package (with window (FA) package); 40 leads (600 mil) **0590B**



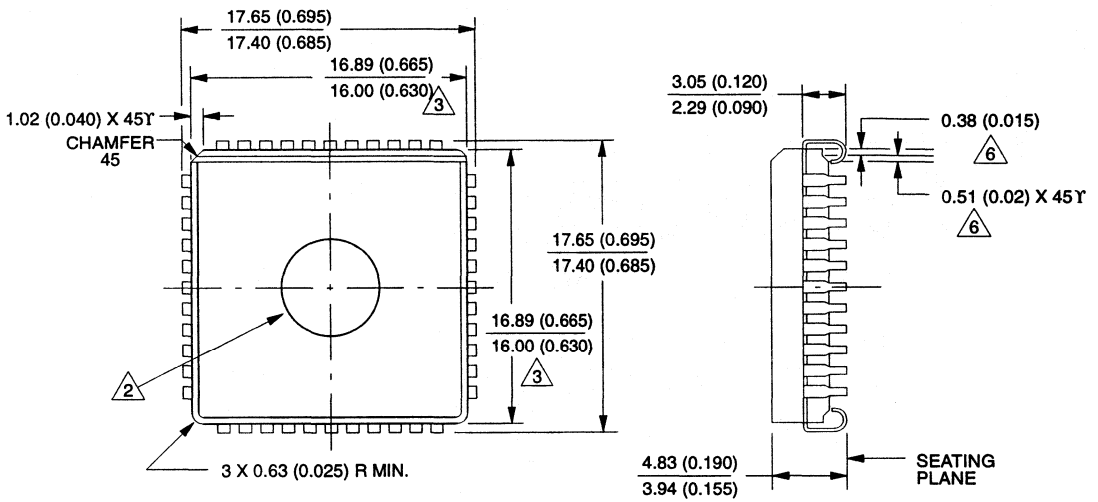


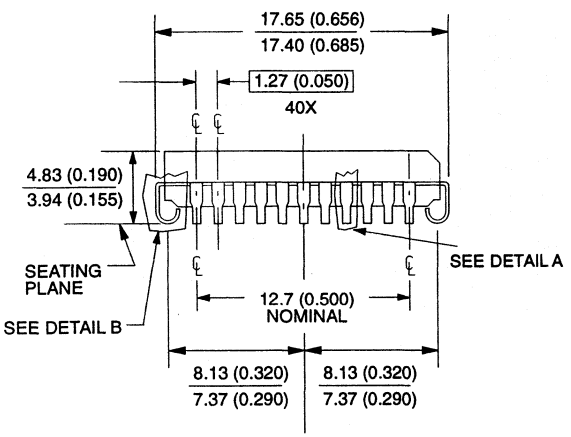
NOTES:

1. Controlling dimension: Inches. Millimeters are shown in parentheses.
2. Dimension and tolerancing per ANSI Y14. 5M-1982.
3. ™TĴ, ™DĴ, and ™EĴ are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #40 when viewed from the top.
6. Denotes window location for EPROM products.

CLCC

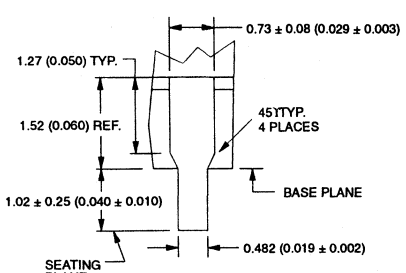
CLCC44: ceramic leaded chip carrier; 44 leads; j-bent 1472A



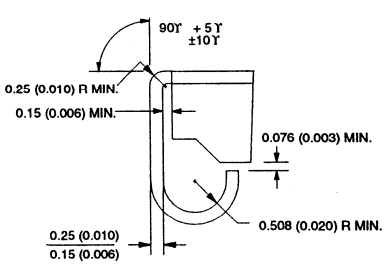


NOTES:

1. All dimensions and tolerances to conform to ANSI Y14.5±1982.
2. UV window is optional.
3. Dimensions do not include glass protrusion. Glass protrusion to be 0.005 inches maximum on each side.
4. Controlling dimension millimeters.
5. All dimensions and tolerances include lead trim offset and lead plating finish.
6. Backside solder relief is optional and dimensions are for reference only.

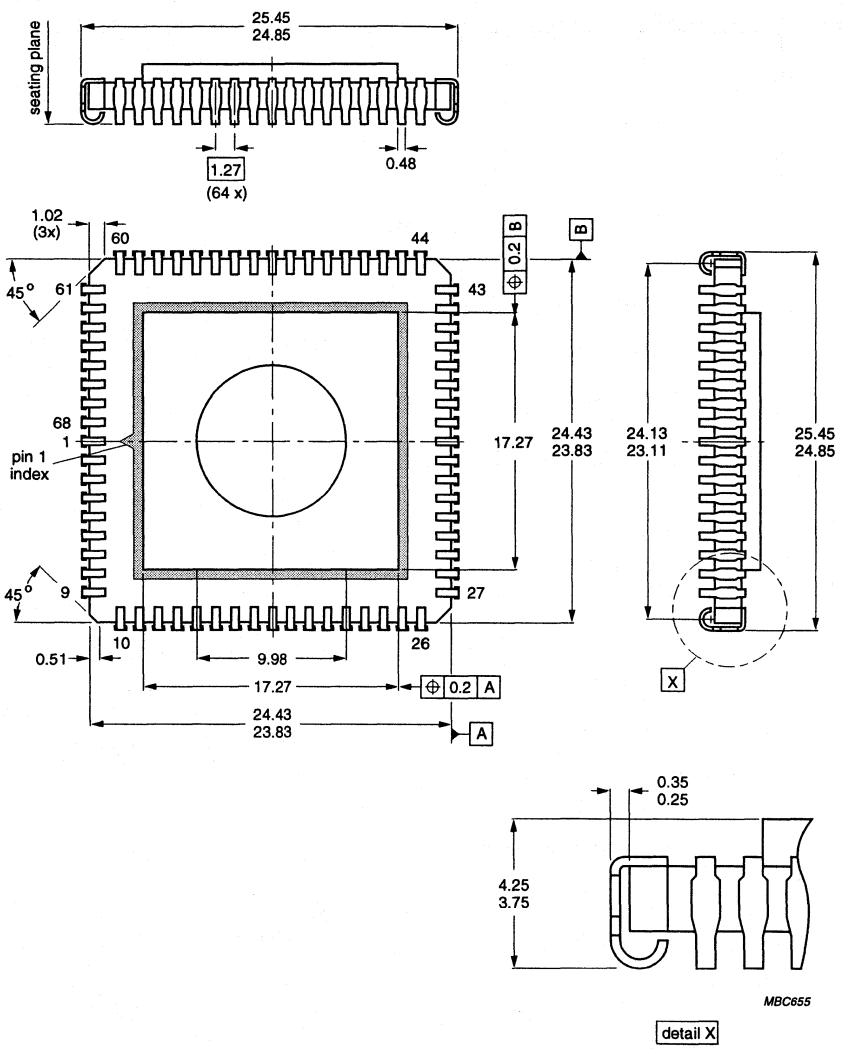


DETAIL A
TYP. ALL SIDES
mm/(inch)



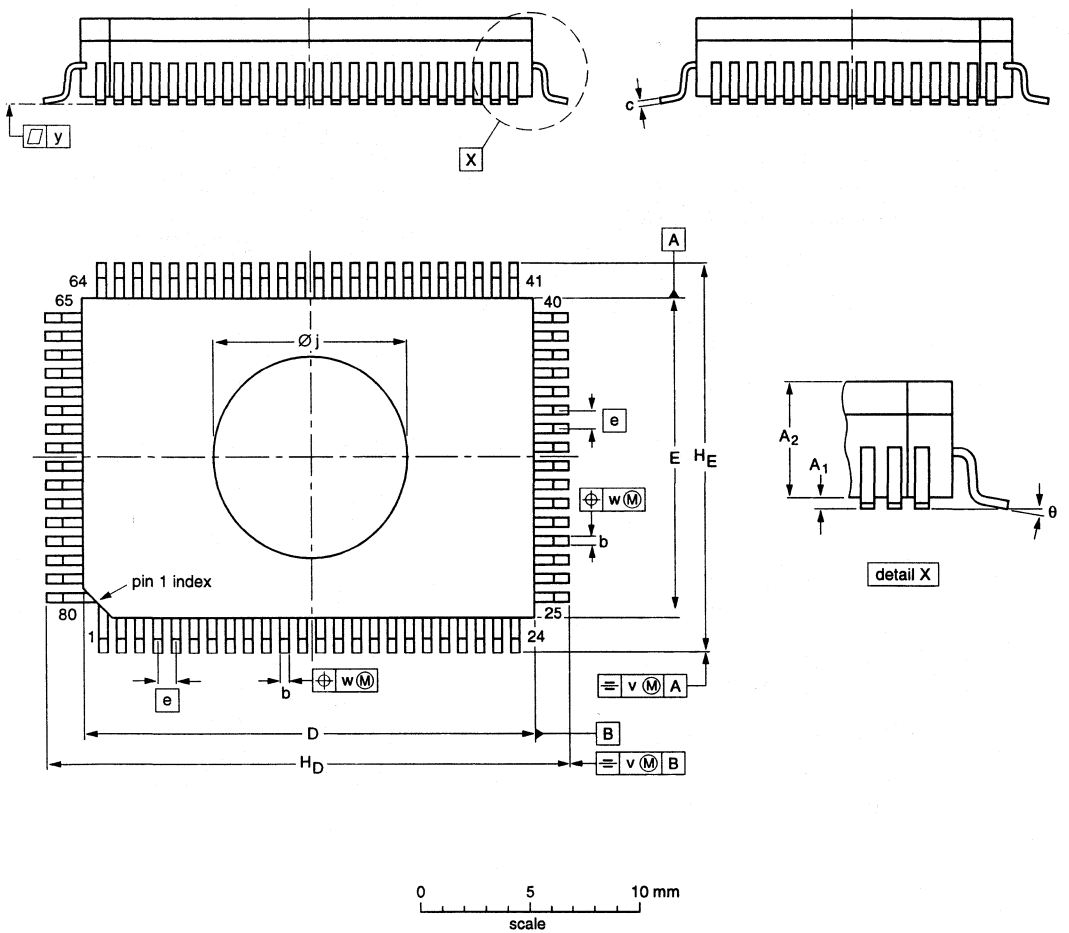
DETAIL B
mm/(inch)

CLCC68: ceramic leaded chip carrier (window); 68 leads **NO330**



CQFP

CQFP80: ceramic quad flat package; 80 leads SOT351-1



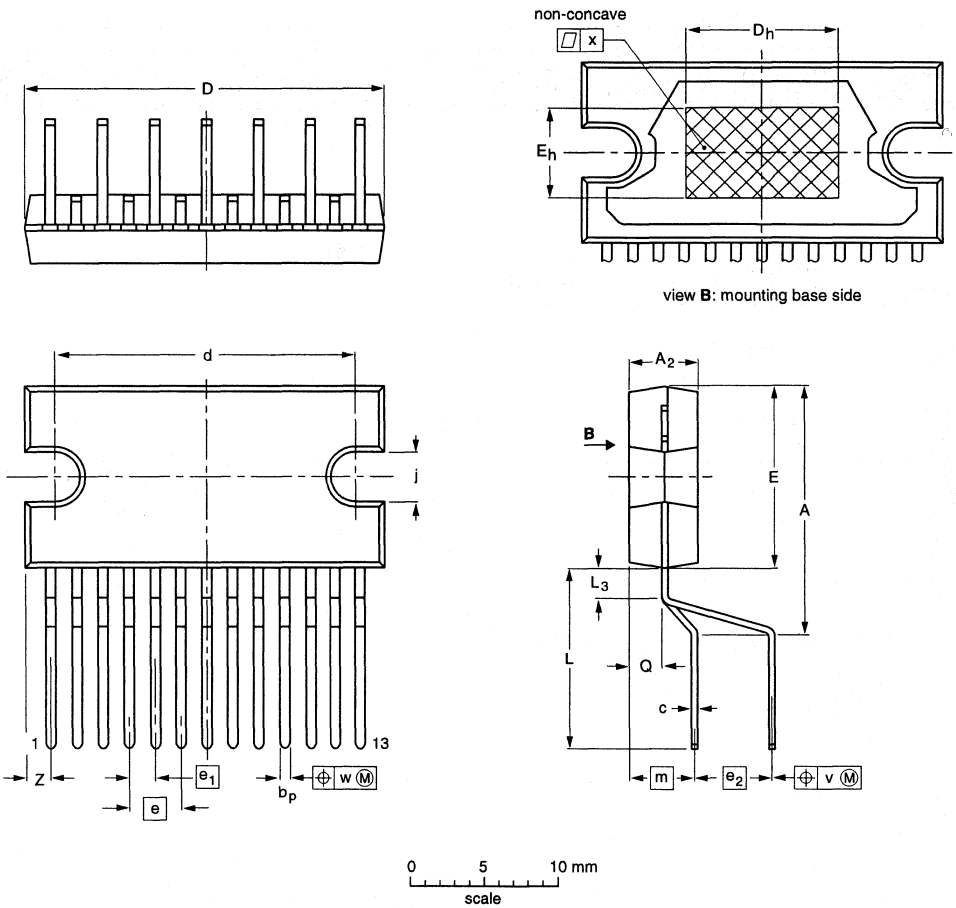
DIMENSIONS (mm are the original dimensions)

UNIT	A_1	A_2	b	c	D	E	e	H_D	H_E	Øj	v	w	y	θ
mm	0.5 0.2	3.9 3.1	0.45 0.30	0.25 0.14	20.2 19.8	14.2 13.9	0.8	24.2 23.6	18.2 17.6	9.00 8.75	0.2	0.2	0.15	7° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT351-1						93-11-02

DBS

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm) SOT141-6



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

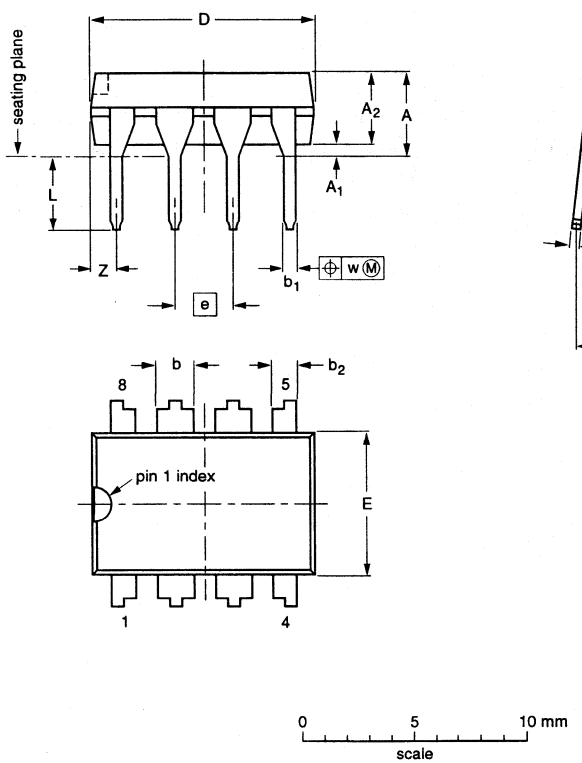
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT141-6						~~92-11-17~~ 95-03-11

DIP

DIP8: plastic dual in-line package; 8 leads (300 mil) SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

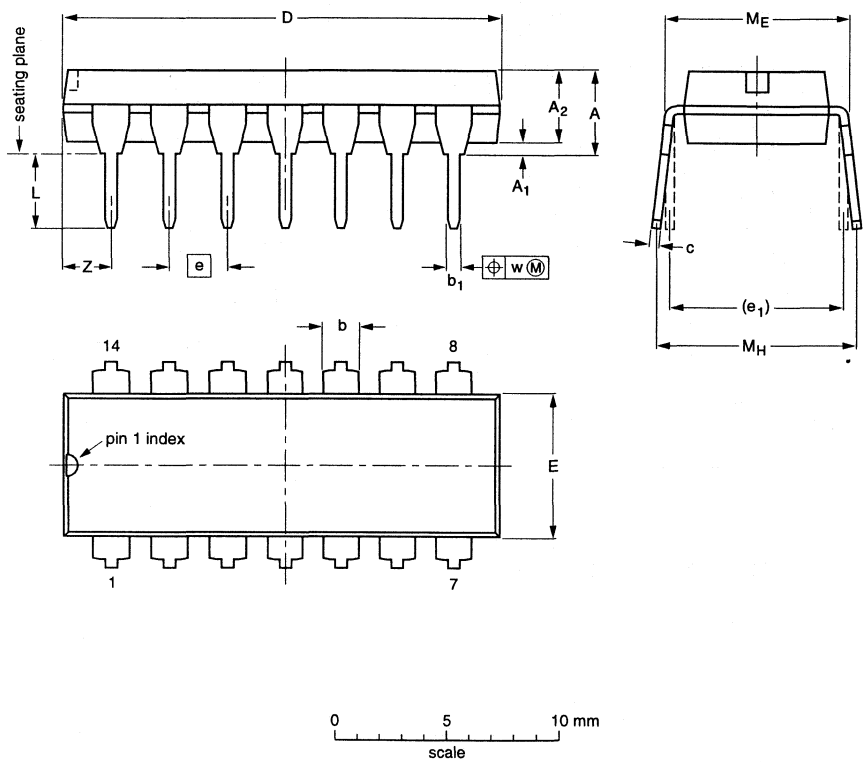
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

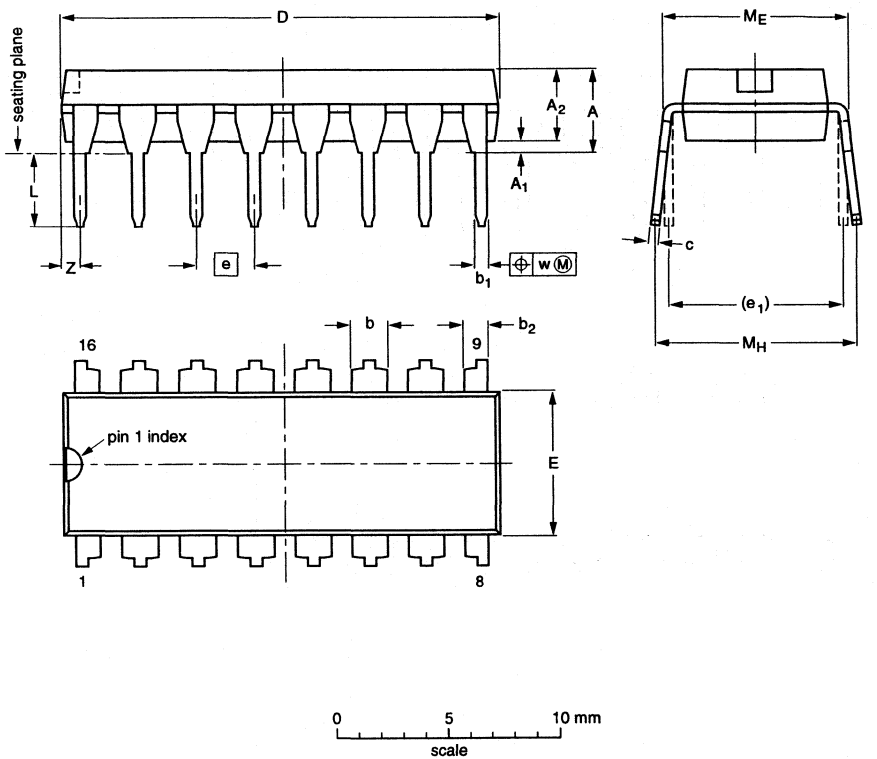
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

DIP16: plastic dual in-line package; 16 leads (300 mil) SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

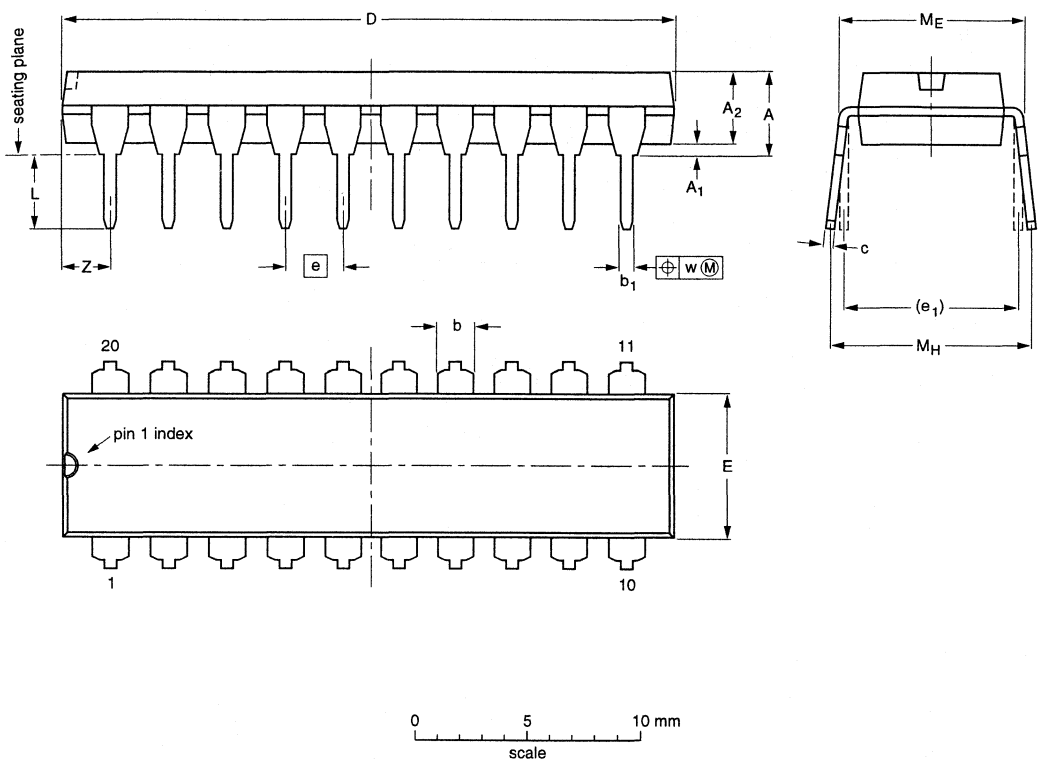
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

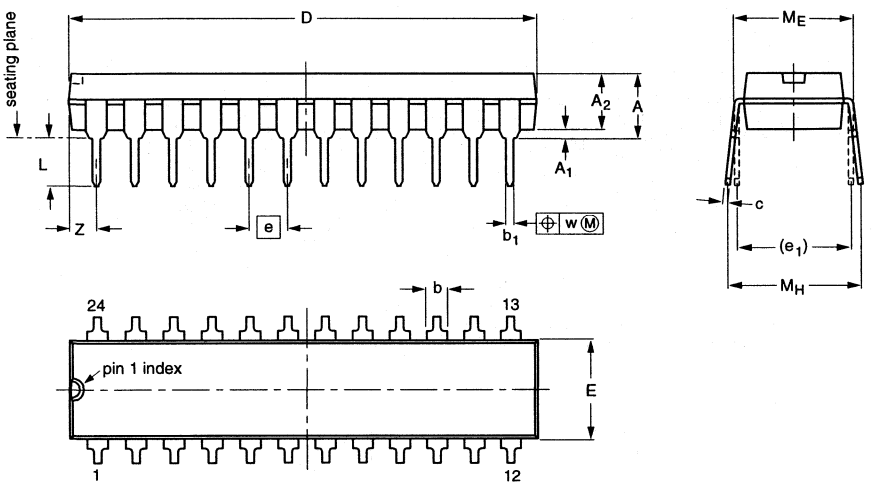
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

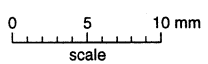
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

DIP24: plastic dual in-line package; 24 leads (300 mil) **SOT222-1**





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

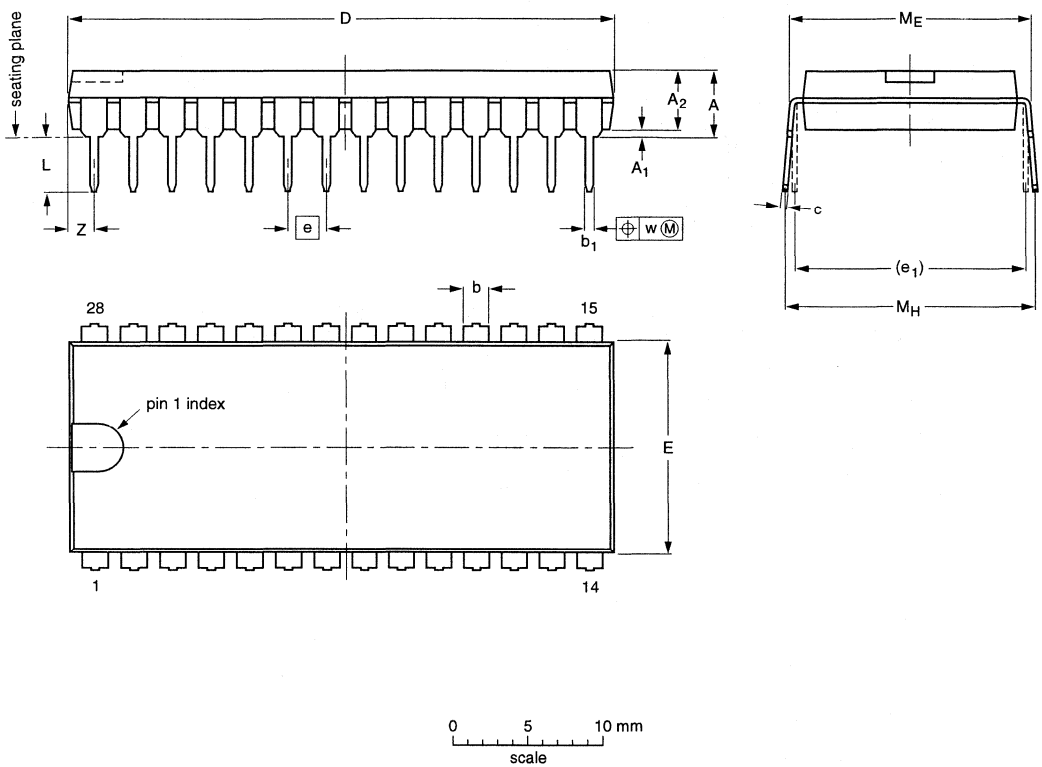
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

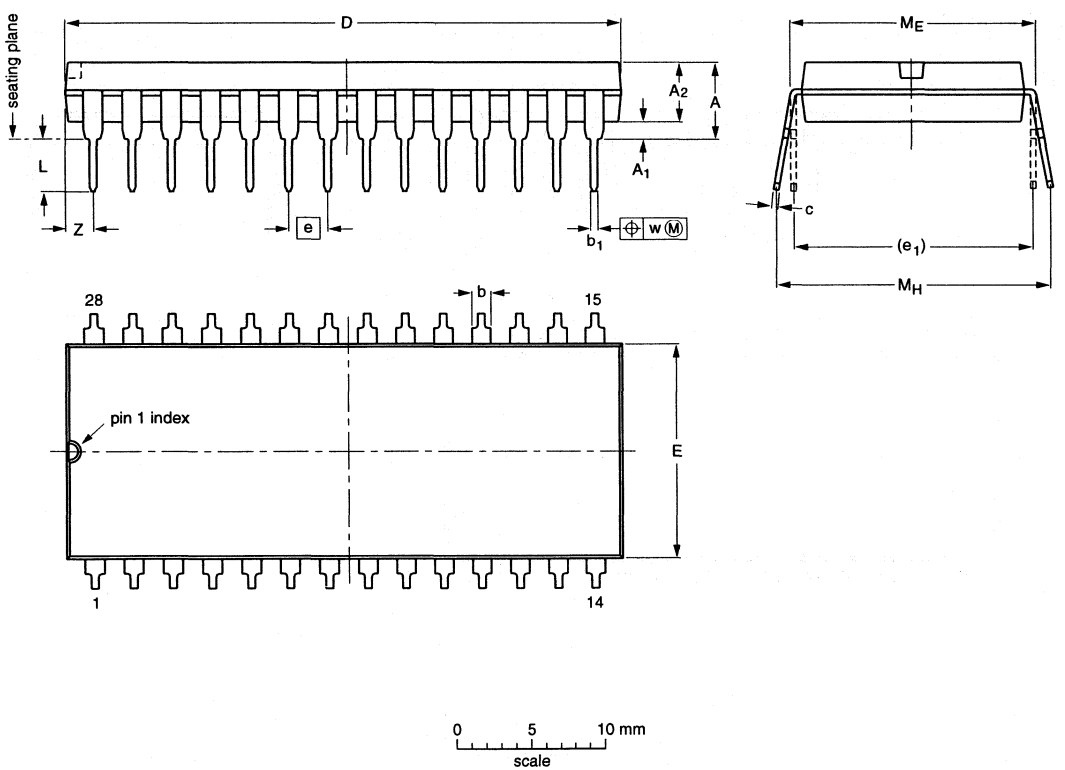
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

DIP28: plastic dual in-line package; 28 leads (600 mil); long body **SOT117-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

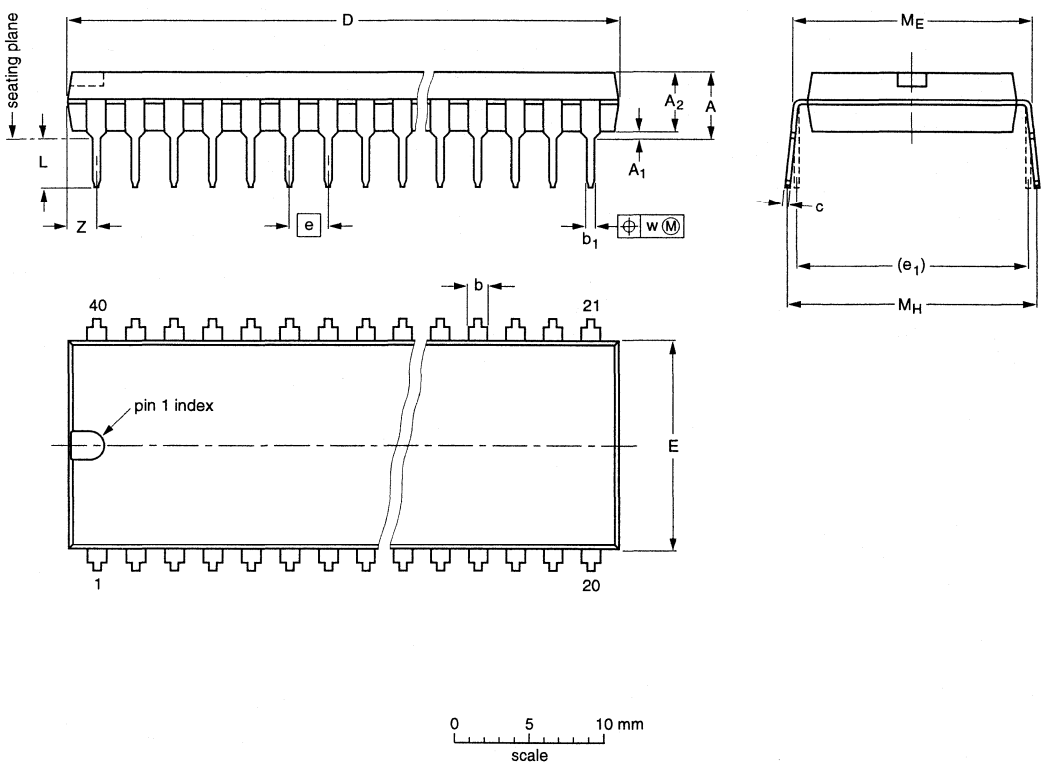
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	5.08	0.51	3.94	1.63 1.14	0.56 0.43	0.38 0.25	37.08 35.94	14.22 13.84	2.54	15.24	3.51 3.05	15.75 15.24	17.65 15.24	0.25	2.10
inches	0.200	0.020	0.155	0.064 0.045	0.022 0.017	0.015 0.010	1.460 1.415	0.560 0.545	0.100	0.600	0.138 0.120	0.62 0.60	0.695 0.600	0.01	0.083

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-2		MS-011AB				95-03-11

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D(1)	E(1)	e	e_1	L	M_E	M_H	w	Z(1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

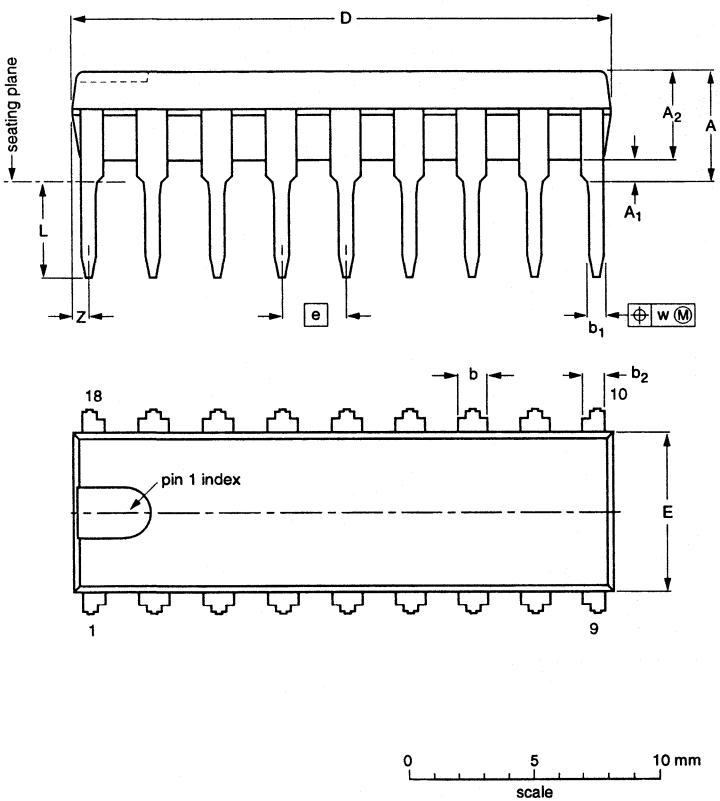
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

HDIP

HDIP18: plastic heat-dissipating dual in-line package; 18 leads SOT398-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.7	0.51	3.7	1.40 1.14	0.67 0.50	1.05 0.75	0.47 0.38	21.85 21.35	6.5 6.2	2.54	7.62	3.9 3.1	8.32 8.02	8.7 7.7	0.25	1.0
inches	0.19	0.02	0.15	0.06 0.04	0.03 0.02	0.04 0.03	0.02 0.01	0.87 0.84	0.26 0.24	0.10	0.30	0.15 0.12	0.33 0.32	0.34 0.30	0.01	0.04

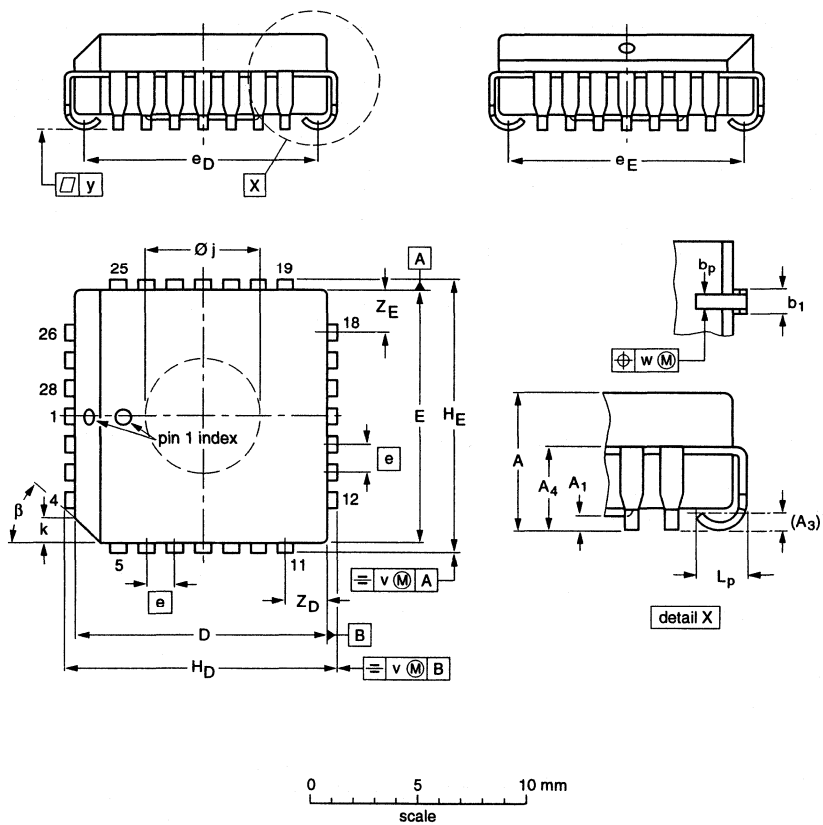
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT398-1						~~94-04-13~~ 95-01-25

PLCC

PLCC28: plastic leaded chip carrier; 28 leads; pedestal SOT261-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	Øj	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	5.69 5.54	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.224 0.218	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

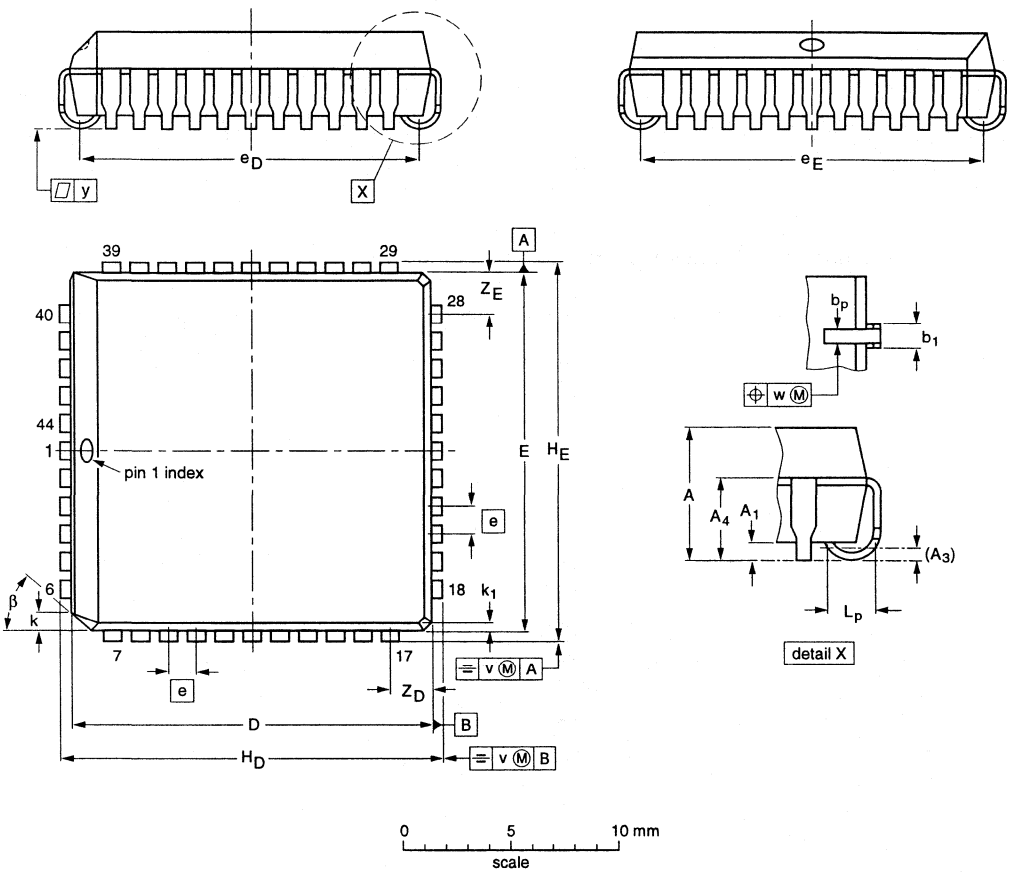
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT261-3		MO-047AB				~~92-11-17~~ 95-02-25

PLCC44: plastic leaded chip carrier; 44 leads

SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

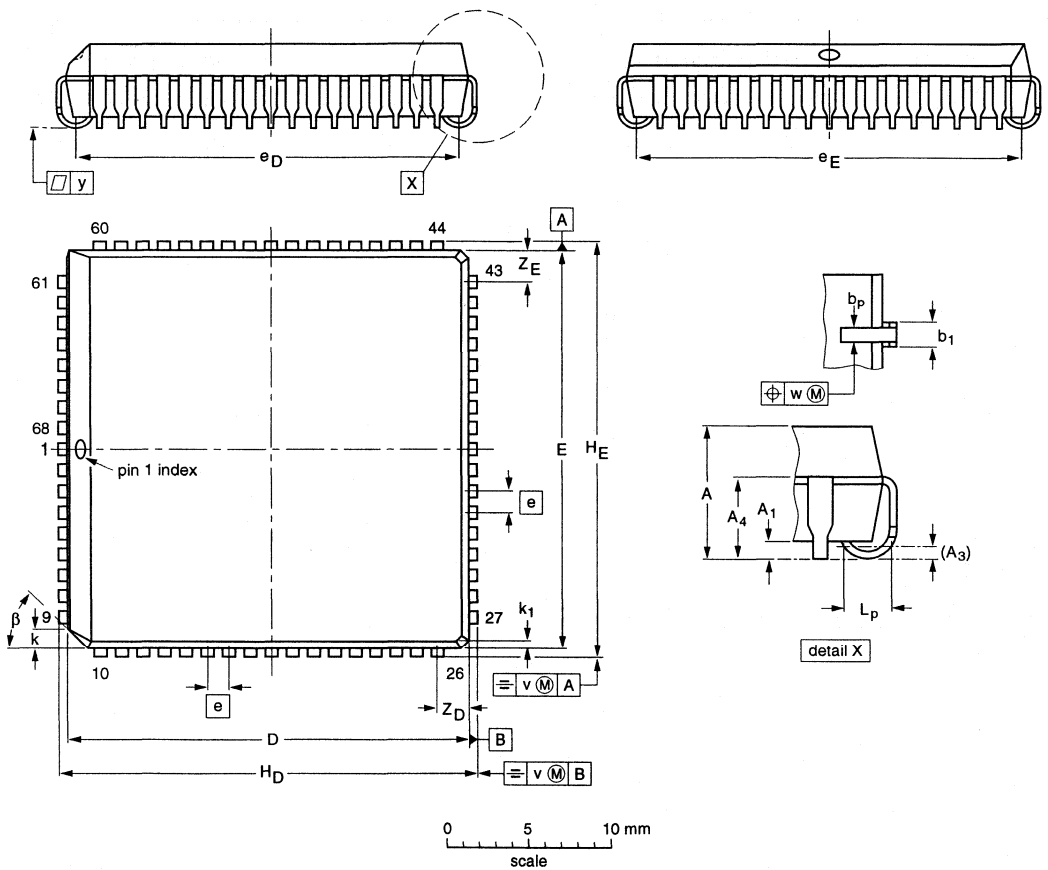
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				~~92-11-17~~ 95-02-25

PLCC68: plastic leaded chip carrier; 68 leads SOT188-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

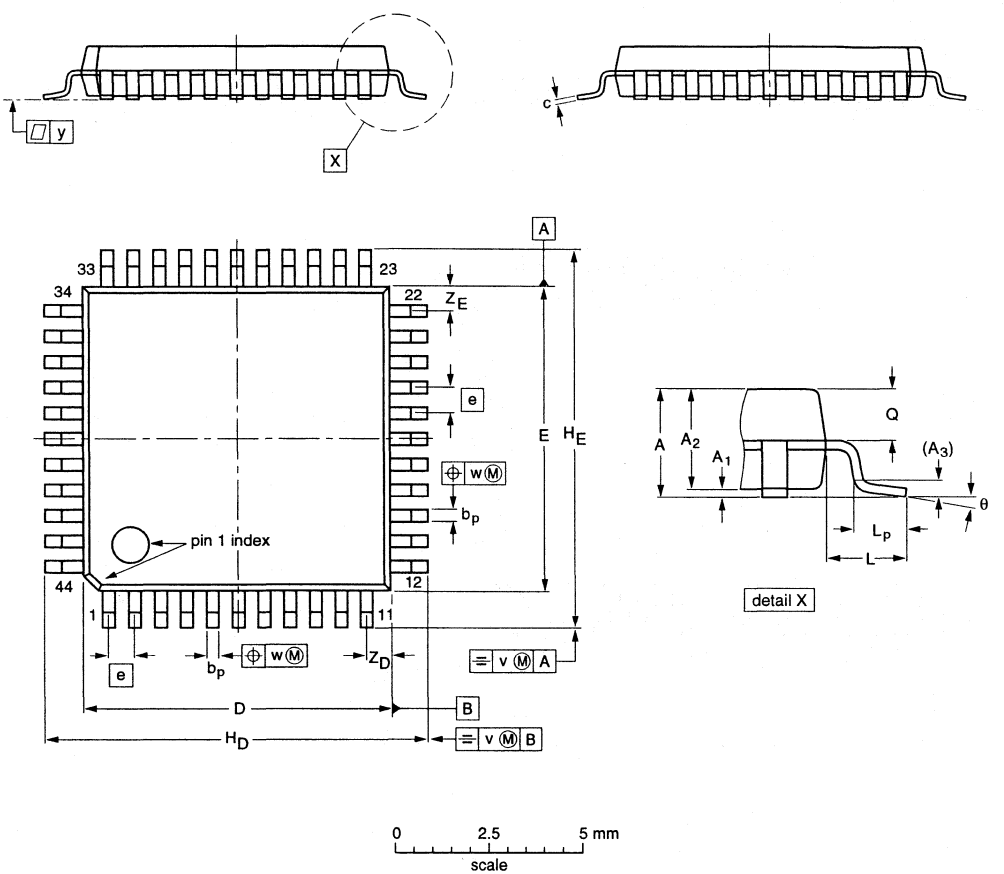
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT188-2	112E10	MO-047AC				~~92-11-17~~ 95-03-11

QFP

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm SOT307-2



DIMENSIONS (mm are the original dimensions)

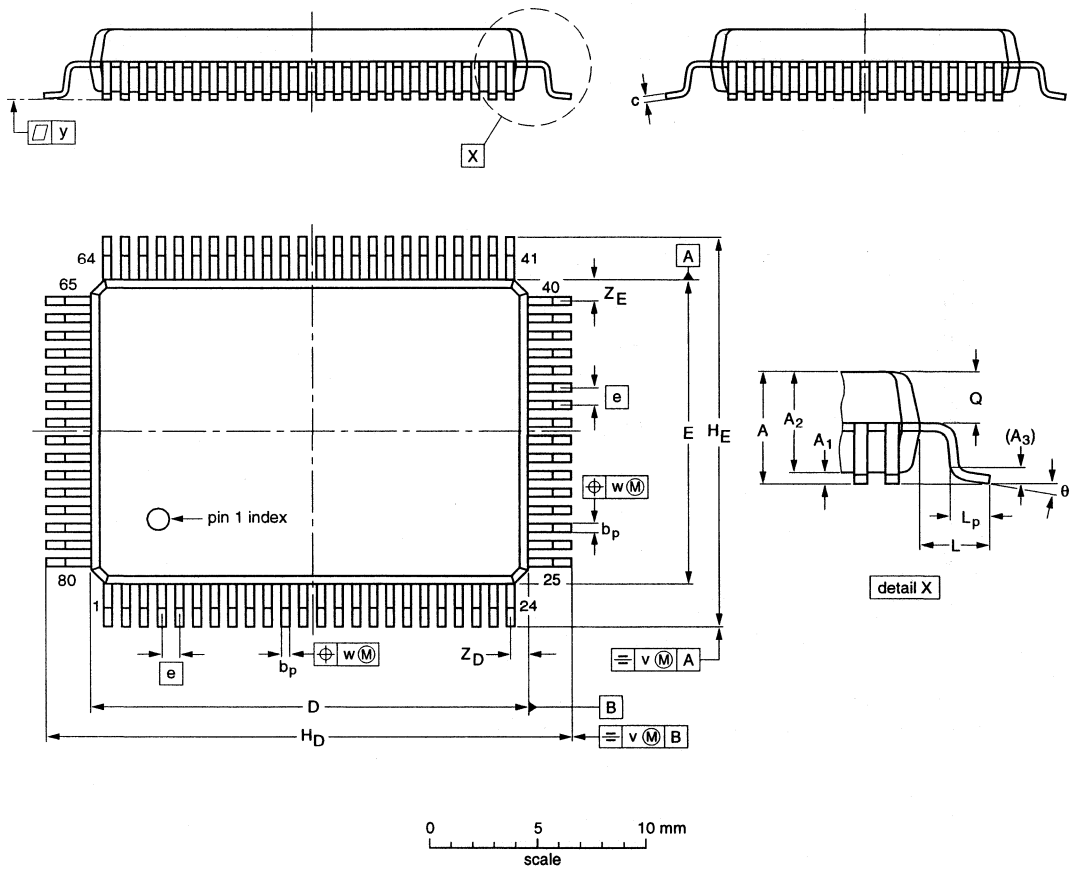
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~92-11-17~~ 95-02-04

QFP80: plastic quad flat package;
80 leads (lead length 1.95 mm); body 14 x 20 x 2.7 mm; high stand-off height **SOT318-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.3	0.36 0.10	2.87 2.57	0.25	0.45 0.30	0.25 0.13	20.1 19.9	14.1 13.9	0.8	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.43 1.23	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7° 0°

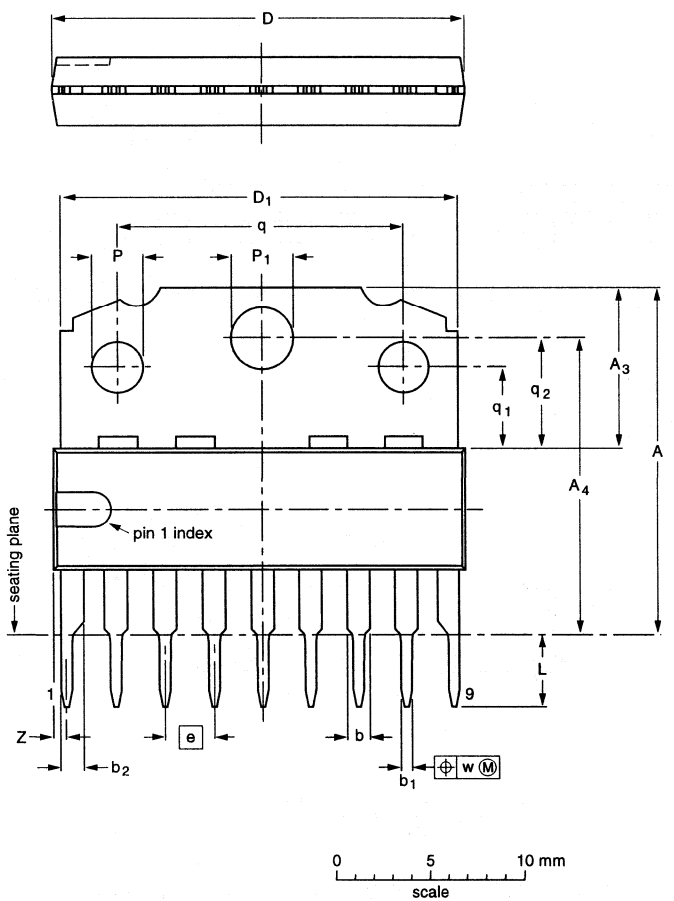
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-1						~~92-11-17~~ 95-02-04

SIL

SIL9MPF: plastic single in-line medium power package with fin; 9 leads SOT110-1



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2 max.	A_3	A_4	b	b_1	b_2	c	$D^{(1)}$	D_1	$E^{(1)}$	e	L	P	P_1	Q	q	q_1	q_2	w	$Z^{(1)}$ max.
mm	18.5 17.8	3.7	8.7 8.0	15.8 15.4	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	6.48 6.20	2.54	3.9 3.4	2.75 2.50	3.4 3.2	1.75 1.55	15.1 14.9	4.4 4.2	5.9 5.7	0.25	1.0

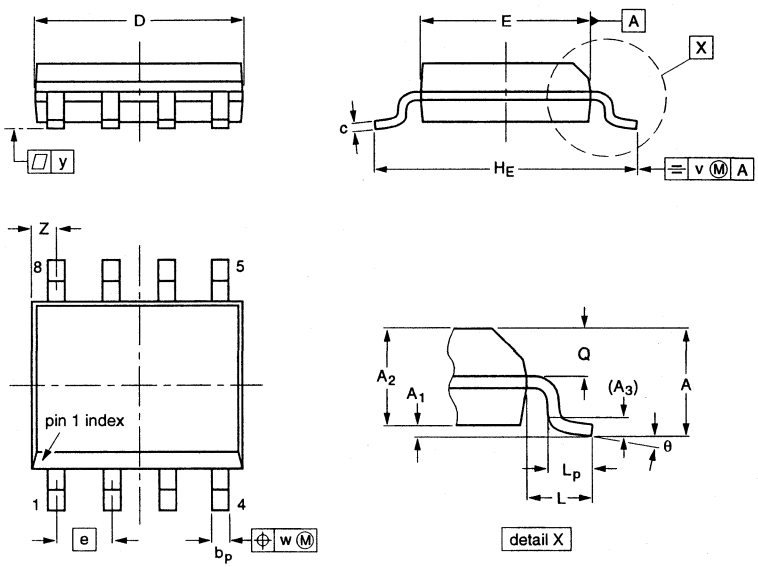
Note

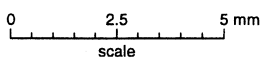
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT110-1						~~92-11-17~~ 95-02-25

SO

SO8: plastic small outline package; 8 leads; body width 3.9 mm SOT96-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

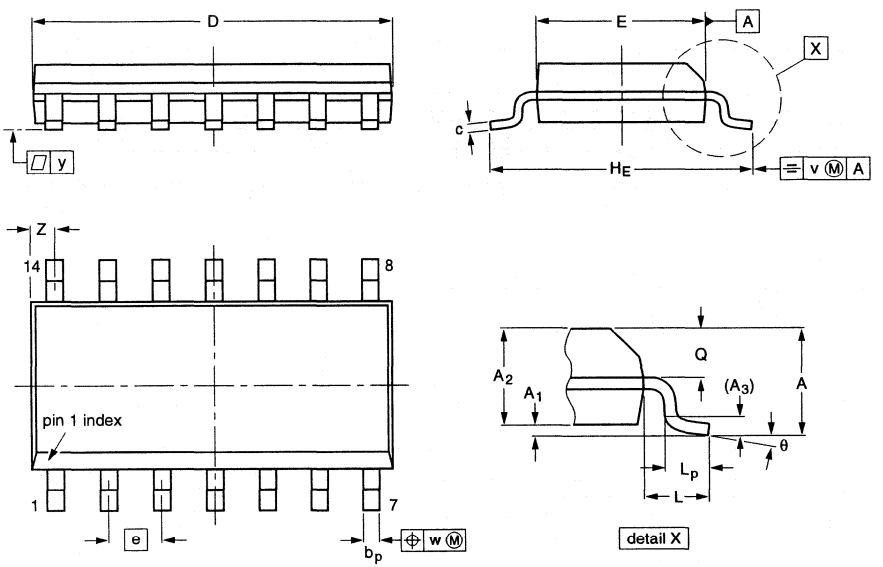
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.20 0.19	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

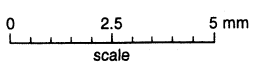
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~92-11-17~~ 95-02-04

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

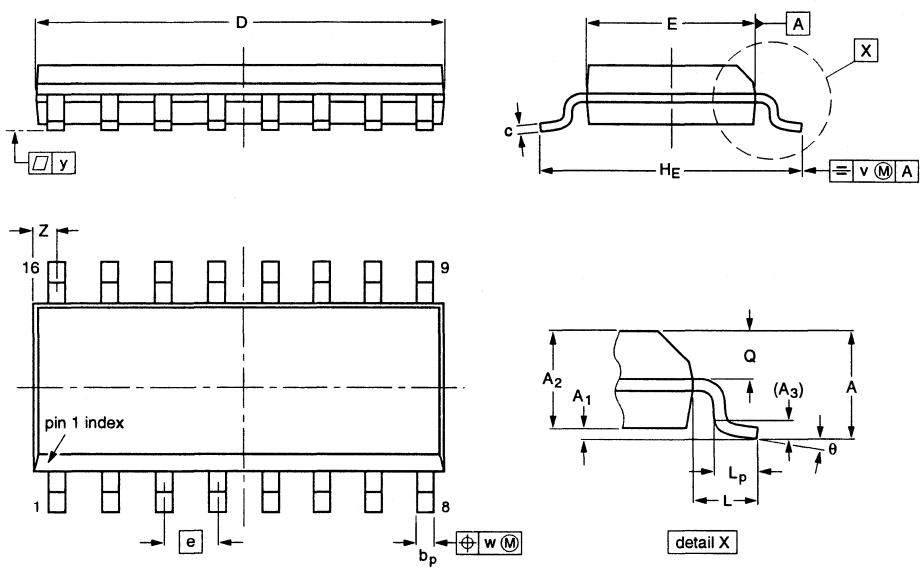
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~91-08-13~~ 95-01-23

SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

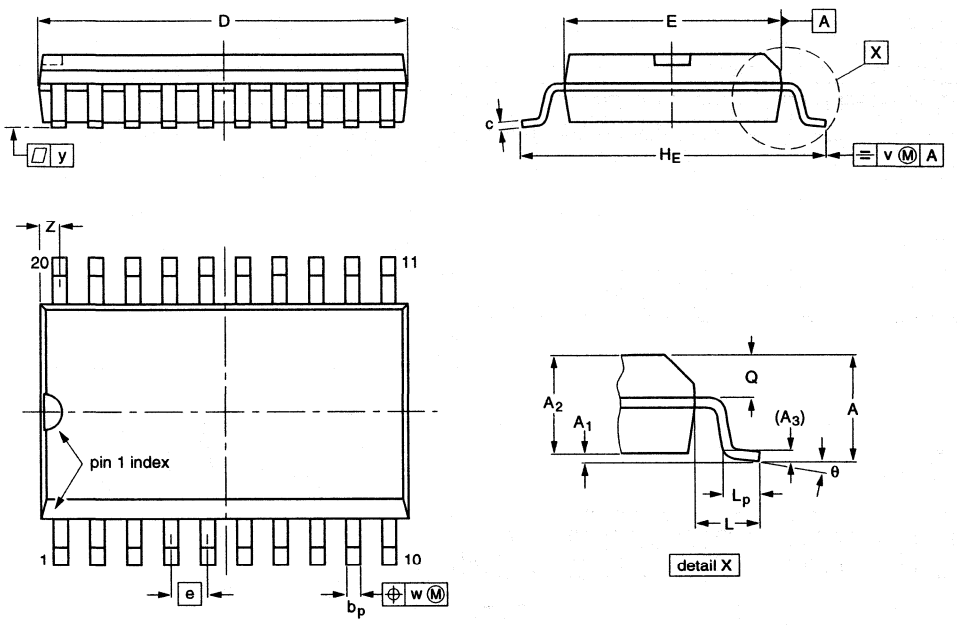
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

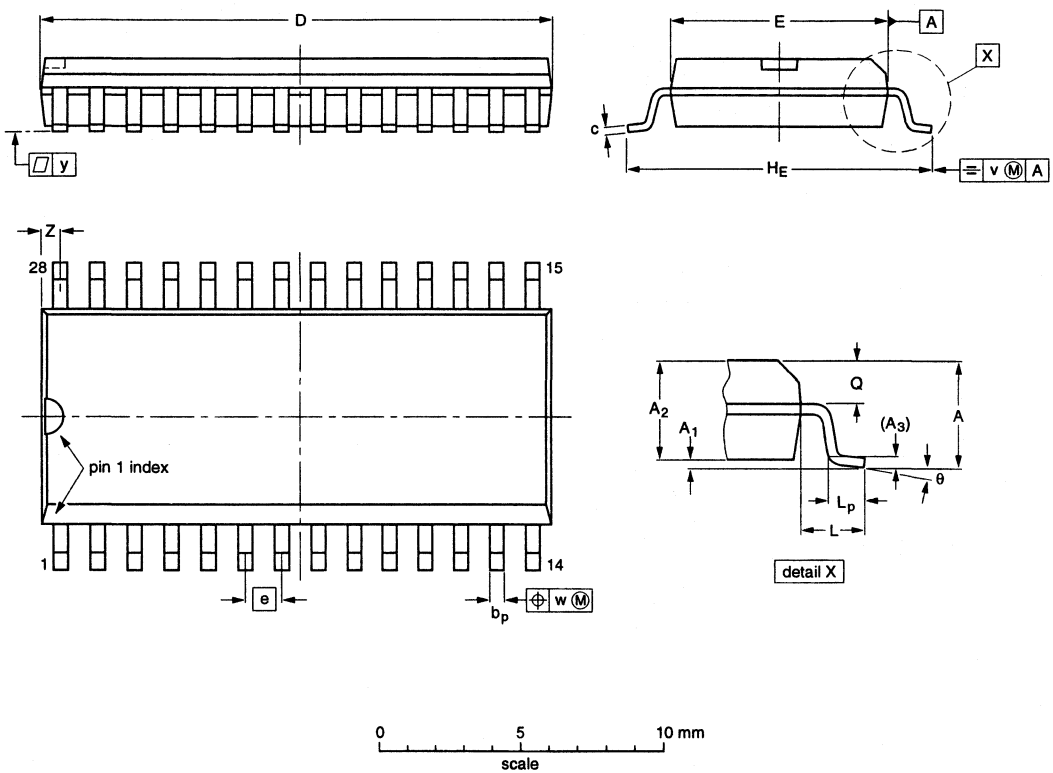
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

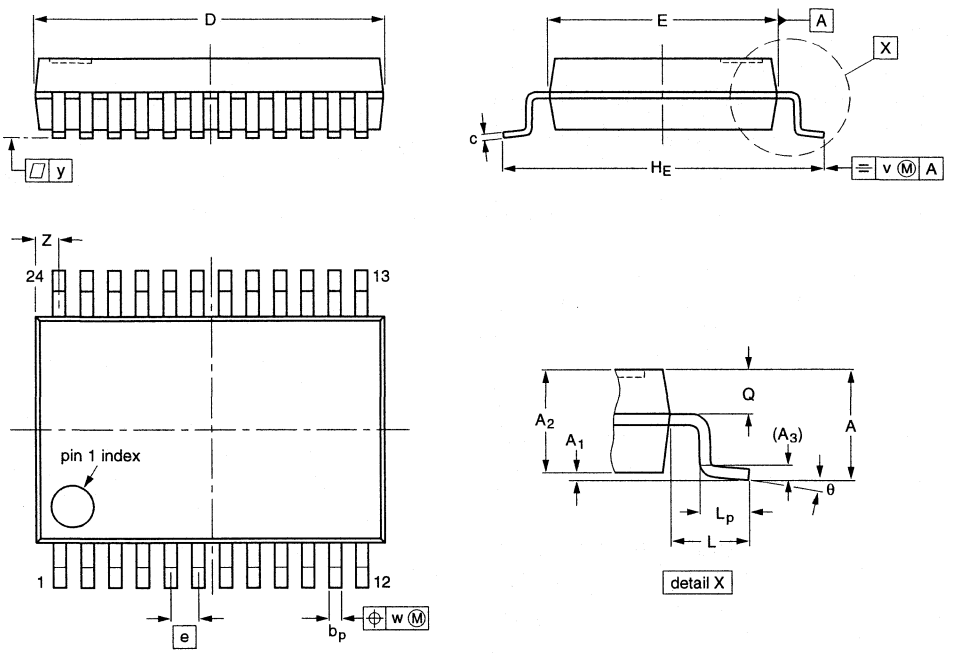
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24

SSOP

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm SOT340-1



DIMENSIONS (mm are the original dimensions)

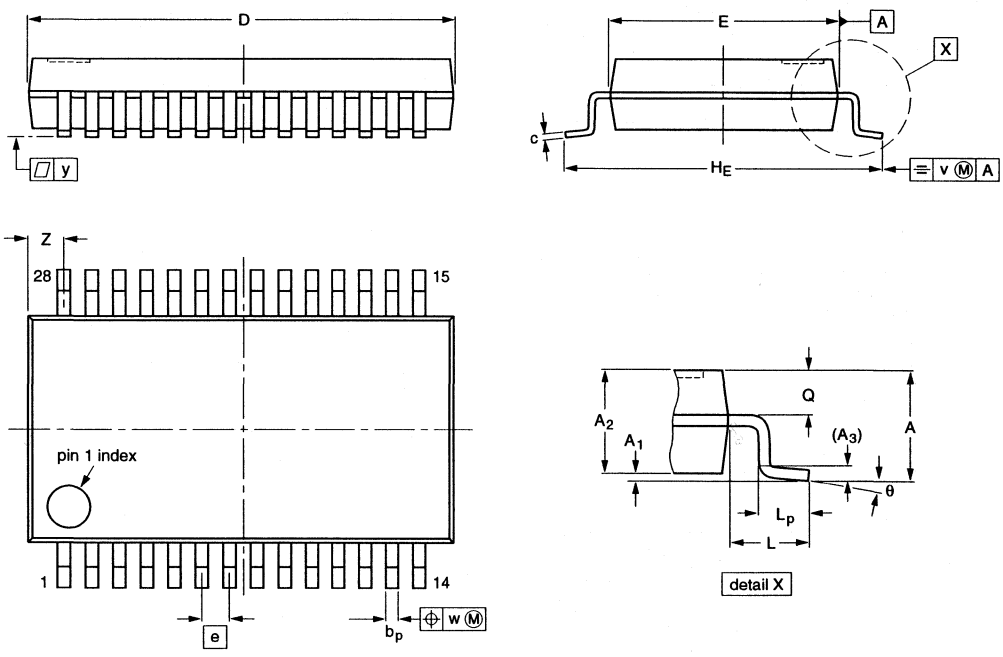
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

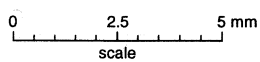
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

INTRODUCTION

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9397 750 0011).

THROUGH-HOLE MOUNTED PACKAGES

Table 1 Types of through-hole mounted packages

TYPE	DESCRIPTION
DIP	plastic dual in-line package
SDIP	plastic shrink dual in-line package
HDIP	plastic heat-dissipating dual in-line package
DBS	plastic dual in-line bent from a single in-line package
SIL	plastic single in-line package

Soldering by dipping or wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SURFACE MOUNTED PACKAGES

Table 2 Types of surface mounted packages

TYPE	DESCRIPTION
SO	plastic small outline package
SSOP	plastic shrink small outline package
TSSOP	plastic thin shrink small outline package
VSO	plastic very small outline package
QFP	plastic quad flat package
LQFP	plastic low profile quad flat package
SQFP	plastic shrink quad flat package
TQFP	plastic thin quad flat package
PLCC	plastic leaded chip carrier

Reflow soldering

Reflow soldering techniques are suitable for all SMD packages, ease of soldering varies with the type of package as indicated in Table 3.

The choice of heating method may be influenced by larger plastic packages (QFP or PLCC with 44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information on moisture prevention, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Table 3 Suitability of surface mounted packages for various soldering methods: rating from 'a' to 'd': **'a' indicates most suitable** (soldering is not difficult); **'d' indicates least suitable** (soldering is achievable with difficulty).

PACKAGE TYPE	REFLOW METHOD					DOUBLE WAVE METHOD
	INFRARED	HOT BELT	HOT GAS	VAPOUR PHASE	RESISTANCE	
SO	a	a	a	a	d	a
SSOP	a	a	a	c	d	c
TSSOP	b	b	b	c	d	d
VSO	b	b	a	b	a	b
QFP	b	b	a	c	a	c
LQFP	b	b	a	c	d	d
SQFP	b	b	a	c	d	d
TQFP	b	b	a	c	d	d
PLCC	c	b	b	d	d	b

Wave soldering

Wave soldering is **not** recommended for SSOP, TSSOP, QFP, LQFP, SQFP or TQFP packages, this is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- For SSOP, TSSOP and VSO packages, the longitudinal axis of the package footprint must be parallel to the solder flow **and** must incorporate solder thieves at the downstream end.
- For QFP, LQFP and TQFP packages, the footprint must be at an angle of 45° to the board direction **and** must incorporate solder thieves downstream and at the side corners.

Even with these conditions, consider wave soldering only for the following package types:

- SO
- VSO
- PLCC
- SSOP **only with body width 4.4 mm**, e.g. SSOP16 (SOT369-1) or SSOP20 (SOT266-1).
- QFP **except** QFP52 (SOT379-1), QFP100 (SOT317-1, SOT317-2, SOT382-1) and QFP160 (SOT322-1); these are **not** suitable for wave soldering.
- LQFP **except** LQFP32 (SOT401-1), LQFP48 (SOT313-1, SOT313-2), LQFP64 (SOT314-2), LQFP80 (SOT315-1); these are **not** suitable for wave soldering.
- TQFP **except** TQFP64 (SOT357-1), TQFP80 (SOT375-1) and TQFP100 (SOT386-1); these are **not** suitable for wave soldering.

SQFP are **not** suitable for wave soldering.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEVELOPMENT SUPPORT TOOLS

DEVELOPMENT SUPPORT TOOLS

DOCUMENT	DESCRIPTION	DOCUMENT ORDER NUMBER
Can Bus related material		
OM4130	CAN evaluation board with the 8XC552 and the 82C200 CAN controller	9398 706 68011
OM4239	CAN evaluation board with the 8XC592 microcontroller	9398 706 69011
OM4240	Evaluation board for the 8XCE598 microcontroller	9398 706 70011
OM4272	SLIO evaluation board with the 82C150 and the 82C250 CAN ICs	9398 706 71011
Identification related material		
OM4282	Demonstration kit for the PCF7930	9398 706 50011
CAR Stereo related material		
CCR52X	"see also: (Handbooks) IC01, IC12 and IC20, (Appnotes) ERA/AN930009 and ERA/AN93010"	
CCR6XX	"see also: (Handbooks) IC01, IC12 and IC20, (Appnotes) AN95070 and AN95081"	

Development support tools

DEVELOPMENT SUPPORT TOOLS

Philips Semiconductors manufactures support tools and also works closely with many "third-party" vendors who provide support tools for our wide variety of 80C51-based microcontroller derivatives.

Development Systems

In most cases, development systems are available in two versions for ROM and ROMless applications. The ROM emulation products are capable of supporting all versions of a given device type, including EPROM, ROM, and ROMless devices. In contrast, a ROMless emulator can only support applications designed for a ROMless microcontroller. Most development systems are designed to connect to an IBM-PC or compatible personal computer.

EPROM Programming Support

Philips Semiconductors works closely with major suppliers of EPROM programming equipment to support our family of EPROM microcontrollers. As a result, EPROM programming support is available within the programming facilities of many major distributors.

The following is a list of vendors that offer support for Philips Semiconductors 80C51 microcontroller family.

DEVELOPMENT SYSTEM CONTACTS

COMPANY	ADDRESS	TELEPHONE
Ashling Microsystems Limited	Plassey Technological Park Limerick, Ireland Eastern Systems Inc. 160 East Main Street Westboro, MA 01581	(353) 61 334 466 (508) 366-3220
BSO Tasking	Norfolk Place 333 Elm Street Dedham, MA 02026-4530	(800) 458-8276
Ceibo Ltd.	105 Gleason Rd. Lexington, MA 02173 Merkazim Building, Industrial Zone P.O. Box 2106 Herzelia 46120, ISRAEL	(617) 863-9927 972-52-555387
Lauterbach Datentechnik GmbH	Fichtenstrasse 27 85649 Hofolding Germany 945 Concord Street Framingham, MA 01701	49 8104 894 328 (508) 620-4521
MetaLink Corp.	325 E. Elliot Road, Suite 23 Chandler, AZ 85225	(602) 926–0797
Nohau Corp.	51 E. Campbell Ave. Campbell, CA 95008-2053	(408) 866–1820
Philips Semiconductors	Corporate Centre Building BAE-2 P.O. Box 218 5600 MD Eindhoven The Netherlands	31-40-724223
SIGNUM Systems	171 E. Thousand Oaks Blvd., #202 Thousand Oaks, CA 91360	(805) 371-4608

EPROM PROGRAMMING SUPPORT CONTACTS

Advin Systems 1050-L East Duane Ave. Sunnyvale, CA 94086 (408) 736-2503	Logical Devices, Inc. 1201 Northwest 65th Place Ft. Lauderdale, FL 33309 (305) 974-0967	North Valley Products P.O. Box 32899 San Jose, CA 95152 (408) 929-5345
BP Microsystems 10681 Haddington #190 Houston, TX 77043 (800) 225-2102, (713) 461-9430	Logical Systems P. O. Box 6184 Syracuse, NY 13217-6184 (315) 478-0722	Strebor Data Communications 1008 N. Nob Hill American Fork, UT 84003 (801) 756-3605
Data I/O Corp. 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (206) 881-6444	Needham's Electronics 4535 Orange Grove Ave. Sacramento, CA 95841 (916) 924-8037	

Development support tools

SOFTWARE SUPPORT CONTACTS

COMPANY	ADDRESS	TELEPHONE
Archimedes Software, Inc.	2159 Union St. San Francisco, CA 94123	(415) 567–4010
BSO/Tasking	Tasking Software BV P.O. Box 899 3800 AW Amersfoort The Netherlands Norfolk Place 333 Elm Street Dedham, MA 02026-4530	31-33-55-85-84 (Telephone) 31-33-55-00-33 (Fax) (617) 320-9400 (Telephone) (617) 320-9212 (Fax) (800) 458-8276 (Toll Free)
Franklin Software, Inc.	888 Saratoga Ave. #2 San Jose, CA 95129	(408) 296–8051
Keil Software	Bretonischer Ring 15 85630 Grasbrunn Germany	49-89-46-50-57 (Telephone) 49-89-46-81-62 (Fax)

MICROCONTROLLER DEVELOPMENT SYSTEMS

PRODUCT	DEVICES SUPPORTED
NOHAU CORPORATION	
EMUL51-PC/E32	12MHz Emulator, 32k emulation memory
EMUL51-PC/E128	12MHz Emulator, 128k emulation memory
EMUL51-PC/E32-16	16MHz Emulator, 32k emulation memory
EMUL51-PC/E128-16	16MHz Emulator, 128k emulation memory
EMUL51-PC/E128-20	20MHz Emulator, 128k emulation memory
EMUL51-PC/E128-24	24MHz Emulator, 128k emulation memory
EMUL51-PC/E128-30	30MHz Emulator, 128k emulation memory
EMUL51-PC/E128-33	33MHz Emulator, 128k emulation memory
EMUL51-PC/E128-BSW	12MHz Emulator, 128k bankswitched CODE memory
EMUL51-PC/E128-BSW-16	16MHz Emulator, 128k bankswitched CODE memory
EMUL51-PC/E128-BSW-24	24MHz Emulator, 128k bankswitched CODE memory
EMUL51-PC/E256-BSW	12MHz Emulator, 256k bankswitched CODE memory
EMUL51-PC/E256-BSW-16	16MHz Emulator, 256k bankswitched CODE memory
EMUL51-PC/E256-BSW-24	24MHz Emulator, 256k bankswitched CODE memory
POD–C054	12MHz 83C053, 83C054, 87C054, 87C055 pod
POD–31	12MHz 8031 pod
POD–C31	12MHz 80C31 pod
POD–C31–1	16MHz 80C31 pod
POD–C31–20	20MHz 80C31 pod
POD–C31–24	24MHz 80C31 pod
POD–C31–30	30MHz 80C31 pod
POD–C31–33	33MHz 80C31 pod
POD–32	12MHz 8032 pod
POD–C32	12MHz 80C32 pod
POD–C32–16	16MHz 80C32 pod
POD–C652	12MHz 80C652 pod
POD–C652–16	16MHz 80C652 pod
POD–C51B	12MHz bondout pod for 8051, 80C51, 83C552, 83C652, 83C654, 83C851, and EPROM or ROMless versions of the above
POD–C51B–16	16MHz bondout pod for 8051, 80C51, 83C552, 83C652, 83C654, 83C851, and EPROM or ROMless versions of the above
POD–C51B–24	24MHz version of the above
POD–C52	12MHz 80C32, 80C52, 87C52
POD–C52–16	16MHz 80C32, 80C52, 87C52
POD-CL410	12MHz 80CL31, 80CL51, 83CL410, 83CL610
POD–C451–DIP	12MHz 80C451 DIP pod
POD–C451–DIP–16	16MHz 80C451 DIP pod
POD–C451–PGA	12MHz 80C451 PLCC pod (PGA from pod)
POD–C451–PGA–16	16MHz 80C451 PLCC pod (PGA from pod)
POD–C451B–PGA	12MHz bondout pod for 83C451, 87C451, 80C451 PLCC (PGA from pod)
POD-C451B-PGA-16	16MHz bondout pod for 83C451, 87C451, 80C451 PLCC (PGA from pod)

MICROCONTROLLER DEVELOPMENT SYSTEMS (Continued)

PRODUCT	DEVICES SUPPORTED
NOHAU CORPORATION (Continued)	
POD–C528	12MHz 83C524, 87C524, 83C528, 87C528
POD–C528–16	16MHz 83C524, 87C524, 83C528, 87C528
POD–C550–PGA	12MHz 80C550, 83C550, 87C550
POD-C550-PGA-16	16MHz 80C550, 83C550,87C550
POD–C552–PGA	12MHz 80C552 PLCC (PGA from pod)
POD–C552B–PGA	12MHz bondout pod for 83C552, 87C552, 80C552 PLCC (PGA from pod), 80C562, 83C562
POD–C552B–PGA–16	16MHz bondout pod for 83C552, 87C552, 80C552 PLCC (PGA from pod), 80C562, 83C562
POD-C552B-PGA-24	24MHz pod for 83552, 87C552, 80C552
POD-C575	12MHz 87C575
POD-C558-16	16MHz 83CE558, 89CE558 pod
POD-CL580	12MHz bondout POD for 83CL580
POD–C592–PGA	12MHz 80C592, 83C592, 87C592 pod
POD–C592-PGA-16	16MHz 80C592, 83C592, 87C592 pod
POD–C652B	Order as POD–C51B
POD–C851B	Order as POD–C51B
POD–C751	12MHz 83C750, 87C750, 83C751, 87C751 pod
POD–C751–16	16MHz 83C750, 87C750, 83C751, 87C751 pod
POD–C752	12MHz 83C752, 87C752 pod
POD–C752–16	16MHz 83C752, 87C752 pod
POD-CL782	12MHz 83CL781, 83CL782, 83CL52 pod
EMUL51–PC/TR4	12MHz 4k trace buffer option
EMUL51–PC/TR16	12MHz 16k trace buffer option
EMUL51–PC/TR4–16	16MHz 4k trace buffer option
EMUL51–PC/TR16–16	16MHz 16k trace buffer option
EMUL51–PC/TR16–20	20MHz 16k trace buffer option
EMUL51–PC/TR16–24	24MHz 16k trace buffer option
EMUL51–PC/TR16–30	30MHz 16k trace buffer option
EMUL51–PC/TR16-33	33MHz 16k trace buffer option
EMUL51–PC/ATR64-16	16MHz 64k Advanced Trace Option
EMUL51–PC/ATR256-16	16MHz 256k Advanced Trace Option
EMUL51–PC/ATR64-24	24MHz 64k Advanced Trace Option
EMUL51–PC/ATR256-24	24MHz 256k Advanced Trace Option
EMUL51–PC/ATR64-33	33MHz 64k Advanced Trace Option
EMUL51–PC/ATR256-30	30MHz 256k Advanced Trace Option
EMUL51–PC/BOX–CS	Serial box with emulator (E128–16) and trace (TR16–16)
EMUL51–PC/BOX–CS–20	Serial box with emulator (E128–20) and trace (TR16–20)
EMUL51–PC/BOX–CS–24	Serial box with emulator (E128–24) and trace (TR16–24)
EMUL51–PC/BOX–CS–30	Serial box with emulator (E128–30) and trace (TR16–30)
EMUL51–PC/BOX–S	Box with serial port and cable. Box allows operation of emulator external to PC.
METALINK CORPORATION	
IM–8051/200–20	iceMASTER–8051 emulator Model 200, 32K emulation memory, 20MHz
IM–8051/400–20	iceMASTER–8051 emulator Model 400, 32K emulation memory, 4K trace buffer, 2 performance analyzers, 20MHz
IM–8051/400–24	iceMASTER–8051 emulator Model 400, 128K emulation memory, 4K trace buffer, 2 performance analyzers, 24MHz
128KUP	128K memory expansion option for iceMASTER–8051
752/1 PGMPC	Programmer accessory for iceMASTER to program 87C751, 87C752
8031–12PC	0.5 to 12MHz 8031, 80C31
8031–16PC	0.5 to 16MHz 8031, 80C31
8031–20PC	0.5 to 20MHz 8031, 80C31
8031–24PC	0.5 to 24MHz 8031, 80C31
8032–12PC	0.5 to 12MHz 8031, 80C31, 8032, 80C32
8032–16PC	0.5 to 16MHz 8031, 80C31, 8032, 80C32
8032–20PC	0.5 to 20MHz 8031, 80C31, 8032, 80C32

Development support tools

MICROCONTROLLER DEVELOPMENT SYSTEMS (Continued)

PRODUCT	DEVICES SUPPORTED
METALINK CORPORATION (Continued)	
8032–24PC	0.5 to 24MHz 8032, 80C32, 8031, 80C31
8052–12PC	0.5 to 12MHz 8031, 80C31, 8032, 80C32, 8051, 8751, 80C51, 87C51, 8052, 8752, 80C52, 87C52
8052–16PC	0.5 to 16MHz 8031, 80C31, 8032, 80C32, 8051, 8751, 80C51, 87C51, 8052, 8752, 80C52, 87C52
80410–12PC	0.5 to 12MHz 80CL410
80451–12PC	1.2 to 12MHz 80C451
80451–16PC	1.2 to 16MHz 80C451
80528–12PC	1.2 to 12MHz 80C528
80528–16PC	1.2 to 16MHz 80C528
80552–12PC	1.2 to 12MHz 80C552, 80C562
80552–16PC	1.2 to 16MHz 80C552, 80C562
80652–12PC	1.2 to 12MHz 8031, 80C31, 80C652
80652–16PC	1.2 to 16MHz 8031, 80C31, 80C652
80851–12PC	1.2 to 12MHz 8031, 80C31, 80C851
83053–12PC	6 to 12MHz 83C053, 83C054, 87C054
83451–12PC	1.2 to 12MHz 80C451, 83C451, 87C451
83528–12PC	1.2 to 12MHz 80C528, 83C528, 87C528, 83C524, 87C524
83528–16PC	1.2 to 16MHz 80C528, 83C528, 87C528, 83C524, 87C524
83550–10PC	1.2 to 10MHz 80C550, 83C550, 87C550
83552–12PC	1.2 to 12MHz 80C552, 83C552, 87C552, 80C562, 83C562
83552–16PC	1.2 to 16MHz 80C552, 83C552, 87C552, 80C562, 83C562
83652–12PC	1.2 to 12MHz 80C652, 83C652, 87C652, 80C552, 83C552, 87C552, 80C562, 83C562
83652–16PC	1.2 to 16MHz 80C652, 83C652, 87C652, 80C552, 83C552, 87C552, 80C562, 83C562
83654–12PC	1.2 to 12MHz 80C652, 83C652, 87C652, 83C654, 87C654, 80C552, 83C552, 87C552, 80C562, 83C562
83654–16PC	1.2 to 16MHz 80C652, 83C652, 87C652, 83654, 87C654, 80C552, 83C552, 87C552, 80C562, 83C562
83751–12PC	0.5 to 12MHz 83C751, 87C751
83751–16PC	0.5 to 16MHz 83C751, 87C751
83752–12PC	0.5 to 12MHz 83C752, 87C752

Development support tools

EPROM MICROCOMPUTER PROGRAMMING SUPPORT

DEVICE	MANUFACTURER/MODEL	MODULE/ADAPTOR	SOFTWARE VERSION
87C054 SDIP	N. Valley Products Philips, Ceibo MP-51	SAM-054SD PPA-054SD	
87C51 DIP	Advin Sailor-PAL/SA, /SB BP Microsystems EP-1140 Ceibo MP-51 (PMP51SD) Data I/O Unisite 40 Data I/O Unipak 2b Data I/O Series 1000 Logical Devices ALLPRO N. Valley Products SPGM–100 Philips LCPX5X40 (P8051LCP40) Strebor PLP-S1A	Adaptor-8751 PPA-51XSD 351B103 SR40 SAM–51SD MC4851DIP	 V2.2 V16 V05 (Use Intel 87C51 menu) V1.47 V1.0
87C51 PLCC	Ceibo MP-51 (PMP51SD) Data I/O Unisite 40 Data I/O Unipak 2b Logical Devices ALLPRO N. Valley Products SPGM–100 Philips LCPX5X40 (P8051LCP40)	PPA-51XSD Chipsite 351B103P Required SAM–51ASD	 V2.3 V16 V1.47 V1.0
87C52 DIP	BP Microsystems EP-1140 Ceibo MP-51 (PMP51SD) Data I/O 29B, Unipak 2b Data I/O Unisite 40 N. Valley Products SPGM–100 Philips LCPX5X40 (P8051LCP40)	 PPA-XSD 351B103 SAM–52SD	 V23 V3.1
87C451 DIP	Ceibo MP-51 (PMP51SD) Logical Devices ALLPRO N. Valley Products SPGM–100	PPA-451SD PPRequired SAM–451SD	 V1.47 V1.0
87C451 PLCC	Advin Sailor-PAL/SA, /SB Ceibo MP-51 (PMP51SD) N. Valley Products SPGM–100 Data I/O Unisite Philips LCPX5X (P8051LCPX)	Adaptor-87451 PPA-451ASD SAM–451ASD Chipsite	 V1.0 V2.8
87C528 DIP	BP Microsystems EP-1140 Ceibo MP-51 N. Valley Products SPGM–100 Philips LCPX5X40 (P8051LCP40)	 PPA-XSD SAM–528	
87C528 PLCC	Ceibo MP-51 (PMP51SD) N. Valley Products SPGM–100 Philips LCPX5X40 (P8051LCP40)	PPA-51XSD SAM–528A	
87C552	Ceibo MP-51 (PMP51SD) N. Valley Products SPGM–100 Data I/O Unisite Philips LCPX5X (P8051LCPX)	PPA-552ASD SAM–552ASD Chipsite	 V2.2 V3.1
87C652 DIP	BP Microsystems EP-1140 Ceibo MP-51 N. Valley Products Philips LCPX5X40 (P8051LCP40)	 PPA-51XSD SAM-52SD	
87C652 PLCC	Ceibo MP-51 (PMP51SD) Philips LCPX5X40 (P8051LCP40)	PPA-51XSD	
87C654 DIP	BP Microsystems EP-1140 Ceibo MP-51 (PMP51SD) N. Valley Products SPGM–100 Philips LCPX5X40 (P8051LCP40)	 PPA-51XSD SAM–654SD	
87C654 PLCC	Ceibo MP-51 (PMP51SD) Philips LCPX5X40 (P8051LCP40)	PPA-51XSD	

Development support tools

EPROM MICROCOMPUTER PROGRAMMING SUPPORT (Continued)

DEVICE	MANUFACTURER/MODEL	MODULE/ADAPTOR	SOFTWARE VERSION
87C751 DIP	Advin Sailor-PAL/SA, /SB	EM-751	
	BP Microsystems EP-1140	HEAD-40A	
	Ceibo MP-51 (PMP51SD)	PPA-751SD	
	Data I/O Unisite 40		V2.3
	Data I/O 29B, Unipak 2b	351B113D	29B V6, Unipak 2B V20
	Logical Devices ALLPRO	OPTAPC–751	V1.47
	N. Valley Products SPGM–100	SAM–751SD	V1.0
	Needham's Electronics		
	MetaLink	752/1 PGMPC	V2.6a (use with MicroICE+)
	Logical Systems (Sunshine EW–901)	PA751	
	Philips LCPX5X (P8051LCPX)		
	Strebor PLP-S1A	MC7512DIP	
87C751 PLCC	Ceibo MP-51 (PMP51SD)	PPA-51XSD	
	Data I/O Unisite 40	Chipsite	V2.6
	Logical Devices ALLPRO	Required	V1.47
	N. Valley Products SPGM–100	SAM–751ASD	V1.0
87C752 DIP	Advin Sailor-PAL/SA, /SB	EM-751	
	BP Microsystems EP-1140	HEAD-40A	
	Ceibo MP-51 (PMP51SD)	PPA-752SD	
	Data I/O Unisite 40		V2.6
	N. Valley Products SPGM–100	SAM–752SD	V1.0 (Use Type 751)
	Needham's Electronics		
	MetaLink	752/1 PGMPC	V2.6a (use with MicroICE+)
	Logical Systems (Sunshine EW–901)	PA751	
	Logical Devices ALLPRO	OPTAPC-752	
	Philips LCPX5X (P8051LCPX)		
	Strebor PLP-S1A	MC7512DIP	
87C752 PLCC	Ceibo MP-51 (PMP51SD)	PPA-752ASD	
	Data I/O Unisite 40	Chipsite	V2.8
	N. Valley Products SPGM–100	SAM–752ASD	V1.0 (Use Type 751)

NOTE:
Philips programmers are available in the U.S.A. through Philips Semiconductors distributors.

Development support tools

ADDITIONAL PROGRAMMING SUPPORT

DEVICE	MANUFACTURER	MODULE/ADAPTOR	COMMENTS
87C51/52/652/ 654/528 PLCC	Logical Systems	PA51–44	Use with any 40-pin microcontroller programming site that supports the appropriate EPROM size.
87C51/52/652/ 654/528 QFP		PA52-QFP	Use with any 40-pin microcontroller programming site that supports the appropriate EPROM size.
87C451 DIP		PA451–64	Use with any 87C51 40-pin programming site.
87C451 PLCC		PA451–68	Use with any 87C51 40-pin programming site.
87C550 DIP		550BASE	Use with any 87C51 40-pin programming site.
87C550 PLCC		PA550–44	Use with any 87C51 40-pin programming site.
87C552 PLCC		PA552–68	Use with any 8752/C52/C252/C51FA 40-pin programming site.
87C752 PLCC		PA28-28	Use with any 87C752 28-pin DIP programmer.
87C751 PLCC	Philips	No part number assigned	This adapter allows programming the 87C751 PLCC part in conjunction with any programmer that can already program the DIP version of the part.

MICROCONTROLLER SUPPORT

PRODUCT	DEVICES SUPPORTED	MANUFACTURER	DESCRIPTION
8051 C Compiler	8051 and derivatives	Franklin Software	C Compiler for 8051 family
8051 C Compiler	8051 and derivatives	Archimedes Software	C Compiler for 8051 family
80C51 C Compiler	8051 and derivatives	BSO/Tasking	C Compiler for 8051 family
P8051DB	8051 and derivatives	Ceibo	80C51 Family Development Board
S87C00KSD	– –	Philips	I^2C Demonstration Board. 87C751 controls various I^2C peripherals. Board has sockets for 87C752, 87C652, and 87C552 also.
– –	– –	Philips	The Philips computer Bulletin Board system has available a microcontroller newsletter, application and demonstration programs for download, and the ability to send messages to microcontroler applications engineers. Access by modem at 2400, 1200, or 300 baud. The telephone numbers are: (800) 451–6644 (in the U.S.) or (408) 991–2406.
SMI–CNV451SD	80/83/87C451	Philips	Philips product adapts a PLCC emulator plug for the 80C451 to the DIP pinout.

Microcontroller bulletin boards

To better serve our customers, Philips maintains two microcontroller bulletin boards. These computer bulletin board systems feature microcontroller newsletters, application and demonstration programs for download, and the ability to send messages to microcontroller application engineers.

The telephone numbers are:

North American Bulletin Board
300/1200/2400 baud 8-N-1
(800) 451-6644 (in the U.S.)
or
(408) 991-2406

European Bulletin Board
MAX 14.400 baud
Standards V32/V42/V42.bis/HST
+31 40 721102

European Application Help Desk
+31 40 722749
9a.m. – 16p.m. CET (Central European Time)

Sunnyvale ROMcode Bulletin Board

We also have a ROM code bulletin board through which you can submit ROM codes. This is a closed bulletin board for security reasons. To get an ID, contact your local sales office. The system can be accessed with a 2400, 1200, or 300 baud modem, and is available 24 hours a day.

The telephone number is:

(408) 991-3459

The following application note files are available on the Philips BBS:

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AN424	WARMBOOT.ZIP	AN440	BOOTSTRP.ZIP
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Data handbook system

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DC03	Television Tuners, Coaxial Aerial Input Assemblies
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